Dec. 19, 1961 H. C. BUSSEY 3,014,211

DIGITAL-TO-ANALOG CONVERTER

Filed June 10, 1957

FIG. 1

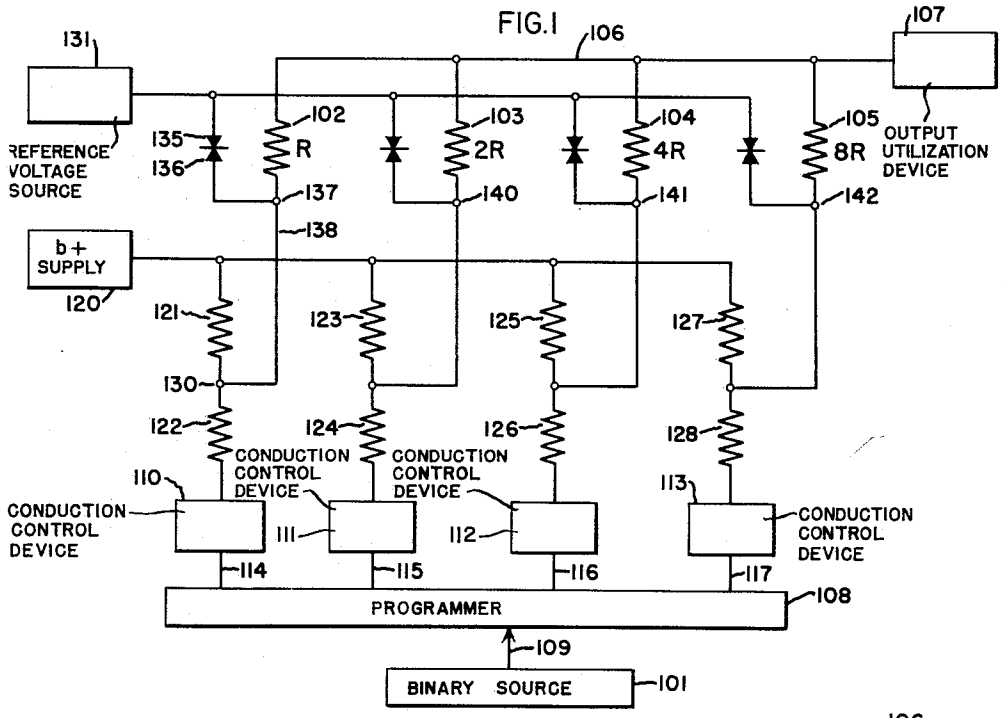


FIG. 2

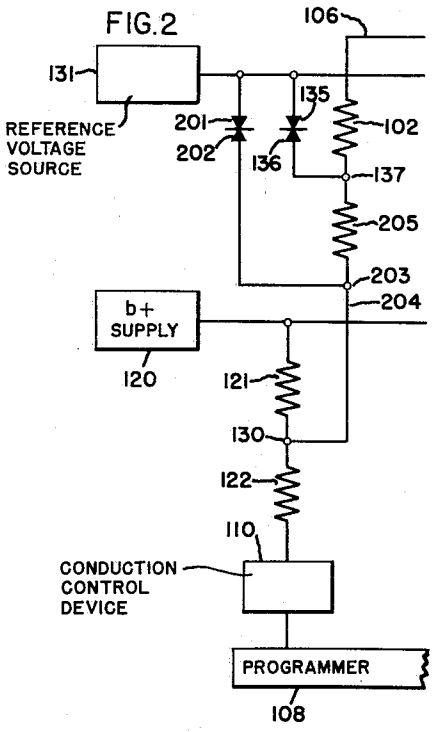
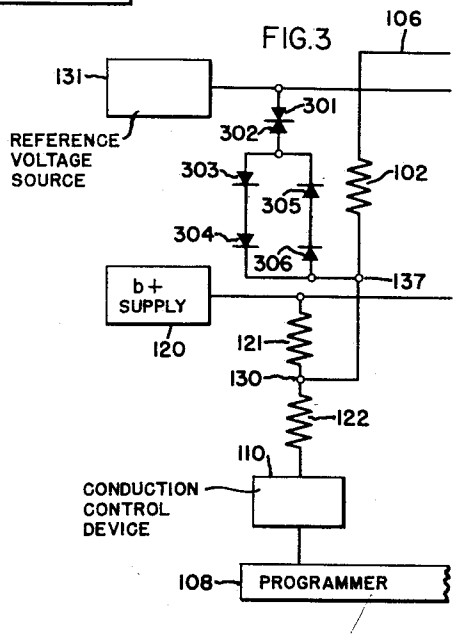


FIG. 3



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United States Patent Office 3,014,211 Patented Dec. 19, 1961

3,014,211

DIGITAL-TO-ANALOG CONVERTER

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Filed June 10, 1957, Ser. No. 664,635
8 Claims. (Cl. 340—347)

This invention relates to the art of conversion of signal form and more particularly to the art of converting digitally coded signals into analog voltages.

In recent years the advantages of digitally coded information representations or signals have been recognized. The advantage of information storage capability and the compatibility of the digital code with present data handling equipments have led to the recent rapid increase in use.

However, in many applications it has been desirable to transform the coded information into analog form because of its compatibility with control and display equipments, such as meter movements, positioning devices, etc. In the prior art there have been developed matrixes using a plurality of resistors whose values are diminisioned in accordance with the weight of each bit in the digitally coded word. Each bit controls the operation of relays which alter the matrix to provide an analog voltage output in accordance with the information contained in the digitally coded word. Such relay controlled matrixes have often been larger and more susceptible to vibration and shock errors than required, particularly in an air borne equipment. Various relay substitutes have been unable to provide the necessary accuracy in conversion.

It is, therefore, one object of my invention to alleviate such problems.

It is a further object of my invention to provide a conversion apparatus for accurate conversion of a digitally coded word into an analog voltage.

It is a further object of my apparatus to provide improved method and means for the conversion of binary coded information into an analog voltage.

In one embodiment of my invention I have provided a plurality of appropriately dimensioned resistors, one for each bit of a digitally coded word. A flip-flop circuit and a precision voltage clamp are operated by each bit to change the voltage applied to each resistor and, thus, to effectively alter the matrix in logical fashion. The matrix changes are used to derive an analog output voltage variable in accordance with the digitally coded word.

The features of my invention which I believe to be novel are set forth with particularity in the appended claims. My invention itself, however, together with further objects and advantages thereof, may best be understood by reference to the following description taken in connection with accompanying drawing in which:

FIGURE 1 is a schematic diagram of one embodiment of my invention.

FIGURE 2 is a schematic diagram of a second embodiment of my invention; and

FIGURE 3 is a schematic diagram of another embodiment of my invention.

Digitally coded words can be converted or translated into analog voltages by means of the circuit shown in FIGURE 1. The circuit may be used to convert a four-bit binary word supplied from source **101** into sixteen different analog voltages, each representative of a different one of the permutations possible in a four-bit number. Four resistances **102**, **103**, **104** and **105** are arranged in a matrix having a common terminal joined by connection **106**. The analog voltage derived in accordance with changes in a digital input signal are applied over this common connection **106** to the output utilization device **107**. Each resistor in the matrix is

associated with one of the bits in a digitally coded word and is so dimensioned as to have the same significance with respect to the other resistors as does its associated bit have to the remainder of the bits in the input word. For example, when using a binary code, the significance of the bits varies in geometric progression having the common ratio of 2. In such applications the resistors will be similarly graded so that resistor **103** is twice the value of resistor **102**, resistor **104** is twice the value of resistor **103** and the resistance of resistor **105** is twice that of resistor **104**. Such proportioning of resistors in the resistance matrix is well known to the art. It will also be apparent to those skilled in the art that with use of different codes the significance of the various bits will vary and the resistors in the matrix should be proportioned accordingly.

The input binary word is applied to programmer **108** over connection **109** for distribution to the matrix. The programmer **108** may consist, for example, of a shift register for storing sequentially applied bits and applying the bits to the proper portion of the matrix circuit by parallel readout. This and similar programmer means are known to the art and further explanation is deemed unnecessary. The programmer is effective to apply the most significant digit to conduction control device **110**, and digits of increasingly less significance to conduction control devices **111**, **112** and **113** over respective connections **114**, **115**, **116** and **117**. The conduction control device **110** is responsive to the state of the applied bit to draw current from the $b+$ supply **120** through resistors **121** and **122** which are serially connected between the devices and the $b+$ supply. The state of the bits may be a positive voltage representing the binary digit "1" and the absence of voltage representing the binary digit "0." It will be apparent to those skilled in the art that the two states could equally be represented by a positive and negative voltage. Each conduction controlled device is, in this embodiment, one stage of a bistable multivibrator, commonly known as a flip-flop. The flip-flop is so arranged to conduct when the bit "0" is applied thereto and to be rendered non-conductive when the bit "1" is applied. Devices **111** through **113** are identical to device **110** having respective associated resistors **123** and **124**, **125** and **126**, and **127** and **128**.

The conduction of device **110** in accordance with the state of the binary bit applied thereto will cause the potential of junction **130** to rise and fall in accordance with the conduction state. For example, if the bit "1" is applied to device **110**, junction **130** will attempt to reach the potential of source **120**. If, on the other hand, the bit "0" is applied, device **110** will conduct and junction **130** will approach the value determined by the dimensioning of the respective resistors **121** and **122**. In order to use this change in junction potential for the derivation of a precise analog signal over the common connection **106**, a source of reference voltage **131** is supplied. Two Zener diodes **135** and **136** connected in bucking relationship are connected between the source **131** and junction **130**. The Zener diodes are precision voltage clamping devices. These diodes are commercially available junction diodes operated in the inverse breakdown region. In this manner the voltage at junction **137**, maintained at the same potential as junction **130** by connection **138**, can be changed from one potential to a second potential in response to the state of the applied binary bit. In the same manner junctions **140**, **141** and **142** are changed in potential in response to the state of the respective applied binary bit.

When device **110** is non-conductive, the voltage at junction **137** rises towards the value of the reference voltage plus the Zener breakdown voltage. When device **110** conducts, junction **137** drops to the value of the ref-

erence voltage minus the Zener breakdown voltage. It will be apparent to those skilled in the art that the limits of potential variation at junction **130** due to the conduction or non-conduction of device **110** must exceed the value of twice the Zener breakdown voltage. Since Zener diodes operate with a breakdown voltage in the range of eight volts, provision for the necessary voltage swings can easily be made by those skilled in the art.

The derivation of an analog voltage as a result of the changing potentials of the junctions of the resistors in the matrix can best be seen by assuming a specific input signal. If the binary coded input signal is 1000, device **110** will be rendered non-conductive and devices **111**, **112** and **113** will conduct. Junction **137** will, therefore, reach the potential of the reference voltage plus the Zener breakdown voltage. Junctions **140**, **141** and **142** will remain at the potential of the reference voltage less the Zener breakdown voltage. Therefore, in effect, the matrix has been rearranged to have resistor **102** serially connected with the parallel combination of resistors **103**, **104** and **105** across a voltage source equal to two times the Zener breakdown voltage. As will be apparent to those skilled in the art, changes in a conduction state of the respective devices **110–113** will effectively change the matrix to vary the analog signal applied over common connection **106** to the output utilization device **107**. Table I gives a summary of the analog output derivable from this circuit in accordance with the various variations in the input binary word.

Table I

Binary Coded Word	Devices 110-113 Non-Conducting (All Others Conducting)	Output Voltage (Ratio); Multiply 2/15 times Zener Breakdown in Volts to Get Output in Volts
0000		0
0001	113	1
0010	112	2
0011	112, 113	3
0100	111	4
0101	111, 113	5
0110	111, 112	6
0111	111, 112, 113	7
1000	110	8
1001	110, 113	9
1010	110, 112	10
1011	110, 112, 113	11
1100	110, 111	12
1101	110, 111, 113	13
1110	110, 111, 112	14
1111	110, 111, 112, 113	15

It will be apparent to those skilled in the art that words having more bits will require more impedance elements in the matrix. It will also be apparent that resistance value will be chosen to meet the operating characteristics of the specific application. However, for clarity of explanation, representative component values found satisfactory for one application of the circuit shown in FIGURE 1 are listed in Table II.

Table II

Reference Numeral	Characteristics
120	+100 Volts (−150 Volts on Cathodes).
131	+7.5 Volts.
135, 136	Zener Diode—7.5 Volt Breakdown.
102	10K Ohms.
103	20K Ohms.
104	40K Ohms.
105	80K Ohms.
121, 123, 125, 127	47K Ohms.
122, 124, 126, 128	22K Ohms.
110	Conducting 0.0035 Amp. Drawn Approx.

At times circuit economy may dictate the use of conduction control devices having large variations in conduction current. In applications wherein a digitally coded word having a large number of bits is to be converted using such devices the circuit shown in FIGURE 2 may be advantageously employed.

In FIGURE 2 there is shown a portion of the matrix shown in FIGURE 1. In FIGURE 2 parts similar to those employed in FIGURE 1 are identically numbered. The resistor **102** is associated with the most significant bit in the digitally coded word. The analog equivalent is derived over output lead **106** in accordance with the applied bit derived from programmer **108**. The operation of the conduction control device in changing the potential of junction **130** is identical with the operation of the similar circuitry as explained in connection with FIGURE 1. In order to limit voltage variations at junction **137** and, thus, variations in the current drawn through the voltage clamping devices **135** and **136**, a second voltage clamping device, comprising two back-to-back Zener diodes, is connected between the reference source **131** and junction **203** maintained at the same potential as junction **130** by connection **204**. A resistor **205** is serially connected between junction **137** and junction **203**. The diodes **201** and **202** must have a higher rating than that of diodes **135** and **136**. In one embodiment diodes **135** and **136** had a breakdown voltage of 7.5 volts. Diodes **201** and **202** had a breakdown voltage of approximately 12.5 volts. It will be apparent to those skilled in the art that the breakdown characteristics of diodes **201** and **202** need not be as precisely defined as those of diodes **135** and **136**. In this manner potential variations at junction **137** are restricted in range. Therefore, current variations through the clamping diodes **135** and **136** are restricted.

It will be apparent to those skilled in the art that the circuitry shown in FIGURE 2 will be necessary only when converting a digitally coded word of many bits due to the flat breakdown characteristics of the Zener diode. Further, it will be apparent to those skilled in the art that the circuit modification of FIGURE 2 need be applied only to the stages utilized for converting the most significant bits in the applied word.

In some applications of the circuitry shown in FIGURE 1 the variations of Zener diode breakdown characteristics with respect to ambient temperature becomes significant. In such applications the circuitry shown in FIGURE 3 may be advantageously employed.

In FIGURE 3 there is shown a portion of the matrix shown in FIGURE 1 in which similar parts are identically numbered. The potential at junction **137** is controlled in accordance with the state of the applied bit in the same manner as explained in connection with the explanation of the operation of the circuit shown in FIGURE 1. However, a plurality of Zener diodes are connected between the reference source **131** and junction **137** for use in conditions of widely varying ambient temperature. It has been found that the temperature compensation for the variation in breakdown voltage of the Zener diode can be made by serially connecting three Zener diodes in oppositely poled direction. To accomplish this temperature compensation in most efficient fashion, I connect diodes **301** and **302** in back-to-back relationship. Two diodes **303** and **304** are serially connected in parallel with oppositely poled serially connected diodes **305** and **306**. The parallel combination is connected between diode **302** and junction **137**. In this manner three oppositely poled diodes are always in series with the diode operating in the Zener breakdown region. Thus, temperature compensation can be effected.

It will be apparent to those skilled in the art that the embodiment shown in FIGURE 2 could employ the temperature compensation circuit shown in FIGURE 3 when applications so require.

Those skilled in the art will recognize that in addition to providing means for effectively changing the matrix arrangement without relays or switches, my circuit greatly improves the accuracy of the analog equivalent voltage by eliminating the reference source from directly influenc-

ing the analog equivalent. Thus, the reference source can be of simpler construction than those employed previously. Also, only a single source is required.

While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from the invention in its broader aspects, and, therefore, the aim in the appended claims is to cover all such changes and modifications that fall within the true spirit and scope of the invention.

What I claim as new and desire to secure by Letters Patent of the United States is:

1. A binary word converter comprising a plurality of resistance elements, the conductivity of each of which bears such relationship to that of the remainder as to form a series of resistance elements, the conductivity of which increases in geometric progression whose common ratio is two, each of said resistance elements having a first and second terminal, an output circuit, means coupling said first terminals of said resistance elements to said output circuit, a source of reference potential, a first and second Zener diode serially connected in bucking relationship between each of said second terminals of said resistance elements and said reference source, and means coupled to each of said second terminals for causing current flow through said diodes in one direction or other in response to the state of a respective bit of said binary word.

2. Apparatus for converting a digitally coded word composed of a plurality of bits having differing significant values comprising a plurality of resistance elements, each of said elements associated with a respective bit and dimensioned so that the conductivity bears the same relationship in the remaining elements as the significance its associated bit bears to the significance of the remaining bits, an output circuit, a common terminal for each of said resistance elements, means coupling said common terminal to said output circuit, a reference source, a voltage clamping means coupling said reference source to the remaining terminal of each of said resistance elements, means responsive to a first state of each bit for applying a voltage of potential less than said reference voltage minus said clamping potential to said remaining terminal of said resistance elements, and means responsive to a second state of each bit for applying a voltage of higher potential than said reference voltage plus said clamping potential to said remaining terminal of said resistance elements.

3. In combination, a matrix comprising a plurality of resistance elements having a common terminal, a source of reference potential, a plurality of clamping means, each of said clamping means coupling the other terminal of one of said elements to said reference source, said clamping means dimensioned to substantially maintain a predetermined voltage drop across said means in the direction of current flow therethrough despite variations in current flow, an output circuit coupled to said common terminal, and means responsive to the bits of a digitally coded word for effectively changing the matrix comprising means for establishing current exceeding a predetermined level through each of said clamping means in one direction in response to one state of a respective bit and for establishing current exceeding a predetermined level through each of said clamping means in the opposite direction in response to the other state of a respective bit in said input word.

4. In combination, a matrix comprising a plurality of resistance elements having a common terminal, a source of reference voltage, voltage clamping means coupling the other terminal of said element to said reference source, said clamping means being dimensioned to have predetermined potential drop across said means, said potential drop being of substantially the same magnitude for condition of current flow from said source to said terminal and for condition of current flow from said terminal to said source, means for initially establishing current flow through each of said clamping means in a first direction, means responsive to one state of each bit in an input digitally coded word for reversing said current flow in said clamping means, a utilization circuit, and means coupling said utilization circuit to said common terminal.

5. Apparatus for converting a digitally coded word composed of bits into an analog quantity comprising a resistance matrix, said matrix comprising a plurality of impedance elements, each of said elements being associated with one bit of said word and being so dimensioned that the admittance thereof bears the same relationship to the admittance of the remainder as does the significance of the associated bit bears to the remaining bits, and means responsive to one state of each bit for applying a first potential to its associated impedance element, and means responsive to the other state of each bit for applying a second potential to its associated impedance element, said first and second potential applying means comprising the same first and second serially connected Zener diodes.

6. Apparatus for converting a binary coded word composed of n bits into an analog quantity, comprising n impedance elements, the admittance of each of which bears such relation to that of the remainder as to form a series of impedance elements the admittance of which increases in geometric progression, an output circuit having one terminal in common with a respective terminal of each of said impedance elements, a source of reference potential, a plurality of voltage clamping means each so dimensioned as to have a predetermined voltage drop thereacross despite variations in current flow therethrough and each connected between a respective impedance element and said reference source, and a plurality of circuit means for establishing current flow through a respective clamping means in one direction in one condition of operation and in the opposite direction in a second condition of operation, each of said circuit means being operative by the state of a bit of said binary coded word.

7. Apparatus for the conversion of a digitally coded word composed of bits, comprising a plurality of resistors, each of said resistors being associated with a single bit in said word and dimensioned to have the same significance with respect to other resistors as does the associated bit with respect to the other bits, an output circuit, means coupling said output circuit to a common terminal on said resistors, a source of reference potential, a plurality of voltage clamping means, each of said clamping means coupling the other terminal of one of said resistors to said reference source and dimensioned to maintain said terminal at potential level which is a predetermined value higher than said reference level in response to current flow therethrough in a first direction and at a potential level which is a predetermined value lower than said reference level in response to current flow therethrough in a second direction, means responsive to one state of each bit for establishing current flow in a first direction through the clamping means coupling the associated resistor to said reference source, and means responsive to another state of each bit for establishing current flow in a second direction through the clamping means coupling the associated resistor to said reference source.

8. Apparatus for converting an n-bit binary coded word into an analog voltage by effectively changing the arrangement of matrix composed of a series of n impedance elements the admittance of each of which increases in geometric progression, comprising in combination a reference voltage source, n clamping means, each of said means connecting one of said impedance elements to said reference source, each of said clamping means dimensioned to substantially maintain a fixed voltage drop across said means despite variations in current flow therethrough, means for establishing current flow in one direction through each of said clamping means in response to

one state of a respective bit, and means for establishing current flow in a second direction through each of said clamping means in response to a second state of a respective act.

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