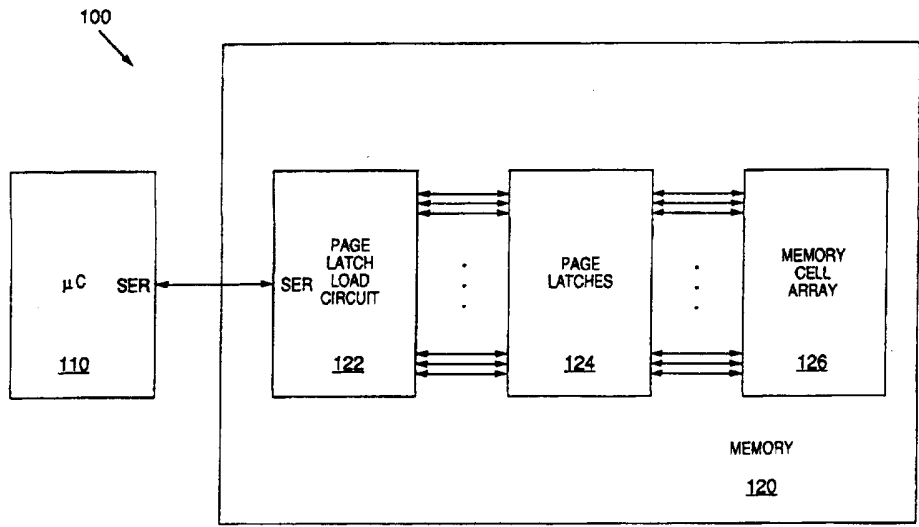




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

<p>(51) International Patent Classification ⁶ : G11C 7/00</p>	<p>A1</p>	<p>(11) International Publication Number: WO 97/30452 (43) International Publication Date: 21 August 1997 (21.08.97)</p>
<p>(21) International Application Number: PCT/US97/01567 (22) International Filing Date: 14 February 1997 (14.02.97) (30) Priority Data: 08/601,963 15 February 1996 (15.02.96) US (71) Applicant: NEXCOM TECHNOLOGY, INC. [US/US]; 532 Mercury Drive, Sunnyvale, CA 94086 (US). (72) Inventors: GANNAGE, Michael, E.; 2735 Bonnie Drive, Santa Clara, CA 95051 (US). WONG, William, K.; 1166 Happy Valley Avenue, San Jose, CA 95129 (US). BAJWA, Asim, A.; 4955 Fontanelle Place, San Jose, CA 95111 (US). (74) Agent: MACPHERSON, Alan, H.; Skjerven, Morrill, MacPherson, Franklin & Friel, Suite 700, 25 Metro Drive, San Jose, CA 95110 (US).</p>		<p>(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).</p> <p>Published <i>With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i></p>

(54) Title: PAGE LATCH



(57) Abstract

A memory device comprising a page latch load circuit (122) which provides serial I/O to the microcontroller (110) and transfers I/O bits in a predetermined order to/from the page latches (124). Page latches (124) are connected over many bit lines to a memory cell array (126). The page latches (124) not only support programming and reading of sectors in the memory cell array (126), but also provide one or more of the following functions: directly accessible to the microcontroller as an SRAM scratch pad, directly loadable from the memory cell array to facilitate single byte "read-modify-write" operations, and loadable during programming operations to support real time applications.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia	GB	United Kingdom	MW	Malawi
AT	Austria	GE	Georgia	MX	Mexico
AU	Australia	GN	Guinea	NE	Niger
BB	Barbados	GR	Greece	NL	Netherlands
BE	Belgium	HU	Hungary	NO	Norway
BF	Burkina Faso	IE	Ireland	NZ	New Zealand
BG	Bulgaria	IT	Italy	PL	Poland
BJ	Benin	JP	Japan	PT	Portugal
BR	Brazil	KE	Kenya	RO	Romania
BY	Belarus	KG	Kyrgystan	RU	Russian Federation
CA	Canada	KP	Democratic People's Republic of Korea	SD	Sudan
CF	Central African Republic	KR	Republic of Korea	SE	Sweden
CG	Congo	KZ	Kazakhstan	SG	Singapore
CH	Switzerland	LI	Liechtenstein	SI	Slovenia
CI	Côte d'Ivoire	LK	Sri Lanka	SK	Slovakia
CM	Cameroon	LR	Liberia	SN	Senegal
CN	China	LT	Lithuania	SZ	Swaziland
CS	Czechoslovakia	LU	Luxembourg	TD	Chad
CZ	Czech Republic	LV	Latvia	TG	Togo
DE	Germany	MC	Monaco	TJ	Tajikistan
DK	Denmark	MD	Republic of Moldova	TT	Trinidad and Tobago
EE	Estonia	MG	Madagascar	UA	Ukraine
ES	Spain	ML	Mali	UG	Uganda
FI	Finland	MN	Mongolia	US	United States of America
FR	France	MR	Mauritania	UZ	Uzbekistan
GA	Gabon			VN	Viet Nam

PAGE LATCH

BACKGROUNDField of the Invention

5 The present invention relates to digital memories, and more particularly page latches for digital memories.

Background of the Invention

10 Byte programming for EEPROM (Electrically Erasable-Programmable Read-Only Memory) devices is longer than byte programming for EPROM (Erasable-Programmable Read-Only Memory) or Flash EPROM. In particular, byte programming requires about 5 ms for EEPROM as opposed to about 10 μ s for EPROM or Flash EPROM. The reason is that EEPROM devices typically use Fowler-Nordheim Tunneling mechanism to inject electrons or retrieve electrons to or from the floating gate, while EPROM or Flash EPROM devices
15 typically use the CHE (channel hot electron) mechanism to inject electrons in the floating gate. The CHE mechanism is quite inefficient and typically requires anywhere from 100 μ A to 1 mA of programming current for each cell. This is why only one byte at a time is usually programmed in EPROM's or FLASH EPROM's devices. On the other hand, the FN (Fowler-Nordheim) tunneling mechanism barely consumes any current, being typically in the
20 nanoampere range. Because of this, many cells, illustratively a few thousand, can be programmed at the same time in parallel.

Because large number of cells can be programmed in parallel, page latches have been widely used in EEPROM devices to speed up their programming time. An early EEPROM
25 device containing page latches is the type 28C64, which is a 64K EEPROM available from various manufacturers including Catalyst and Xicor. Each page latch is connected to a bitline; typically for a given EEPROM device, there are as many page latches as there are bitlines. For example, a 64K EEPROM (type 28C64) has 32 bytes of page latches, a 256K EEPROM

-2-

(type 28C256) has 64 bytes of page latches, and a 1Mb EEPROM (type 28C010) has 128 bytes of page latches. A serial 8Mbit Flash EEPROM type 26F080 available from Nexcom Technology, Inc. of Sunnyvale, California has 536 bytes of page latches.

5 Page latches typically operate in the following way. The user provides to the memory the column address as well as the data byte followed by \overline{WE} and \overline{CE} to load the page latches. After all of the page latches are loaded, the memory device goes into a self-timed programming cycle at the end of which the data in the page latches is transferred to the selected row decoded by the X-Address decoder. The device programming is sped up by a considerable factor. For
10 example, if all 32 bytes are loaded in the page latches, the programming time per byte is cut from an average of 5 ms to 5 ms/32 or 156 μ s. For an 8 Mbit device having 2048 sectors of 536 bytes each, the average programming time is 5 ms/536 bytes or about 9 μ s.

 A page latch has some features in common with an SRAM cell. For example, both
15 page latches and SRAM cells typically include two inverters connected back-to-back. However, page latches and SRAM cells have many differences as well. For example, SRAM cells are differential devices, while page latches are single ended. As a differential device, an SRAM cell is able to interact with high capacitance differential bit lines without affecting the value stored therein. However, as a single ended device, a page latch is not able to interact
20 with a high capacitance line without potentially changing the value stored therein. While a page latch can be used as temporary storage before transferring data to a selected row of memory, a page latch is not usable as a data buffer.

 One-transistor Flash EEPROM devices containing page latches have a further
25 weakness, relative to regular EEPROM devices. Regular EEPROM devices, which contain two transistor memory cells, use a byte-select transistor for every byte, so that every byte is uniquely accessible. Eight page latches are associated with every byte, and an additional page latch is associated with the byte select. If only one byte needs to be modified, the modification can be easily achieved because only that byte will go through the Erase & Write cycle.
30 However, Flash EEPROM devices using one-transistor memory cells have no byte-select transistors. If only one byte needs to be modified, the entire sector is erased (high threshold

-3-

voltage V_i) and is subsequently entirely written. Typically, if a "Read-Modify-Write" operation is desired, the entire sector is read and stored in external RAM, the selected byte is modified, and the entire sector is loaded back into the page latches before the self timed Erase-Write Operation is initiated. Unfortunately, this process is time-consuming.

5

Memory devices containing page latches have a further weakness, which is problematical in some real time applications requiring continuous writes to memory. During programming of a sector in which data is transferred from the page latches to the selected sector, the page latches cannot be accessed until the sector programming is complete.

10

Typically, a self-timed programming cycle takes about 5 ms. In a real time application generating sectors of data more frequently than once every 5 ms, an external memory device must be used to temporarily store the stream of real time data until programming of the present sector is complete.

15

SUMMARY OF THE INVENTION

In one embodiment, the invention is a memory comprising a plurality of page latches, each of the page latches being loadable and readable through a data node coupled thereto; and a memory array having a plurality of memory cells coupled in groups to respective column lines, the column lines being respectively coupled to the page latches.

20

In another embodiment, the invention is a method of operating a memory comprising selecting all cells associated with a word line of the memory, and loading data from the selected cells into all page latches of the memory.

25

BRIEF DESCRIPTION OF THE FIGURES

Figure 1 is a block schematic diagram of a computer system;

Figure 2 is a schematic diagram of a page latch circuit;

30

Figure 3 is a timing diagram for the page latch of Figure 2; and

Figure 4 is a schematic diagram of a page latch circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1 shows an illustrative computer system 100 which includes a computing device such as a microcontroller 110 (other computing devices such as microprocessors, controllers and processors are suitable as well) and a memory device 120. The memory device 120 is illustratively a serial device connected to the serial port of the microcontroller 110, although a parallel memory device connected to the microcontroller 110 by a bus may be used if desired. The memory device 120 includes a page latch load circuit 122, which typically includes a shift register, which provides serial I/O to the microcontroller 110 and transfers I/O a byte at a time in a predetermined order to/from the page latches 124. Page latches 124 is connected over many bit lines to a memory cell array 126. Page latches 124 not only support programming and reading of sectors in the memory cell array 126, but also provide one or more of the following functions: directly accessible to the microcontroller 110 as an SRAM scratch pad, directly loadable from the memory cell array 126 to facilitate single byte "read-modify-write" operations, and loadable during programming operations to support real time applications. These various embodiments of the page latches 124 are described herein in further detail. Various circuits and methods for the page latch load circuit 122, the memory cell array 126, and other elements of the memory device 120 (omitted for clarity) are described in United States Patent No. 5,414,658, which is entitled "Electrically Erasable Programmable Read-Only Memory Array" and issued May 9, 1995 to Challa et al.; United States Patent No. 5,410,680, which is entitled "Solid State Memory Device Having Serial Input/Output" and issued April 25, 1995 to Challa et al.; United States Patent No. 5,291,584; and United States Patent No. 5,222,040, which is entitled "Single Transistor EEPROM Memory Cell" and issued June 22, 1993 to Challa. A variety of other circuits and methods for the page latch load circuit 122, the memory cell array 126, and other memory device elements may be suitable as well.

Figure 2 shows a page latch 200 that is writable as well as readable, and is in effect an SRAM and is capable of supporting functions normally supported by SRAMS. One application is as an SRAM scratch pad for systems that need extra SRAM. For example, this is particularly useful for microcontroller systems in which the use of external SRAM is not desired. For example, the type 8051 microcontroller usually has either 128 bytes or 256 bytes

of internal SRAM but this amount of SRAM may not be enough. Hence, page latches such as 200 made internal to an EEPROM provide useful additional functionality to the overall system.

In the page latch 200 of Figure 2, transistor 202 is a column select transistor and
5 transistor 204 is a load transistor. Inverters 208 and 214 are connected back-to-back to implement a volatile memory element 206. Each inverter includes two transistors connected in a conventional manner; for example, inverter 208 includes a *p*-type transistor 210 and an *n*-type transistor 212. The N-wells of the inverters 208 and 214 are tied to VCMSTR2. Transistor 218 is switched by signal WRHV and is used to provide a suitable voltage V_{C3} for
10 writing to the array or reading from the page latch 200. Transistor 220 provides isolation so that the content of the volatile memory element 206 is not disturbed when read. Transistor 224 is a sense transistor.

The page latch 200 operates as follows. To load the page latch 200 with a "1" or a
15 "0", COLSEL goes to V_{CC} and LOAD goes to V_{CC} . If a "0" state is loaded then node 216 is "1" and if a "1" state is loaded then node 216 is "0." During erase, the word line (not shown) of the addressed sector goes high, and after erase the addressed memory cell connected to the bit line 222 is in a high V_T state ("1" state). To write to the addressed sector of the memory array involves transferring the contents of all page latches into the selected sector.
20 Illustratively, the various signals applied to the page latch 200 during a write operation are as follows: WRHV is a "1" state, V_{C3} is 4V, and the word line of the selected sector (not shown) is minus 11V. If node 216 is at a "1" state, tunneling occurs in the memory cell associated with the page latch 200 and having minus 11V on its gate and 4V on its drain, so that the memory cell goes into a low V_T (state "0"). If node 216 is at a "0" state, then the bit line 222
25 floats to "0" so that tunneling does not occur in the memory cell associated with the page latch 200 and the memory cell stays at the high V_T achieved by the ERASE operation.

The memory cell associated with the page latch 200 is read as follows. Illustratively, the various signals applied to the page latch 200 during a read operation are as follows:
30 WRHV is a "0" state (illustratively zero volts), LOAD is zero volts, SENSE is V_{CC} , COLSEL is V_{CC} , the bit line 222 is 1.5 volts, and the word line of the selected sector (not shown) is

about 3V. If the memory cell is in a low V_T state, then the sense amplifier associated with the page latch 200 and connected to node DL (data line) will detect a "0" and current flows from the sense amplifier into the memory cell. Otherwise, the memory cell is off and the Sense Amp detects a "1" state.

5

The page latch 200 is read as follows. Illustratively, the various signals applied to the page latch 200 during a read operation are the same as for reading a memory cell associated with the page latch 200, except that the word lines of the memory array are turned off (zero volts or minus 1V, for example), WRHV is V_{CC} , and V_{C3} is zero volts. If node 216 is in a "1" state, then the sense amplifier indicates a "0" state by detecting current flowing from the sense amplifier into V_{C3} . If node 216 is in a "0" state, then the sense amplifier indicates a "1" state by detecting no current flowing.

10

The page latch of Figure 2 also supports a direct transfer of the contents of an addressed sector of a memory array into the page latches of the memory array, which enables a rapid read-modify-write of one byte of the memory array. Illustratively, the sequence and values of the various signals applied to the page latch 200 during a direct-from-memory load operation are illustrated in Figure 3. During period TBUFST0, both inverters 208 and 214 are powered down by bringing VCMSTR1 and VCMSTR2 from V_{CC} to zero volts. The row deselect signal DSELROWN (active low) is also raised high in period TBUFST0. During period TBUFST1, the bitline 222 is biased to about two volts by raising VCMSTR2 to about 2 volts to power up the weak inverter 214. At this time, both LOAD and SENSE are raised high so that a current path is established through transistors 204 and 224 to the bit line 222. If the memory cell associated with the page latch 200 is on, then the bit line 222 is pulled low. Otherwise, the bit line remains at about 2 volts. During period TBUFST2, VCMSTR1 is raised to about 2 volts to power up the stronger inverter 208 and latch the logical value on the bit line 222 into the volatile cell 206. During period TBUFST3, both LOAD and SENSE are lowered to zero volts to decouple the bit line 222 from the volatile cell 206. During period TBUFST4, both VCMSTR1 and VCMSTR2 are raised to V_{CC} to strongly latch the stored value.

15

20

25

30

-7-

The sequence illustrated in Figure 3 has the further advantage of avoiding power glitches from simultaneously switching a large number of page latches, which could improperly change the state stored in the volatile cell 206. This is achieved by raising VCMSTR1 and VCMSTR2 initially to about 2 volts in the sequence shown to latch the proper value into the volatile cell 206, then by raising VCMSTR1 and VCMSTR2 to V_{CC} to strongly latch the stored value.

Figure 4 shows a page latch 400 that is writable as well as readable, and in addition includes a slave stage so that data can be transferred to the page latch 400 or read from the page latch 400 even while prior data is being written into the memory array. The page latch 400 includes the elements of the page latch 200 of Figure 2, but in addition includes elements to implement a slave stage 410 and the ability to read or write from a master stage 402. Transistor 404 controls the transfer of the value stored in the master stage 402 to the slave stage 410. The slave stage 410 includes inverters 412 and 414, which are connected back-to-back to implement a volatile memory element. Transistor 422 is switched by signal RMSTR and is used to provide a suitable voltage, in this case reference or zero volts, for reading from the master stage 402. Transistor 420 provides isolation so that the content of the volatile first stage 402 is not disturbed when read.

In the page latch 400 of Figure 4, the master stage 402 is loaded from the external interface. Just before programming, the contents of the master stage 402 is transferred into the slave stage 410. In the memory, the transfer of all the page latches to all of the slave stages occurs in parallel. The slave stage controls bit line biasing during the programming mode.

The page latch 400 operates as follows. Preferably, the master stages of the page latches of the memory are loaded one byte at a time, from the dataline 226. To load the master stage 402 with a "1" or a "0", illustratively COLSEL is high (V_{CC}), SENSE is low (zero volts), read master signal RMSTR is low, load master signal LMSTR is high, load slave signal LSLV is low, and V_{CMSTR1} and V_{CMSTR2} are V_{CC} . If a "0" state is loaded then node 216 is "1" and if "1" state is loaded then node 216 is "0."

-8-

Preferably, the master stages of the page latches of the memory are read one byte at a time using the eight sense amplifiers. To read the master stage 402, illustratively COLSEL is high, RMSTR is high, LMSTR is low, SENSE is low, LSLV is low, and V_{CMSTR1} and V_{CMSTR2} are V_{CC} . If "0" were loaded from the data line 226, node 216 would be a "1" and the sense amplifier connected to the data line 226 would sense "0".

Preferably, the transfer of data from the master stages to the slave stages of the page latches of the memory is done for all of the bytes in the sector at one time, illustratively 536 bytes at a time for an 8 Mbit device. To avoid big I_{CC} glitches that would disturb the master and slave stages of the page latches, power down techniques are used in the master-to-slave transfer operation. To perform a master-to-slave transfer, illustratively the following sequence is used. First, power down the inverters 412 and 414 of the slave stage 410 by lowering V_{CSLV} from V_{CC} to zero volts. Next, slowly ramp up LSLV and V_{CSLV} toward V_{CC} . Then, when V_{CC} is reached, change LSLV to zero volts to isolate the slave stage 410 from the master stage 402 while maintaining V_{CSLV} at V_{CC} .

Preferably, the slave stages of the page latches of the memory are read one byte at a time using the eight sense amplifiers. To read the slave stage 410, illustratively COLSEL is high, RMSTR is low, LMSTR is low, SENSE is high, LSLV is low, WRHV is high, V_{C3} is zero volts, and V_{CSLV1} and V_{CSLV2} are V_{CC} . If "0" were loaded from the data line 226, node 416 would be "1" and the sense amplifier connected to the data line 226 would sense "0".

The page latch 400 of Figure 4 also supports a direct transfer of the contents of an addressed sector of a memory array into the master stages of the page latches of the memory array, which enables a rapid read-modify-write of one byte of the memory array.

The description of the invention set forth herein is illustrative, and does not limit the scope of the invention as set forth in the following claims. Variations and modifications of the embodiments disclosed herein are possible. For example, the particular voltage values set forth herein are illustrative, but do establish relationships that enable or disable Fowler-Nordheim tunneling and reading of the memory cells. Moreover, the sizes of the various

-9-

transistors shown in the figures may be any values consistent with the operation of the page latches described herein. Moreover, typically in Flash EEPROM, sector is the same as word line. These and other variations and modifications of the embodiments disclosed herein may be made without departing from the scope and spirit of the invention.

WHAT IS CLAIMED IS:

- 5 1. A memory comprising:
a plurality of page latches, each of the page latches being loadable and readable
through a data node coupled thereto; and
a memory array having a plurality of memory cells coupled in groups to respective
column lines, the column lines being respectively coupled to the page latches.
- 10 2. A memory as in claim 1 wherein each of the page latches is a single stage.
3. A memory as in claim 1 wherein each of the page latches comprises a master stage
and a slave stage, each of the master stages being loadable and writable through a data
node coupled thereto, and each of the slave stages being loadable from a respective
master stage and readable through a data node coupled thereto.
- 15 4. A page latch comprising:
a memory element;
a load path coupled to the memory element;
a sense path coupled to the memory element; and
a bit line node coupled to the memory element.
- 20 5. A page latch as in claim 4 wherein the memory element is a volatile memory
element.
6. A page latch as in claim 5 wherein the volatile memory element comprises back-to-back
connected inverters.
7. A page latch as in claim 4 wherein the load path is coupled to a true node of the memory

-11-

element and the sense path is coupled to a complement node of the memory element, the load path and the sense path further having a common data node.

8. A page latch as in claim 4 further comprising:

5 a second memory element having an input coupled to an output of the first-mentioned memory element;

a second load path coupled to the second memory element; and

a second bit line node coupled to the second memory element.

9. A method of operating a memory comprising:

selecting all cells associated with a word line of the memory; and

10 loading data from the selected cells into all page latches of the memory.

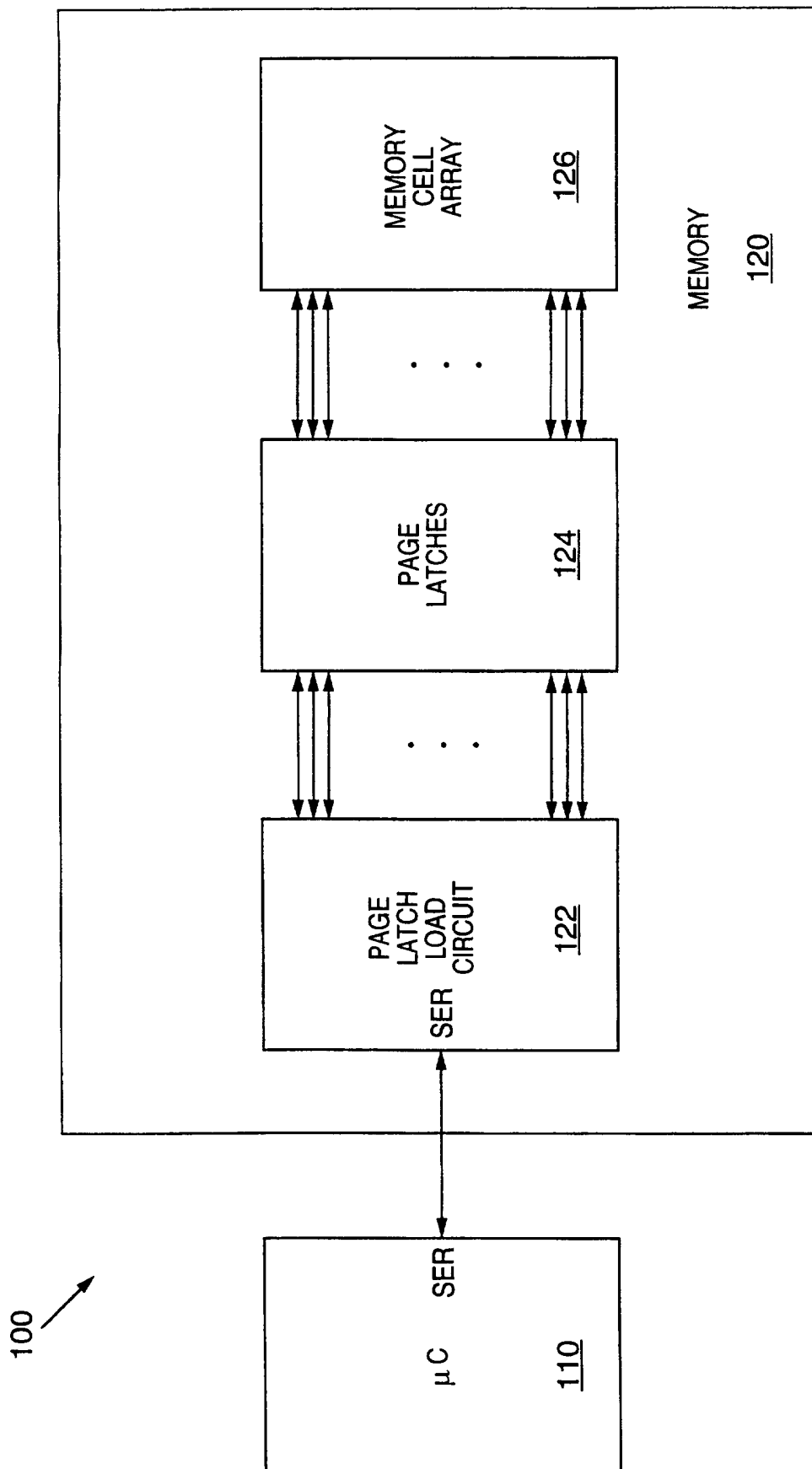


FIG. 1

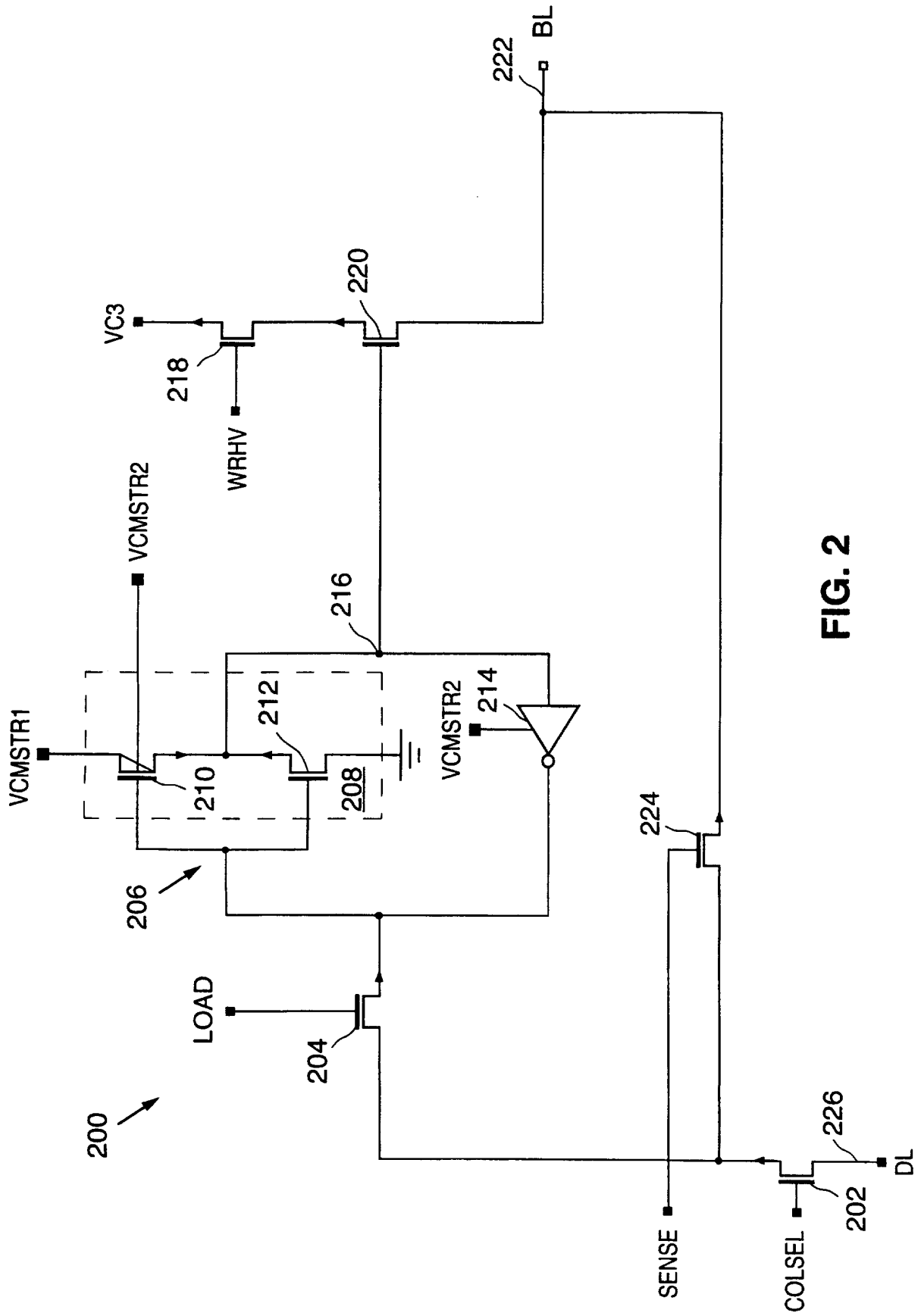


FIG. 2

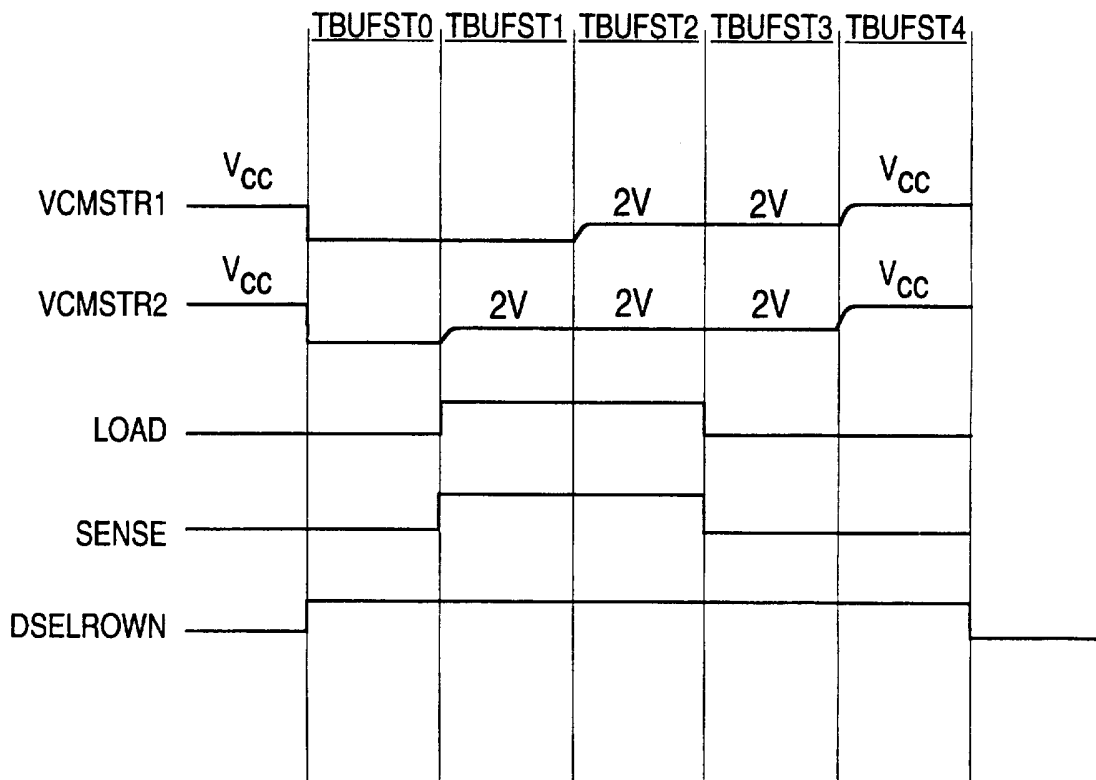


FIG. 3

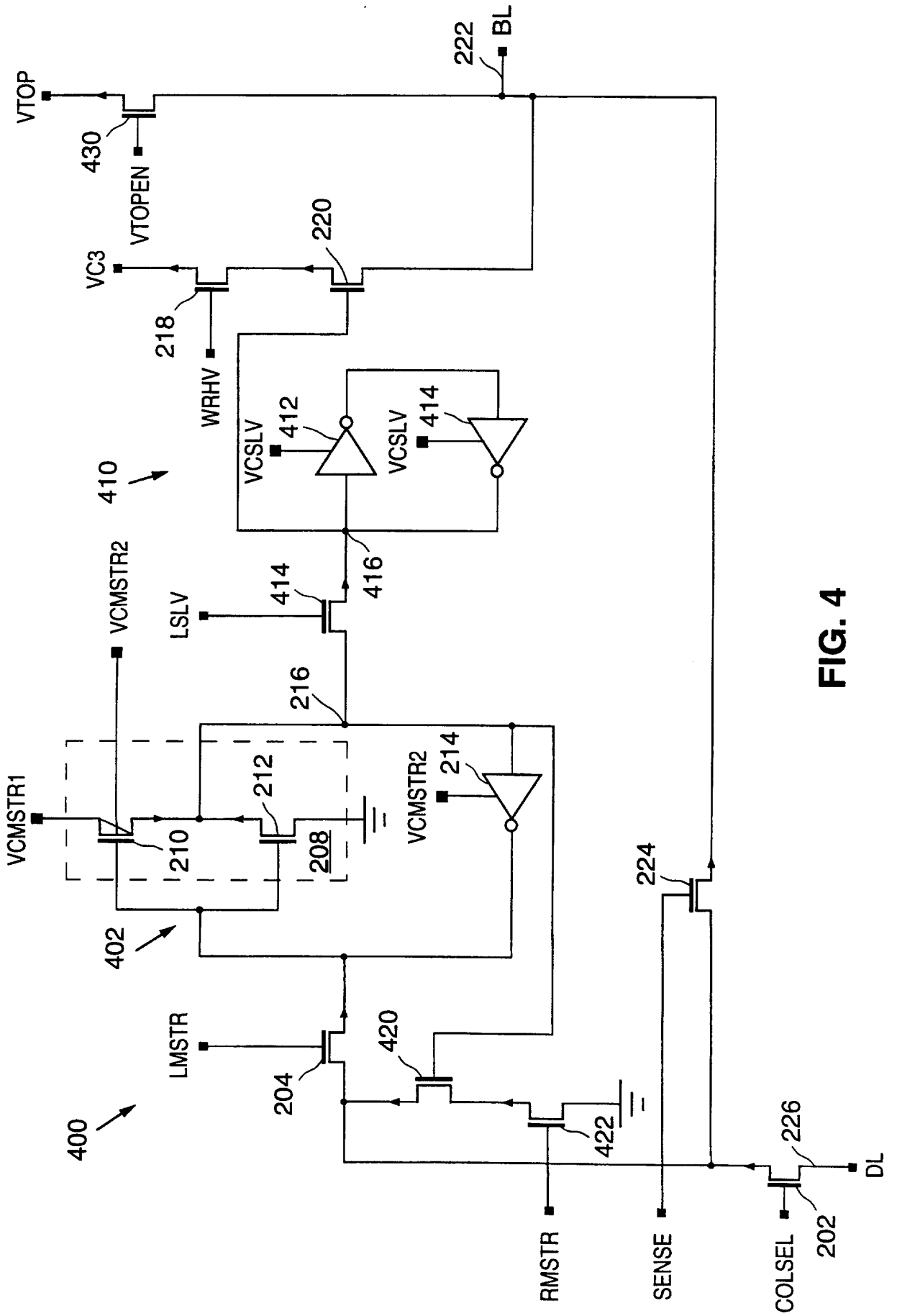


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/01567

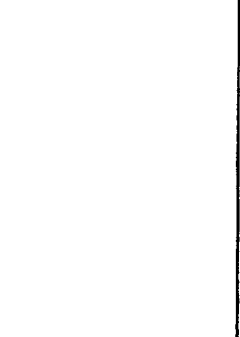
<p>A. CLASSIFICATION OF SUBJECT MATTER IPC(6) : G11C 7/00 US CL : 365/189.05, 230.08, 238.5 According to International Patent Classification (IPC) or to both national classification and IPC</p>
<p>B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) U.S. : 365/189.05, 230.08, 238.5</p>
<p>Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched NONE</p>
<p>Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) NONE</p>

C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y, P	US 5,535,159 A (NII) 09 JULY 1996 (07/09/96), See figure 12.	1-9
A	US 5,361,229 A (CHIANG ET AL) 01 NOVEMBER 1994 (11/01/94), See entire document	1-9

Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier document published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"I" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 04 JUNE 1997	Date of mailing of the international search report 16 JUL 1997
---------------------------------------------------------------------------	-------------------------------------------------------------------

Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer SON DINH  Telephone No. (703) 308-4120
-------------------------------------------------------------------------------------------------------------------------------------------------------	-----------------------------------------------------------------------------------------------------------------------------------------------------