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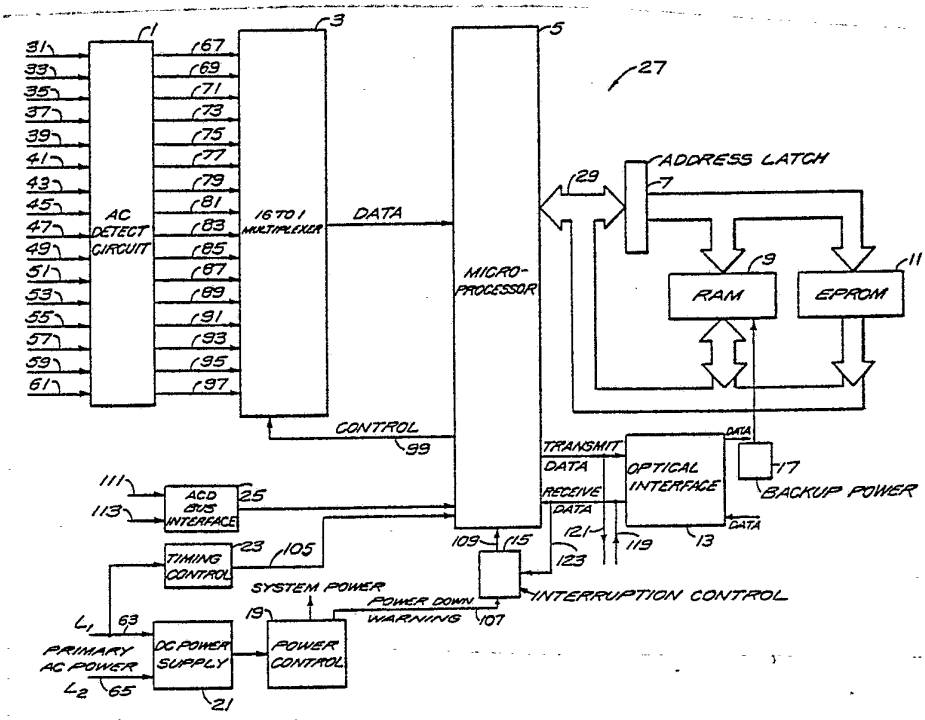
(54) Title: PROGRAMMABLE VENDING MACHINE ACCOUNTABILITY APPARATUS

(57) Abstract

Programmable accountability apparatus (27) for installation into a vending machine. The accountability apparatus includes a plurality of monitoring wires (31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 51, 53, 55, 57, 59, 61) attachable to points within the vending machine carrying AC signals selected for monitoring, circuitry (1) for converting the AC signals into digital signals, a multiplexer (3), a microprocessor (5) which is programmed to monitor and collect data from the digital signals, and a memory (9, 11) for storing both data collected from the digital signals and data for programming the microprocessor. The data for programming the microprocessor comprises a selected digital word for each monitoring wire which determines whether the occurence of the AC signal monitored by that wire is to be counted, timed or measured in duration.



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PROGRAMMABLE VENDING MACHINE ACCOUNTABILITY APPARATUS

Technical Field

This invention relates to vending machine accountability apparatus and, more particularly, to apparatus for monitoring and recording cash transactions and the occurrence of other events within a vending machine.

Background Art

In recent years, vending machines have become increasingly complex. Now, a large variety of products at a variety of prices can be dispensed by a single vending machine. In addition to coins, banknotes and credit cards can be used to obtain credit for a purchase in some systems. As an aid in the management of such machines, vending machine accountability apparatus has been developed to monitor and record electronically cash transactions and other events occurring within the machine. However, many older machines do not have such apparatus, and, where such apparatus does exist, they are inflexible in that the particular transactions or events monitored within the vending machine are fixed. Thus, vending machine managers are prohibited from temporarily or permanently varying the information recorded by this apparatus.

Disclosure of Invention

The present invention is an accountability apparatus comprising a small box which can be installed on any flat, metal surface inside a vending machine. Extending from the box are a number of monitoring wires which can be attached to wires within the vending machine carrying AC signals selected for monitoring. The apparatus can be installed in the vending machine without rewiring or other significant physical modification of the vending machine. The box contains a microprocessor and associated memory devices which store both data monitored from the vending machine and programming data for the microprocessor. The particular programming data stored depends upon the particular AC signals selected for monitoring and the particular information sought from these signals.

The accountability apparatus can monitor cash transactions as reported by the coin mechanism along with the occurrence, time and duration of events related to product vending, vending machine operation or malfunctions, and the servicing of the vending machine by route personnel. The apparatus is programmed by a central computer at the time of installation into the vending machine and can be reprogrammed by the computer for installation into a different vending machine or for monitoring different AC signals within the same vending machine. Rewiring of the vending machine or apparatus is unnecessary to effect either of these changes. Interrogation of the accountability apparatus to obtain monitored data takes place without removal of the apparatus from the vending machine through an optical data transmission link.

Brief Description of Drawings

The present invention will be understood more readily when considered together with the accompanying drawings, in which:

FIG. 1 is a schematic block diagram of a first embodiment of the invention.

FIG. 2 is a schematic diagram of a section of an AC detection circuit for the embodiment of Fig. 1.

FIG. 3 is a schematic diagram of a clock circuit for the embodiment of Fig. 1.

FIG. 4 is a schematic diagram of a DC power supply and a power control circuit for the embodiment of Fig. 1.

FIG. 5 is a schematic diagram of an interruption control circuit for the embodiment of Fig. 1.

FIG. 6 illustrates a matrix of masking data for the embodiment of Fig. 1.

FIG. 7 illustrates the format of coinage input data for the embodiment of Fig. 1.

FIG. 8 illustrates the data storage structure for the embodiment of Fig. 1.

FIG. 9 is a schematic block diagram of a second embodiment of the invention.

FIG. 10 is a schematic diagram of a credit bus interface circuit and an illustration of the signal received by this circuit for the embodiment of Fig. 9.

FIG. 11 illustrates a matrix of masking data for the embodiment of Fig. 9.

Best Mode for Carrying Out the Invention

A schematic block diagram of a programmable vending machine accountability apparatus 27 in accordance with the present invention is shown in Figure 1.

All operations of accountability apparatus 27 are controlled by a single microprocessor 5. Non-volatile, random access memory (RAM) 9 and non-volatile, electrically programmable read-only memory (EPROM) 11 are connected to microprocessor 5 through address latch 7 and communicate with microprocessor 5 over bidirectional data bus 29. RAM 9 and EPROM 11 store both data for programming the microprocessor and data monitored from the vending machine. Programming data specific to the particular signals within the vending machine monitored, and data from these signals, are stored in RAM 9.

The sixteen AC monitoring wires 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 51, 53, 55, 57, 59 and 61 are attached to wires within the vending machine carrying AC signals selected for monitoring. These AC monitoring wires simply are clipped to the selected vending machine wires, using insulation piercing clips, type no. 53440, manufactured by AMP, Inc., without modification of the vending machine's wiring scheme. The AC monitoring wires 31-61 each are connected to one section of the AC detect circuit 1. One such section is illustrated in detail in Fig. 2. AC detect circuit 1 detects the presence of AC signals on the monitoring wires having an amplitude between 20 and 135 volts. Each section of detect circuit 1 produces a logic level output indicating the presence or absence of an AC signal on its

associated monitoring wire. An output level of zero volts indicates an AC signal is present and an output level of five volts indicates the absence of an AC signal. Ground reference for detect circuit 1 is the midpoint of the primary AC input lines 63 and 65 (L_1 and L_2). This ground reference enables the AC detect circuit to react to the presence of AC signals of either L_1 or L_2 polarity.

The output of AC detect circuit 1 appears on output lines 67, 69, 71, 73, 75, 77, 79, 81, 83, 85, 87, 89, 91, 93, 95 and 97 which are connected to sixteen-to-one multiplexer 3 which is caused, by signals over control line 99 from the microprocessor, to scan these output lines continuously. Timing control circuit 23, illustrated in Fig. 3, produces a square wave signal from the L_1 primary input line 63 and supplies this signal to microprocessor 5 over line 105. This signal provides a phase and timing reference for the microprocessor which enables the microprocessor to control multiplexer 3 such that all sixteen outputs of detect circuit 1 are scanned each half-cycle of the primary AC signal. This signal also enables the microprocessor to maintain the correct reference to the L_1 or L_2 positive half-cycle.

Primary AC input lines 63 and 65 provide 115 VAC to DC power supply 21, illustrated in Figure 4, which operates in conjunction with power control circuit 19, also illustrated in Figure 4, to generate a well-regulated +5 volt DC supply for normal operation of all logic circuits. Power control circuit 19 provides a signal on line 107 warning of the imminent loss of primary power. This warning signal is supplied to interruption control circuit 15, illustrated in Figure 5, which supplies a signal

to microprocessor 5 over line 109. Upon receipt of this signal from the interruption control circuit, microprocessor 5 completes data transfers to and from RAM 9 and ensures that all data files are secure. Backup power supply 17, which comprises a long-life, non-rechargeable lithium battery, automatically supplies backup power to RAM 9 until primary power is restored.

Cash transaction data is obtained over a two-wire serial data link (referred to as the accountability display bus or ACD bus) built into coinage mechanisms recently manufactured by Mars Money Systems, Inc., of Folcroft, Pa., such as model nos. 800 and 900. Wires 111 and 113 are connected to this bus and to interface circuit 25 which accepts this data. The data, illustrated in Fig. 7, are monitored for both the total cash value of each vend and the value of each coin directed to the cashbox.

Accountability apparatus 27 receives programming data and is interrogated for monitored data through two-way LED optical interface 13 or directly, bypassing the optical interface, over wire 119. Output data from accountability apparatus 27 can pass either directly over wire 121 or through LED optical interface 13. Line 123 activates interruption control circuit 15 causing microprocessor 5 to cease scanning the AC detect circuit until interrogation or the transmission of programming data is complete.

Figure 2 illustrates one section of AC detect circuit 1. The section illustrated is that which operates in conjunction with AC monitoring wire 31 and output wire 67. AC detect circuit 1 contains sixteen such circuits, identical to that illustrated in Figure 2, for detecting AC signals on the sixteen AC monitoring wires of accountability apparatus 27.

As shown in Figure 2, monitoring wire 31 is in series with a 270K resistor. The output of this resistor is shunted to ground through a 47K resistor and connected to the base of transistor Q1. The emitter of transistor Q1 is grounded and the collector is connected to the +5 volt DC power supply through a 10K resistor. Diode D1 protects the emitter-base junction of the transistor during the negative half-cycle of AC signals appearing on monitoring wire 31. In the absence of an AC signal on the monitoring wire, transistor Q1 is in the non-conducting state and output line 67 is at +5 volts. The appearance of an AC signal on monitoring wire 31 saturates transistor Q1 and drives the voltage of output line 67 to ground. Ground reference is the midpoint of the L_1 and L_2 primary AC input lines. Thus, the input data to multiplexer 3 on line 67 and the other output lines of AC detect circuit 1 is a series of logic level pulses indicating the presence or absence of an AC signal. AC detect circuit 1 will respond with logic level outputs to AC signals having an amplitude of between 20 and 135 volts.

Figure 3 is a schematic diagram of timing control circuit 23. Line 201, which is connected to the L_1 primary AC input line, is connected to the base of transistor Q2 through a 470K resistor. The AC signal on line 201 causes transistor Q2 to alternate between the saturated and non-conducting states and produce a square-wave signal on line 205. Diode D2 protects the emitter-base junction of the transistor during the negative half-cycle of the AC signal. The square-wave signal is shaped by a .1 uf capacitor and Schmitt trigger 203 and passes on line 105 to the T1 pin of the microprocessor. This signal provides universal timing for all microprocessor

operations and enables microprocessor 5 to control multiplexer 3 such that all sixteen AC monitoring wires are scanned for input data every 8.3 MS which is one half-cycle of the primary AC input signal.

Figure 4 is a schematic diagram of DC power supply circuit 21 and power control circuit 19. The power supply circuit receives primary AC input over wires 63 and 65 which are isolated from each other by transient suppression device 307 and two 100K resistors. DC ground is referenced between these two 100K resistors. The primary AC voltage is reduced by transformer 309 and rectified by full-wave bridge rectifier 301. A 22 uf filter capacitor and regulator 303 produce a +5 volt DC output. LED 311 in series with 470 ohm resistor 315 provides a "power on" indication. The large 2200 uf capacitor assures that power supply 21 will provide DC power for a sufficient time after an AC power outage for microprocessor 5 to complete the tasks necessary to prevent the loss of data. The zener diode 305 permits current to flow through the 10K resistor putting a positive voltage on the emitter-base junction of transistor Q3. This voltage causes current to flow through the 1K resistor connected to the collector of this transistor. An AC power outage is detected by zener diode 305 which stops conducting immediately upon such an occurrence causing transistor Q3 to become inactive. A signal of +5 volts appears on line 107 which is connected to the interruption control circuit 15. This circuit signals microprocessor 5 to secure data and prepare for the loss of primary power.

Figure 5 is a schematic diagram of interruption control circuit 15. The signal on power-down warning line 107 goes to +5V immediately

after the interruption of primary AC power. This signal saturates transistor Q4 grounding both inputs of NOR gate 405 whose output on line 407 goes to +5V. This output is applied to the P1-2 pin of microprocessor 5 and to one input of NOR gate 403. If programming or interrogation data is not being received by microprocessor 5, the second input of NOR gate 403 on line 409 is at ground, and, therefore, the +5V signal on line 407 causes the output of NOR gate 403 to go to ground. This output from NOR gate 403 goes to the interrupt (INT) pin of microprocessor 5 causing the microprocessor to terminate scanning the outputs of AC detect circuits 1 and to prepare for the cessation of primary AC power.

The initial receipt of incoming programming or interrogation data on wire 411 causes the signal on this wire to go to ground. Inverter 401 inverts this signal and applies it, across diode D3 in parallel with a 2K resistor, to one input of NOR gate 403 on line 409 causing the output of this NOR gate to go to ground. This output from the NOR gate causes microprocessor 5 to interrupt the scanning of AC monitoring wires and to receive programming or interrogation instructions.

The resumption of primary AC power causes transistor Q4 to return to the non-conducting state and +5V to appear at the reset (RST) pin of the microprocessor. If no data is incoming on line 411, the microprocessor causes multiplexer 3 to resume scanning the outputs of AC detect circuits 1. A signal on reset line 413 causes the resumption of scanning following receipt and servicing of programminng and interrogation instructions.

Accountability apparatus 27 is specifically programmed by a central computer for the particular

vending machine into which it is to be installed and for the particular AC signals within the vending machine selected for monitoring. This programming of the accountability apparatus is accomplished by storing a series of sixteen bytes (eight bits each) of programming data in RAM 9. These sixteen bytes of programming data, referred to as "mask bytes," guide microprocessor 5 in the interpretation and processing of data as it appears on the sixteen AC monitoring wires. A serial number and a security code, each comprising six hexadecimal characters, also are stored in RAM 9. The serial number is part of all messages from the accountability apparatus to identify the source of the data. The security code precedes each interrogation request. Microprocessor 5 compares the transmitted security code with the code stored in RAM 9 and, if the two codes match, the interrogation protocol is allowed to proceed. If the codes do not match, microprocessor 5 will refuse all interrogation requests for a one minute period. This refusal renders impractical any efforts to determine the security code by a series of messages containing all possible security codes.

Accountability apparatus 27 can be programmed (1) to count events associated with the delivery of products in return for deposited cash ("vend events"), (2) to count events not timed with product delivery such as compressor actuations ("counted events"), (3) to record the time and date on which an event occurs such as the time and date on which cups are sold-out ("timed events"), and (4) to record both the time and date on which an event occurs and the duration of the event such as the time, date and duration of a door opening ("time and duration events"). In addition, when accountability

apparatus 27 is installed in vending machines containing coinage mechanisms recently manufactured by Mars Money Systems, Inc., the accountability apparatus can be programmed to record both the total cash value of each vend and the value of each coin directed to the cash box. A maximum of sixteen AC signals (not including cash transaction signals on the ACD bus) can be monitored for events in any of the four categories listed above.

The mask bytes program the microprocessor for the particular characteristics of each AC signal selected for monitoring and for the particular data sought from each signal. The upper table in Figure 6 illustrates a matrix of masking data in which each column represents a mask byte for interpreting the data appearing on one AC monitoring wire. Each mask byte answers the following eight questions regarding the data appearing on the monitoring wire:

(1) If the signal monitored is a vend event, does the signal occur before the vend-in-progress signal ("VIP" signal) from the vending machine? A "1" means yes and a "0" means no.

(2) If the signal monitored is a vend event, does the signal occur after the VIP signal? A "1" means yes and a "0" means no.

(3) Is the monitoring wire monitoring a counted event? A "1" means yes and a "0" means no.

(4) Is the monitoring wire monitoring a timed event? A "1" means yes and a "0" means no.

(5) Is the monitored signal referenced to the L_1 or L_2 positive half-cycle of the primary AC signal? A "1" means the reference is to L_1 and a "0" means the reference is to L_2.

(6) Does the monitored signal have a short duration (less than 48 MS) or a long duration

(greater than 48 MS)? A "1" means the duration is short and a "0" means the duration is long.

(7) Is the monitored signal normally present or normally absent? A "1" means the signal is normally absent and a "0" means the signal is normally present.

(8) Is the monitoring wire monitoring a time and duration event? A "1" means yes and a "0" means no.

If any of the AC signals monitored are vend events, then the first monitoring wire (monitoring wire 31 in Fig. 6) must be connected to the VIP signal from the vending machine. This signal is always an open circuit when a vend occurs. Both VIP bits are "0" and the counted event bit is "1" for the byte defining the signal on this monitoring wire. AC signals monitored for vend events must be assigned to consecutive monitoring wires beginning with the second monitoring wire. Either the "before VIP" or the "after VIP" bits must be "1" for the bytes defining the signals on these wires (monitoring wires 33, 35, 37, 39, 41 and 43 in Fig. 6). AC signals monitored for counted events must be assigned to consecutive monitoring wires beginning with the first wire immediately following the last wire monitoring a vend event. No wire in Fig. 6 is monitoring a counted event. AC signals monitored for timed events must be assigned to consecutive monitoring wires beginning with the first wire immediately following the last wire monitoring a counted event. Monitoring wires 45, 47, 49, 51, 53 and 55 in Fig. 6 are assigned to monitor timed events. AC signals monitored for time and duration events must be assigned to consecutive monitoring wires beginning with the first wire immediately following the last

wire monitoring an event in the first three categories. Monitoring wire 57 in Fig. 6 is assigned to monitor a time and duration event. If the first, second, third, fourth and eighth bits of the mask byte defining the signal on a monitoring wire are all "0", i.e., if the monitored event is neither in the vend, counted, timed nor time and duration categories, then the wire is unused (monitoring wires 59 and 61 in Fig. 6). Unused wires must follow all used wires. More than one monitoring wire can be assigned to the same signal if, for example, the event defined by that signal is to be both timed and counted.

The matrix of masking data is arranged as a linear series of thirty-two hexadecimal characters as illustrated in the lower table in Fig. 6. Each character represents four consecutive bits of the mask matrix proceeding from right to left across each row, beginning with the top row and proceeding continuously through the bottom row. This linear format is used to program the masking data serially into RAM 9 of accountability apparatus 27.

Multiplexer 3 scans all outputs of AC detect circuit 1 once during each half-cycle of the primary AC signal. During each half-cycle scan, microprocessor 5 refers to the L_1 and L_2 bits of each mask byte to select data for processing only from signals referenced to that half-cycle. The absent/present bits are used to select data for processing only from those input signals in an "activated" state (the state opposite their normal state). After each full cycle of the primary AC signal, microprocessor 5 generates a "sample word" of two bytes (sixteen bits) in which each "1" indicates detection of a signal activated during the half-cycle

to which the signal is referenced. For each "1", the microprocessor refers to the long/short bit of the mask byte defining that signal. If this bit is "0" (long duration), the sample word is registered in a "long stack," and if this bit is "1" (short duration), the sample word is registered in a "short stack."

The long stack is used to detect AC events lasting longer than three cycles of the primary AC signal (48 MS). This stack contains three successive sample words. If the same bit is "1" in all three samples, a "1" is set in a bit of a long "status word" indicating detection of the event represented by that bit. Similarly, three successive samples in which this bit is "0" causes a "0" to be set in this bit of the status word indicating the failure to detect this monitored event.

The short stack is used to detect AC events lasting less than three cycles of the primary AC signal. This stack contains the current sample word and also, if there is a change in any bit of the current sample word, the previous sample word. If a bit of the current sample is "1" and the same bit in the previous sample is "0", a "status flag" for that bit is set indicating detection of the event represented by that bit. The status flag is reset when this bit in the current sample is "0" and the same bit of the previous sample is "1".

After confirmation of a monitored event, microprocessor 5 interrogates the active signal's mask byte to determine the type of event, i.e., whether vend, counted, timed or time and duration, and, if a vend event, its relationship to the VIP signal. If the event is in the vend or counted categories, microprocessor 5 increments a counter for

that event and the new count is stored in RAM 9. If the event is timed, the microprocessor stores the time on which the event occurs in the data file in RAM 9 for that event. The microprocessor is programmed to keep elapsed time continuously. If the event is of the time and duration category, the microprocessor stores both the time and date of the event and its duration in RAM 9. Duration is determined using a timer, internal to the microprocessor, which is activated and deactivated at the initiation and termination of the event, respectively.

Figure 7 illustrates the format of input data on the ACD bus from the coinage mechanism. Each message contains six characters transmitted at 1200 baud in an asynchronous manner. Each character comprises a start bit, eight data bits and a stop bit. The characters are grouped into three identical pairs with each pair comprising an address character for identification of the message, followed by a value character. The pair is transmitted three times to allow redundancy checking which avoids data errors resulting from noise. The signal on the ACD bus is normally at +5 V (logical "1") and falls to 0 volts for the start bit. The stop bit for each character remains at +5V for at least one bit period. Addresses 01 and 03 indicate coin-to-cashbox and vended-cash messages, respectively. Microprocessor 5 ignores all other messages appearing on the ACD bus. The value character has a range of between 1 and 255 with each unit representing five cents.

The storage of monitored data in RAM 9 is organized into four storage fields as illustrated in Fig. 8. These fields are: 1) the fixed field; 2) the counted and vend event field; 3) the timed event

field; and 4) the time and duration event field. The data files in each field are updated continuously as monitoring of vending machine operations proceeds.

If accountability device 27 monitors an ACD bus, the fixed-field storage configuration comprises thirty-two hexadecimal characters. If accountability device 27 does not monitor an ACD bus, the twelve characters allocated to storage of this data are not updated. The fixed field is organized and defined as the following table indicates.

Parameter	Length	Units	Range
Serial Number	6 char.	N/A	000000 to 999999
Vended Cash	6 char.	5 cents	0 to $838,860.75
Cashbox Cash	6 char.	5 cents	0 to $838,860.75
Vend Count	6 char.	1 cnt.	0 to 65,535
INT. Complete	2 char.	1 cnt.	0 to 255
INT. Refused	2 char.	1 cnt.	0 to 255
Elapsed Time	4 char.	6 min.	0 to 273 days

The serial number file stores an arbitrary number selected to identify the accountability apparatus. The elapsed time file indicates the state of a counter, internal to the microprocessor, which increments as long as primary power is applied to the apparatus. The state of this counter is used to measure elapsed time on a continuous basis. The remaining files in the fixed field accumulate data continuously beginning with the time of initiation of monitoring of the vending machine by the accountability apparatus. The vended cash file, containing data obtained from the ACD bus, indicates the total cash value of all product vends. The cashbox cash file, whose data also are obtained from the ACD bus, indicates the total value of all coins directed to the cashbox. The vend count file indicates the total number of vends of all products from the vending machine.

The interrogation complete and interrogation refused files indicate the total number of successful and the total number of unsuccessful interrogations of the accountability apparatus, respectively.

The remaining data fields in RAM 9 are of variable length depending upon the number of vend, counted, timed, and time and duration events for which the accountability apparatus is programmed to monitor. Four characters are allocated to each monitored event in the counted and vend event field enabling storage of up to 65,535 counts. This field accumulates data continuously beginning with the time of initiation of monitoring of the vending machine by the accountability device.

The characters allocated to each monitored event in both the timed and the time and duration fields are organized into three groups containing data for the most recent three occurrences of the event monitored. Four characters are allocated to each group in the timed event field enabling recordation of the elapsed time (to the nearest six minutes) of an occurrence. The time and duration event field has an allocation of six characters per group with four characters allocated to the time of the event and two allocated to its duration. The information recorded as to the time of the event is identical to that in the timed event field. The duration characters record duration to the nearest six minutes and have a range of up to twenty-five days. Events lasting less than one minute are not recorded.

The embodiment of the present invention illustrated in Figure 1 was designed with the following components:

Microprocessor 5:	Part No. 8748 manufactured by Intel.
Address Latch 7:	Part No. 74C373 manufactured by National Semiconductor.
RAM 9:	Part No. 5101L manufactured by Intel (storage capacity 128 x 8).
EPROM 11:	Part No. 2758 manufactured by Intel.
Multiplexer 3:	Part No. 74C150 manufactured by National Semiconductor.

A schematic block diagram of a second embodiment of a programmable accountability apparatus in accordance with the present invention is shown in Figure 9. Accountability apparatus 501 is controlled by microprocessor 503. RAM 505 and EPROM 507 store programming and monitoring data and work in conjunction with microprocessor 503 through address latch 515 in a manner similar to RAM 9 and EPROM 11 of accountability apparatus 27. Primary AC input lines L_1 and L_2 provide 115 VAC to DC power supply 509 which operates with power control circuit 511 to generate a system power supply of +5V. Power line 513 from power control circuit 511 provides power to RAM 505. Backup power supply 514, comprising a long-life lithium battery, is connected to power control circuit 511 and keeps

power line 513 to RAM 505 active even if primary AC power is lost. Optical interface circuits 517, interruption control circuit 519, timing control circuit 521 and ACD bus interface circuit 523 perform substantially the same functions as optical interface circuit 13, interruption control circuit 15, timing control circuit 23 and ACD bus interface circuit 25 of accountability device 27.

AC detect circuit 525 comprises twenty-four AC monitoring wires 542-565 for attachment to selected AC monitoring points within the vending machine and twenty-four output wires which are connected to multiplexer 567. Each AC monitoring wire is connected to a section of the AC detect circuit, substantially similar to the section illustrated in Fig. 2 for accountability apparatus 27, which produces a logic level output (OV or +5V) indicating the presence or absence of an AC signal.

Accountability apparatus 501 also contains credit bus interface circuit 527, test vend switch 529 and status indicator 531. Credit bus interface circuit 527 is connected to the credit bus (also referred to as the cash counter) of coinage mechanisms not containing an ACD bus. The signal on the credit bus is used to determine the total cash value of each completed vend. Test vend switch 529 enables route personnel to test vend a machine after product loading or maintenance without updating data files. Each activation of this switch causes microprocessor 503 to enter a test-vend mode for one minute. During this period, the microprocessor updates a counter to reflect the total number of test vends performed. Status indicator 531 comprises an LED which glows steadily

while accountability apparatus 501 is operating and which flashes when microprocessor 503 is in the test-vend mode. Microprocessor 503 also updates a counter to reflect the total number of free vends, i.e., vends which occur when the microprocessor is neither in the test vend mode nor in receipt of a corresponding signal from the coinage mechanism via ACD bus interface 523 or credit bus interface 527.

Figure 10 is a schematic of credit bus interface circuit 527 and the signal appearing on the credit bus. This signal consists of a series of pulses having an amplitude of 12V and a duration of 50MS. Each pulse corresponds to five cents. The total number of pulses multiplied by five cents is the total cash value of a completed vend.

Credit bus interface 527 comprises a 2K resistor in series with optical coupler 533. Diode 539 protects LED section 537 of optical coupler 533 from negative swings of the signal on the credit bus. During the +12V positive half-cycle of the credit bus signal, current flows through LED section 537 of optical coupler 533, phototransistor section 535 of the coupler is in the conducting state, and the voltage on data line 541 goes to ground. When the signal on the credit bus is at ground, no current flows through LED section 537, phototransistor section 535 is in the non-conducting state and the voltage on data line 541 goes to +5V. The resulting signal on data line 541, which is connected to microprocessor 503, is a series of pulses, alternating between +5V and ground, each representing five cents in value.

The mask matrix for programming accountability apparatus 501, illustrated in Figure 11, is a modification of the matrix used for

programming accountability apparatus 27. The mask word defining the signal appearing on each monitoring wire contains seven bits rather than eight because there is no timed event category. For all timed events, a determination of duration also is made which results in all timed events being time and duration events. The meaning of each bit of the mask words for accountability apparatus 501 is the same as for corresponding bits of the mask bytes for accountability apparatus 27, except that the counted event bit is "1" for all wires monitoring both counted events and vend events. As with accountability apparatus 27, if any of the events monitored are vend events, the first monitoring wire (monitoring wire 542 in Fig. 11) must be connected to the VIP signal from the vending machine, and both VIP bits must be "0" for the word defining the signal on this monitoring wire. AC signals monitored for vend events must be assigned to consecutive monitoring wires beginning with the second monitoring wire, and one of the VIP bits must be "1" for the words defining the signals on these wires (monitoring wires 543, 544, 545, 546, 547, 548 and 549 in Fig. 11). AC signals monitored for counted events must be assigned to consecutive monitoring wires beginning with the first wire immediately following the last wire monitoring a vend event. Both VIP bits are "0" for these wires (monitoring wires 550, 551 and 552 in Fig. 11). AC signals monitored for time and duration events must be assigned to consecutive monitoring wires beginning with the first wire immediately following the last wire monitoring a counted event. Monitoring wires 553, 554, 555, 556, 557, 558, 559, 560 and 561 in Fig. 11 are assigned to monitor time and duration events.

Unused wires (monitoring wires 562, 563, 564 and 565 in Fig. 11) must follow the last wire monitoring a time and duration event. Both the counted-event and the time-and-duration-event bits are "0" for unused wires.

The matrix of masking data for accountability apparatus 501 is arranged as a series of forty-two hexadecimal characters with each character representing four consecutive bits of the mask matrix proceeding from left to right across each row beginning with the top row and proceeding continuously through the bottom row. This string of characters is programmed serially into RAM 505 of accountability apparatus 501.

The format for storage of monitored data in RAM 505 of accountability apparatus 501 is identical to that illustrated in Figure 8 for RAM 9 of accountability apparatus 27 with the following exceptions: 1) The fixed field contains forty characters rather than thirty-two. The additional eight characters are assigned equally to files for recording the total number of test vends and files for recording the total number of free vends. The range for both files is 0 to 65,535 counts. 2) Since no events are merely timed (a determination of duration also is made), there are only two fields of variable length, the counted and vend event field and the time and duration event field.

The embodiment of the present invention illustrated in Figure 9 was constructed with the following components:

Microprocessor 503: Part No. 8035 manufactured by Intel.

Address Latch 515: Part No. 74L5373 manufactured by National Semiconductor.

RAM 505: Constructed using two identical 256 x 4 CMOS RAM's. Each is Part No. HM-6561 manufactured by Harris Semiconductor.

EPROM 507: Part No. 2716 manufactured by Intel. (Storage capacity 2K x 8.)

Multiplexer 567: Constructed using three identical multiplexer units. Each is Part No. 74C244 manufactured by National Semiconductor.

I claim:

1. A programmable accountability apparatus for a vending machine comprising

a plurality of monitoring wires attachable to points within the vending machine carrying AC signals selected for monitoring,

means for converting the AC signals to digital signals,

a microprocessor programmed to monitor and collect data from the digital signals,

a memory, operatively associated with the microprocessor, for storing both data collected from the digital signals and data for programming the microprocessor, the data for programming the microprocessor comprising a selected digital word for each monitoring wire, the word selected for each wire determining the data collected and stored by the microprocessor upon the occurrence of the AC signal monitored by that wire.

2. The accountability apparatus of claim 1 wherein the data collected by the microprocessor upon the occurrence of the AC signal on a monitoring wire indicates either the count, time or duration of the AC signal.

3. The accountability apparatus of claim 1 further comprising an interface circuit for receiving a digital signal from the vending machine's coinage mechanism, wherein the microprocessor stores data from this signal indicating the total cash value of completed vends.

4. The accountability apparatus of claim 3 wherein the data stored from the signal from the vending machine's coinage mechanism also indicates the value of coins directed to the cash box.

5. The accountability apparatus of claim 1 wherein the number of monitoring wires is sixteen.

6. The accountability apparatus of claim 1 wherein the number of monitoring wires is twenty-four.

7. The accountability apparatus of claim 2 wherein the selected digital word for each monitoring wire comprises eight bits.

8. The accountability apparatus of claim 7 wherein one bit of the selected digital word determines whether the occurrence of the AC signal is to be counted, a second bit determines whether the occurrence of the AC signal is to be timed, a third bit determines whether the occurrence of the AC signal is to be both timed and measured in duration, a fourth bit indicates whether the AC signal occurs before the vend-in-progress signal from the vending machine, a fifth bit indicates whether the AC signal occurs after the vend-in-progress signal from the vending machine, a sixth bit indicates whether the AC signal is of short or long duration, a seventh bit indicates whether the AC signal is normally absent or normally present, and an eighth bit indicates whether the AC signal is referenced to the first or second positive half-cycle of the primary AC signal powering the vending machine.

9. The accountability apparatus of claim 2 wherein the selected digital word for each monitoring wire comprises seven bits.

10. The accountability apparatus of claim 9 wherein one bit of the selected digital word determines whether the occurrence of the AC signal is to be counted, a second bit determines

whether the occurrence of the AC signal is to be both timed and measured in duration, a third bit indicates whether the AC signal occurs before the vend-in-progress signal from the vending machine, a fourth bit indicates whether the AC signal occurs after the vend-in-progress signal from the vending machine, a fifth bit indicates whether the AC signal is of short or long duration, a sixth bit indicates whether the AC signal is normally absent or normally present, and a seventh bit indicates whether the AC signal is referenced to the first or second positive half-cycle of the primary AC signal powering the vending machine.

11. The accountability apparatus of claim 1 wherein the digital words for programming the microprocessor are transmitted into the memory as a series of hexadecimal characters.

12. The accountability apparatus of claim 1 wherein the data collected from the wires monitoring AC signals are stored in assigned fields of variable length in the memory.

13. The accountability apparatus of claim 12 wherein one memory field is assigned to store data collected from wires monitoring AC signals whose occurrences are counted and a second memory field is assigned to store data collected from wires monitoring AC signals whose occurrences are both timed and measured in duration.

14. The accountability apparatus of claim 13 wherein a third memory field is assigned to store data collected from wires monitoring AC signals whose occurrences are timed.

15. The accountability apparatus of claim 13 or 14 further comprising a monitored-data storage field in memory of fixed length.

16. The accountability apparatus of claim 13 wherein the data collected from each wire monitoring AC signals whose occurrences are counted are stored as four hexadecimal characters, and the data collected from each wire monitoring AC signals whose occurrences are both timed and measured in duration are stored as eighteen hexadecimal characters.

17. The accountability apparatus of claim 14 wherein the data collected from each wire monitoring AC signals whose occurrences are counted are stored as four hexadecimal characters, the data collected from each wire monitoring AC signals whose occurrences are timed are stored as twelve hexadecimal characters, and the data collected from each wire monitoring signals whose occurrences are both timed and measured in duration are stored as eighteen hexadecimal characters.

18. The accountability apparatus of claim 16 or 17 wherein the data stored from wires monitoring AC signals whose occurrences are both timed and measured in duration comprises data indicating the time and duration for the most recent three occurrences of the signal on each wire, wherein the time for each occurrence is stored as four hexadecimal characters and the duration of each occurrence is stored as two hexadecimal characters.

19. The accountability apparatus of claim 17 wherein the data stored from wires monitoring AC signals whose occurrences are timed comprises data indicating the time of the most recent three occurrences of the signal on each wire, wherein the time of each occurrence is stored as four hexadecimal characters.

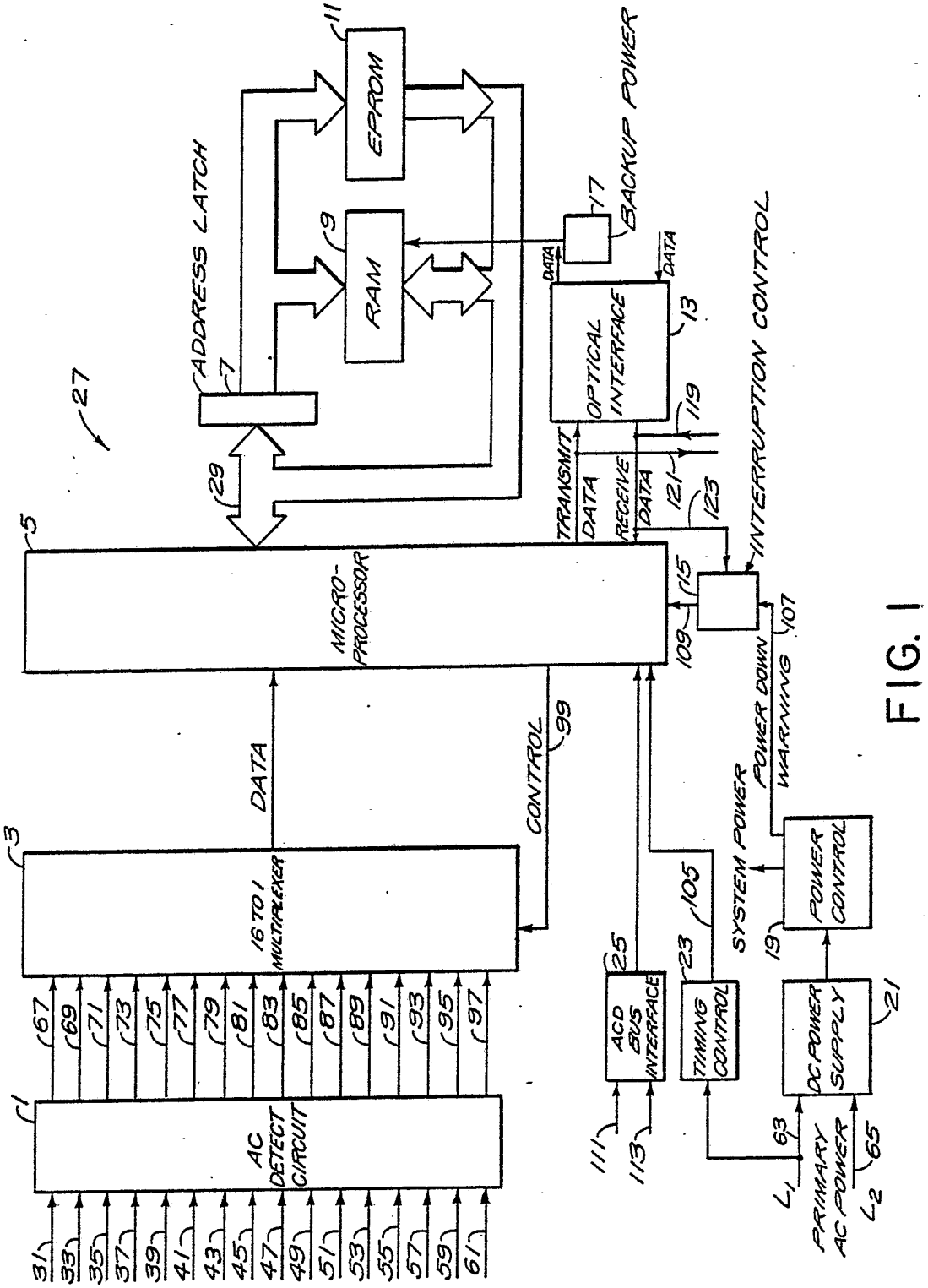

FIG. 1

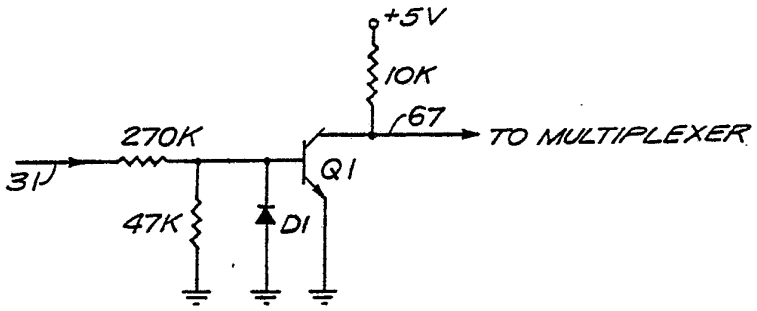

FIG. 2

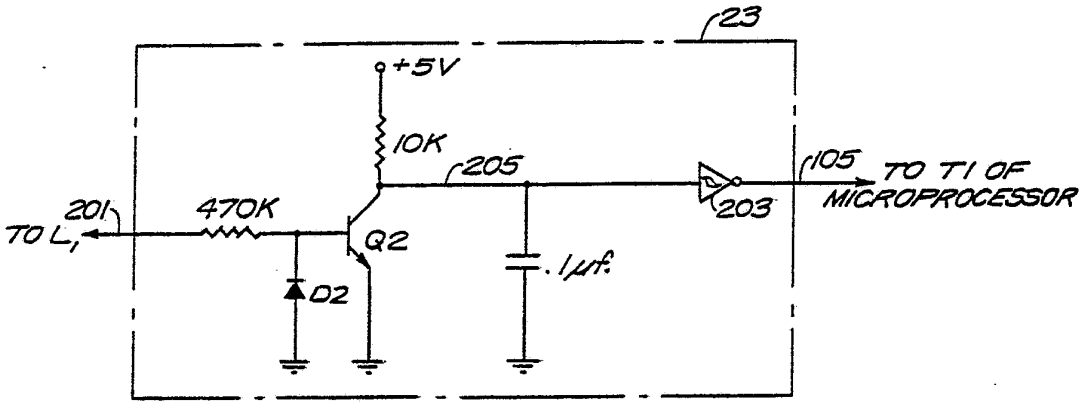

FIG. 3

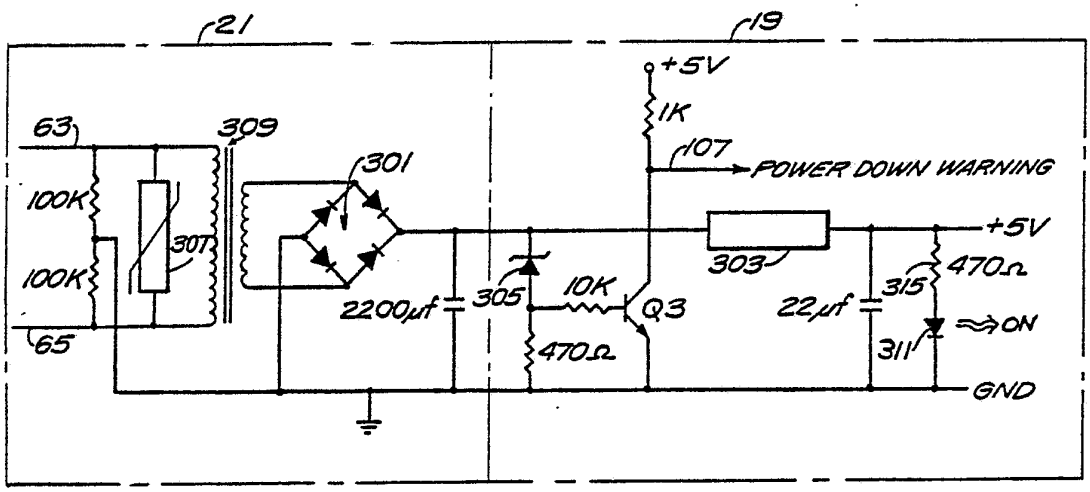

FIG. 4

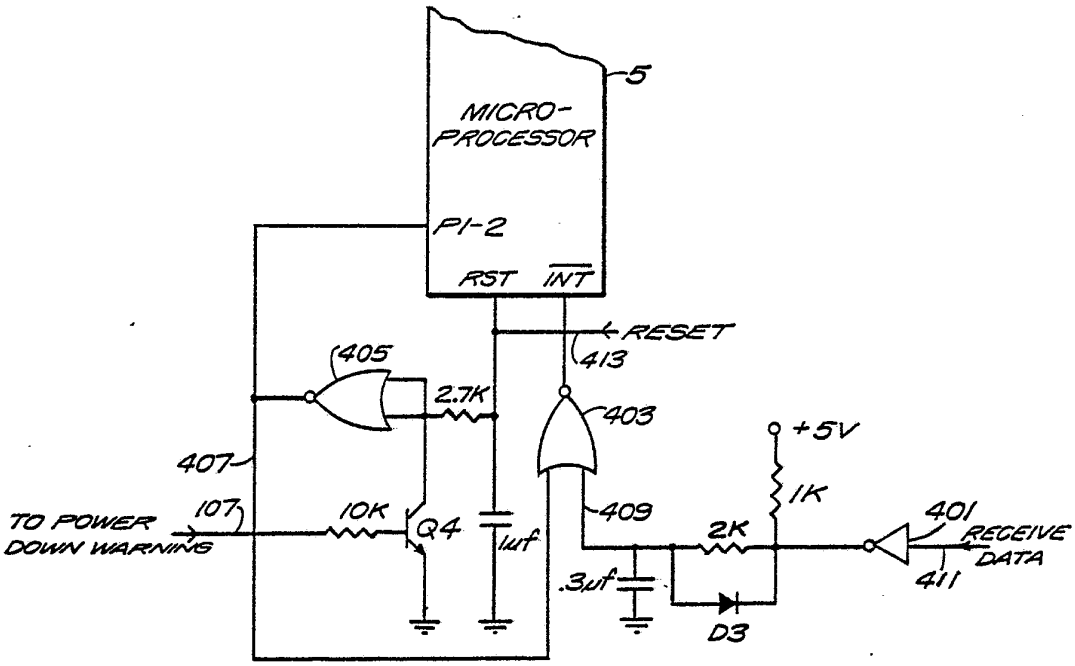

FIG. 5

FORMAT OF COINAGE INPUT DATA

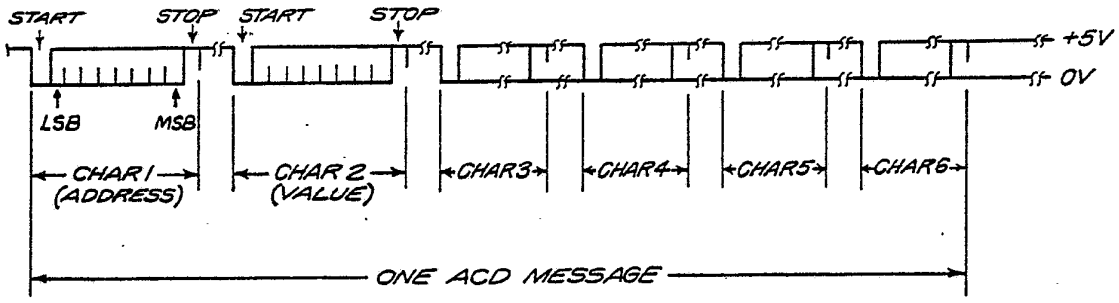

FIG. 7

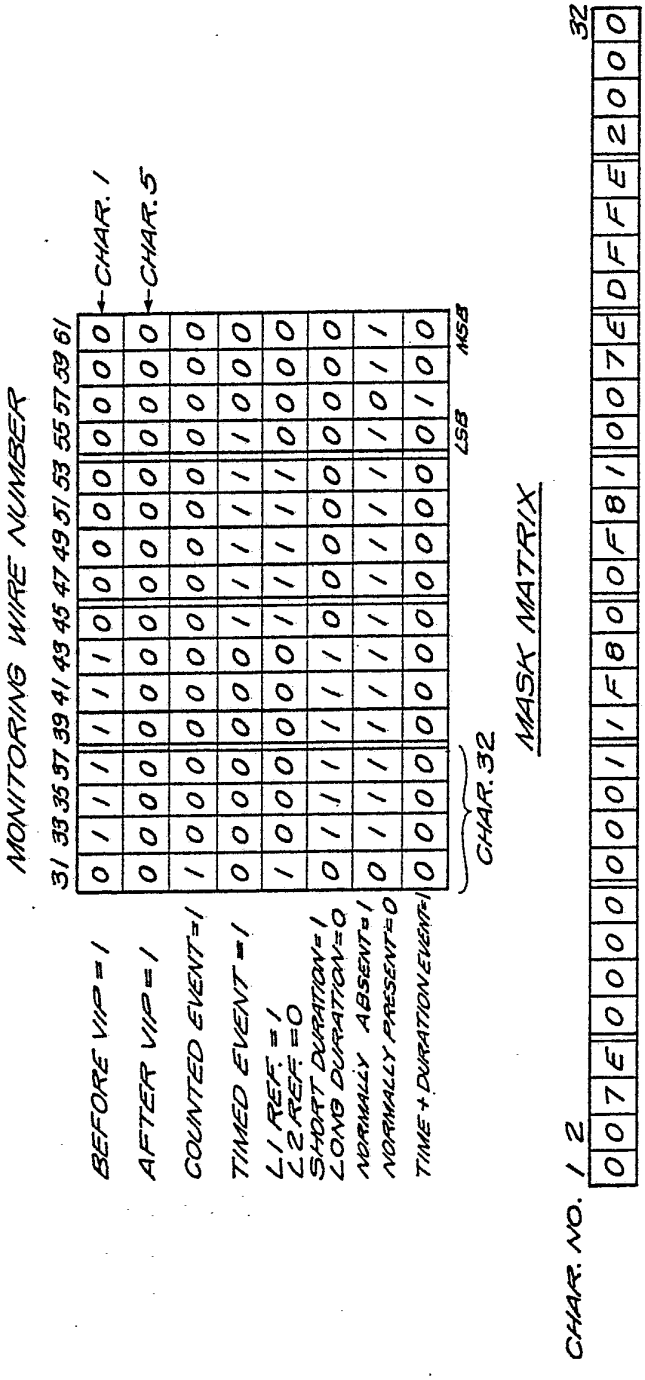

FIG. 6

MONITORED DATA STORAGE STRUCTURE

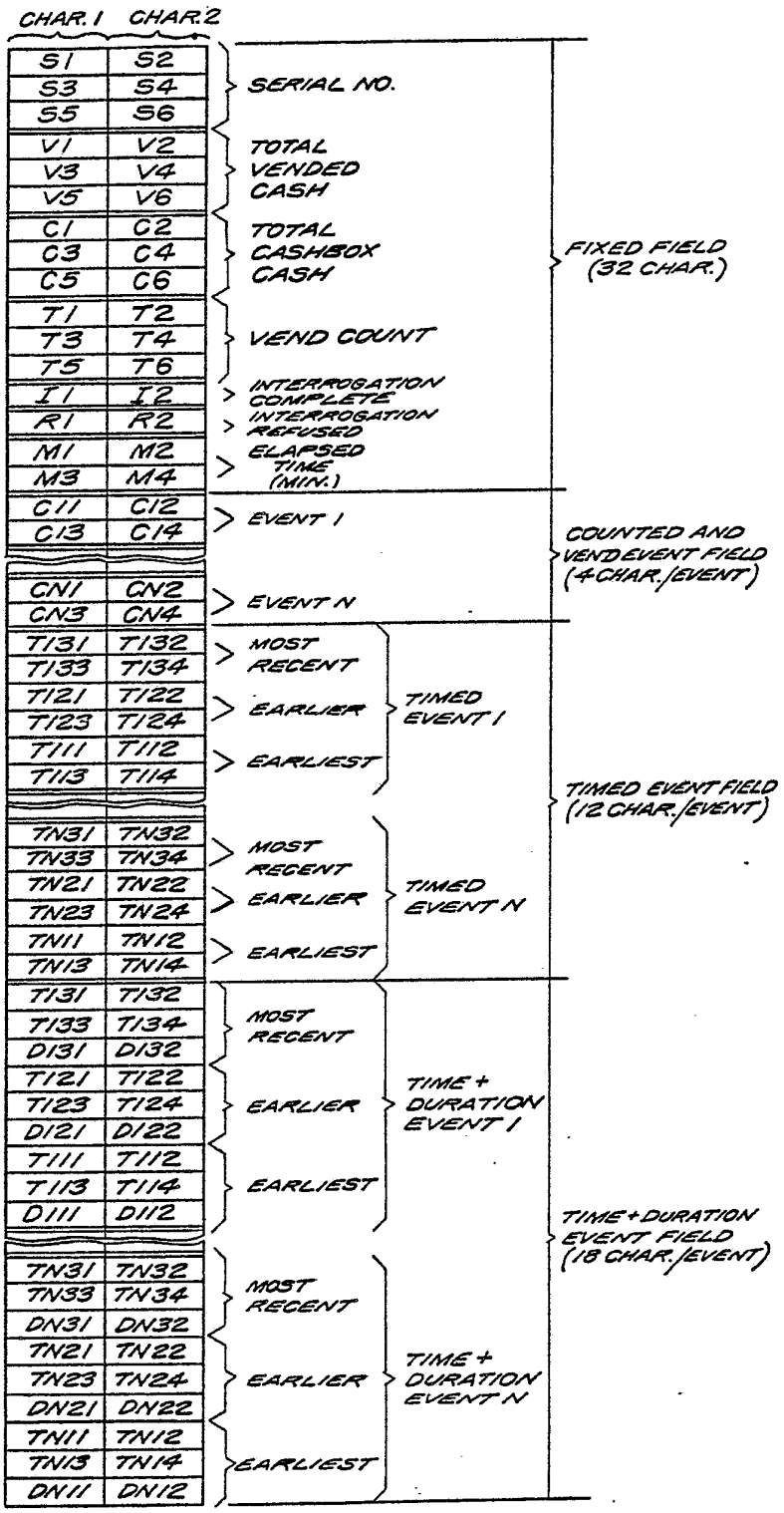

FIG. 8

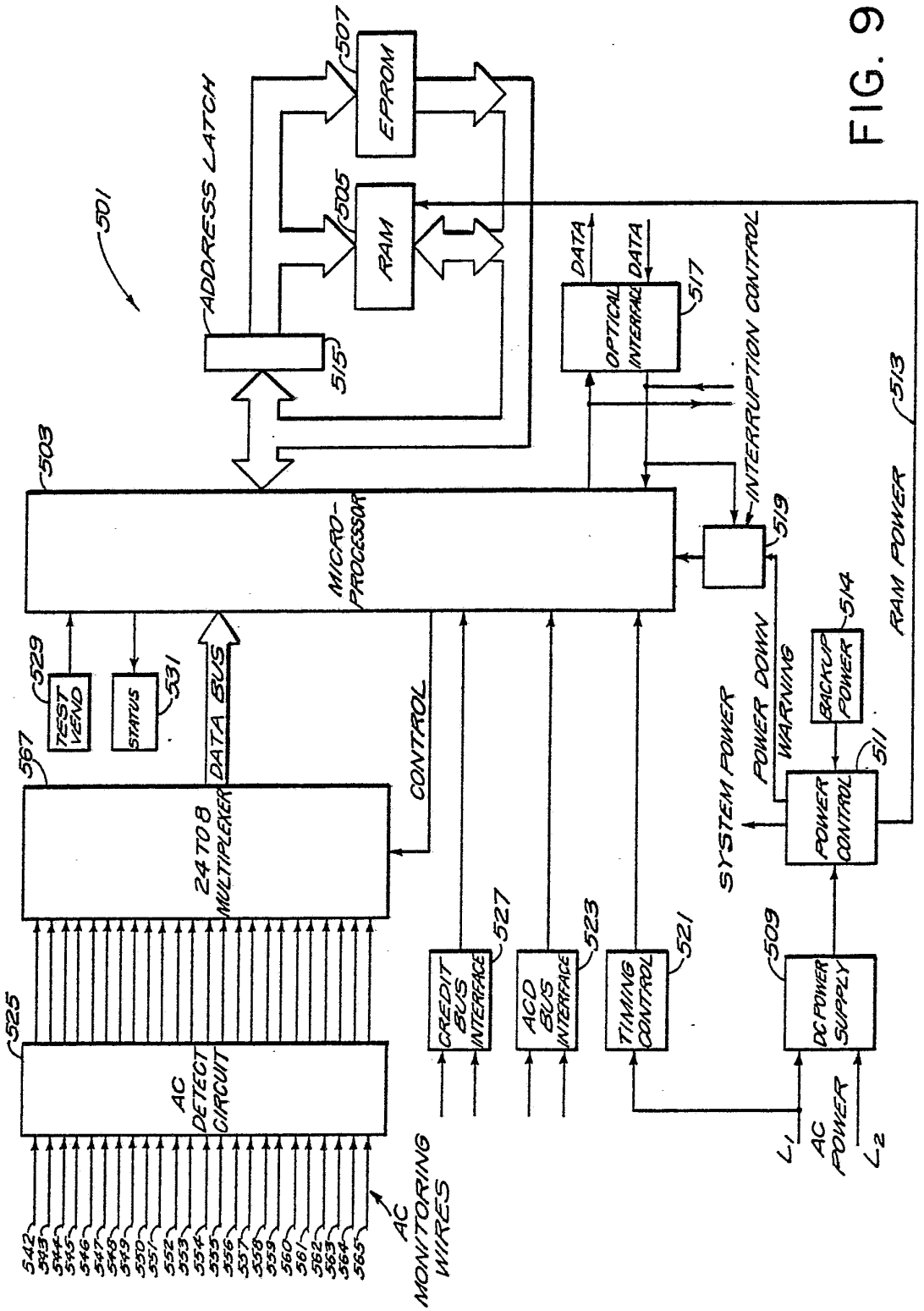

FIG. 9

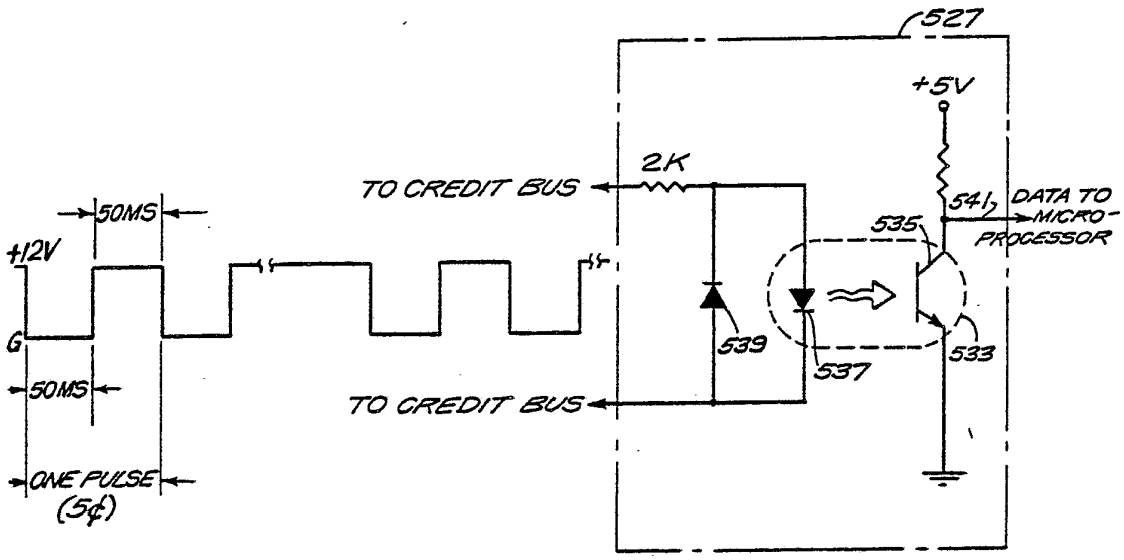

FIG. 10

	CHAR. 1																				CHAR. 6			
MONITORING WIRE NUMBER	542	543	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565
COUNTED EVENT=1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
TIME & DURATION EVENT=1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0
BEFORE VIP=1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
AFTER VIP=1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
L_1 REF. = 1 L_2 REF. = 0	1	1	1	1	1	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
SHORT DURATION=1 LONG DURATION=0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NORMALLY ABSENT=1 NORMALLY PRESENT=0	0	1	1	1	1	0	0	0	1	0	1	1	1	0	0	1	1	1	0	1	0	0	0	0
	CHAR. 37								MASK MATRIX												CHAR. 42			

FIG. 11

INTERNATIONAL SEARCH REPORT

International Application No PCT/US82/01130

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl.[3] G06F 15/20, G06F 13/06, G06F 3/00

U.S. Cl. 364/200, 364/900 364/478, 364/479

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	364/200 364/478 364/900 364/479

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X E	U.S.,A, 4,354,613, Published 19 October 1982, Desai et al.	1-19
X P	U.S.,A, 4,328,539 Published 4 May 1982 Heeger	1-19
A	U.S.,A, 4,282,575 Published 4 August 1981, Hoskinson et al.	1-19
A	U.S.,A, 4,216,461 Published 5 August 1980, Werth et al.	1-19
A	U.S.,A 4,233,660 Published 11 November 1980, Fagan	1-19

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
23 November 1982	02 DEC 1982
International Searching Authority [1]	Signature of Authorized Officer [20]
ISA/US	Garth D. Shaw