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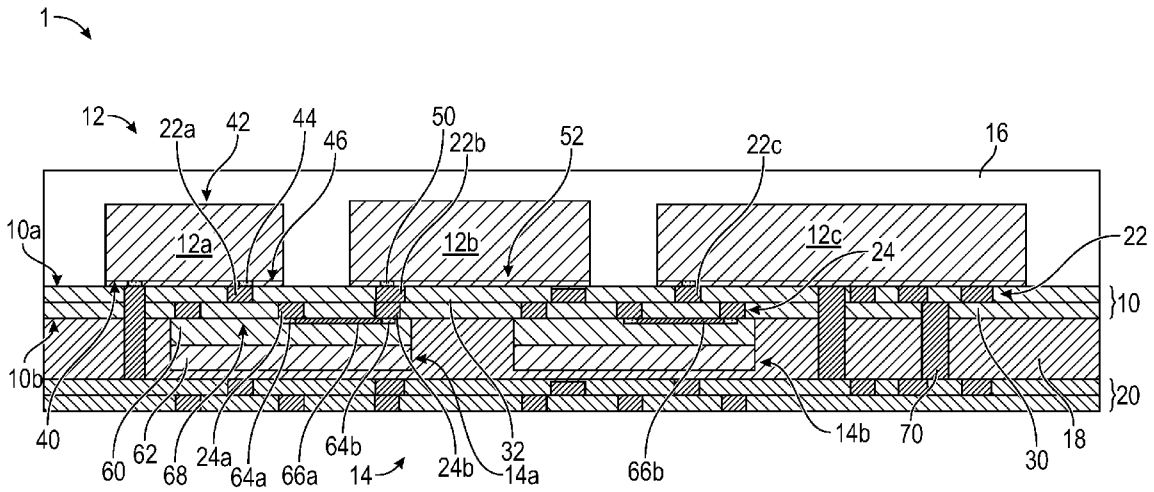


FIG. 1B

(57) **Abstract:** A bonded structure is disclosed. The bonded structure can include an interconnect structure that has a first side and a second side opposite the first side. The bonded structure can also include a first die that is mounted to the first side of the interconnect structure. The first die can be directly bonded to the interconnect structure without an intervening adhesive. The bonded structure can also include a second die that is mounted to the first side of the interconnect structure. The bonded structure can further include an element that is mounted to the second side of the interconnect structure. The first die and the second die are electrically connected by way of at least the interconnect structure and the element.

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BONDED STRUCTURE WITH INTERCONNECT STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Patent Application No. 63/075,038, filed September 4, 2020, titled "BONDED STRUCTURE WITH INTERCONNECT STRUCTURE," the entire contents of each of which are hereby incorporated herein by reference.

BACKGROUND

Field

[0002] The field generally relates to bonded structures, and in particular, to bonded structures with an interconnect structure.

Description of the Related Art

[0003] An electronic component can be connected to a redistribution layer (RDL), which can comprise conductive routing traces to route signals laterally outside the footprint of the electronic component. The RDL can be formed on the electronic component by way of a deposition process. When the RDL is formed, there can be misalignments between the conductive portions of the RDL and contact pads of the electronic component. Accordingly, there remains a continuing need for improved structures and methods for manufacturing an electronic component.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Specific implementations will now be described with reference to the following drawings, which are provided by way of example, and not limitation.

[0005] Figure 1A shows a schematic side view of integrated device dies and a plurality of elements prior to being mounted to an interconnect structure.

[0006] Figure 1B shows a schematic cross sectional side view of a bonded structure according to an embodiment.

[0007] Figure 2A shows a step in a process of manufacturing a bonded structure according to an embodiment.

[0008] Figure 2B shows another step in the process of manufacturing a bonded structure after Figure 2A.

[0009] Figure 2C shows another step in the process of manufacturing a bonded structure after Figure 2B.

[0010] Figure 2D shows another step in the process of manufacturing a bonded structure after Figure 2C.

[0011] Figure 2E shows another step in the process of manufacturing a bonded structure after Figure 2D.

[0012] Figure 3A shows a step in a process of manufacturing a bonded structure according to another embodiment.

[0013] Figure 3B shows another step in the process of manufacturing a bonded structure after Figure 3A.

[0014] Figure 3C shows another step in the process of manufacturing a bonded structure after Figure 3B.

[0015] Figure 3D shows another step in the process of manufacturing a bonded structure after Figure 3C.

[0016] Figure 3E shows another step in the process of manufacturing a bonded structure after Figure 3D.

[0017] Figure 4 shows a schematic cross sectional side view of a bonded structure according to another embodiment.

[0018] Figure 5 is a schematic diagram of a system incorporating one or more microelectronic assemblies, according to various embodiments.

DETAILED DESCRIPTION

[0019] Integrated device packages can use a redistribution layer (RDL) to redistribute signals from one or more integrated device dies in the package to other devices (*e.g.*, other devices outside the footprint of the integrated device die). For example, fan-out redistribution can convey signals from finely-pitched bond pads of an integrated device die to other devices laterally spaced from the die. In some implementations, the fan-out RDL can convey signals from a die to leads or contact pads configured to connect to a system board (*e.g.*, a printed circuit board, or PCB). In some implementations, the fan-out RDL can

convey signals from the die to other devices, such as other integrated device dies, etc. In some packages that include multiple integrated device dies, the dies may be mounted to a sacrificial carrier, and a molding compound can be provided over the dies and carrier. The sacrificial carrier can be removed, and the molded device dies can be flipped over. The RDL can be deposited over the molding compound and the device dies to form a reconstituted wafer. The reconstituted wafer can be singulated into a plurality of packages, with each package including one or multiple dies connected to an RDL.

[0020] However, in reconstituted wafers that utilize a deposited RDL, the dies may have small misalignments relative to their intended position, *e.g.*, rotational and/or translational misalignments. When hundreds or thousands of dies are misaligned across a reconstituted wafer, misalignment of the deposited RDL may accordingly be magnified by a significant amount. In such situations, the misalignment can be compensated for by using a coarse pitch on the die(s) and/or a limited number of interconnects between the dies. However, it may be undesirable to reduce the number of contact pads on the die and/or the number of interconnects between dies. The misalignment problem can be compounded when more than two dies are used in a system. Accordingly, there remains a continuing need for improved alignment of integrated device dies in packages that utilize fan-out redistribution.

[0021] Various embodiments disclosed herein can beneficially ensure that multiple device dies are aligned relative to one another by mounting (*e.g.*, directly bonding) the device dies to an interconnect structure (*e.g.*, an RDL) which can serve as an alignment layer to accurately align the dies relative to one another and/or a desired position in the reconstituted wafer. One or more elements can be mounted (*e.g.*, directly bonded) to an opposite side of the interconnect structure to electrically connect laterally spaced device dies. Molding compound can be provided over one or both sides of the interconnect structure, dies, and elements. Directly bonding the device dies and/or connecting elements to a common interconnect structure (*e.g.*, an alignment layer serving as an RDL) can improve alignment between dies. The reconstituted wafer can be singulated to form a plurality of packages, with each package including multiple device dies and connecting elements on opposing sides of the interconnect structure.

[0022] Two or more semiconductor elements (such as integrated device dies, wafers, etc.) may be stacked on or bonded to one another to form a bonded structure.

Conductive contact pads of one element may be electrically connected to corresponding conductive contact pads of another element. Any suitable number of elements can be stacked in the bonded structure.

[0023] Referring to Figures 1A and 1B, in some embodiments, the elements (e.g., a plurality of dies 12 and an interconnect structure 10) are directly bonded to one another without an adhesive. In various embodiments, a non-conductive material 46 of a first element (*e.g.*, a first semiconductor device die with active circuitry or the first integrated device die 12) can be directly bonded to a corresponding dielectric field region (e.g., a non-conductive material 30) of a second element (*e.g.*, a second semiconductor device die with active circuitry or the interconnect structure 10) without an adhesive. The non-conductive material 46 can be referred to as a nonconductive bonding region of the first element. In some embodiments, the non-conductive material of the first element can be directly bonded to the corresponding dielectric field region of the second element using dielectric-to-dielectric bonding techniques. For example, dielectric-to-dielectric bonds may be formed without an adhesive using the direct bonding techniques disclosed at least in U.S. Patent Nos. 9,564,414; 9,391,143; and 10,434,749, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes.

[0024] In various embodiments, hybrid direct bonds can be formed without an intervening adhesive. For example, dielectric bonding surfaces can be polished to a high degree of smoothness. The bonding surfaces can be cleaned and exposed to a plasma and/or etchants to activate the surfaces. In some embodiments, the surfaces can be terminated with a species after activation or during activation (*e.g.*, during the plasma and/or etch processes). Without being limited by theory, in some embodiments, the activation process can be performed to break chemical bonds at the bonding surface, and the termination process can provide additional chemical species at the bonding surface that improves the bonding energy during direct bonding. In some embodiments, the activation and termination are provided in the same step, *e.g.*, a plasma or wet etchant to activate and terminate the surfaces. In other embodiments, the bonding surface can be terminated in a separate treatment to provide the additional species for direct bonding. In various embodiments, the terminating species can comprise nitrogen. Further, in some embodiments, the bonding surfaces can be exposed to fluorine. For example, there may be one or multiple fluorine peaks near layer and/or bonding

interfaces. Thus, in the directly bonded structures, the bonding interface between two dielectric materials can comprise a very smooth interface with higher nitrogen content and/or fluorine peaks at the bonding interface. Additional examples of activation and/or termination treatments may be found throughout U.S. Patent Nos. 9,564,414; 9,391,143; and 10,434,749, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes.

[0025] In various embodiments, conductive contact pads of the first element can be directly bonded to corresponding conductive contact pads of the second element. For example, a hybrid bonding technique can be used to provide conductor-to-conductor direct bonds along a bond interface that includes covalently direct bonded dielectric-to-dielectric surfaces, prepared as described above. In various embodiments, the conductor-to-conductor (*e.g.*, contact pad to contact pad) direct bonds and the dielectric-to-dielectric hybrid bonds can be formed using the direct bonding techniques disclosed at least in U.S. Patent Nos. 9,716,033 and 9,852,988, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes.

[0026] For example, dielectric bonding surfaces can be prepared and directly bonded to one another without an intervening adhesive as explained above. Conductive contact pads (which may be surrounded by nonconductive dielectric field regions) may also directly bond to one another without an intervening adhesive. In some embodiments, the respective contact pads can be recessed below exterior (*e.g.*, upper) surfaces of the dielectric field or nonconductive bonding regions, for example, recessed by less than 20 nm, less than 15 nm, or less than 10 nm, for example, recessed in a range of 2 nm to 20 nm, or in a range of 4 nm to 10 nm. The nonconductive bonding regions can be directly bonded to one another without an adhesive at room temperature in some embodiments and, subsequently, the bonded structure can be annealed. Upon annealing, the contact pads can expand and contact one another to form a metal-to-metal direct bond. Beneficially, the use of Direct Bond Interconnect, or DBI®, techniques can enable high density of pads connected across the direct bond interface (e.g., small or fine pitches for regular arrays). In some embodiments, the pitch of the bonding pads may be less 40 microns or less than 10 microns or even less than 2 microns. For some applications the ratio of the pitch of the bonding pads to one of the dimensions of the bonding pad is less than 5, or less than 3 and sometimes desirably less than

2. In various embodiments, the contact pads can comprise copper, although other metals may be suitable.

[0027] Thus, in direct bonding processes, a first element can be directly bonded to a second element without an intervening adhesive. In some arrangements, the first element can comprise a singulated element, such as a singulated integrated device die. In other arrangements, the first element can comprise a carrier or substrate (*e.g.*, a wafer) that includes a plurality (*e.g.*, tens, hundreds, or more) of device regions that, when singulated, form a plurality of integrated device dies. Similarly, the second element can comprise a singulated element, such as a singulated integrated device die. In other arrangements, the second element can comprise a carrier or substrate (*e.g.*, a wafer).

[0028] As explained herein, the first and second elements can be directly bonded to one another without an adhesive, which is different from a deposition process. The first and second elements can accordingly comprise non-deposited elements. Further, directly bonded structures, unlike deposited layers, can include a defect region along the bond interface in which nanovoids are present. The nanovoids may be formed due to activation of the bonding surfaces (e.g., exposure to a plasma). As explained above, the bond interface can include concentration of materials from the activation and/or last chemical treatment processes. For example, in embodiments that utilize a nitrogen plasma for activation, a nitrogen peak can be formed at the bond interface. In embodiments that utilize an oxygen plasma for activation, an oxygen peak can be formed at the bond interface. In some embodiments, the bond interface can comprise silicon oxynitride, silicon oxycarbonitride, or silicon carbonitride. As explained herein, the direct bond can comprise a covalent bond, which is stronger than van Der Waals bonds. The bonding layers can also comprise polished surfaces that are planarized to a high degree of smoothness.

[0029] In various embodiments, the metal-to-metal bonds between the contact pads can be joined such that copper grains grow into each other across the bond interface. In some embodiments, the copper can have grains oriented along the 111 crystal plane for improved copper diffusion across the bond interface. The bond interface can extend substantially entirely to at least a portion of the bonded contact pads, such that there is substantially no gap between the nonconductive bonding regions at or near the bonded contact pads. In some embodiments, a barrier layer may be provided under the contact pads

(*e.g.*, which may include copper). In other embodiments, however, there may be no barrier layer under the contact pads, for example, as described in US 2019/0096741, which is incorporated by reference herein in its entirety and for all purposes.

[0030] Figure 1A shows a schematic side view of integrated device dies 12a-12c and a plurality of elements 14a-14b prior to being mounted to an interconnect structure 10. Figure 1B shows a schematic cross sectional side view of a bonded structure 1 according to an embodiment. The bonded structure 1 of Figure 1B may represent a singulated structure that has been separated (*e.g.*, by sawing or punching) from a reconstituted wafer. The bonded structure 1 can include an interconnect structure 10 that has a first side 10a and a second side 10b, a plurality of integrated device dies 12 (e.g., a first die 12a, a second die 12b, and a third die 12c) that are mounted to the first side 10a of the interconnect structure 10, and a plurality of connecting elements 14 (e.g., a first element 14a and a second element 14b) that are mounted to the second side 10b of the interconnect structure 10. The bonded structure can also include a first molding material 16 disposed on the first side 10a of the interconnect structure, a second molding material 18 disposed on the second side 10b of the interconnect structure, and a second interconnect structure 20.

[0031] The first side 10a of the interconnect structure 10 can comprise a plurality of conductive contact pads 22 (e.g., a first contact pad 22a, a second contact pad 22b, and a third contact pad 22c), and the second side 10b of the interconnect structure 10 can comprise a plurality of conductive contact pads 24 (e.g., a first contact pad 24a, a second contact pad 24b). In some embodiments, the first contact pad 22a and the first contact pad 24a can be electrically connected, and the second contact 22b and the second contact pad 24b can be electrically connected. The first contact pad 22a can be laterally offset relative to the first contact pad 24a. The second contact pad 22b can be laterally offset relative to the second contact pad 24b. In some embodiments, the interconnect structure 10 can comprise a redistribution layer (RDL). The interconnect structure 10 can comprise a non-conductive material 30, a plurality of conductive lines 32 formed in the non-conductive material 30, a plurality of conductive vias (not illustrated) formed in the non-conductive material 30. The non-conductive material 30 can comprise any suitable material. For example, the non-conductive material 30 can comprise a dielectric material, such as silicon oxide, or a polymer such as polyimide. In some embodiments, the conductive lines 32 can comprise a power line

for providing power to the dies 12. In some embodiments, the conductive lines 32 can comprise signal lines for transferring signals between the dies 12a-12c. In some embodiments, the conductive lines 32 can transfer or redistribute signals laterally between contact pads (e.g., the first contact pad 22a and the second pad 22b) on the first side 10a and contact pads (e.g., the first contact pad 24a and the second contact pad 24b) on the second side 10b.

[0032] The interconnect structure 10 can be provided by way of a transfer process. For example, in some embodiments, the interconnect structure 10 (*e.g.*, an RDL) can be formed on a carrier (such as a semiconductor or glass carrier) and directly bonded to the plurality of dies 12. The carrier can be removed from the interconnect structure 10 to transfer the RDL to the plurality of dies 12. Therefore, in some embodiments, the interconnect structure 10 can comprise a transfer RDL. The first, second, and third dies 12a, 12b, 12c can be spaced apart from one another along the first side 10a of the interconnect structure 10. The interconnect structure 10 can beneficially serve to align multiple dies 12a, 12b, 12c and elements 14 relative to a common interconnect structure 10 (*e.g.*, RDL).

[0033] In some embodiments, one or more of the plurality of integrated device dies 12 can be flip-chip mounted to the interconnect structure 10. The plurality of integrated device dies 12 can comprise any suitable type of device die. For example, one or more of the plurality of integrated device dies 12 can comprise an electronic component such as a processor die, a memory die, a microelectromechanical systems (MEMS) die, an optical device, or any other suitable type of device die. In other embodiments, the electronic component can comprise a passive device such as a capacitor, inductor, or other surface-mounted device. Circuitry (such as active components like transistors) can be patterned at or near active surface(s) of one or more of the plurality of integrated device dies 12 in various embodiments. The active surfaces may be on a side of one or more of the plurality of integrated device dies 12 which is opposite respective backsides of the one or more of the plurality of integrated device dies 12. The backsides may or may not include any active circuitry or passive devices. The first integrated device die 12 and the second integrated device die 14 may be the same type of integrated device die or a different type of device die.

[0034] The first die 12a can comprise a bonding surface 40 and a back surface 42 opposite the bonding surface 40. The bonding surface 40 can have a plurality of conductive

bond pads including a conductive bond pad 44, and a non-conductive material 46 proximate to the conductive bond pad 44. In some embodiments, the conductive bond pad 44 can be bonded to the first conductive pad 22a, and the non-conductive material 46 can be bonded to a portion of the non-conductive material 30. In some embodiments, the conductive bond pad 44 can be directly bonded to the first conductive pad 22a without an intervening adhesive, and the non-conductive material 46 can be directly bonded to the portion of the non-conductive material 30 without an intervening adhesive. The non-conductive materials 46, 30 and conductive pads 44, 22a can be directly bonded without an adhesive as described throughout U.S. Patent Nos. 7,126,212; 8,153,505; 7,622,324; 7,602,070; 8,163,373; 8,389,378; 7,485,968; 8,735,219; 9,385,024; 9,391,143; 9,431,368; 9,953,941; 9,716,033; 9,852,988; 10,032,068; 10,204,893; 10,434,749; and 10,446,532, the contents of each of which are hereby incorporated by reference herein in their entirety and for all purposes. In some embodiments, the plurality of integrated device dies 12 can alternatively be bonded to the interconnect structure 10 by way of a thermal conductive bonding (TCB).

[0035] The second die 12b and the third die 12c can be bonded to the interconnect structure in a similar manner as the first die 12a. In some embodiments, the second die 12b can comprise a plurality of contact pads including conductive contact pad 50 that can be bonded to the conductive contact pad 22b of the interconnect structure 10, and a non-conductive material 52 that can be bonded to a portion of the non-conductive material 30 of the interconnect structure 10. In some embodiments, the second die 12b can comprise a conductive contact pad 50 that can be directly bonded to the conductive contact pad 22b of the interconnect structure 10 without an intervening adhesive, and a non-conductive material 52 that can be directly bonded to a portion of the non-conductive material 30 of the interconnect structure 10 without an intervening adhesive.

[0036] In some embodiments, the plurality of elements 14 (e.g., the first element 14a and the second element 14b) can comprise an interconnect layer 60 and an element body 62. In some embodiments, the interconnect layer 60 can comprise a redistribution layer (RDL) with conductors embedded in an insulating or nonconductive material. In some embodiments, the element body 62 can comprise a substrate, such as a silicon substrate, a glass substrate, etc. In some embodiments, the element body 62 can comprise an integrated device die. In some embodiments, the plurality of elements 14 can comprise a high density

interconnect substrate. The elements 14 can beneficially provide electrical communication between the dies 12a, 12b, 12c by connecting to conductors in the interconnect structure 10 that connect to the dies 12a-12c. In some arrangements, the interconnect structure 10 can include traces that laterally electrically connect the dies 12a-12c. However, the interconnect structure 10 may comprise one or a few layers, which may not be sufficient for providing dense signal lines between the dies 12a-12c. Beneficially, the elements 14 can include numerous or dense interconnects and signal lines that can convey a significant number of signals between the dies 12a-12c. For example, in some embodiments, the interconnect structure 10 can vertically transfer signals from the pads of the die 12a to the element 14a by way of vias in the interconnect structure 10. The first element 14a can transfer the signals laterally by way of traces or conductors 66a within the element. The signals can be transferred vertically to the die 12b by way of vias in the interconnect structure 10. The second element 14b can transfer signals laterally by way of traces or conductors 66b within the element.

[0037] The first element 14a can comprise a first conductive contact pad 64a, and a second conductive contact pad 64b. The first conductive contact pad 64a and the second conductive contact pad 64b can be electrically coupled to each other by way of a conductive line 66a. The first and second conductive pads 64a, 64b can be bonded to corresponding pads on the second side 10b of the interconnect structure 10. In some embodiments, the first and second conductive pads 64a, 64b can be bonded to corresponding pads on the second side 10b of the interconnect structure 10, in the same or generally similar manner as how the conductive contact pad 44 of the first die 12a is bonded to the conductive contact pad 22a of the interconnect structure. The element 14b can also comprise a non-conductive material 68 that is bonded to the second side 10b of the interconnect structure 10. In some embodiments, the non-conductive material 68 can be directly bonded to a portion of the non-conductive material 30 at the second side 10b of the interconnect structure 10, in the same or generally similar manner as how the non-conductive material 46 of the first die 12a is bonded to a portion the non-conductive material 30 at the first side 10a of the interconnect structure 10.

[0038] The interconnect structure 10 and the first element 14a can define at least a portion of a conductive pathway between the first die 12a and the second die 12b. In some embodiments, the first element 14a and the second element 14b can be generally similar. For

example, the first element 14a and the second element 14b can be identically structured. In other embodiments, the first element 14a and the second element 14b can comprise different structures. Although in Figure 1B, the first element 14a defines a portion of the conductive pathway between the two adjacent dies (the first die 12a and the second die 12b), in some embodiments, an element may define at least a portion of a conductive pathway between two or more adjacent dies, or two or more remotely located dies on the interconnect structure 10. Electrically coupling the dies 12 to each other only through the interconnect structure 10 (e.g., an RDL, without the elements 14a, 14b) can cause certain problems and difficulties. For example, forming a conductive routing in the RDL for two or more dies 12 may require a complicated multi-layer structure and the RDL may not be able to provide enough density for proper connection between the dies 12. Also, forming a conductive routing for two or more dies 12 in the interconnect structure can be relatively expensive. Therefore, the elements 14 can provide solutions to these problems and difficulties associated with having the conductive routing for dies 12 in the interconnect structure 10.

[0039] The first molding material 16 can comprise a polymer, epoxy, resin, or the like material. In some embodiments, the first molding material 16 provide mechanical support for the first integrated device die 12a, the second integrated device die 12b and/or the third integrated device die 12c. In some embodiments, the first molding material 16 can at least partially be disposed about the first integrated device die 12a, the second integrated device die 12b, and the third integrated device die 12c.

[0040] The second molding material 18 can comprise the same or generally similar material as the first material 18. In some embodiments, the first molding material 16 and the second molding material 18 can comprise functionally similar materials. The second molding material 18 can comprise a polymer, epoxy, resin, or the like material. In some embodiments, the second molding material 18 provide mechanical support for the first element 14a and/or the second element 14b. In some embodiments, the second molding material 18 can at least partially be disposed about the first element 14a and the second element 14b.

[0041] The bonded structure 1 can further include a conductive via 70 formed at least in the second molding material 18. In some embodiments, the conductive via 70 can extend at least partially though a thickness of the second molding material 18. In some

embodiments, the conductive via 70 can extend from the second side 10b of the interconnect structure 10 to the second interconnect structure 20. In some embodiments, the conductive via 70 can extend from the first side 10a of the interconnect structure 10 to the second interconnect structure 20, thereby being in direct contact with one of the plurality of dies 12.

[0042] The second interconnect structure 20 can comprise the same or generally similar structure as the first interconnect structure 10. In some embodiments, the first interconnect structure 10 and the second interconnect structure 20 can comprise functionally similar structures.

[0043] Figures 2A-2E show a process flow of manufacturing the bonded structure 1 according to one embodiments. Figure 2A shows a schematic cross sectional side view of an interconnect structure 10 formed on a carrier 74. In some embodiments, the carrier 74 can comprise a semiconductor or glass carrier. At Figure 2B, a plurality of dies 12 can be provided on a first side 10a of the interconnect structure 10. The dies 12 can be directly bonded to the interconnect structure 10 without an adhesive (*e.g.*, conductive contacts and nonconductive field regions of the dies 12 and interconnect structure 10 can respectively be directly bonded to one another). At Figure 2B, a first molding material 16 can also be provided over the first side 10a of the interconnect structure 10, including over the first side 10a of the interconnect structure 10, side surfaces of the dies 12, and upper surfaces of the dies 12. The carrier 74 can be removed from the interconnect layer 10. At Figure 2C, one or more elements 14 can be provided on a second side 10b of the interconnect structure 10 opposite the first side 10a. In some embodiments, the elements 14 can be directly bonded to the second side 10b of the interconnect structure 10 without an adhesive (*e.g.*, conductive contacts and nonconductive field regions of the elements 14 and interconnect structure 10 can respectively be directly bonded to one another). The one or more elements 14 can electrically couple two or more of the plurality of integrated device dies 12 by way of the interconnect structure 10 (*e.g.*, RDL). In some embodiments, the structure shown in Figure 2C can be a final structure that can be mounted to another device, such as a system board.

[0044] At Figure 2D, a second molding material 18 can be provided at least partially about the elements 14, *e.g.*, over the second side 10b of the interconnect structure 10. In the illustrated embodiment, the elements 14 can be completely embedded in the second molding material 18 such that the second molding material 18 covers side and upper

surfaces of the elements 14. In some embodiments, the second molding material 18 can comprise a conductive via 70 that extends at least partially though a thickness of the second molding material 18. In some embodiments, the structure shown in Figure 2D can be a final structure that can be mounted to another device, such as a system board or other device.

[0045] At Figure 2E, a second interconnect structure 20 can be provided. In some embodiments, the structure shown in Figure 2E can be a final structure that can be mounted to another device, such as a system board or other device. In some embodiments, the structure shown in Figure 2E can be mounted to a system board or PCB. In other embodiments, multiple structures such as that shown in Figure 2E can be stacked on one another, or can be stacked on different types of structures such as reconstituted wafers or elements, dies, interposers, etc.

[0046] Figures 3A-3E show a process flow of manufacturing the bonded structure according to another embodiment. Figure 3A shows a schematic cross sectional side view of an interconnect structure 10 formed on or in a carrier 74. In some embodiments, the carrier 74 can comprise a semiconductor or glass carrier. At Figure 3B, one or more elements 14 can be provided on a second side 10b of the interconnect structure 10. As explained above, in some embodiments, the elements 14 can be directly bonded to the interconnect structure 10 without an adhesive. A second molding material 18 can be provided at least partially about the elements 14. In some embodiments, the second molding material 18 can comprise a conductive via 70 that extends at least partially through (*e.g.*, completely through) a thickness of the second molding material 18.

[0047] At Figure 3C, a second carrier 76 can be provided. In some embodiments, the second carrier 76 can comprise a semiconductor or glass carrier. The carrier 74 can be removed from the interconnect layer 10. At Figure 3D, a plurality of dies 12 can be provided on a first side 10a of the interconnect structure 10. As explained above, in some embodiments, the dies 12 can be directly bonded to the interconnect structure 10 without an adhesive. A first molding material 16 can also be provided over the first side 10a of the interconnect structure 10. At Figure 3E, the second carrier 76 can be removed. The structure shown in Figure 3E can be the same or generally similar as the structure shown in Figure 2D.

[0048] Figure 4 shows a schematic cross sectional side view of a bonded structure 2 according to an embodiment. Unless otherwise noted, the components of Figure 4 may be

the same as or generally similar to like-numbered components of Figures 1A-3E. The bonded structure 2 of Figure 4 may represent a singulated structure that has been separated (*e.g.*, by sawing or punching) from a reconstituted wafer. The bonded structure 2 can include an interconnect structure 10' that has a first side 10'a and a second side 10'b, a plurality of integrated device dies 12 (e.g., a first die 12a, a second die 12b, and a third die 12c) that are mounted to the first side 10'a of the interconnect structure 10', and a plurality of connecting elements 14 (e.g., a first element 14a and a second element 14b) that are mounted to the second side 10'b of the interconnect structure 10'. The bonded structure can also include a first molding material 16 disposed on the first side 10'a of the interconnect structure, a second molding material 18 disposed on the second side 10'b of the interconnect structure, and a second interconnect structure 20.

[0049] The interconnect structure 10' of Figure 4, can be generally similar to the interconnect structure 10 illustrated in Figures 1A -3E. In the interconnect structure 10', conductive contact pads 22 are not internally connected electrically. For example, the first conductive contact pad 22a and the second conductive contact pad 22b are not internally connected together electrically within the interconnect structure 10'. Rather, the first conductive contact pad 22a and the second conductive contact pad 22b are electrically coupled by way of the first conductive contact pad 64a and the second conductive contact pad 64b of the first element 14a , which are respectively connected to the first contact pad 24a and the second contact pad 24b.

[0050] Figure 5 is a schematic diagram of a system 80 incorporating one or more bonded structure 5, according to various embodiments. The system 80 can comprise any suitable type of electronic device, such as a mobile electronic device (*e.g.*, a smartphone, a tablet computing device, a laptop computer, etc.), a desktop computer, an automobile or components thereof, a stereo system, a medical device, a camera, or any other suitable type of system. In some embodiments, the electronic device can comprise a microprocessor, a graphics processor, an electronic recording device, or digital memory. The system 80 can include one or more device packages 82 which are mechanically and electrically connected to the system 80, *e.g.*, by way of one or more motherboards. Each package 82 can comprise one or more bonded structures 5. The bonded structures 5 shown in Figure 5 can comprise

any of the bonded structure disclosed herein. The bonded structure 5 can include one or more integrated device dies which perform various functions for the system 80.

[0051] In one aspect, a bonded structure is disclosed. The bonded structure can include an interconnect structure that has a first side and a second side opposite the first side. The first side includes a first conductive pad, a second conductive pad, and a non-conductive region. The bonded structure can also include a first die that is mounted and directly bonded to the first side of the interconnect structure. The first die electrically is connected to the first conductive pad of the interconnect structure. The bonded structure can also include a second die that is mounted to the first side of the interconnect structure. The second die is electrically connected to the second conductive pad of the interconnect structure. The second die is spaced apart from the first die laterally along the first side of the interconnect structure. The bonded structure can further include an element that is mounted to the second side of the interconnect structure. The first die and the second die are electrically connected by way of at least the interconnect structure and the element.

[0052] In one embodiment, the first die includes a bonding surface. The bonding surface can include a first conductive bond pad and a first non-conductive material. The first conductive bond pad can be directly bonded to the first conductive pad without an intervening adhesive. The first non-conductive material can be directly bonded to a first portion of the non-conductive region without an intervening adhesive. The second die includes a bonding surface. The bonding surface can include a second conductive bond pad and a second non-conductive material. The second conductive bond pad can be directly bonded to the second conductive pad without an intervening adhesive. The second non-conductive material can be directly bonded to a second portion of the non-conductive region without an intervening adhesive.

[0053] In one embodiment, the element is directly bonded to the second side of the interconnect structure without an intervening adhesive.

[0054] In one embodiment, the first die is mounted to the first side of the interconnect structure by way of a thermal conductive bonding (TCB).

[0055] In one embodiment, the interconnect structure includes a redistribution layer (RDL). The RDL layer includes a single layer RDL.

[0056] In one embodiment, the element is mounted to the second side of the interconnect structure by way of a thermal conductive bonding (TCB).

[0057] In one embodiment, the element includes a third die.

[0058] In one embodiment, the element includes a redistribution layer (RDL) formed on a substrate.

[0059] In one embodiment, the element include a high density interconnect substrate.

[0060] In one embodiment, the bonded structure further includes a first molding material that is disposed over the interconnect structure and at least partially between the first die and the second die.

[0061] In one embodiment, the bonded structure further includes a second molding material disposed about the element. The bonded structure can further include a conductive via extending at least through a thickness of the second molding material. The bonded structure can further include a second interconnect structure that is electrically coupled to the interconnect structure through the via. The element can be positioned between the interconnect structure and the second interconnect structure.

[0062] In one aspect, a bonded structure is disclosed. The bonded structure can include an interconnect structure that has a first side and a second side opposite the first side. The first side includes a first conductive pad, a second conductive pad, and a non-conductive region. The second side includes a third conductive pad and a fourth conductive pad. The bonded structure can also include a first die that is mounted to the first side of the interconnect structure. The first die is electrically connected to the first conductive pad of the interconnect structure. The bonded structure can also include a second die that is mounted to the first side of the interconnect structure. The second die is electrically connected to the second conductive pad of the interconnect structure. The second die is spaced apart from the first die laterally along the first side of the interconnect structure. The bonded structure further includes an element that is mounted and directly bonded to the second side of the interconnect structure and electrically connected to the third conductive pad and the fourth conductive pad. The element is configured to provide at least a portion of a conductive pathway between the first die and the second die.

[0063] In one embodiment, the third conductive pad is laterally offset relative to the first conductive pad.

[0064] In one embodiment, the first die includes a bonding surface. The bonding surface can include a first conductive bond pad and a first non-conductive material. The first conductive bond pad can be directly bonded to the first conductive pad without an intervening adhesive. The first non-conductive material can be directly bonded to a first portion of the non-conductive region. The second die can include a bonding surface. The bonding surface can include a second conductive bond pad and a second non-conductive material. The second conductive bond pad can be directly bonded to the second conductive pad without an intervening adhesive. The second non-conductive material can be directly bonded to a second portion of the non-conductive region without an intervening adhesive.

[0065] In one embodiment, the element is directly bonded to the second side of the interconnect structure without an intervening adhesive.

[0066] In one embodiment, the first die is mounted to the first side of the interconnect structure by way of a thermal conductive bonding (TCB).

[0067] In one embodiment, the interconnect structure includes a redistribution layer (RDL). The RDL layer comprises a single layer RDL.

[0068] In one embodiment, the element is mounted to the second side of the interconnect structure by way of a thermal conductive bonding (TCB).

[0069] In one embodiment, the element includes a third die.

[0070] In one embodiment, the element includes a redistribution layer (RDL) formed on a substrate.

[0071] In one embodiment, the element includes a high density interconnect substrate.

[0072] In one embodiment, the bonded structure further includes a first molding material that is disposed over the interconnect structure at least partially between the first die and the second die.

[0073] In one embodiment, the bonded structure further includes a second molding material disposed about the element. The bonded structure can further include a conductive via extending at least through a thickness of the second molding material. The bonded structure can further includes a second interconnect structure that is electrically

coupled to the interconnect structure through the via. The element can be positioned between the interconnect structure and the second interconnect structure.

[0074] In one aspect, a bonded structure is disclosed. The bonded structure can include an interconnect structure that has a first side and a second side opposite the first side. The first side is configured to support a plurality of dies. The second side includes a first conductive pad, a second conductive pad, and a non-conductive region between the first conductive pad and the second conductive pad. The bonded structure can also include an element that has a bonding surface. The bonding surface includes a first conductive bond pad, a second conductive bond pad, and a non-conductive material between the first conductive bond pad and the second conductive bond pad. The first conductive bond pad and the second conductive bond pad are directly bonded to the first conductive pad and the second conductive pad, respectively, without an intervening adhesive. The non-conductive material is directly bonded to a portion of the non-conductive region. The element is configured to define at least a portion of a conductive pathway between two or more of the plurality of dies.

[0075] In one embodiment, the bonded structure further includes a first die that is mounted to the first side of the interconnect structure, and a second die that is mounted to the first side of the interconnect structure. The second die can be spaced apart from the first die laterally along the first side of the interconnect structure. The first die is electrically coupled with the second die by way of at least the interconnect layer and the element. The bonded structure can further include a first molding material disposed over the interconnect structure at least partially between the first die and the second die. The first die can be directly mounted to the first side of the interconnect structure without an intervening adhesive.

[0076] In one embodiment, the interconnect structure includes a redistribution layer (RDL). The RDL layer can include a single layer RDL.

[0077] In one embodiment, the element includes an integrated device die.

[0078] In one embodiment, the element includes a redistribution layer (RDL) formed on a substrate.

[0079] In one embodiment, the element includes a high density interconnect substrate.

[0080] In one embodiment, the bonded structure further includes a second molding material that is disposed about the element. The bonded structure can further includes a conductive via that extends at least through a thickness of the molding material. The bonded structure can further include a second interconnect structure that is electrically coupled to the interconnect structure through the via. The element is positioned between the interconnect structure and the second interconnect structure.

[0081] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," "include," "including" and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to." The word "coupled", as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Likewise, the word "connected", as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0082] Moreover, conditional language used herein, such as, among others, "can," "could," "might," "may," "e.g.," "for example," "such as" and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments.

[0083] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel apparatus, methods, and systems described herein may be

embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. For example, while blocks are presented in a given arrangement, alternative embodiments may perform similar functionalities with different components and/or circuit topologies, and some blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these blocks may be implemented in a variety of different ways. Any suitable combination of the elements and acts of the various embodiments described above can be combined to provide further embodiments. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

WHAT IS CLAIMED IS:

1. A bonded structure comprising:

an interconnect structure having a first side and a second side opposite the first side, the first side comprising a first conductive pad, a second conductive pad, and a non-conductive region;

a first die mounted and directly bonded to the first side of the interconnect structure, the first die electrically connected to the first conductive pad of the interconnect structure;

a second die mounted to the first side of the interconnect structure, the second die electrically connected to the second conductive pad of the interconnect structure, the second die spaced apart from the first die laterally along the first side of the interconnect structure; and

an element mounted to the second side of the interconnect structure,

wherein the first die and the second die are electrically connected by way of at least the interconnect structure and the element.

2. The bonded structure of Claim 1, wherein the first die comprises a bonding surface, the bonding surface comprising a first conductive bond pad and a first non-conductive material, the first conductive bond pad directly bonded to the first conductive pad without an intervening adhesive, and the first non-conductive material directly bonded to a first portion of the non-conductive region without an intervening adhesive.

3. The bonded structure of Claim 2, wherein the second die comprises a bonding surface, the bonding surface comprising a second conductive bond pad and a second non-conductive material, the second conductive bond pad directly bonded to the second conductive pad without an intervening adhesive, and the second non-conductive material directly bonded to a second portion of the non-conductive region without an intervening adhesive.

4. The bonded structure of Claim 1, wherein the element is directly bonded to the second side of the interconnect structure without an intervening adhesive.

5. The bonded structure of Claim 1, wherein the first die is mounted to the first side of the interconnect structure by way of a thermal conductive bonding (TCB).

6. The bonded structure of Claim 1, wherein the interconnect structure comprises a redistribution layer (RDL).

7. The bonded structure of Claim 6, wherein the RDL layer comprises a single layer RDL.

8. The bonded structure of Claim 1, wherein the element is mounted to the second side of the interconnect structure by way of a thermal conductive bonding (TCB).

9. The bonded structure of Claim 1, wherein the element comprises a third die.

10. The bonded structure of Claim 1, wherein the element comprises a redistribution layer (RDL) formed on a substrate.

11. The bonded structure of Claim 1, wherein the element comprises a high density interconnect substrate.

12. The bonded structure of Claim 1, further comprising a first molding material disposed over the interconnect structure at least partially between the first die and the second die.

13. The bonded structure of Claim 1, further comprising a second molding material disposed about the element.

14. The bonded structure of Claim 13, further comprising a conductive via extending at least through a thickness of the second molding material.

15. The bonded structure of Claim 14, further comprising a second interconnect structure electrically coupled to the interconnect structure through the via, the element is positioned between the interconnect structure and the second interconnect structure.

16. A bonded structure comprising:

an interconnect structure having a first side and a second side opposite the first side, the first side comprising a first conductive pad, a second conductive pad, and a non-conductive region, and the second side comprising a third conductive pad and a fourth conductive pad;

a first die mounted to the first side of the interconnect structure, the first die electrically connected to the first conductive pad of the interconnect structure;

a second die mounted to the first side of the interconnect structure, the second die electrically connected to the second conductive pad of the interconnect structure, the second die spaced apart from the first die laterally along the first side of the interconnect structure; and

an element mounted and directly bonded to the second side of the interconnect structure and electrically connected to the third conductive pad and the fourth conductive pad, the element configured to provide at least a portion of a conductive pathway between the first die and the second die.

17. The bonded structure of Claim 16, wherein the third conductive pad is laterally offset relative to the first conductive pad.

18. The bonded structure of Claim 16, wherein the first die comprises a bonding surface, the bonding surface comprising a first conductive bond pad and a first non-conductive material, the first conductive bond pad directly bonded to the first conductive pad without an intervening adhesive, and the first non-conductive material directly bonded to a first portion of the non-conductive region.

19. The bonded structure of Claim 18, wherein the second die comprises a bonding surface, the bonding surface comprising a second conductive bond pad and a second non-conductive material, the second conductive bond pad directly bonded to the second conductive pad without an intervening adhesive, and the second non-conductive material directly bonded to a second portion of the non-conductive region without an intervening adhesive.

20. The bonded structure of Claim 16, wherein the element is directly bonded to the second side of the interconnect structure without an intervening adhesive.

21. The bonded structure of Claim 16, wherein the first die is mounted to the first side of the interconnect structure by way of a thermal conductive bonding (TCB).

22. The bonded structure of Claim 16, wherein the interconnect structure comprises a redistribution layer (RDL).

23. The bonded structure of Claim 22, wherein the RDL layer comprises a single layer RDL.

24. The bonded structure of Claim 16, wherein the element is mounted to the second side of the interconnect structure by way of a thermal conductive bonding (TCB).

25. The bonded structure of Claim 16, wherein the element comprises a third die.

26. The bonded structure of Claim 16, wherein the element comprises a redistribution layer (RDL) formed on a substrate.

27. The bonded structure of Claim 16, wherein the element comprises a high density interconnect substrate.

28. The bonded structure of Claim 16, further comprising a first molding material disposed over the interconnect structure at least partially between the first die and the second die.

29. The bonded structure of Claim 16, further comprising a second molding material disposed about the element.

30. The bonded structure of Claim 29, further comprising a conductive via extending at least through a thickness of the second molding material.

31. The bonded structure of Claim 30, further comprising a second interconnect structure electrically coupled to the interconnect structure through the via, the element is positioned between the interconnect structure and the second interconnect structure.

32. A bonded structure comprising:

an interconnect structure having a first side and a second side opposite the first side, the first side being configured to support a plurality of dies, the second side comprising a first conductive pad, a second conductive pad, and a non-conductive region between the first conductive pad and the second conductive pad; and

an element having a bonding surface, the bonding surface comprising a first conductive bond pad, a second conductive bond pad, and a non-conductive material between the first conductive bond pad and the second conductive bond pad, the first conductive bond pad and the second conductive bond pad directly bonded to the first conductive pad and the second conductive pad, respectively, without an intervening adhesive, and the non-conductive material directly bonded to a portion of the non-conductive region,

wherein the element is configured to define at least a portion of a conductive pathway between two or more of the plurality of dies.

33. The bonded structure of Claim 32, further comprising:

a first die mounted to the first side of the interconnect structure; and

a second die mounted to the first side of the interconnect structure, the second die being spaced apart from the first die laterally along the first side of the interconnect structure,

wherein the first die is electrically coupled with the second die by way of at least the interconnect layer and the element.

34. The bonded structure of Claim 33, further comprising a first molding material disposed over the interconnect structure at least partially between the first die and the second die.

35. The bonded structure of Claim 33, wherein the first die is directly mounted to the first side of the interconnect structure without an intervening adhesive.

36. The bonded structure of Claim 32, wherein the interconnect structure comprises a redistribution layer (RDL).

37. The bonded structure of Claim 36, wherein the RDL layer comprises a single layer RDL.

38. The bonded structure of Claim 32, wherein the element comprises an integrated device die.

39. The bonded structure of Claim 32, wherein the element comprises a redistribution layer (RDL) formed on a substrate.

40. The bonded structure of Claim 32, wherein the element comprises a high density interconnect substrate.

41. The bonded structure of Claim 32, further comprising a second molding material disposed about the element.

42. The bonded structure of Claim 41, further comprising a conductive via extending at least through a thickness of the molding material.

43. The bonded structure of Claim 42, further comprising a second interconnect structure electrically coupled to the interconnect structure through the via, the element is positioned between the interconnect structure and the second interconnect structure.

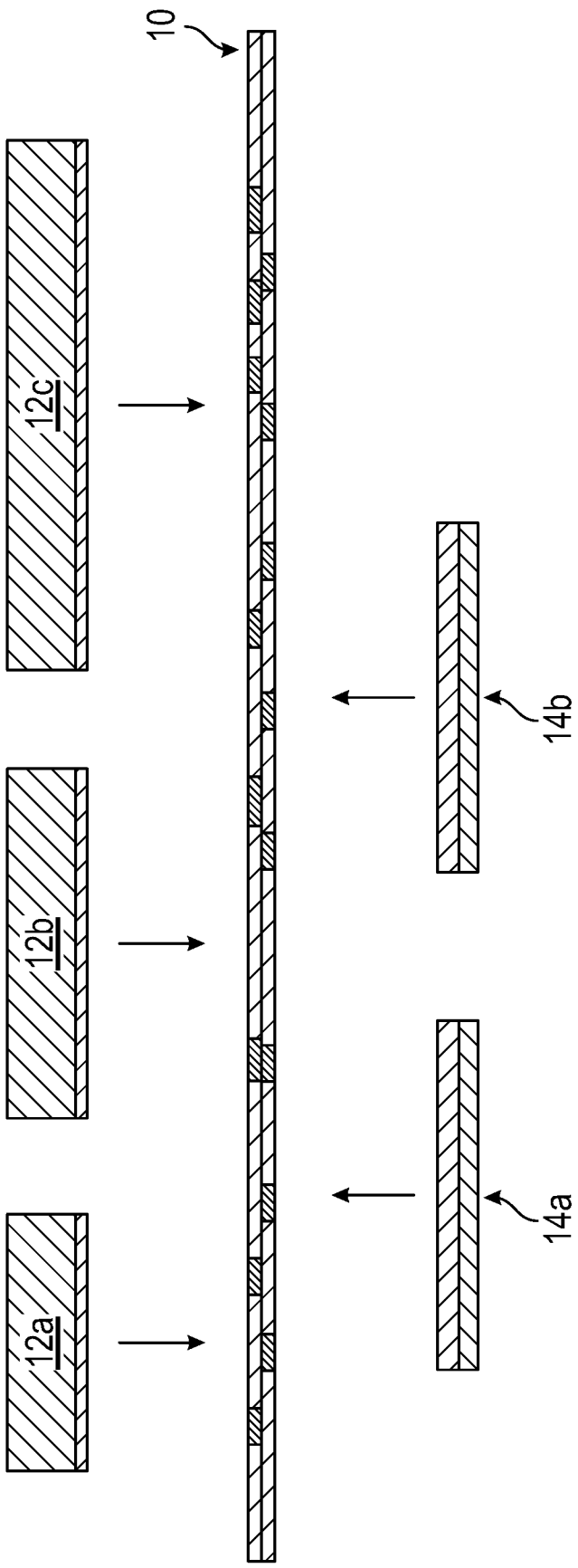


FIG. 1A

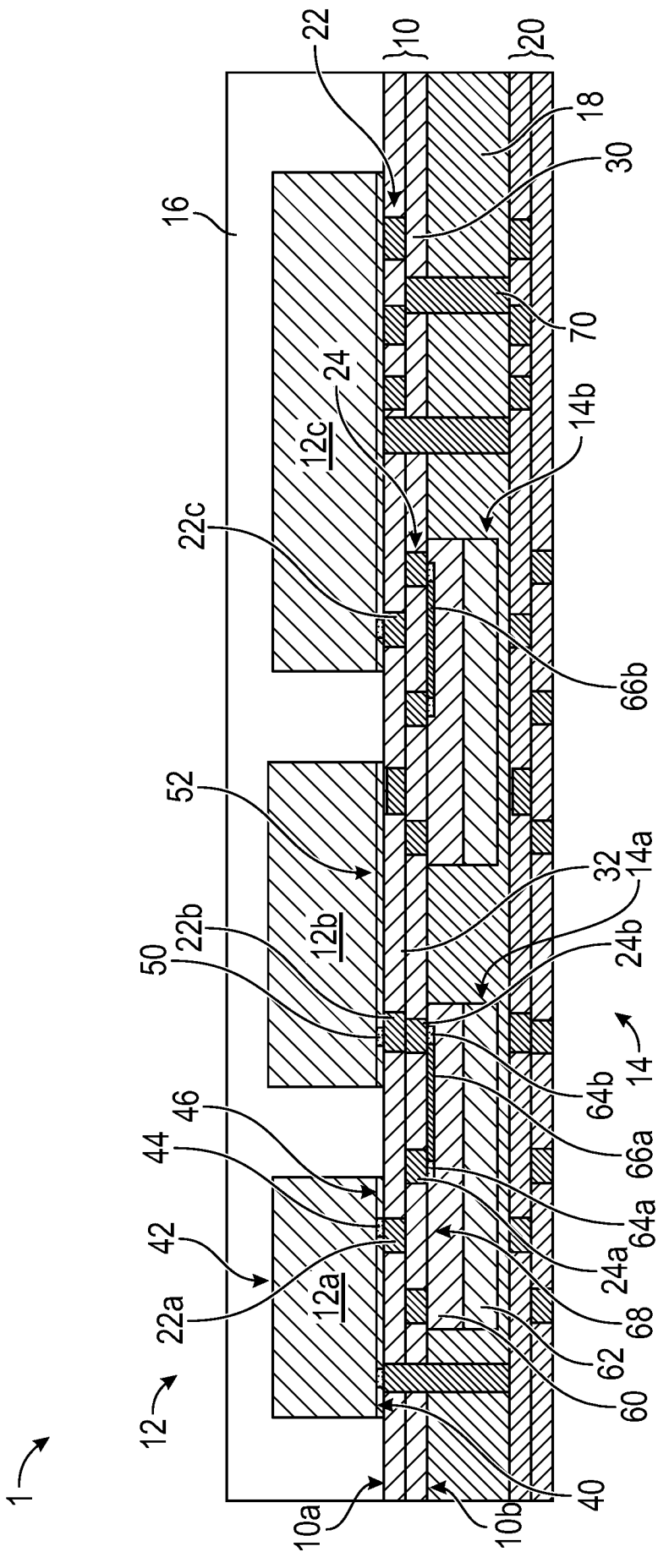

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FIG. 1B

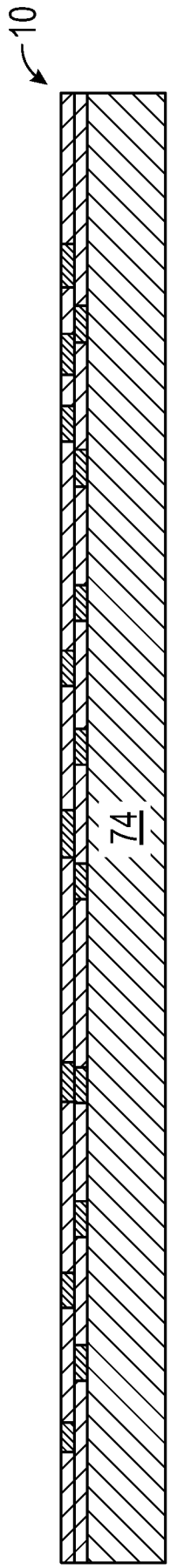


FIG. 2A

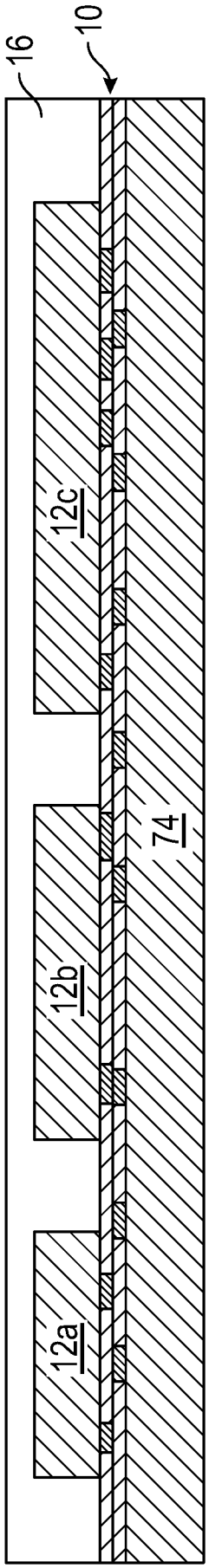


FIG. 2B

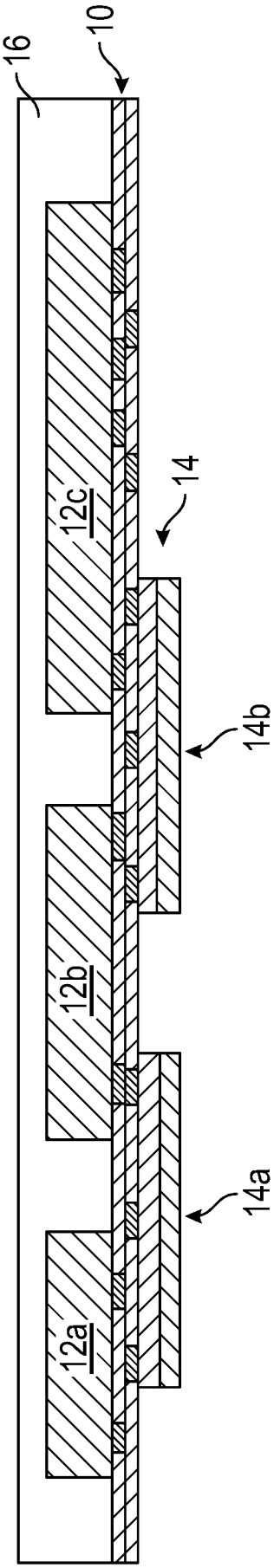


FIG. 2C

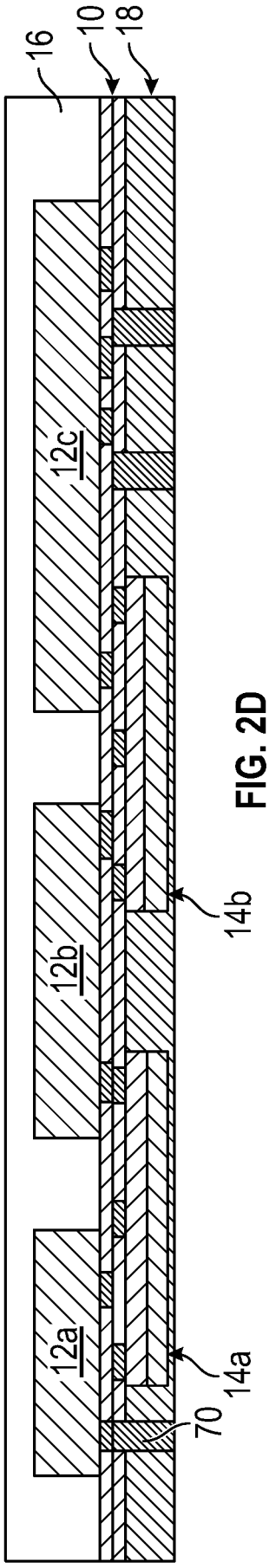


FIG. 2D

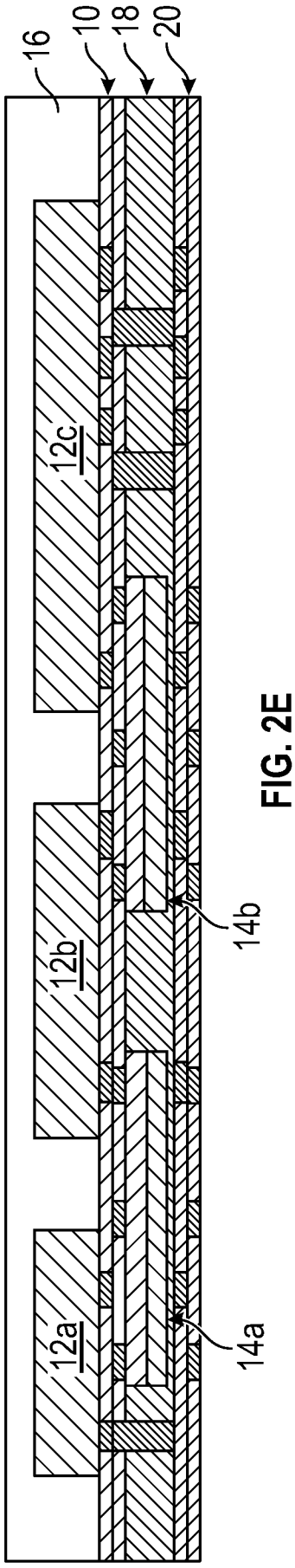


FIG. 2E

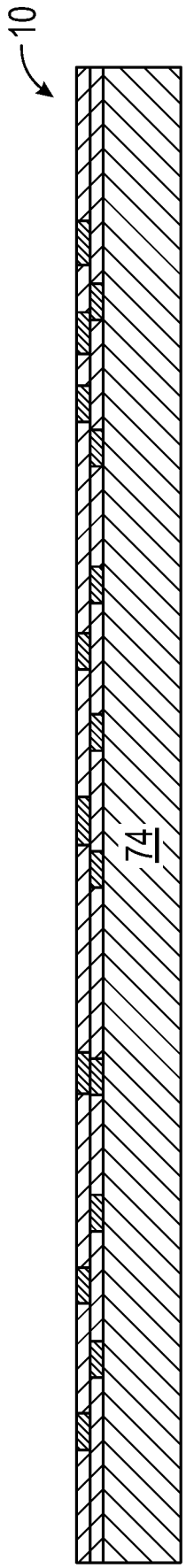


FIG. 3A

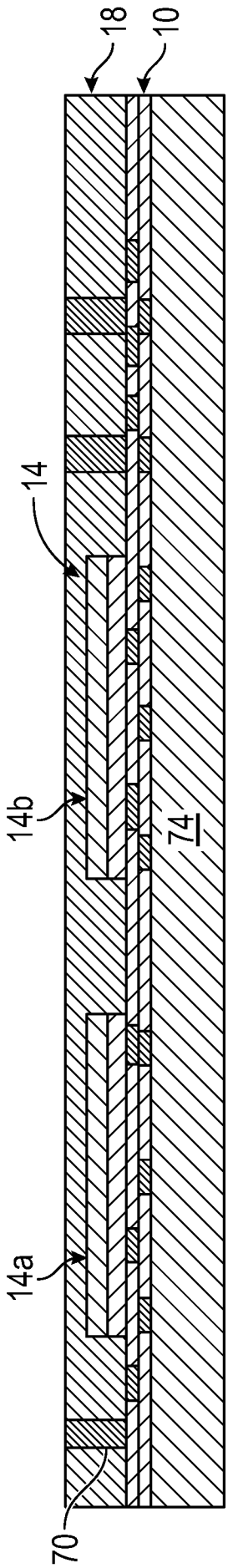


FIG. 3B

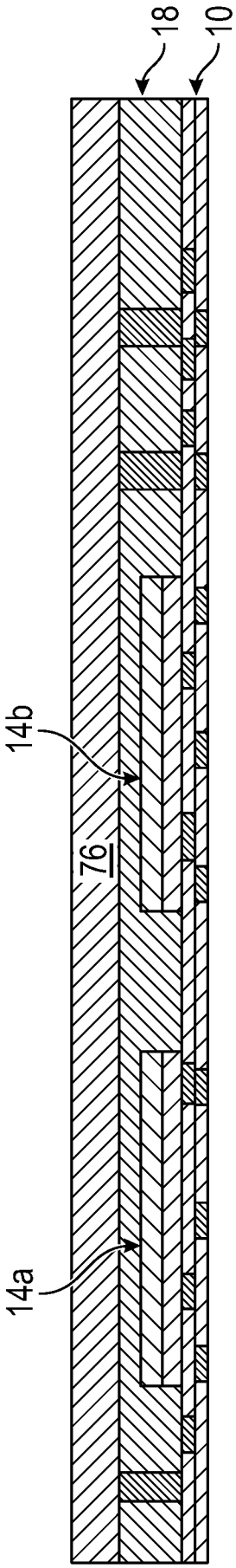


FIG. 3C

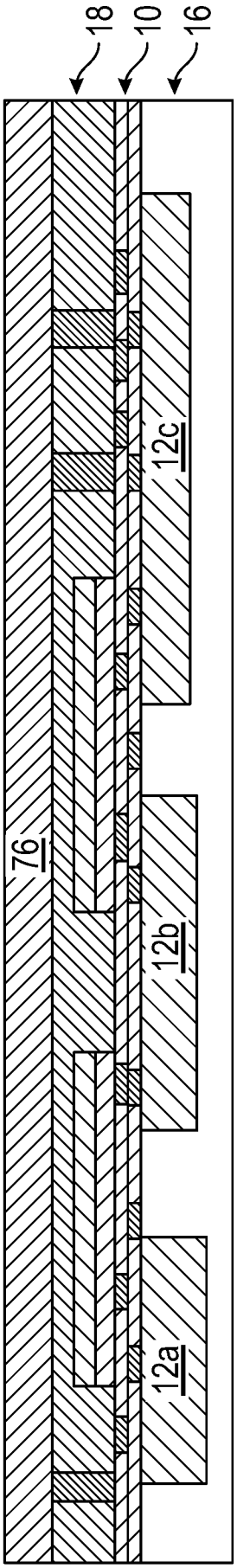


FIG. 3D

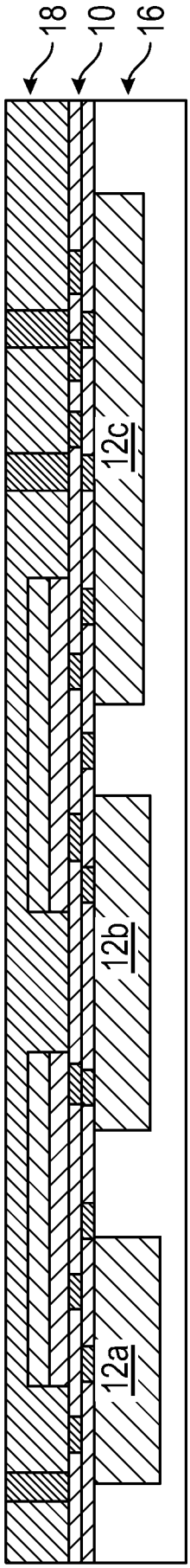


FIG. 3E

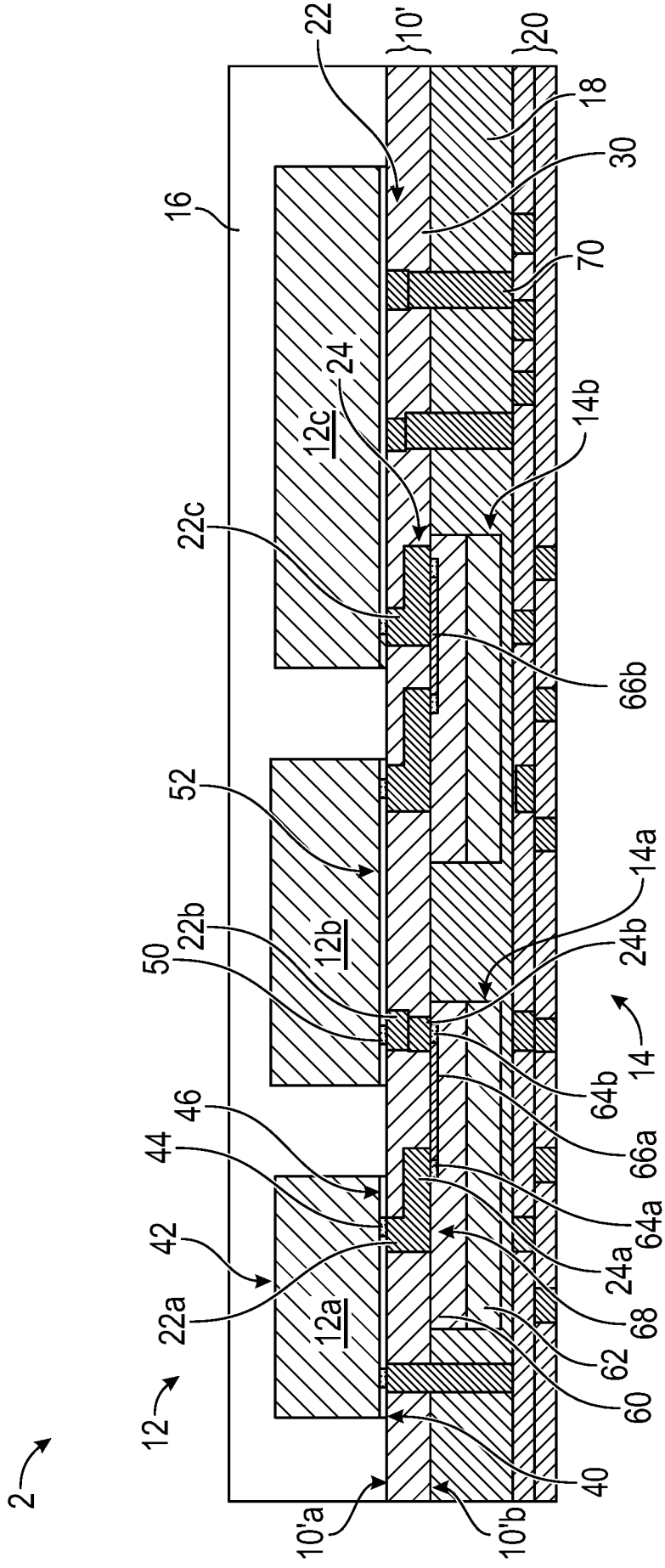

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10'b

FIG. 4

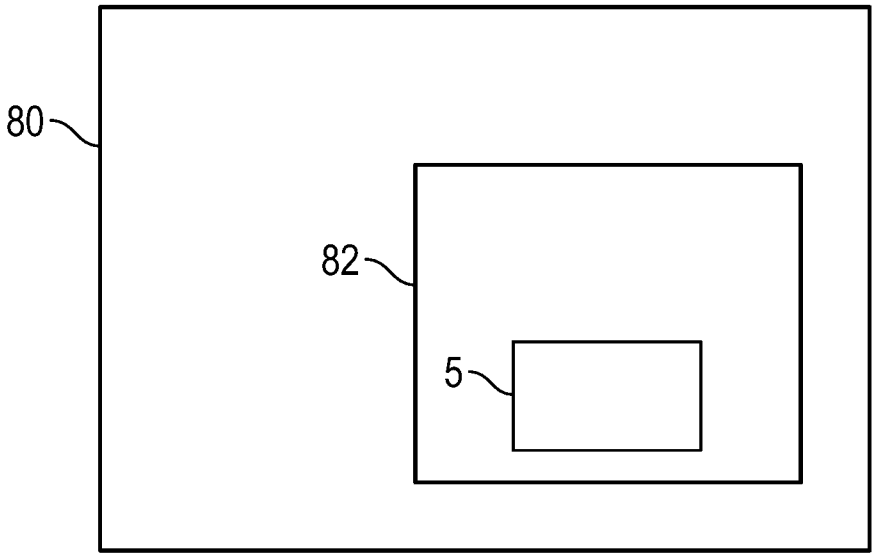


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2021/046749

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/538(2006.01)i; **H01L 23/00**(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/538(2006.01); H01L 21/00(2006.01); H01L 21/66(2006.01); H01L 23/00(2006.01); H01L 23/522(2006.01); H01L 25/00(2006.01); H01L 25/065(2006.01); H01L 27/146(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: direct, bonding, interconnect, redistribution-layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2017-0062383 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 02 March 2017 (2017-03-02) Paragraphs 17-71; and figures 3-15.	1-4,6-7,9-20, 22-23,25-43
Y		5,8,21,24
Y	US 10559507 B1 (FACEBOOK TECHNOLOGIES, LLC) 11 February 2020 (2020-02-11) Column 5, lines 19-28; and figure 1.	5,8,21,24
A	US 2016-0260684 A1 (APPLE INC.) 08 September 2016 (2016-09-08) Paragraphs 41-57; and figures 1-7B, 12.	1-43
A	US 2015-0171050 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 18 June 2015 (2015-06-18) The entire document.	1-43

☑ Further documents are listed in the continuation of Box C.

☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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Date of the actual completion of the international search	Date of mailing of the international search report
08 December 2021	**08 December 2021**

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INTERNATIONAL SEARCH REPORT

International application No.
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