Dec. 27, 1966 B. K. NELSON 3,295,138

PHASED ARRAY SYSTEM

Filed Oct. 31, 1963 2 Sheets-Sheet 1

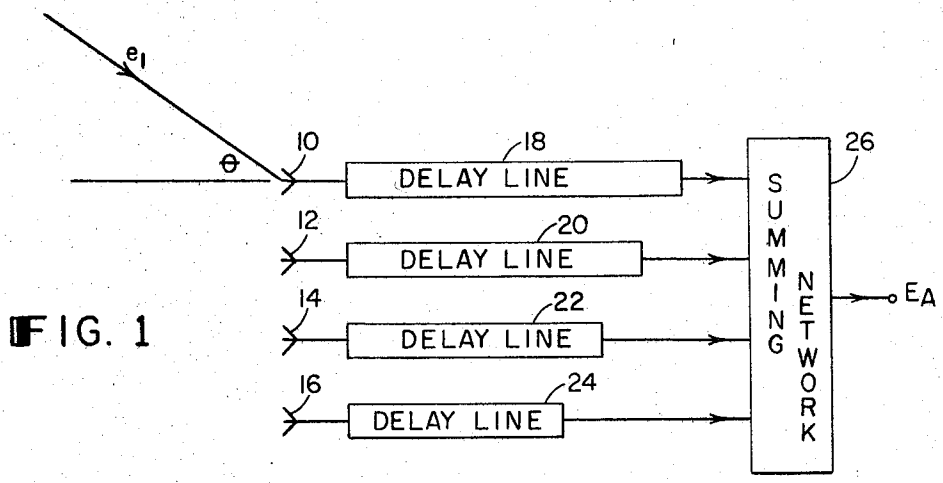

FIG. 1

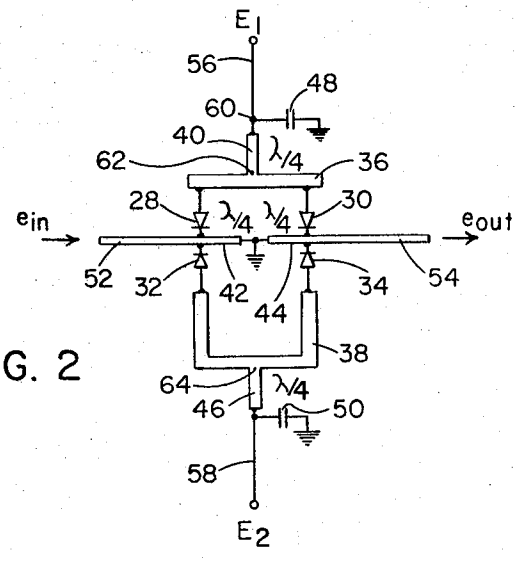

FIG. 2

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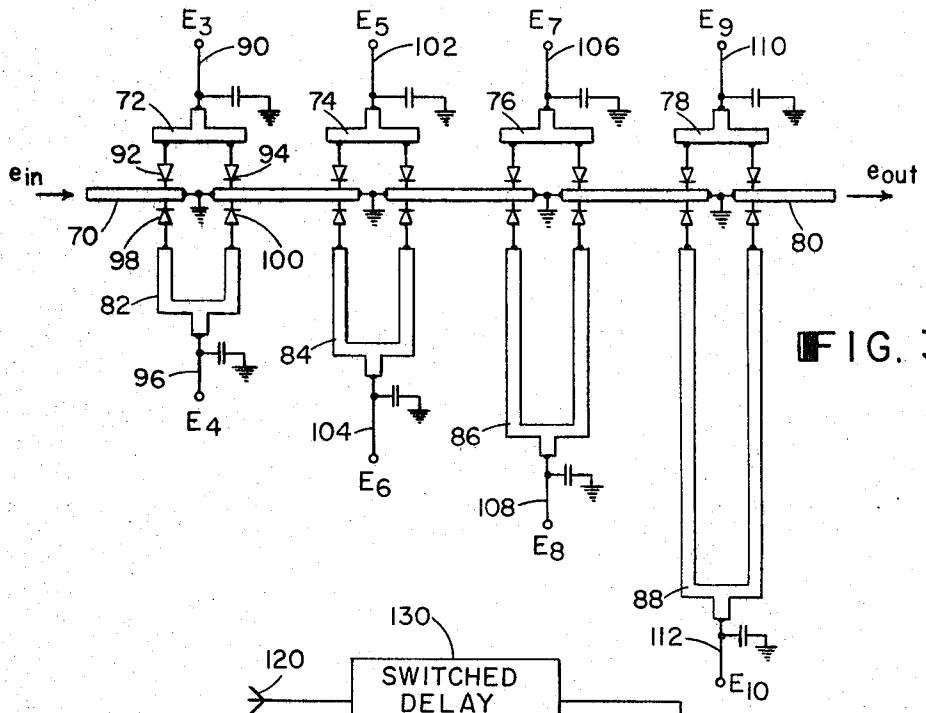

FIG. 3

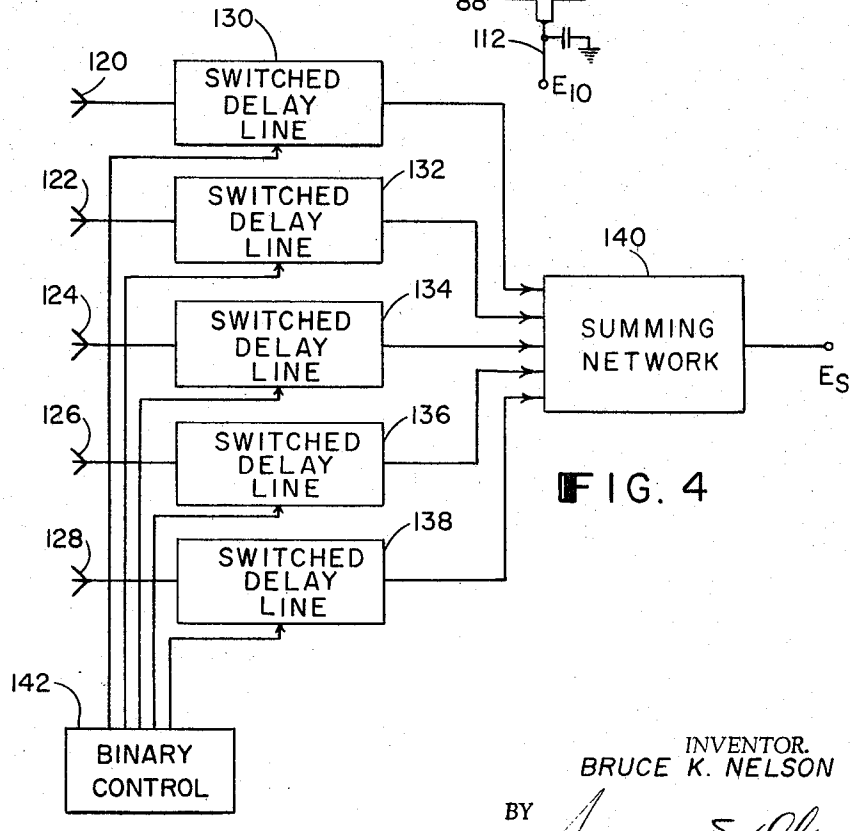

FIG. 4

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PHASED ARRAY SYSTEM

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5 Claims. (Cl. 343—854)

This invention relates to phased array antennas and more particularly to digitally controlled beam steering systems therefor.

In a phased array antenna, the antenna beam is steered by adjusting the relative phase shifts in individual antenna element channels of the array such that coherent addition of signals received by the array occurs for signals arriving from a specified direction. These arrays are, however, inherently frequency sensitive due to the frequency dependent nature of the signal phase, and, consequently, the antenna beam steering direction. To overcome the disadvantage of frequency sensitivity that is inherent in these arrays, time delay steering has evolved wherein signals propagating in each antenna element channel are time delayed by selected amounts in order to bring the signals into time coherence, and thus steer the antenna beam to a specified direction. A broadband beam steering system can, therefore, be provided by varying the time delay, rather than the phase shift, in each element channel.

Heretofore, various systems have been proposed to implement time delay steering. In one known system, a helical delay line is employed and a variable time delay provided by coupling signals off the delay line at various points on the helix. Another known scheme employs a plurality of fixed delay lines, such as coaxial cables, each having a different delay time, which are individually switched into an antenna element channel to provide a given time delay. These techniques, however, suffer the disadvantages of slow switching speeds, being cumbersome to fabricate, and unwieldy in size and weight. A primary object of the present invention is, therefore, to provide a phased array having a compact, rapidly adjustable, time delay beam steering system.

Another object of the invention is to provide a phased array having a beam steering system employing switched delay lines.

A further object of the invention is to provide a phased array beam steering system having binary controlled switched delay lines.

Briefly, the invention comprises a phased array beam steering system in which binary controlled switched delay lines are employed to appropriately delay signals in each antenna element channel. Each switched delay line comprises a plurality of fixed time delays which are variously combined to produce successive increments of delay in response to binary control signals. Binary control is especially advantageous since it can be easily provided by well-known means, and in addition, rapid switching speeds are practicable with such control. Accordingly, an antenna beam can be rapidly steered in response to binary control signals.

The foregoing, together with other objects, features, and advantages of the present invention will become more apparent from the following detailed description, taken in conjunction with the drawings in which:

FIG. 1 is a schematic diagram of a phased array antenna employing time delay steering;

FIG. 2 is a schematic diagram of a switched delay line in accordance with the present invention;

FIG. 3 is a schematic diagram of a four-bit binary switched delay line in accordance with the invention; and

FIG. 4 is a schematic diagram of a preferred embodiment of the invention.

Referring to FIG. 1, there is shown a phased array receiver consisting of antenna elements **10**, **12**, **14**, and **16**, connected, respectively, to delay lines **18**, **20**, **22**, and **24**, which are of progressively decreasing length. The outputs of these delay lines are connected to a summing network **26**, the output E_A of which is a signal representative of the antenna beam. It is evident that a received signal e_1 arriving, for example, at an angle θ with respect to the broadside axis of the array takes increasingly longer times to reach elements **12**, **14**, and **16** than to reach element **10**. In order to bring the received signal into time coherence, and thus enhance the sensitivity of the array to a signal arriving at an angle θ, the signals in each element channel must be suitably delayed such that coherent addition can be achieved. Thus, a signal arriving at an angle θ, and received by elements **10**, **12**, **14**, and **16**, is delayed by delay lines **18**, **20**, **22**, and **24**, each of which provides progressively less delay of suitable magnitude to bring the signals into time coherence. The magnitude of the delay in each element channel is proportional to the distance of its respective antenna element from the electrical center of the array, as is well known. Of course, the array can function equally as well in the transmitting mode, in this event the summing network being replaced by a power dividing network to energize the antenna elements, as is also well known.

In order to steer the array through a given angular sector it is, of course, necessary to suitably vary the interchannel time delay. An expeditious way of providing this variable time delay is by a binary controlled switched delay line, illustrated in FIG. 2, wherein two signal paths are provided, one path having a relatively greater time delay than the other. By switching between these two signal paths, either of two time delays can be provided in response to appropriate binary control signals. Alternatively, one signal path can have essentially zero time delay, in which case switching between signal paths provides either zero delay or some finite delay. A greater number of time delays can be provided by serially connecting individual switched delay lines to provide a multisection delay line of the type shown in FIG. 3, as will be more fully explained hereinafter. Referring now to FIG. 2, diodes **28**, **30**, **32**, and **34** are arranged in a bridge configuration with a signal path **36** between the anodes of diodes **28** and **30**, and a second signal path **38** of greater length than path **36**, disposed between the anodes of diodes **32** and **34**. Diodes **28** and **30** are rendered conducting by a suitable direct current bias signal E_1 applied to bias line **56**, while diodes **32** and **34** are caused to conduct by a direct current bias signal E_2 applied to bias line **58**. Signal paths **36** and **38**, and input and output lines **52** and **54**, respectively, are, for example, strip transmission lines. Other energy transmission means can be employed in the construction of a switched delay line, although the circuit configuration lends itself particularly to a strip transmission line embodiment.

In order to isolate the RF signal paths from the biasing circuit, a suitable decoupling circuit must be employed, a typical one being illustrated in FIG. 2 and consisting of quarter wave sections **40**, **42**, **44**, and **46**, and capacitors **48** and **50**. Capacitors **48** and **50** have a low reactance at the operating frequencies thereby presenting a high impedance to the direct current bias signals E_1 and E_2, respectively. At RF frequencies, however, capacitor **48** offers essentially a short circuit from point **60** to ground. This short circuit, translated through quarter wave section **40**, presents a high impedance at point **62**. In this manner, RF energy propagating through signal path **36** is not affected by the biasing circuit since the latter is decoupled by the high impedance at point **62**. In like manner, a high impedance is presented at point

64 due to the reflected short circuit to ground through capacitor 50. Thus, RF energy propagating through signal path 38 is unaffected by the biasing circuit due to the high impedance at point 64.

In operation, a signal e_{in}, applied to input line 52 can propagate by way of either signal path 36 or 38, depending on which path is activated. Bias signal E_1, applied to bias line 56 causes diodes 28 and 30 to conduct thereby presenting a low impedance to RF energy present on input line 52, which allows signal e_{in} to propagate through diode 28, path 36 and diode 30, to the output line 54. Since bias signal E_2 is not applied, the diodes 32 and 34 are not conducting and, therefore, present an open circuit to oppose the flow of RF energy in signal path 38. On the other hand, a bias signal E_2, applied to bias line 58, causes diodes 32 and 34 to conduct thus allowing signal e_{in} to traverse the path consisting of diode 32, delay path 38, and diode 34, to output line 54. Path 38 being longer than path 36, an output signal e_{out} appearing on line 54, has one of two delays, depending on which signal path is traversed. Thus, if the length of signal path 38 is dimensioned such that it has a time delay τ with respect to the time delay of path 36, a time delay τ can be imparted to the output signal e_{out} depending upon whether path 36 or 38 is energized by bias signals E_1 or E_2, respectively. It is seen that bias signals E_1 and E_2 are binary in nature, one being applied while the other is not; therefore, digital control means can be employed to vary the time delay.

By expanding the design of a switched delay line of the type shown in FIG. 2 to a multi-section delay line, such as that illustrated in FIG. 3, a greater number of time delay increments is possible, and particular advantage can be made of the simplicity of digital control. Referring to FIG. 3, a four-section switched delay line is shown with the output of each section connected to the input of each succeeding section. Signal paths 72, 74, 76, and 78 have essentially zero time delay, while signal paths 82, 84, 86, and 88 have time delays in the ratio $\tau:2\tau:4\tau:8\tau$, respectively, where τ is the smallest increment of time delay. It is evident that time delays from zero to 15τ, in integral multiples of τ, are possible by judiciously combining the various signal paths. To provide zero delay, an input signal e_{in} is directed through signal paths 72, 74, 76, and 78 to the output line 80. For a maximum delay of 15τ, input signal e_{in} is directed through signal paths 82, 84, 86, and 88 to output line 80. Intermediate values of delay are provided by shunting the input signal through selected combinations of signal paths. RF decoupling is provided as in the delay line of FIG. 2.

The operation of each delay line section is identical to that of the delay line of FIG. 3. For example, a bias signal E_3 causes diodes 92 and 94 to conduct, thereby providing a low impedance path by which input signal e_{in} can traverse signal path 72. Similarly, a bias signal E_4 applied to bias line 96 energizes diodes 98 and 100, thereby allowing the input signal to propagate through delay path 82. In like manner, a bias signal applied to bias lines 102, 104, 106, 108, 110, and 112, respectively, causes the corresponding diodes to conduct, thereby shunting the input signal through the signal path associated with the conducting diodes.

It will be remembered that the bias signals applied to each section of the delay line are binary in nature, and it is evident that binary values 0 to 1 can be assigned to the OFF and ON bias signals, respectively. The bias signal applied to each section of the delay line is, therefore, equivalent to one bit in a four-bit binary word. Thus, the binary progression 0000, 0001, . . . 1111, is representative of the progression of bias signals required to provide progressively increasing time delays from 0 to 15τ, in increments of τ. For a given time delay, the binary control word necessary to provide that delay is applied, respectively, to bias terminals 96, 104, 108, and 112, while the complement of this binary word is applied, respectively, to bias lines 90, 102, 106, and 110. Thus, a variable time delay can be provided by well known digital control techniques, with the accompanying advantages of extremely fast speed, and relative simplicity of equipment.

The incorporation of these binary controlled switched delay lines into an antenna array is illustrated in FIG. 4, wherein a five element linear array is schematically shown including antenna elements 120, 122, 124, 126, and 128, each having associated therewith a respective switched delay line 130, 132, 134, 136, and 138. The output of each switched delay line is connected to a summing network 140, the output E_s of which is a signal representative of the assembled antenna beam. Suitable biasing of each switched delay line is provided by a binary control 142, which can be one of several well known means, such as a digitally programmed power supply.

The antenna array can, of course, be used equally well for both transmitting and receiving, the beam steering system being essentially the same in both instances. For simplicity of explanation, its operation will be described in the receiving mode. In operation, a signal received by each antenna element is applied to a corresponding switched delay line which introduces the appropriate time delay into each element channel in response to a proper binary control signal produced by binary control 142. The output signal from each switched delay line is thus suitably time delayed so that coherent addition of the signals from each antenna element can be accomplished by summing network 140. To scan the antenna beam, it is merely necessary to appropriately alter the binary control signals applied to each switched delay line. As an illustration of the expediency of binary control, consider the situation where the electrical and physical center of an array are coincident. In the embodiment of FIG. 4, the center would be at antenna element 124. Since the time delay for a given element channel is related to the distance of the antenna element of that channel from the electrical center of the array, it is evident that the delay inserted in each element channel on one side of the array center must have an equal and opposite time delay inserted in corresponding element channels on the opposite side of the array center. For example, in the embodiment of FIG. 4, for a given beam steering direction, the time delay associated with delay line 132 is the complement of the time delay associated with delay line 136. Similarly, the time delays associated with delay lines 130 and 138 are complementary. These complementary time delays are easily provided by applying a suitable binary control word to the appropriate switched delay lines on one side of the array center, while applying the binary complement of these words to the corresponding switched delay lines on the opposite side of the array center.

From the foregoing, it is evident that a phased array has been provided having a compact, rapidly adjustable, binary controlled, time delay beam steering system. The invention is not, of course, limited to the particular embodiments or construction illustrated and described herein, as many alternatives will occur to those skilled in the art. For example, while a linear array is illustrated, the invention can be employed with equal advantage in a two-dimensional array. In addition, the switched delay lines can be of a variety of constructions and can have as many delay paths as are necessary to suit the particular operating requirements. Accordingly, it is not intended to limit the invention by what has been particularly shown and described, except as indicated in the appended claims.

What is claimed is:

1. In a phased array antenna system which includes a plurality of antenna elements and a like plurality of signal processing channels, means for steering said array to a selected direction comprising, a source of binary control signals, and a switched delay line operatively associated with each of said channels, each of said switched delay lines comprising, a first plurality of delay lines having substantially zero time delay, a second like plurality of delay

lines having in succession time delays of geometrically increasing value, and diode switching means connected between respective ones of said first and second plurality of delay lines and operative in response to said binary control signals to selectively combine said delay lines to provide selected amounts of delay in each channel.

2. The invention according to claim 1 in which said diode switching means includes a diode bridge and RF isolated biasing circuitry.

3. The invention according to claim 2 in which said RF isolated biasing circuitry comprises a quarter wave transmission line section and a capacitor connected in series between each delay line and ground to thereby provide a high impedance to RF signals propagating in said delay lines.

4. The invention according to claim 1 in which said binary control signals are representative of progressively increasing binary numbers.

5. The invention according to claim 1 in which said second plurality of delay lines have fixed time delays related in a geometric progression with a common ratio of two.

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