United States Patent

Jachimek et al.

[15] **3,705,423**

[45] **Dec. 5, 1972**

[54] **ARRANGEMENT FOR TRANSLATING A TRAIN OF PULSES INTO LOGIC WORDS**

[72] Inventors: **Thomas P. Jachimek,** Evergreen Park, Ill. 60642; **Jack A. Mulford,** Springfield, Mo. 65804

[73] Assignee: **Seeburg Corporation,** Chicago, Ill.

[22] Filed: **Feb. 19, 1971**

[21] Appl. No.: **116,864**

[52] **U.S. Cl.**.....**340/347 DD,** 340/168 R

[51] **Int. Cl.**.....**H03r 13/00**

[58] **Field of Search**.....340/172.5, 347 DD, 168 S; 178/17.5, 26; 235/92 R, 92 CC

[56] **References Cited**

UNITED STATES PATENTS

3,235,661	2/1966	Oxley et al.	340/347 DD
3,209,330	9/1965	Bonomo	235/92 R

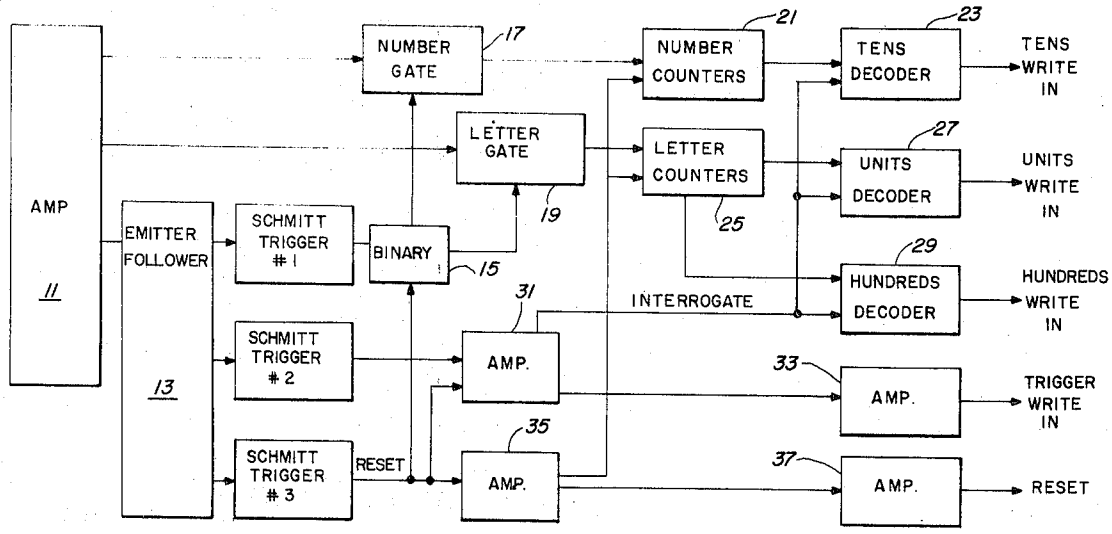
Primary Examiner—Thomas A. Robinson

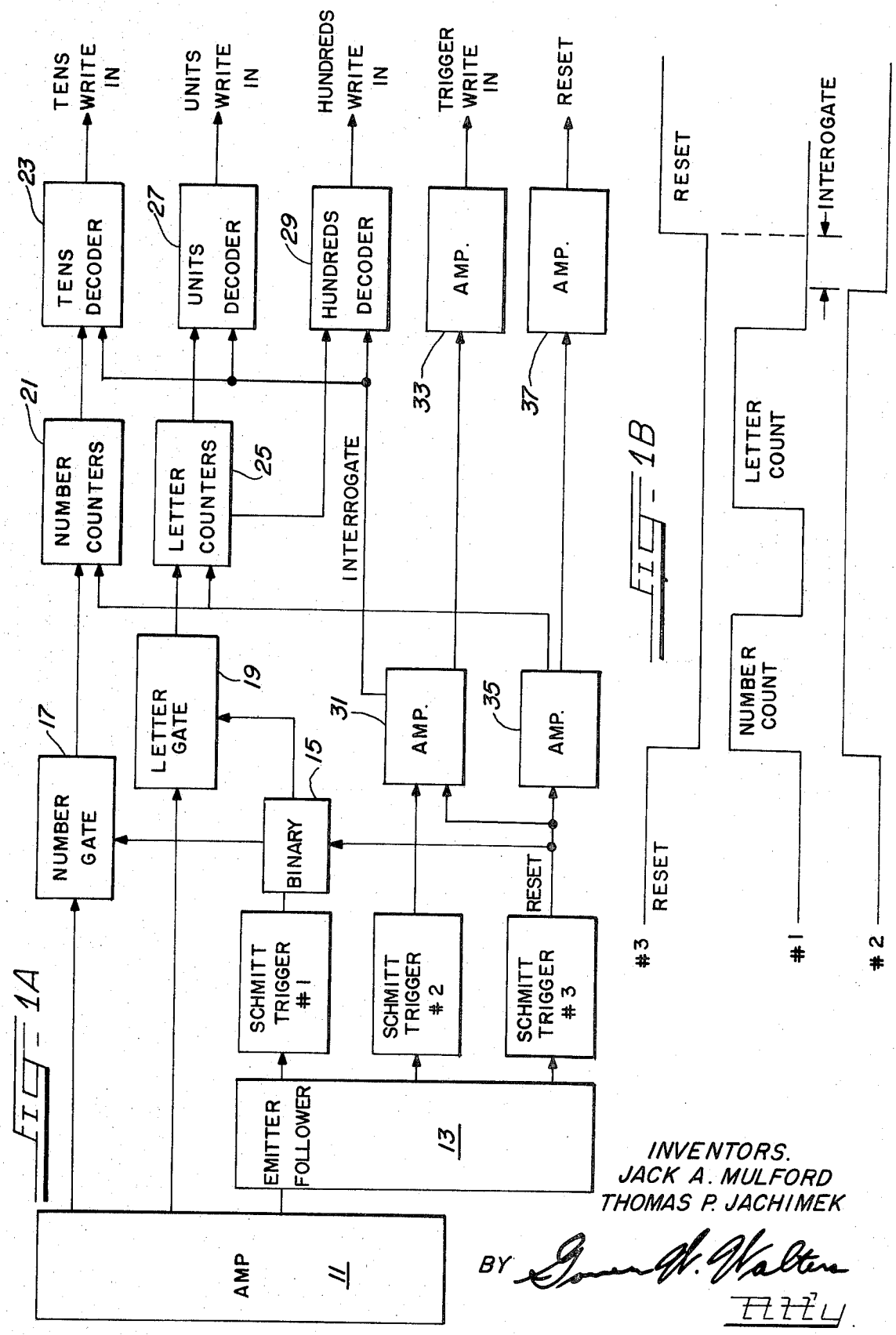
Attorney—Ronald L. Engel, Daniel W. Vittum, Jr., Gomer W. Walters, John A. Waters and James M. Amend

[57] **ABSTRACT**

A train of pulses divided into different sets of pulses has each set of pulses directed to a different counting and storing arrangement. The counting and storing arrangements are then actuated in proper time sequence to yield time spaced logic words incorporating appropriate bits of data.

11 Claims, 14 Drawing Figures





INVENTORS.
JACK A. MULFORD
THOMAS P. JACHIMEK

BY Thomas N. Walters

ATTY

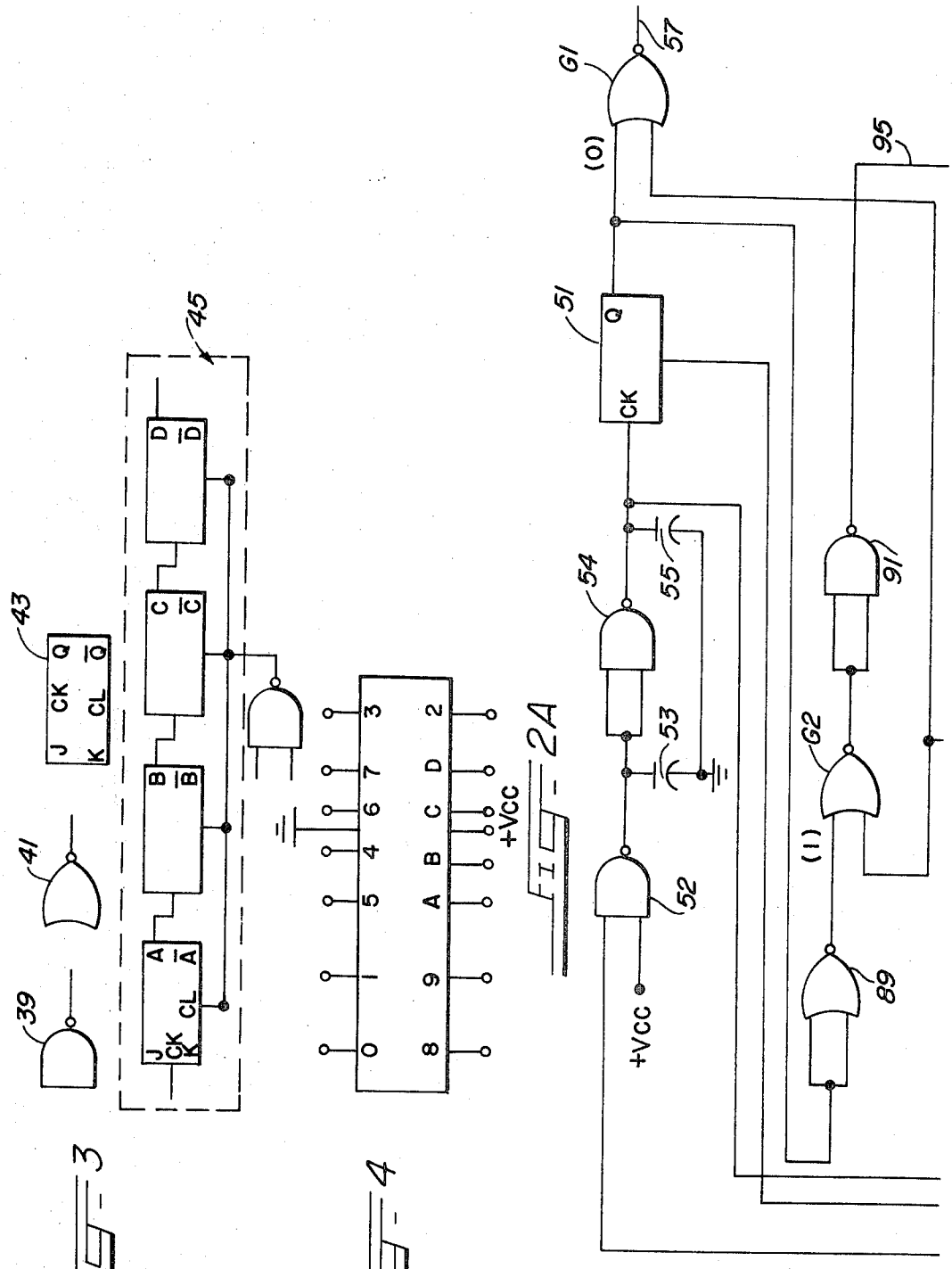


FIG-3

FIG-4

FIG-2A

INVENTORS.
JACK A. MULFORD
THOMAS P. JACHIMEK

BY George H. Walters

ATTY

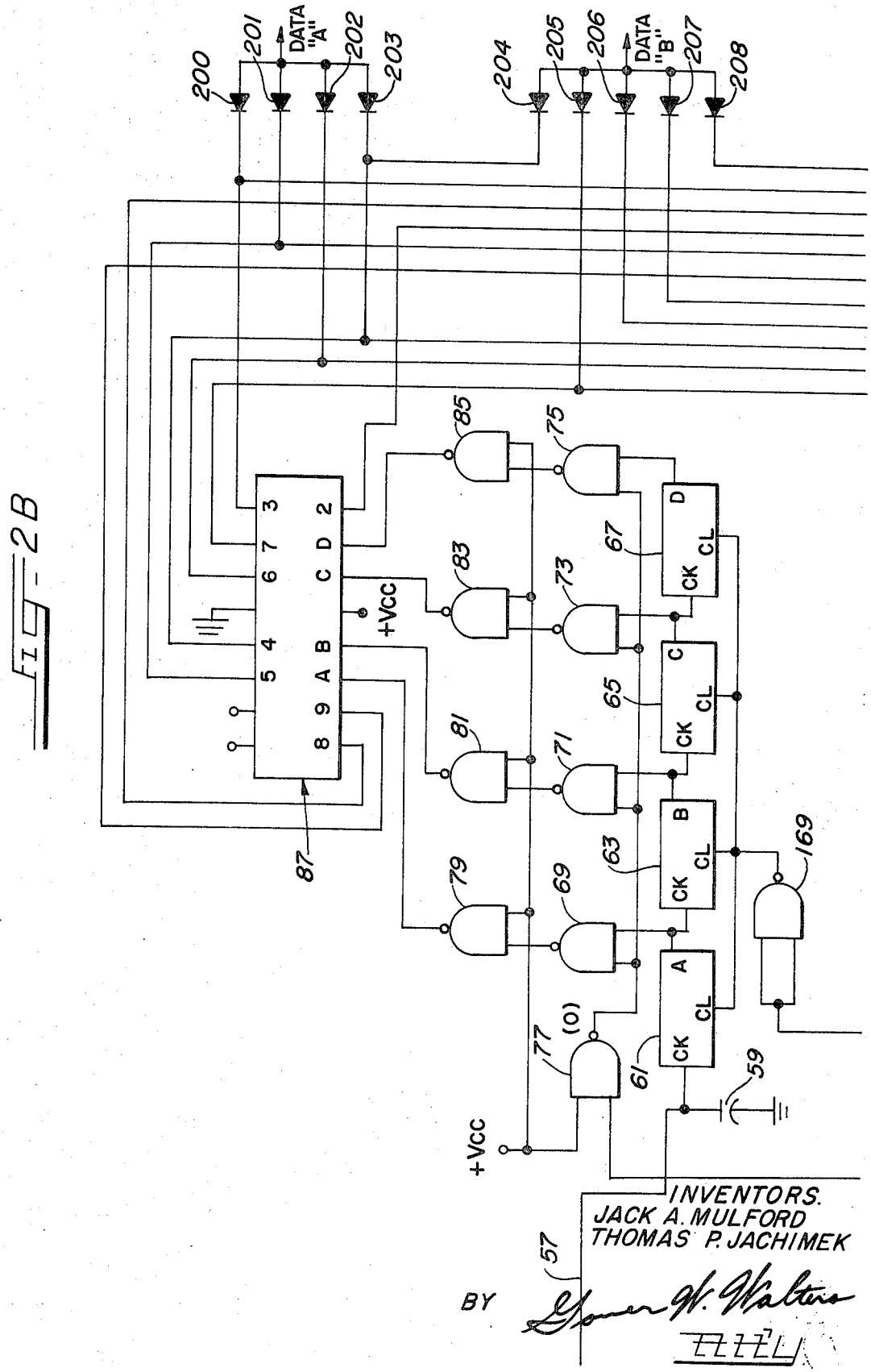

200
201
DATA "A"
202
203
204
205
206
DATA "B"
207
208
85
75
83
73
81
71
79
69
77
(0)
61
59
67
65
63
169
87
+Vcc
+Vcc
D
C
B
A
CK
CL
INVENTORS.
JACK A. MULFORD
THOMAS P. JACHIMEK
57
BY

FIG-2B

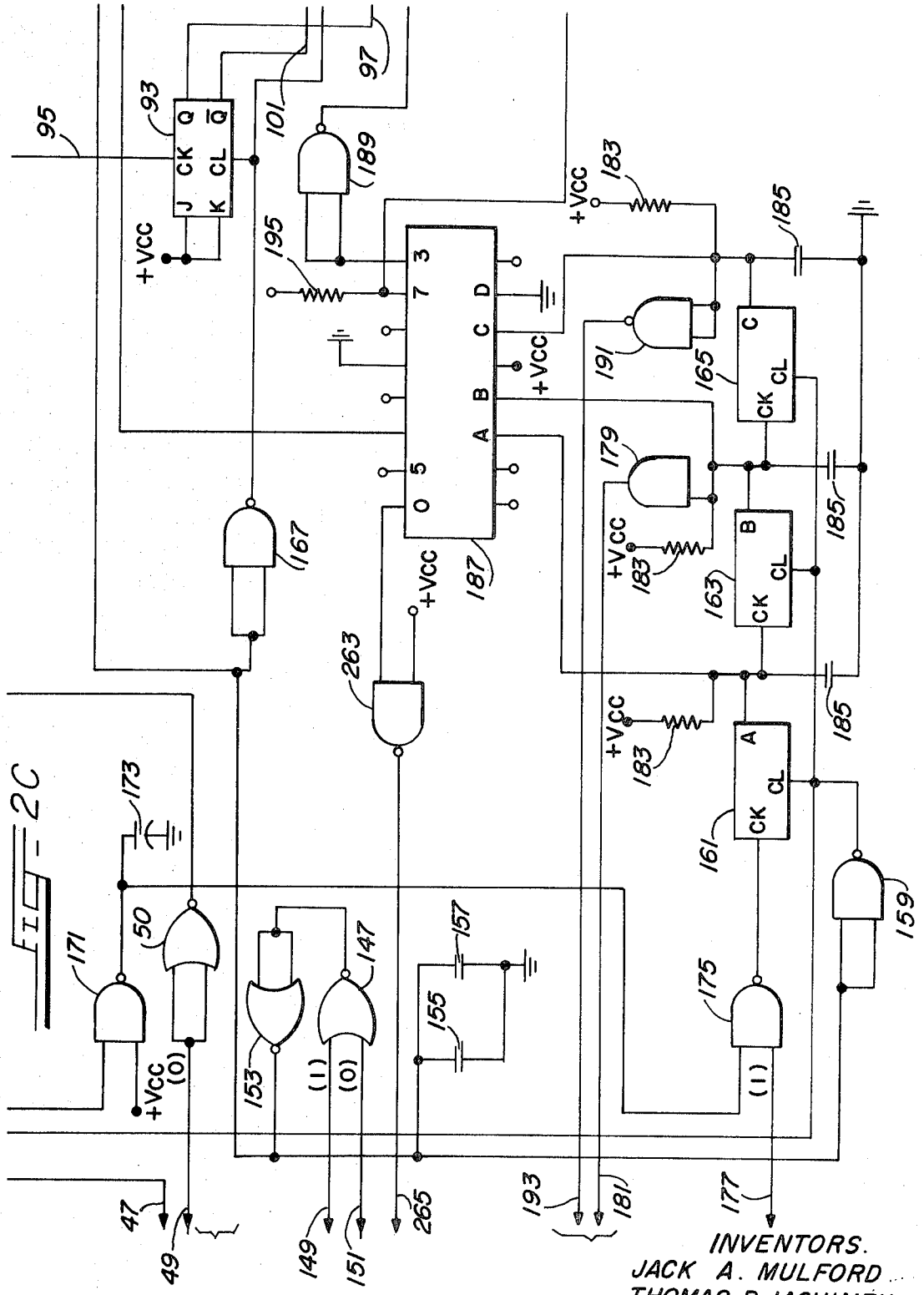


FIG-2C

INVENTORS.
JACK A. MULFORD
THOMAS P. JACHIMEK

BY George W. Walters

ATTY

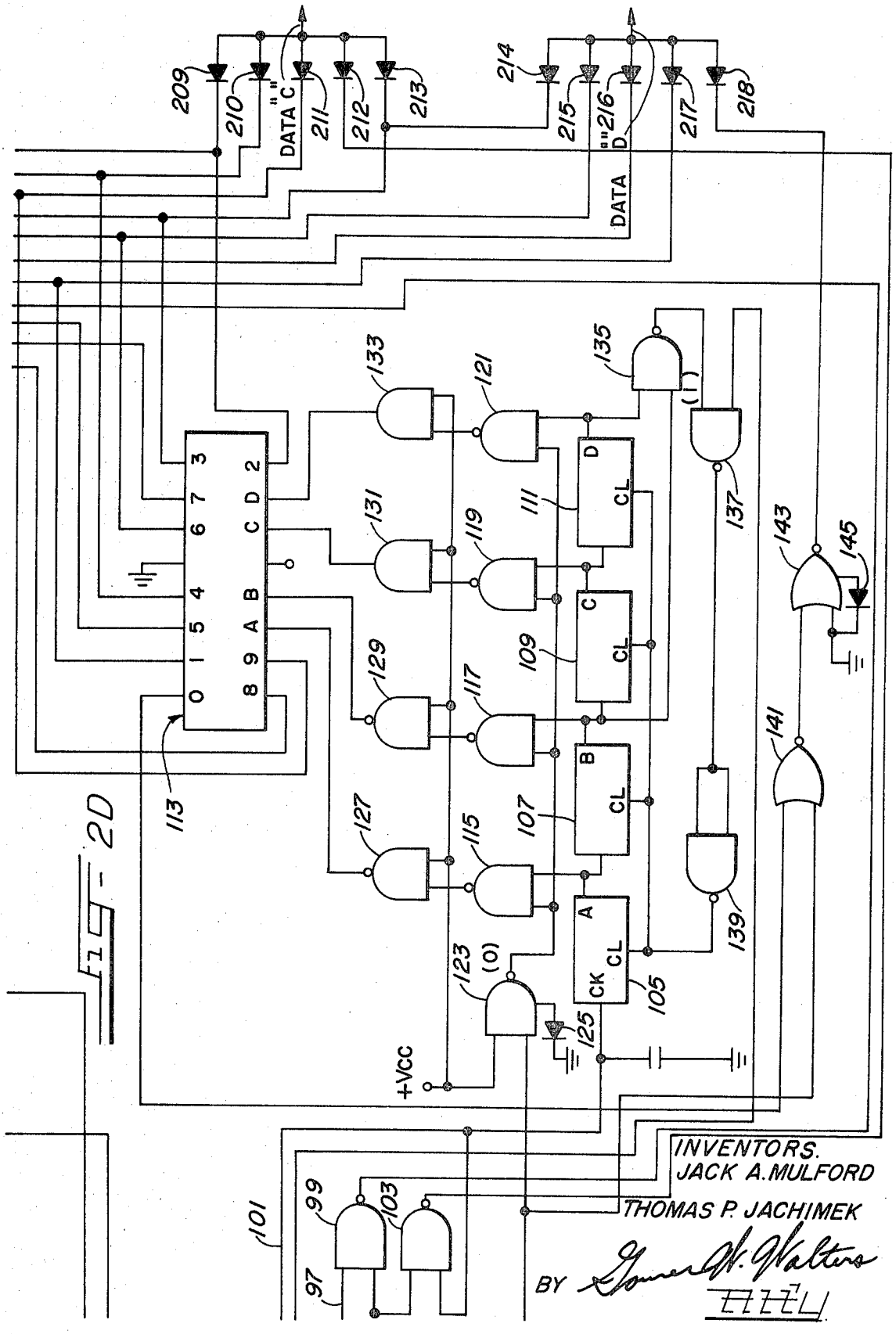


FIG-2D

INVENTORS.
JACK A. MULFORD
THOMAS P. JACHIMEK
BY Gomer H. Walters
ATTY

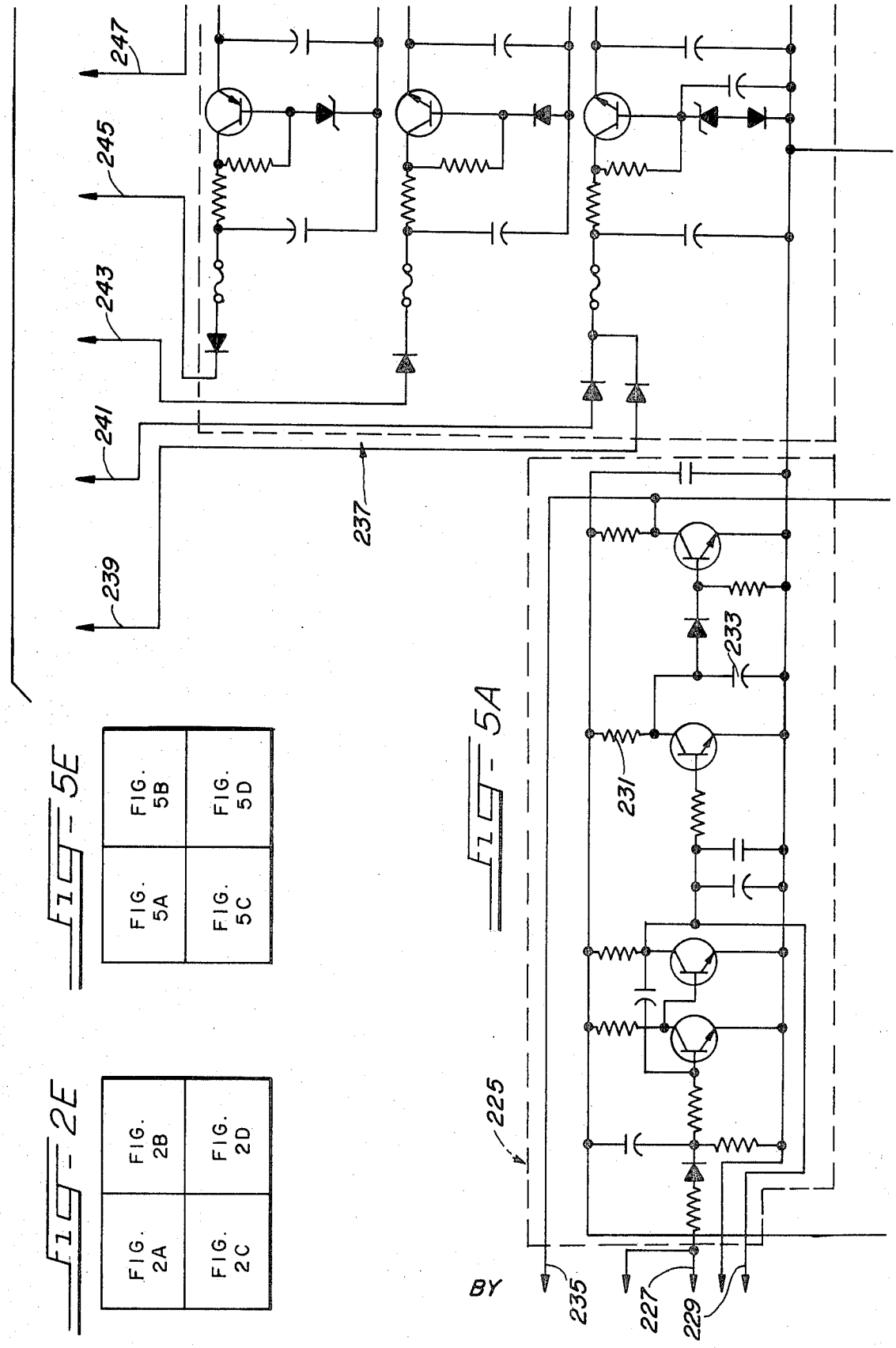


FIG. 5A

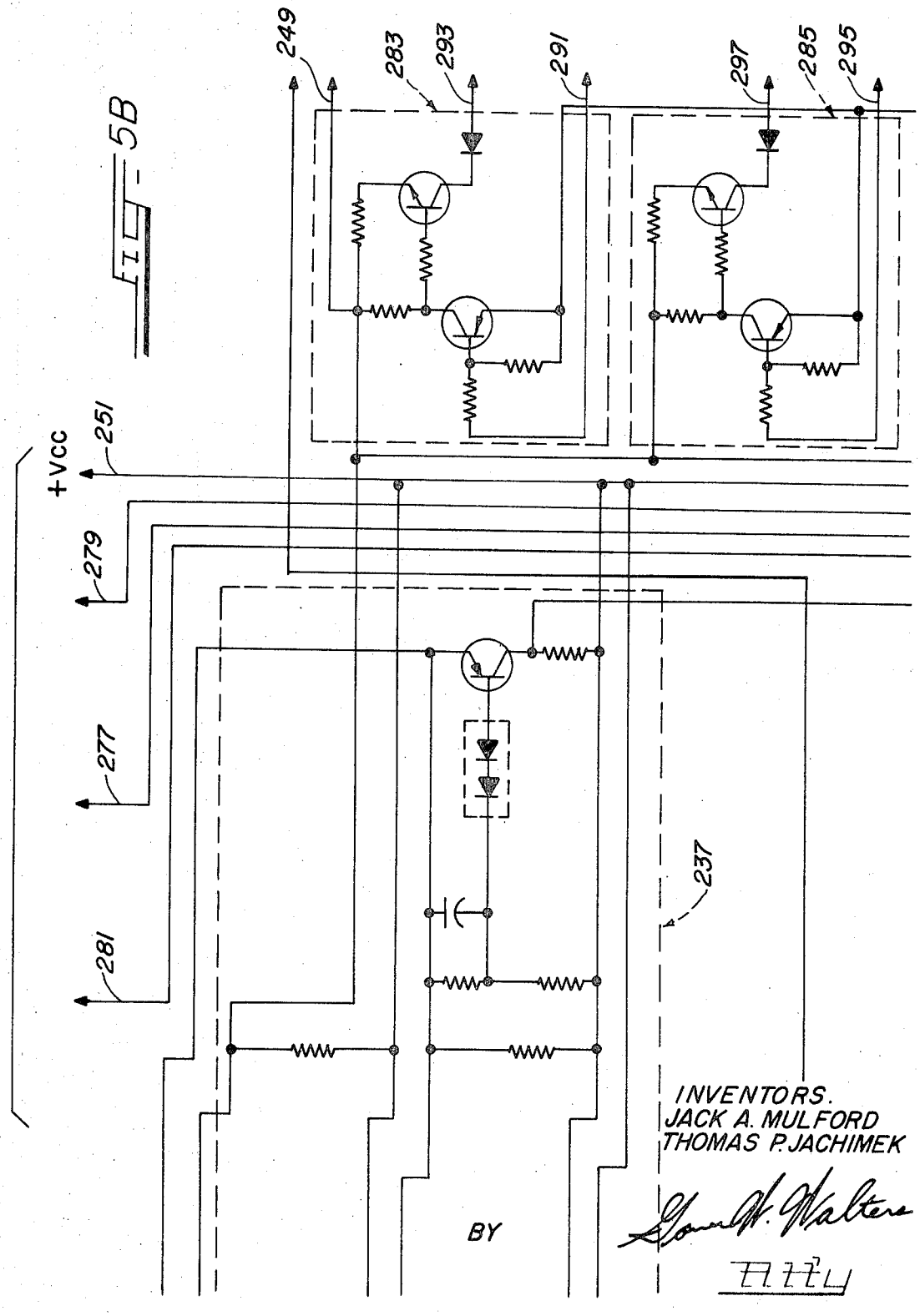
FIG. 5E

FIG. 5A	FIG. 5B
FIG. 5C	FIG. 5D

FIG. 2E

FIG. 2A	FIG. 2B
FIG. 2C	FIG. 2D

FIG. 5B



INVENTORS.
JACK A. MULFORD
THOMAS P. JACHIMEK

BY

Glenn H. Walters

Atty

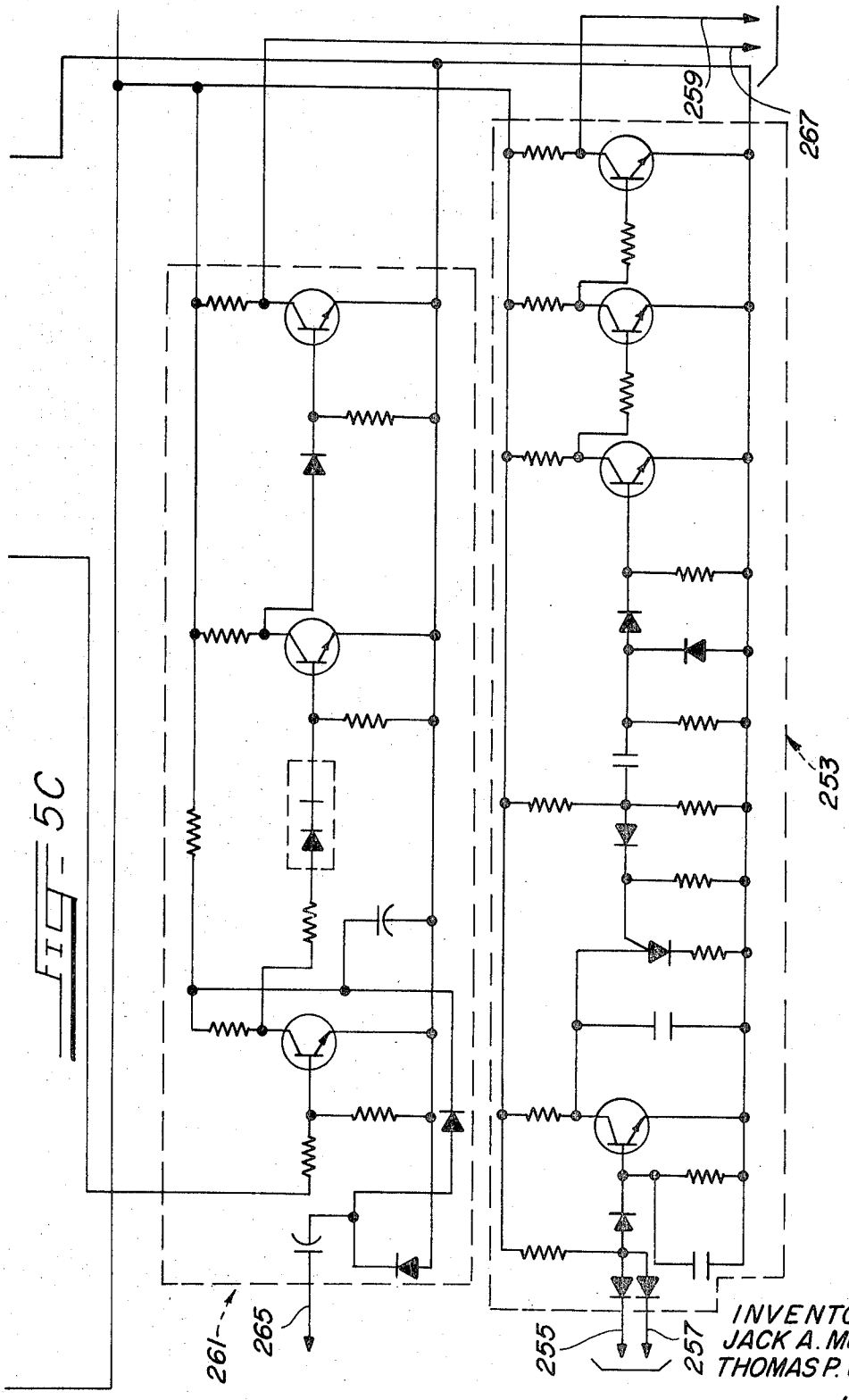


FIG- 5C

INVENTORS.
JACK A. MULFORD
THOMAS P. JACHIMEK

BY Glover W. Walters
ATTY

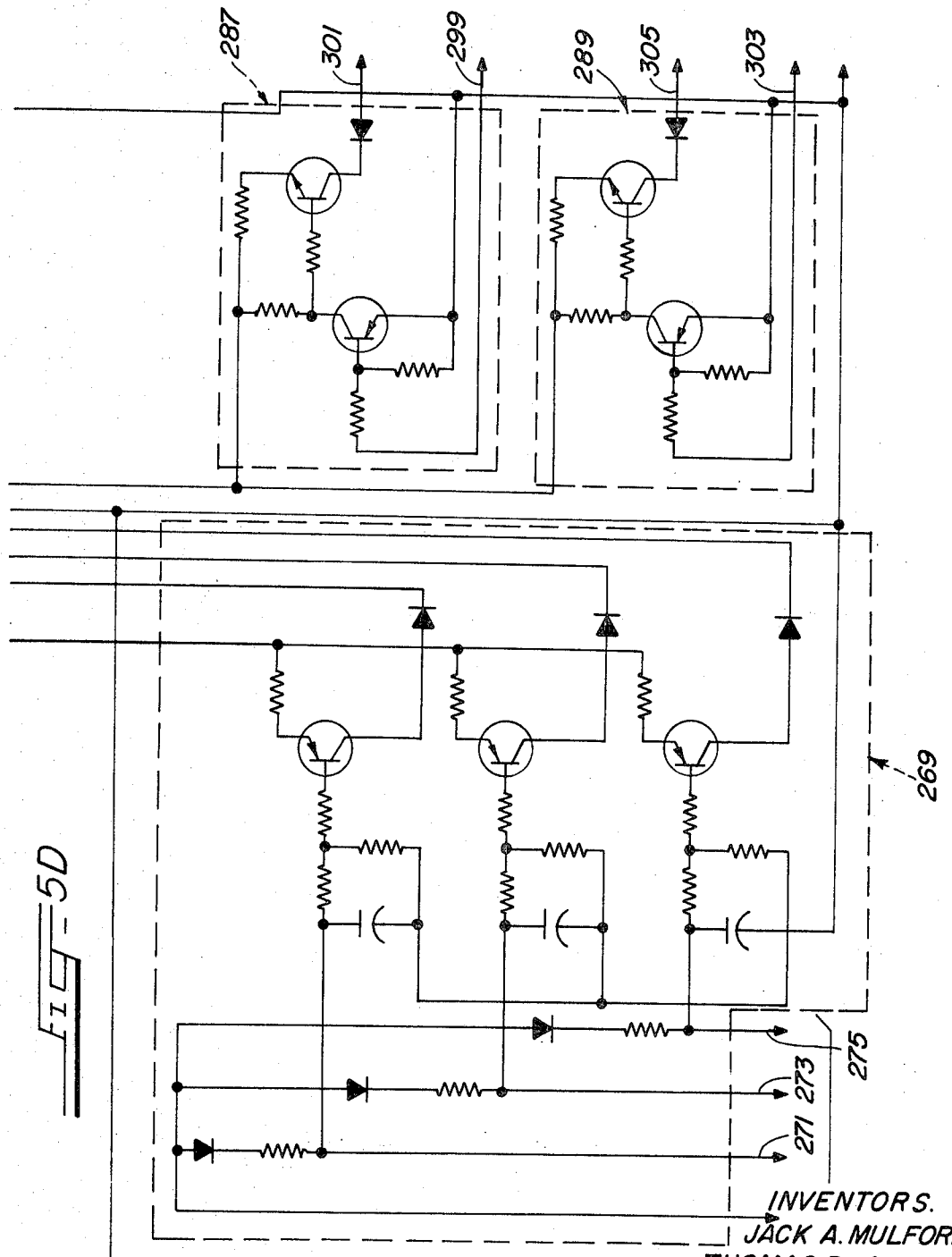


FIG-5D

INVENTORS.
JACK A. MULFORD
THOMAS P. JACHIMEK

BY Gomer H. Walters
ATTY

ARRANGEMENT FOR TRANSLATING A TRAIN OF PULSES INTO LOGIC WORDS

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to an arrangement for translating serially transmitted trains of pulses into logic words having data bits on parallel lines, and, more specifically, this invention relates to a coin-operated phonograph having an arrangement by which a train of pulses separated into sets of pulses is serially transmitted from a remote selecting station and is converted at the phonograph into logic words formed of data bits transmitted in parallel.

2. Description of the Prior Art

In the past, phonograph selecting arrangements have utilized letter-number combinations to identify the chosen selections. In a conventional type of arrangement of this nature, depression of a letter button and number button causes a series of pulses representative of the selected characters to be transmitted. This series, or train, of pulses would be divided into two sets of pulses, one corresponding to the letter selected and the other corresponding to the number selected. These pulses would be transmitted to the centrally located coin-operated phonograph which would include a device, such as a stepping relay, which would respond to the series of pulses and cause the appropriate recorded selection to be played.

With the advent of integrated circuits, it has been possible to dispense with the old letter-number approach and utilize series of digits to identify selections which may be easily chosen, such as by a telephone dial or push buttons. An example of such a system is that disclosed in the co-pending application of Thomas P. Jachimek and Thomas A. Murrell, entitled Selecting Apparatus and Method for Phonograph, Ser. No. 71,501, filed on Sept. 11, 1970.

Remote selecting stations now being put into use are adapted to transmit appropriate logic words, such as the three word, four bit system utilized in the above identified co-pending application. However, an establishment with a large number of remote selecting apparatuses may not be willing to replace them all at one time. Thus, it is necessary to provide some means for translating trains of pulses produced under the old letter-number approach into logic words at the coin-operated phonograph.

SUMMARY OF THE INVENTION

The present invention permits the utilization of older remote selecting stations based upon a letter-number selection identification with the more recent integrated circuit logic systems based upon a three digit numeral for selection identifying. Although the description herein is based upon the translation of a series, or train, of pulses arranged in two sets into three logic or binary words each of which contains four bits of data, it should be realized that the invention is not limited to such an arrangement as it could equally well encompass variations such as transmitted trains of pulses having more than two sets or logic systems responsive to different types of logic or binary words. Also, the selecting arrangement need not be based upon either a letter-number identification or a multi-digit numeral, but could utilize any type of character designations.

With respect to the particular embodiments disclosed herein, the remote selector produces a set of pulses for each number and letter selected. The particular number of pulses in any set will depend upon the number or letter selected, as each letter and number has a corresponding number of pulses associated therewith. In the particular arrangement discussed herein, the number pulses are transmitted in the first set, which as an envelope or "window" encompassing the set of pulses. After a short time delay, the letter pulses are transmitted in a set that has a characteristic letter envelope or "window" encompassing the entire set of pulses.

Upon arrival of the train of pulses at the coin-operated phonograph, the pulses are directed to a translating arrangement for conversion into logic words that may be utilized in the logic system of the phonograph. The number pulses, which arrive first, are passed through a first gate to a first counting and storing arrangement. The first counting and storing arrangement includes a binary counter utilizing conventional flip-flop stages. A distributing arrangement, which in this case includes a first decoder to form the binary outputs of the counting and storing arrangement into numerical signals, is adapted to convey the outputs of the counting and storing arrangement to appropriate data lines.

In response to termination of the number "window", a transfer device closes the first gate and opens a second gate, which was previously closed to transmittal of the number pulses. Thus, the letter pulses are not transmitted through the first gate but are passed through the second gate to a second counting and storing arrangement. The second counting and storing arrangement includes a first flip-flop and a second binary counter having flip-flop stages. In essence, the first flip-flop is another stage of the second binary counter, but due to an inversion of the output signal applied to the first stage of the second binary counter, the result is not merely that of an additional stage. A second distribution system connects the outputs of the first flip-flop and the second binary counter to appropriate data lines. The second distributing system incorporates a second decoder for the outputs of the second binary counter.

A timing control circuit is utilized to cause the first and second counting and storing arrangements to have their outputs distributed to the appropriate data lines in the proper time sequence. The timing control circuit utilizes a third binary counter which is responsive to the "window" signals and to an automatic clock input. The automatic clock is actuated upon termination of the letter "window," so that all of the letter pulses have been properly counted and stored in the second counting and storing arrangement prior to activation of the timing control circuit. The outputs of the third binary counter are conveyed to a third decoder, which produces outputs to cause the first flip-flop outputs to appear on the data lines first, the first binary counter outputs to appear on the data lines after the first flip-flop outputs, and the outputs of the second binary counter to appear on the data lines after the outputs of the first binary counter.

After transmission of all of the data on the data lines, all of the flip-flops and counters are cleared or reset to

the quiescent state in preparation for the next coming train of pulses.

Accordingly, it is a primary object of this invention to provide an arrangement for translating a series of pulses into logic words comprising bits of data transmitted in parallel.

Another object of this invention is to provide an arrangement to permit the use of existing letter-number remote selecting units with more recent coin-operated phonographs having selections identified by multi-digit numerals.

A further object of this invention is to provide an arrangement that can translate two sets of serially transmitted pulses into three word, four bit logic signals.

These and other objects, advantages, and features of this invention will hereinafter appear, and for purposes of illustration, but not of limitation, exemplary embodiments of the subject invention are shown in the appended drawing.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1A is a block diagram schematically illustrating one embodiment of the subject invention.

FIG. 1B schematically illustrates the wave forms of signals appearing at selected points in the circuit of FIG. 1B.

FIGS. 2A – 2D are a circuit diagram schematically illustrating a preferred embodiment of the subject invention.

FIG. 2E illustrates the relative placement of FIGS. 2A – 2D.

FIG. 3 illustrates various components appearing in the circuit diagram of FIGS. 2A – 2D.

FIG. 4 illustrates a decoder arrangement appearing in the circuit diagram of FIGS. 2A – 2D.

FIGS. 5A – 5D are a circuit diagram schematically illustrating circuit features utilized in connection with the preferred embodiment of FIGS. 2A – 2D.

FIG. 5E illustrates the relative placement of FIGS. 5A – 5D.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

With reference to FIG. 1A, a system is illustrated in block diagram form by which selections made at a conventional remote station may be translated to control a logic system responsive to three-word, four-bit logic signals.

In FIG. 1A, a conventional series of pulses is applied to an amplifier **11**. The output of the amplifier **11** is connected to an emitter follower circuit **13**. The output of the emitter follower **13** is utilized to actuate three Schmitt Trigger circuits, identified as Schmitt Trigger **01**, Schmitt Trigger **02**, and Schmitt Trigger **03**.

The wave forms produced at the output of the Schmitt Triggers are illustrated in FIG. 1B, the wave for Schmitt Trigger **03** appearing at the top, followed by that of Schmitt Trigger **01**, with the wave form at the output of Schmitt Trigger **02** illustrated at the bottom of that FIGURE. From these wave diagrams, it may be seen that all three of these Schmitt Triggers are actuated upon the application of a pulse train and that each of them is formed to have an inherent delay such that it does not respond to the individual number and letter pulses. However, the delay of Schnitt Trigger **01** is such that it does respond to the lag between transmission of number pulses and letter pulses, so that the signal at the output thereof is the pulse envelope, including the number "window" and the letter "window." Neither of the other Schmitt Triggers respond to the transition between windows. Schmitt Trigger **02** is provided with an inherent delay such that it returns to a quiescent state prior to the time that Schmitt Trigger **03** returns to a quiescent state.

The output of Schmitt Trigger **01** is applied to a binary circuit **15**, such as a conventional flip-flop. One output of binary **15** is connected to a number gate **17**, while a second output thereof is connected to a letter gate **19**. In the quiescent state, number gate **17** is normally open, while letter gate **19** is normally closed. Each of these gates also receives inputs directly from amplifier **11**.

Since number gate **17** is normally open, application of a series of number and letter pulses to amplifier **11** results in the pulses in the number "window" being conveyed to number counters **21**. These number counters **21** may be a conventional binary counter, the output of the various stages of which are connected to a decoder circuit **23**. Due to a predetermined correspondence between the letter-number designations at the conventional serially transmitting remote stations and the three digit identifying numerals in the logic circuits, the numbers counted in counters **21** will be the second or tens digit of the three digit numerals. Decoder **23** may be any appropriate type, one form being that utilized in connection with the decoder of the receiver in the system described in the above-identified co-pending application.

Upon termination of the number "window," binary **15** is activated to close number gate **17** and open letter gate **19**. Thus, the pulses in the letter "window" will be passed to letter counters **25**. The outputs of the various stages of the letter counters are connected to a third or units digit decoder circuit **27** and a first or hundreds digit decoder circuit **29**. Letter counters **25** essentially correspond to letter counters **21**, and decoders **27** and **29** correspond to decoder **23**.

Upon resetting of Schmitt Trigger **02** after termination of the letter "window," an interrogate signal is passed through an amplifier **31** to decoders **23**, **27** and **29** in order to produce appropriate four bit words to be introduced into the receiver illustrated in the above-identified copending application. The signal passing through amplifier **31** is also conveyed through an amplifier **33** to trigger the write-in cycle of the receiver.

The turn-off of Schmitt Trigger **03** shortly later resets binary **15** and amplifier **31** to their quiescent states. In addition, the reset signal is passed through an amplifier **35** to reset counters **21** and **25**. Further, the output of amplifier **35** is conveyed to an amplifier **37** to initiate the reset cycle of the receiver.

While one embodiment of a translator has been discussed in connection with the block diagram of FIG. 1A, a preferred embodiment of this invention is illustrated in FIGS. 2A–2D. However, before proceeding with a detailed description of this preferred embodiment, reference should be made to FIGS. **3** and **4**. In these FIGS., there are illustrated the basic circuit elements and arrangements utilized, together with the nomenclature utilized in connection therewith.

In FIG. 3 there i illustrated a NAND gate 39 and a NOR gate 41. A NAND gate will produce a "0" output only when all of the inputs thereto are at a "1" state. On the other hand, a NOR gate will produce a "0" output when any input is a "1." FIG. 3 also illustrates a J-K flip-flop or binary 43. In this type of flip-flop, the input signal is applied to the CK terminal and the outputs are derived from Q and Q terminals. A "1" appearing on the CK terminal is transferred to the Q terminal (and the inverse thereof to the Q terminal) upon transition from a "1" to a "0." A reset or clear signal is applied to the CL terminal to return the flip-flop to its quiescent state. A counter circuit 45 utilizing flip-flops 43 is also illustrated in FIG. 3. It will be noted that the output terminal notation has been altered to A, A: B, B, etc. to denote the stage from which the output is obtained.

A decoder for transforming a binary signal into a numerical signal is illustrated in FIG. 4. Any type of appropriate decoder may be utilized, such as the logic arrangement utilized in connection with the receiver in the above-identified copending application. For purposes of this description, the decoder will have the input and output values illustrated in FIG. 4. The A–D inputs are taken from the stages of a binary counter 45. Thus, a signal appearing at A is representative of a one pulse count, a B input represents a two pulse count, a C input represents a four pulse count, and a D input represents an eight pulse count. The numerical signals are taken from the appropriate terminals, according to the notation thereon. Thus, if an input were obtained at both A and C, these inputs would add to produce a signal on the output terminal marked 5.

With these definitions, it is now possible to describe the preferred embodiment. However, before getting into circuit details, it is necessary to cover the specific correspondence between the letter-number selecting system and the three digit selecting system. First of all, as previously mentioned, the serially transmitted letter-digit designation utilizes a number "window" containing pulses representative of a selected number, this number series of pulses being transmitted first. The number "window" is followed after a predetermined time delay by a letter "window" which contains pulses representative of the letter selected. The number of pulses transmitted in the number "window" for a particular number chosen are those indicated in the following chart:

Number selected	Number of pulses transmitted
1	9
2	8
3	7
4	6
5	5
6	4
7	3
8	2

In a similar fashion, the number of pulses for each letter selected are as follows:

Letter selected	Number of pulses transmitted
A	20
B	19
C	18
D	17
E	16
F	15
G	14
H	13
J	12
K	11
L	10
M	9
N	8
P	7
Q	6
R	5
S	4
T	3
U	2
V	1

Another correlation that is necessary to understand the operation of this preferred embodiment is the correspondence between the letter-number designations and the three digit designations. The following chart illustrates this correspondence, where the number at the far left and the letters at the top are the numbers and letters in the letter-number designation:

	A B	C D	E F	G H	J K	L M	N P	Q R	S T	U V
	100	101	102	103	104	105	106	107	108	109
1										
	200	201	202	203	204	205	206	207	208	209
	110	111	112	113	114	115	116	117	118	119
2										
	210	211	212	213	214	215	216	217	218	219
	120	121	122	123	124	125	126	127	128	129
3										
	220	221	222	223	224	225	226	227	228	229
	130	131	132	133	134	135	136	137	138	139
4										
	230	231	232	233	234	235	236	237	238	239
	140	141	142	143	144	145	146	147	148	149
5										
	240	241	242	243	244	245	246	247	248	249
	150	151	152	153	154	155	156	157	158	159
6										
	250	251	252	253	254	255	256	257	258	259
	160	161	162	163	164	165	166	167	168	169
7										
	260	261	262	263	264	265	266	267	268	269
	170	171	172	173	174	175	176	177	178	179
8										
	270	271	272	273	274	275	276	277	278	279

Still another factor that must be realized in order to comprehend the operation of this preferred embodiment is the manner in which the bits of information characterize the individual selection identifying numerals in the three digit approach. The bits of information appear on data lines A–D. The following chart illustrates the data lines on which signals are produced to represent a particular digit in the three digit selection identifying approach:

DATA LINES

Digits	A	B	C	D
0				1
1			1	
2				1
3	1			
4	1			1
5	1	1		
6	1		1	
7			1	1
8		1	1	
9		1		1

With this background information, it is now possible to explain in detail the preferred embodiment illustrated in FIGS. 2A–2D. With reference first to FIG. 2A, a NOR gate G1 is illustrated. NOR gate G1 serves to control the passage of pulses representing letters and numbers in the letter-number selection arrangement. Specifically, NOR gate G1 permits the passage of pulses representative of a number, but prevents the passage of pulses representative of a letter. As in the case of the embodiment discussed in connection with FIG. 1A, and as may be seen from the chart relating the letter-number and three digit identifications, the number in the letter-number system corresponds to the second or tens digit in the three-digit identification.

NOR gate G1 has a "0" at one input terminal in the quiescent state, as illustrated. A pulse "window" signal appearing on terminal **47** (FIG. 2C) brings about a change in this condition, but until this change occurs input pulses appearing on terminal **49** are conveyed through a NOR gate **50** to another input of NOR gate G1 and pass through NOR gate G1. Since NOR gate G1 will produce a "0" output only when there is a "1" at one of its inputs, the output of NOR gate will vary as a result of the signals transmitted through NOR gate **50** during this initial period. NOR gate **50** serves essentially as an inverter for the pulses applied to terminal **49**.

Upon application of a pulse "window" signal to terminal **47**, NAND gate **52** produces a "0" output, since both inputs are then in a "1" state. The output of NAND gate **52** is conveyed to a NAND gate **54**, which essentially serves to invert the signal coming from NAND gate **52** before applying it to the CK terminal of flip-flop **51**. Capacitors **53** and **55** are utilized to shape the pulse applied to flip-flop **51** and to provide some buffering of undesired signals.

The "1" applied to the CK terminal of flip-flop **51** as a result of the appearance of the pulse "window" signal is not transferred through flip-flop **51** until the trailing edge thereof is reached, i.e., the end of the number pulse transmission. Upon the production of a "1" at the Q terminal of flip-flop **51**, NOR gate G1 has the output thereof held at a "0." Thus, any pulses appearing at the other input of NOR gate G1 do not affect the output thereof, and hence are not transmitted.

The output pulses from NOR gate G1 are conveyed on a line **57** and formed across a capacitor **59** at the CK terminal of a flip-flop **61** (FIG. 2B). The pulses appearing on line **57** are counted in the counter formed of flip-flop **61** and its related flip-flop **63**, **65** and **67**. The outputs of flip-flops **61**, **63**, **65** and **67** are connected to respective NAND gates **69**, **71**, **73** and **75**. A NAND gate **77** normally maintains a "0" at one input to each of the NAND gates **69**, **71**, **73** and **75**, thus holding the outputs of these gates at "1". When NAND gate **77** produces a "1" output, a "1" appearing at the output of a flip-flop **61**, **63**, **65** or **67** is conveyed through the associated NAND gate **69**, **71**, **73** or **75** to another corresponding NAND gate **79**, **81**, **83** or **85** to provide appropriate inputs to a decoder **87**. The outputs of the decoder **87** are connected to appropriate ones of the Data A, Data B, Data C, and Data D lines.

Referring back to FIG. 2A, a NOR gate G2 has its output normally maintained at "0" due to the presence of a "1", as indicated, at one input thereof. However, when flip-flop **51** produces a "1" at its Q terminal, a NOR gate **89** inverts the "1" and produces a "0" at the input of NOR gate G2. Thus, at the same time that NOR gate G1 is rendered incapable of transmitting the pulses from terminal **49** applied to one input thereof, NOR gate G2 is rendered capable of passing the same pulses which are applied to an input thereof. In other words, NOR gate G1 passes the number pulses while blocking the letter pulses, and NOR gate G2 does the precise inverse by blocking the number pulses and passing the letter pulses.

The letter pulses appearing on terminal **49** are conveyed through NOR gate **50** and NOR gate G2 to an inverting NAND gate **91**, from where they are conveyed to the CK terminal of a flip-flop **93** (FIG. 2C) via a line **95**.

Both the Q and Q outputs of flip-flop **93** are utilized. The Q output is conveyed via a line **97** to an input of a NAND gate **99** (FIG. 2D). Similarly, the Q output is conveyed via a line **101** to an input of a NAND gate **103**. NAND gate **99** provides a Data B pulse, while NAND gate **103** provides a Data C pulse.

The Q output of flip-flop **93** is also conveyed to the CK terminal of a flip-flop **105**. Flip-flop **105** is the first counter stage of a counter that also includes flip-flops **107**, **109**, and **111**. Counter stages **105**, **107**, **109**, and **111** correspond to the counter stages **61**, **63**, **65**, and **67** illustrated in FIG. 2B. However, due to the use of the Q output of flip-flop **93**, the outputs of the individual flip-flop counter stages represent different count values than the outputs of the flip-flop counter stages **61**, **63**, **65**, and **67**, although as far as the associated decoder **113** is concerned the results are the same. In other words, even though the A, B, C, and D inputs to decoder **113** represent different count values than the same inputs to decoder **87**, the numerical outputs are the same.

The A, B, C, and D outputs of flip-flop counter stages **105**, **107**, **109**, and **111** are conveyed, respectively, to NAND gates **115**, **117**, **119**, and **121**. The output signals applied to NAND gates **115**, **117**, **119**, and **121** are normally blocked due to a "0" applied to one input thereof by a NAND gate **123**. The threshold voltage of NAND gate **123** is increased by a diode **125**. When NAND gate **123** produces a "1" at its output, the outputs from flip-flop counter stages **105**, **107**, **109**, and **111** are conveyed through NAND gates **115**, **117**, **119**, and **121** to NAND gates **127**, **129**, **131**, and **133**. These latter NAND gates convey the signals to appropriate inputs on the decoder **113**, which in turn transmits appropriate signals to the Data A, Data B, Data C, and Data D lines.

As previously mentioned, the fact that the input to flip-flop counter stage **105** is obtained from the Q output of flip-flop **93** means that the A, B, C and D signals represent count values different from those represented by the signals appearing at the outputs of flip-flop counter stages **61**, **63**, **65** and **67**. Thus, an A output is produced by flip-flop counter stage **105** upon the first, fifth, ninth, 13th and 17th pulses passing through NOR gate G2. Similarly, the B outputs are produced upon the third, 11th and 19th pulses passing through NOR gate G2. A C output from flip-flop counter stage **109** is produced upon the seventh pulse passing through NOR gate G2, while a D output from

flip-flop counter stage 111 is produced upon the is pulse. With this arrangement, the counter comprising flip-flop stages 105, 107, 109 and 111 will produce the same numerical output for two input pulses. As an example, after the production of both three and four pulses, which pass through gate G2, these counter stages will produce a B output on flip-flop 107. Since the B output corresponds to a numerical 2, Data B and Data C lines will have a signal impressed thereon as the third logic word, corresponding to the third or units digit of the numerical identification of the chosen selection. However, separate identification of the three and four pulse signals would be achieved by different outputs from NAND gates 99 and 103, corresponding to the first or hundreds digit of the selection identifying numeral.

To permit the use of single ten digit decoder arrangement, NAND gates 135, 137 and 139 are incorporated into the circuit. It will be noted that NAND gate 137 has a "1" at one of its inputs in the quiescent state. Immediately upon power turn on, a "1" is produced at the other input of NAND gate 137, so that a "0" appears at the output of NAND gate 137. This "0" is inverted by the NAND gate 139 and applied to the clear or CL terminals of flip-flop counter stages 105, 107, 109 and 111. Since a "0" is utilized to clear the flip-flops, the "1" appearing thereat releases the flip-flops for operation. When 19 pulses have been introduced into the counter stages 105, 107, 109 and 111, B and D outputs are obtained from flip-flop counter stages 107 and 111. With these two inputs applied thereto, the output of NAND gate 135 goes to a "0," and a "0" is applied to the CL terminals of flip-flops 105, 107, 109 and 111 to clear the counter.

However, as it is necessary to count up to twenty pulses, some arrangement must be made for providing data pulses upon production of 19 and 20 counts. To achieve this, NOR gates 141 and 143 are utilized. The threshold voltage of NOR gate 143 is increased by diode 145. One input for NOR gate 141 is obtained from the 0 terminal of decoder 113. Thus, for 19 and 20 pulses introduced into the flip-flop counter stages 105, 107, 109 and 111, the output of NOR gate 141 will be responsive to signals appearing at the other input thereof. Since the other input is obtained from the same source as the input to NAND gate 123, it is normally at "1." However, upon a "0" appearing upon that line, the output of NOR gate 141 will go to a "1" and the output of NOR gate 143 will go to a "0." This results in a signal appearing on the Data D line as the third logic word, or the third or units digit of the selection identifying numeral. Again, this output will be the same for both 19 and 20 counts, but the first or hundreds digit will vary depending upon whether NAND gate 99 or NAND gate 103 produces an output.

Referring back now to FIG. 2C, it may be seen that a NOR gate 147 obtains inputs from a cycle reset terminal 149 and a turn-on reset terminal 151. The turn-on reset terminal 151 is perpetually held at "0", while the cycle reset terminal 149 is at a "1" when no signal is applied to the translator. However, upon application of a signal to the translator the cycle reset terminal 149 will go to a "0" and a "1" will be produced at the output of NOR gate 147. An inverting NOR gate 153 will produce a "0" at the output thereof in response to the "1" applied thereto from NOR gate 147. The "0" at the output of a NOR gate 153 is produced across a parallel arrangement of capacitors 155 and 157.

The signal at the output of NOR gate 153 is applied to the CL terminals of the flip-flops in the circuit to clear or reset the flip-flops. Since a "0" is utilized to clear the flip-flops, the "0" appearing at the output of NOR gate 153 must be converted to a "1" for application to the various flip-flops to release these flip-flops for operation upon application of a selection signal to the translator.

The output signal from NOR gate 153 is conveyed to NAND gate 159, which serves to invert the "0" appearing at the output of NOR gate 153. This "1" is applied to the CL terminals of flip-flop 51 and the flip-flop counter stages 161, 163 and 165 in FIG. 2C. The output of NOR gate 153 is also conveyed to another inverting NAND gate 167, which provides a "1" for the CL terminal of flip-flop 93, and for NAND gate 137 in FIG. 2D. The output of NOR gate 153 is applied to still another inverting NAND gate 169 which applies the "1" to flip-flop counter stages 61, 63, 65 and 67 in FIG. 2B.

When the application of the number "window" causes NAND gate 54 to produce a "1", the "1" is applied to a NAND gate 171 in FIG. 2C. Since the other input of NAND gate 171 is provided with a constant "1", the "1" from the output of NAND gate 54 causes NAND gate 171 to produce a "0" across a capacitor 173. This "0" is applied to a NAND gate 175 which normally has a "1" applied to the other input thereof from an automatic clock terminal 177.

The "0" arriving at the input of NAND gate 175 causes the output thereof to go to a "1." At the trailing edge of the number "window" signal the output of NAND gate 175 returns to a "0," which causes an A signal to be produced at the output of flip-flop 161. Upon application of the letter "window", the output of NAND gate 175 returns to a "1," and after removal of the letter "window" the output of NAND gate 175 returns to a "0" which removes the A output and causes a B output to be produced by flip-flop 163. The B output of flip-flop 163 is conveyed through NAND gate 179 to a terminal 181. The signal appearing on terminal 181 is connected to an automatic clock circuit to begin operation of that circuit to apply pulses to terminal 177. It may be noted that the A, B, and C output terminals of flip-flops 161, 163 and 165 are each biased by a resistor-capacitor arrangement incorporating a resistor 183 and a capacitor 185.

Upon actuation of the automatic clock another A output is produced by flip-flop 161. Since there is also a B output from flip-flop 163, the application of these outputs to the appropriate terminals of a decoder 187 produces an output at the 3 terminal thereof. This output is conveyed through a NAND gate 189 to NAND gates 99 and 103. Thus, three pulses applied to counter stages 161, 163 and 165 will cause the appropriate one of NAND gates 99 and 103 to pass the "1" applied thereto from flip-flop 93 to the appropriate data line.

The next pulse applied by the automatic clock will produce a C output from flip-flop 165, which is passed through a NAND gate 191 to a terminal 193. The signal appearing on terminal 193 actuates the automatic clock to keep it operating. Upon the application of

another pulse from the automatic clock to NAND gate 175, an A output will appear at the output of flip-flop 161 and a C output will be obtained from flip-flop 165. When these outputs are conveyed to the appropriate inputs of decoder 187, an output signal is derived from the 5 terminal thereof. This signal is applied to NAND gate 77 to cause the signals counted and stored in flip-flop stages 61, 63, 65 and 67 to be transferred to decoder 87.

Application of two more signals from the automatic clock to NAND gate 175 will produce an output across resistor 195 at the 7 terminal of decoder 187. This signal is conveyed to NAND gate 123 to cause the signals stored in flip-flop counter stages 105, 107, 109 and 111 to be transferred to decoder 113.

To briefly describe the operation of this arrangement, NOR gate G1 passes the number pulses applied thereto to flip-flop counter stages 61, 63, 65 and 67. These pulses are counted and stored and NOR gate G1 is turned off to prevent the passage of any more pulses therethrough. At this time NOR gate G2 is opened up to permit the passage of letter pulses therethrough. These pulses are conveyed to flip-flop 93, which produces signals representative of the first or hundreds digit of the selection identifying numeral. The letter pulses are also conveyed to flip-flop counter stages 105, 107, 109 and 111, where the pulses are counted and stored. At the end of the letter "window" an automatic clock applies pulses to counter stages 161, 163 and 165, which actuates a decoder 187 to produce 3, 5 and 7 count outputs. The 3 count output causes the first or hundreds digit signal to be conveyed from flip-flop 93 to an appropriate data line. The 5 count output causes the information stored in flip-flop counter stages 61, 63, 65 and 67 to be transferred to decoder 87 and then conveyed to appropriate data lines. Similarly, and finally, the 7 count output causes the information stored in flip-flop counter stages 105, 107, 109 and 111 to be transferred to decoder 113 and then conveyed to the appropriate data lines. It should be noted that the data line inputs are all passed through appropriate diodes 200–218.

To further explain the operation, a specific example will be utilized. For this example, assume that the selection identified as R–4 has been chosen at the remote selecting station. From the charts listed above, it may be seen that six pulses will be transmitted for the number 4 and five pulses will be transmitted for the letter R. From the charts, it may also be seen that the selection R–4 corresponds to the selection 237. From the final chart, it may be seen that to produce the selection identifying numeral 237, the first word or digit will have to be a pulse on the Data B line, the second digit will have to have a pulse on the Data A line, and the third digit will have to have pulses on the Data C line and the Data D line.

Application of the serial train of pulses results in the six number pulses being stored in flip-flop stages 61, 63, 65 and 67, after passing through NOR gate G1. These six pulses produce a C output from flip-flop stage 65 and a B output from stage 63.

Similarly, the five pulses representative of the letter R are transmitted through NOR gate G2 to flip-flop 93 and flip-flop counter stages 105, 107, 109 and 111. These five pulses will produce a "1" on the Q terminal of flip-flop 93. These five pulses will also produce an A output from flip-flop 105 and a B output from flip-flop 107.

Upon termination of the letter pulses, the automatic clock will drive flip-flop stages 161, 163 and 165 to produce output pulses from decoder 187. Upon a three count output being produced, the "1" at the Q terminal of flip-flop 93 is conveyed through NAND gate 99, where it is inverted and connected to the Data B line through diode 206. Upon a five count output being produced by decoder 187, the B and C outputs of flip-flop stages 63 and 65 are conveyed to decoder 87, which produces an output at terminal 6, which is then conveyed to the Data A line through diode 202.

Upon the production of a seven count output by decoder 187, the A and B outputs of flip-flop stages 105 and 107 are conveyed to a decoder 113, which produces an output at terminal 3, which is then conveyed to the Data C line through diode 213 and to the Data D line through diode 214. Thus, it may be seen that the R–4 selection has been translated into three logic words, each having four data bits, corresponding to the three digit numerical designation of the selection.

The circuit illustrated in FIGS. 5A – 5D relates to various features of the system utilized in connection with the logic circuitry of FIGS. 2A – 2D. Inasmuch as these various features utilize relatively conventional circuitry, the individual circuits will be not be discussed in detail. However, this circuitry is being included to provide a complete disclosure in order to permit full comprehension of the operation of the invention.

With reference first to FIG. 5A, a buffer and timing circuit 225 is illustrated. Serially transmitted pulses from the remote selector are applied to terminal 227. The individual pulses are shaped and buffered and then applied to terminal 229, which corresponds to terminal 49 in FIG. 2C. The pulses are then conveyed to the next portion of circuit 225 where, as a result of the RC time constant of resistor 231 and capacitor 233, signals representing the envelope of the pulses (the envelopes of the individual sets of pulses being termed "windows") are produced. These "window" signals appear at terminal 235, which corresponds to terminal 47 in FIG. 2C.

Power supply circuits 237 are illustrated in FIGS. 5A and 5B. There are fairly conventional power circuits and need no further discussion at this point. It may be noted that 10 volt AC signals are applied to terminals 239, 241, and 243. A 31 volt AC signal is applied to terminal 245. The power supply circuits 237 produce a +8 volt regulated DC voltage on terminal 247. On terminal 249, a −27 volt regulated DC signal is provided. Finally, on terminal 251 a +*Vcc* supply signal, which is also connected to the chassis ground, is produced.

An automatic clock circuit 253 is illustrated in FIG. 5C. This clock circuit responds to input signals on terminals 255 and 257, which correspond to terminals 193 and 181 in FIG. 2C. The automatic clock signal outputs are obtained on terminal 259 and connected to terminal 177 in FIG. 2C.

At the top of FIG. 5C there is illustrated a cycle reset circuit 261. The cycle reset circuit 261 is responsive to a 0 count output from decoder 187 in FIG. 2C. This 0 count output from decoder 187 is passed through

NAND gate 263 to terminal 265, which causes a cycle reset signal to be produced on terminal 267. Terminal 267 corresponds to terminal 149 in FIG. 2C, and the output produced as a result of the 0 count at decoder 187 returns the input to NOR gate 147 to the quiescent state values illustrated. This in turn causes all the counters in the circuit of FIGS. 2A – 2D to be cleared, or reset.

Referring now to FIG. 5D, a totalizer circuit 269 is illustrated. This circuit obtains coin switch information on terminals 271, 273, and 275 and shapes and buffers the pulses for use in a logic circuit. The coin switch information is transmitted over the same transmission lines utilized to transmit selection information, so terminals 277, 279, and 281 are connected, respectively, to the Data B, Data C, and Data D transmission lines.

In FIGS. 5B and 5D there are illustrated buffer circuits 283, 285, 287, and 289. These circuits buffer and shape the data outputs from FIGS. 2B and 2D, and transform the pulses to −27 volt logic pulses, before the pulses are transmitted on the data transmission lines. Thus, the Data A output from FIG. 2B is applied to terminal 291 and the resulting Data A pulses on terminal 293 are conveyed to the Data A transmission line. Similarly, terminal 295 receives input from the Data B output of FIG. 2B and terminal 297 is connected to the Data B transmission line. Continuing in FIG. 5D, terminals 299 and 303 are connected to the Data C and Data D outputs, respectively, in FIG. 2D, and terminals 301 and 305 are connected to the Data C and Data D transmission lines, respectively.

It should be understood that various modifications, changes, and variations may be made in the arrangements, operations, and details of construction of the elements disclosed herein without departing from the spirit and scope of the present invention.

We claim:

1. An arrangement for translating two spaced sets of pulses transmitted in a train, which represent a letter-number identification of a record selection to be played in a coin-operated phonograph, into three logic words of four data bits each, which represent a three digit numerical identification of the record selection, comprising:

first gate means having the train of pulses applied thereto;

second gate means having the train of pulses applied thereto;

transfer means adapted to open said first gate means for only one of the sets of pulses in the train and to open said second gate means for only the other set of pulses in the train;

a first binary counter adapted to accumulate the pulses passing through said first gate means and preserve the total thereof;

a first flip-flop and a second binary counter adapted to accumulate the pulses passing through said second gate means and preserve the total thereof;

timing control means actuated after termination of the train of pulses to cause the signals stored in said first flip-flop to be conveyed to the data lines first in a time sequence, the pulse totals in said first binary counter to be conveyed to the data lines second, and the post totals in said second binary counter to be conveyed to the data lines last;

first distributing means to convey the pulse totals in said first binary counter to appropriate data output lines; and

second distributing means to convey the pulse totals in said second binary counter to appropriate data output lines.

2. An arrangement as claimed in claim 1 wherein said first and second distributing means comprise first and second decoder circuits, respectively.

3. An arrangement as claimed in claim 2 wherein said timing control means comprises a third binary counter and a third decoder circuit.

4. An arrangement as claimed in claim 3 and further comprising a clock circuit activated upon termination of the train of pulses to actuate said third binary counter.

5. An arrangement as claimed in claim 1 and further comprising reset means to clear all flip-flops and counters after the signal stored in said first flip-flop and the pulse totals preserved in said first and second binary counters have been distributed to the appropriate data lines.

6. An arrangement as claimed in claim 1 wherein said transfer means comprises a second flip-flop.

7. An arrangement for translating a train of pulses, which is divided into a first set of pulses and a second set of pulses, into three four-bit logic words comprising:

a first logic gate to which the train of pulses is applied, said first logic gate normally open to permit passage of the first set of pulses therethrough;

a second logic gate to which the train of pulses is applied, said second logic gate normally closed to prevent passage of the first set of pulses therethrough;

a transfer flip-flop actuated after the first set of pulses has passed through said first logic gate to close said first logic gate to prevent passage of the second set of pulses therethrough and open said second logic gate to permit passage of the second set of pulses therethrough;

a first binary counter adapted to count and store pulses passed through said first logic gate;

a first flip-flop and a second binary counter adapted to count and store pulses passed through said second logic gate;

a third binary counter actuated by the envelopes of the first and second sets of pulses;

a clock circuit, said clock circuit being activated upon actuation of said third binary counter by the envelope of the second set of pulses to automatically actuate said third binary counter with a series of pulses;

a third decoder adapted to convert the outputs of said third binary counter to signals representing numerical values, upon said third decoder reaching a first predetermined numerical count the outputs of said first-flip being conveyed to appropriate data lines;

a first decoder adapted to convert the outputs of said first binary circuit to signals representing numerical values and to direct the resulting signals to appropriate data lines, the outputs of said first binary counter being applied to said first decoder upon said third decoder reaching a second predetermined numerical count;

a second decoder adapted to convert the outputs of said second binary circuit to signals representing numerical values and to direct the resulting signals to appropriate data lines, the outputs of said second binary counter being applied to said second decoder upon said third decoder reaching a third predetermined numerical count; and

a reset circuit actuated upon said third decoder reaching a fourth predetermined numerical count to clear all of said flip-flops and binary counters.

8. An arrangement as claimed in claim 7 wherein said transfer flip-flop is actuated by the envelopes of the sets of pulses.

9. An arrangement as claimed in claim 7 wherein said first predetermined count of said third decoder is three, said second predetermined count is five, said third predetermined count is seven and said fourth predetermined count is zero.

10. An arrangement as claimed in claim 7 wherein said first and second logic gates are NOR gates.

11. An arrangement as claimed in claim 7 and further comprising a logic circuit adapted to convey signals to appropriate data lines when said second decoder reaches a numerical count of zero.

* * * * *