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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H03K 17/16

A1

(11) International Publication Number: **WO 95/29532**

(43) International Publication Date: 2 November 1995 (02.11.95)

(21) International Application Number: PCT/US95/04844

(22) International Filing Date: 20 April 1995 (20.04.95)

(30) Priority Data:
08/231,394 22 April 1994 (22.04.94) US

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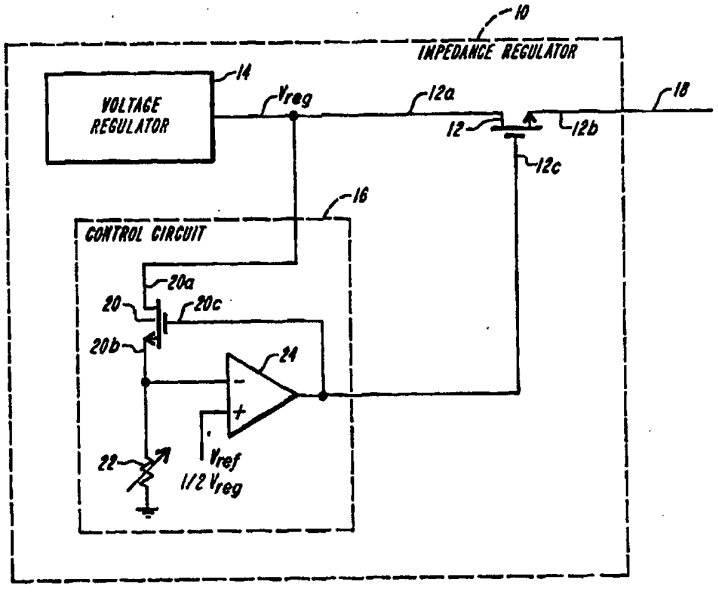
(81) Designated States: CA, JP, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: IMPEDANCE EMULATOR



(57) Abstract

A low capacitance impedance emulator suitable for active conductor termination. This impedance emulator includes an emulating FET (12) and a control circuit (16) coupled to the gate of the emulating FET for maintaining the FET in a linear region of operation. The control circuit includes a control FET (20), an impedance setting resistor (22), and an amplifier (24). The control FET is driven in a closed-loop fashion so that the impedance of the control FET has a known relationship with respect to that of the resistor. The output of the amplifier controls the conduction of both the emulating and control FETs so that the emulating FET provides an impedance proportional to that of the control FET and thus, related to the impedance of the resistor.

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IMPEDANCE EMULATOR

FIELD OF THE INVENTION

This invention relates generally to impedance emulation and more particularly, to a low capacitance impedance emulator well suited for active conductor termination.

BACKGROUND OF THE INVENTION

It is well known to terminate a conductor with an impedance which is ideally matched to the dynamic impedance of the conductor in order to reduce signal reflections and concomitant degradation of data transmitted on the conductor. One such terminator comprises a resistor having a resistance value nominally matched to that of the conductor. While the nominal resistance value may match a typical conductor impedance, tolerances can affect the conductor and resistor impedances, thereby degrading the resulting impedance "match". Moreover, the resistance value of such a terminator is fixed so that its use to terminate conductors having different dynamic impedances is precluded.

Another type of terminator utilizes an active device and thus, may be referred to as an active terminator. An example of an active terminator is one utilizing a field effect transistor (FET) biased to saturation. In this operating condition, the FET has a highly non-linear, current source characteristic which generally does not reduce signal reflections as well as terminators having a linear, substantially resistive characteristic.

SUMMARY OF THE INVENTION

In accordance with the invention, a low capacitance impedance emulator is provided for emulating a selected impedance having a substantially linear characteristic. The emulator is well suited for use in terminating one or more conductors of a high-speed data bus where accurate, low capacitance termination is critical. the low capacitance of the emulator ensures that when the terminator is coupled to the bus in a disconnect mode, the emulator does not adversely affect the conductor impedance. The impedance emulator utilizes an emulating FET operated in the linear region. The linear operation of the emulating FET provides an impedance across the drain and source electrodes of the FET which is substantially resistive (i.e., characterized by a linear relationship between the current through the FET and the voltage across the FET). This resistive characteristic is particularly effective in signal termination to reduce unwanted signal reflections.

A control circuit is provided for maintaining the emulating FET in the linear region of operation and includes a control FET having like characteristics to the emulating FET and coupled in series with a resistor. The control FET is operated in a closed-loop fashion so that its conduction is controlled to maintain a predetermined voltage thereacross and more particularly, to provide an impedance having a predetermined relationship with respect to the resistance of the resistor. The emulating FET receives the same gate signal as the control FET, thereby causing the emulating FET to provide an impedance proportional to the impedance of the control FET. The resistor may be a trimmable or a variable resistor so that the impedance provided by the control and emulating FETs can be adjusted by trimming or adjusting the value of the resistor accordingly.

In one embodiment, the emulating FET provides the termination impedance of a signal transmission conductor. More particularly, the emulating FET is coupled in series

between a voltage regulator and the conductor and the resistance value of the resistor is selected or trimmed to correspond to the dynamic impedance of the conductor.

Use of the impedance emulator in signal bus termination is advantageous due to the linear, highly resistive characteristic of the FET in the linear region of operation. More particularly, this arrangement serves to reduce signal reflections on the conductor, thereby enhancing the effectiveness of the terminator. Moreover, simple adjustment of the termination impedance is achieved by trimming the resistor of the control circuit to ensure that the emulating FET provides an impedance corresponding to the dynamic impedance of the bus.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing features of this invention, as well as the invention itself, may be more fully understood from the following detailed description of the invention in which:

Fig. 1 is a schematic of an impedance emulator in accordance with the present invention;

Fig. 2 shows illustrative characteristic curves of an NMOS FET;

Fig. 3 is a schematic of an active bus terminator utilizing the impedance emulator of Fig. 1; and

Fig. 4 is a detailed schematic of the active bus terminator of Fig. 3.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Fig. 1, an impedance emulator 10 is shown to include an active emulating device 12 for providing a substantially linear predetermined impedance. The active device 12 is a metal oxide field effect transistor (MOSFET) having a drain electrode 12a, a source electrode 12b, and a gate electrode 12c but alternatively may be any suitable FET. The predetermined impedance is provided across the drain and source electrodes 12a, b of the FET 12 which, in the

embodiments described herein is an NMOS FET 12. The impedance emulator 10 further includes a voltage regulator 14 providing a regulated voltage V_{reg} and a control circuit 16 coupled to the gate electrode 12c for controlling the operation of the emulating FET 12. More particularly, the control circuit 16 maintains the FET 12 in its linear region of operation in order to provide the predetermined impedance with a linear, resistive characteristic.

Referring also to Fig. 2, illustrative characteristic curves of an NMOS FET, exemplary of the emulating FET 12, are shown to include a linear region of operation labelled 28. The linear region 28 is characterized by a linear relationship between the current I_{DS} between the drain and source electrodes of the FET and the voltage V_{DS} across such electrodes. Operation of the emulating FET 12 in the linear region causes the impedance across the drain and source electrodes 12a,b to approximate that of a resistor. A resistive impedance is particularly advantageous where the impedance emulator is utilized in terminating one or more conductors of a signal transmission bus, such as conductor 18 coupled to the source electrode 12b of the emulating FET 12, in order to reduce unwanted signal reflections. The characteristic curves reveal that the slope of the curves in the linear region (i.e., representative of the drain to source impedance) varies in proportion to the gate to source voltage V_{GS}. In order for a FET to be in the linear region, the gate to source voltage V_{GS} must be greater than the sum of the drain to source voltage V_{DS} and the threshold voltage V_T at which the FET begins to conduct (typically 0.7 volts).

The control circuit 16 includes a control FET 20 of the same type as the emulating FET 12 and having a drain electrode 20a, a source electrode 20b, and a gate electrode 20c, a resistor 22 and an operational amplifier 24. The control FET 20 has like characteristics to the emulating FET 12 so that the ratio of the impedance of the two FETs 12, 20

is equal to the ratio of the gate width to gate length of FET 12 to the gate width to gate length of FET 20. The emulating and control FETs 12, 20, respectively, may be identical in size or alternatively, may be scaled in size relative to one another. Preferably FETs 12, 20 are NMOS devices. While PMOS devices may be alternatively utilized, use of NMOS FETs provide certain advantages, including smaller size which equates to lower capacitance. An additional advantage of utilizing an NMOS emulating FET 12 is the electrostatic discharge protection provided by the inherent diode from the source electrode 12b to ground.

The control FET 20 is operated in a closed-loop fashion so that the impedance of the control FET 20 has a known relationship with respect to that of the series coupled resistor 22. Moreover, the emulating FET 12 is controlled by the same control signal as the control FET 20 so that the emulating FET 12 provides an impedance proportional to the impedance of the control FET 20. More particularly, the impedance of the emulating FET 12 is directly proportional to the impedance of the control FET 20 at a nominal operating point (i.e., corresponding to a gate voltage midway between the expected voltage swing at the source electrode 12b of the emulating FET 12). With sufficient gate voltage, the second order effect (i.e., nonlinearity) in the proportionality of the impedance of the emulating FET 12 to that of the control FET 20 is minimized. The impedance of the emulating FET 12 is thus also related to that of the resistor 12 and can be adjusted by varying the resistance of resistor 12.

The resistor 22 may be a trimmable integrated circuit resistor, such as a polysilicon resistor. With this arrangement, the resistor 22 is trimmed to ensure the desired impedance is provided by emulating FET 12. More generally, the resistor 22 is a variable resistor having an adjustable resistance value to facilitate adjustment of the predetermined impedance of the emulating FET 12. In some

applications, a fixed precision resistor may provide suitable control of the impedance of the emulating FET 12.

The operational amplifier 24 of the control circuit 16 has an output terminal coupled to the gate electrode 20c of the control FET 20 and the gate electrode 12c of the emulating FET 12. One input of the amplifier 24 is coupled to a reference voltage V_{ref} and another input of the amplifier 24 is coupled to the interconnection between the source electrode 20b of the control FET 20 and the series coupled resistor 22, as shown. The reference voltage V_{ref} has a predetermined relationship with respect to the regulated voltage V_{reg} across the series combination of the control FET 20 and the resistor 22. Here, the reference voltage is equal to $\frac{1}{2}V_{reg}$ since this voltage corresponds to the nominal operating point of midway between the permissible voltage swing on conductor 18 (i.e., such permissible voltage swing being from V_{reg} to ground). More generally however, the reference voltage may be other fractional values of the voltage V_{reg} across the series combination.

With this arrangement, the voltage at the source electrode 20b of the control FET 20 is forced to equal the reference voltage $V_{ref}=\frac{1}{2}V_{reg}$. Since the drain electrode 20a of the control FET 20 is coupled to the regulated voltage V_{reg}, the voltage across the drain and source electrodes 20a,b of the control FET 20 is equal to $\frac{1}{2}V_{reg}$ (i.e., the same voltage as appears across the variable resistor 22). Thus, since the current through the FET 20 and resistor 22 is also equal, the impedance across the control FET 20 is equal to the resistance of resistor 22.

Since the emulating FET 12 is controlled by the same amplifier output signal as the control FET 20, the emulating FET 12 provides an impedance proportional to the impedance of the control FET 20 and thus also, proportional to the resistance of resistor 22. More particularly, if FETs 12, 20 are identical in size, then the impedance of the emulating FET 12 is equal to that of the control FET 20 which, in turn,

is equal to the resistance of resistor 22. More generally however, if the control FET 20 is scaled in size relative to the emulating FET 12 so that $FET_{12} = XFET_{20}$, then the respective impedances are scaled by the same factor X such that the impedance of FET 12 is equal to the impedance of FET 20 divided by the scale factor X.

In order to ensure that the emulating and control FETs 12, 20, respectfully, are maintained in their respective linear regions of operation, the ratio of the gate width "W" to the gate length "L" of each such FET meets the following criteria:

$$\frac{W}{L} < \frac{I_D}{K_{p(max)} \cdot 0.5 \cdot V^2_{DS(max)}} \quad (1)$$

where I_D is the FET drain current, K_p is a constant associated with the FET equal to the product of the surface mobility and the oxide capacitance, and V_{DS} is the voltage across the drain and source electrodes of the respective FET. Compliance with the FET gate size relationship of equation (1) ensures that the gate voltage V_{GS} remains a threshold voltage above the maximum drain to source voltage V_{DS}.

As noted above, with sufficient gate voltage, the second order effect on the relationship between the impedances of the emulating FET 12 and the control FET 20, such as is caused by variations in the voltage at the source electrode 12b of the emulating FET 12, is minimized. More particularly, the drain to source resistance of emulating FET 12 is given as follows:

$$R_{12} = \frac{1 + \theta \cdot V_{GS}}{K_p \cdot (V_{GS} - V_T) \cdot (\frac{W_{12}}{L_{12}})} \quad (2)$$

where θ is a mobility degradation constant. It follows from equation (2) that the change in the resistance of FET 12 with changes in V_{GS} is given by:

$$\frac{\partial R_{12}}{\partial V_{GS}} \alpha \frac{1}{V_{GS}} \quad (3)$$

Equation (3) reveals that as V_{GS} increases, the change in resistance of emulating FET 12 decreases, as is desirable to reduce the second order effect. Stated differently, the higher the gate voltage, the less significant the effect of voltage variations at the source electrode 12b of the emulating FET 12 on the proportionality between the resistance of the emulating FET 12 and the control FET 20.

As is apparent from the above discussion, the impedance of the emulating FET 12 is a function of the resistance of resistor 22, the size scale factor X between the emulating and control FETs, and the relationship between the reference voltage V_{ref} and the regulated voltage V_{reg}. By utilizing a trimmable or variable resistor for the resistor 22, the impedance provided by the emulating FET 12 can be readily adjusted as desired for a particular application.

Referring also to Fig. 3, a further embodiment of the impedance emulator 30 is shown to include a plurality of emulating FETs 32a-n. The impedance emulator 30 is adapted for actively terminating a plurality of conductors 34a-n, such as the conductors of a SCSI bus. More particularly, the gate electrode of each of the emulating FETs 32a-n is coupled to the output of a control circuit 36, substantially identical to the control circuit 16 of Fig. 1 and having a control FET 40 coupled in series with a variable resistor 46 and controlled in a closed-loop manner by an amplifier 42. The drain electrodes of each of the plurality of emulating FETs 32a-n are coupled to a voltage regulator 38 providing a regulated voltage V_{reg}, like the voltage regulator 14 of Fig. 1. With this arrangement, each of the FETs 32a-n presents the same resistive impedance to a corresponding one of the plurality of conductors 34a-n.

Referring to Fig. 4, a detailed schematic of the impedance emulator 30 of Fig. 3 is shown to include the

plurality of emulating FETs 32a-n, voltage regulator 38, and control circuit 36. The control circuit 36 includes NMOS control FET 40 and variable resistor 46, as mentioned above. The non-inverting input V+ of the amplifier 42 receives the reference voltage $V_{ref}=\frac{1}{2}V_{reg}$, as shown. The inverting input V- to the amplifier 42 is coupled to the interconnection between the source electrode 40b of the control FET 40 and the resistor 46. A temperature compensation circuit 47, including a resistor 48 and a current source 50, is coupled between the inverting amplifier input V- and a differential input stage 44 including bipolar transistors 44a,b, as shown. The output stage of the amplifier 42 includes a bipolar transistor 54 coupled to a voltage source V_p where $V_p \gg V_{reg}$ and a FET 56, the interconnection between which provides the amplifier output V_o. In one illustrative embodiment, the regulated voltage V_{reg} is equal to five volts and the voltage V_p is on the order of ten to fifteen volts in order to provide sufficient gate voltage to the FETs 12, 20 to reduce second order effects, as discussed above. Output transistor 54 provides a low output impedance for maintaining loop stability while driving the plurality of emulating FETs 32a-n in the linear region of operation. A current source 58, a diode-connected FET 60, and a diode-connected bipolar transistor 62 are coupled in series between the voltage source V_p and the input transistor 44a to maintain a bias current through transistors 54, 56 making this a class AB amplifier.

As temperature increases, the resistance value of resistor 46 increases. Without the temperature compensation circuit 47, the increased resistance of resistor 46 would cause the impedance of FETs 20 and 12 to concomitantly increase. The temperature compensation circuit 47 compensates for the effect of temperature variations on the resistance value of resistor 46. This compensation is achieved by using a resistor 48 and current whose voltage drop varies with temperature in the same manner as the

impedance controlling resistor 46. More particularly, the voltage at the base of transistor 44a is equal to the voltage at the inverting amplifier input V- minus the product of the resistance of resistor 48 and current I_2. As the resistor 48 increases with temperature, the voltage V- at the inverting input of the amplifier 42 is made to increase at one half the rate of the temperature coefficient associated with resistor 46. This arrangement causes the resistance of FET 40 to remain constant with temperature since increasing the voltage V- has a dual effect of increasing the voltage V_{DS} across the drain and source electrodes of the FET 40 and decreasing the current through the FET 40. As will be appreciated from the above discussion, maintaining the resistance of FET 12 constant with temperature concomitantly maintains the resistance of the emulating FETs 32a-n constant with temperature.

Having described the preferred embodiments of the invention, it will be apparent to one of skill in the art that other embodiments incorporating their concepts may be used. Accordingly, the invention should be limited only by the spirit and scope of the appended claims.

CLAIMS

1. A terminator for terminating a conductor comprising:

a voltage source;

an emulating FET having a first electrode, a second electrode, and a third electrode, said second and third electrodes adapted for being coupled in series between said voltage source and said conductor; and

a control circuit coupled to said first electrode of said emulating FET for maintaining said emulating FET in a linear region of operation.

2. The terminator recited in Claim 1 wherein said emulating FET is an NMOS device and wherein said first electrode is a gate electrode, said second electrode is a drain electrode coupled to said voltage source, and said third electrode is a source electrode adapted for coupling to said conductor.

3. The terminator recited in Claim 2 wherein said control circuit comprises:

(a) a control FET having a gate electrode, a source electrode, and a drain electrode;

(b) a resistor having a resistance value associated therewith and coupled in series with said control FET; and

(c) an amplifier providing an output signal coupled to said gate electrodes of control FET and said emulating FET, said output signal causing said control FET and said emulating FET to provide an impedance having a predetermined relationship with respect to said resistance value of said resistor.

4. The terminator recited in Claim 3 wherein said amplifier has a pair of inputs, a first one receiving a reference voltage and a second one coupled to said resistor and said control FET.

5. The terminator recited in Claim 3 wherein said resistor has a variable resistance value and wherein said emulating FET provides an impedance proportional to said resistance value of said resistor.

6. The terminator recited in Claim 3 wherein said amplifier includes a temperature compensation circuit for compensating for the effect of temperature variations on said resistance value of said resistor.

7. The terminator recited in Claim 1 wherein said voltage source is a voltage regulator.

8. A circuit for emulating an impedance comprising:

a voltage source;

an emulating FET having a gate electrode, a source electrode, and a drain electrode, said drain electrode being coupled to said voltage source; and

a control circuit coupled to said gate electrode of said emulating FET for providing a control signal to maintain said emulating FET in a linear region of operation, said control circuit comprising a resistor having a resistance value, wherein said control signal causes said emulating FET to provide an impedance proportional to said resistance value.

9. The circuit recited in Claim 8 wherein said resistor is a variable resistor having a variable resistance value so that said impedance provided by said emulating FET is adjustable in accordance with variable resistance value.

10. The terminator recited in Claim 8 wherein said control circuit comprises:

(a) a control FET having a gate electrode, a source electrode, and a drain electrode;

(b) a resistor having a resistance value associated therewith and coupled in series with said control FET; and

(c) an amplifier providing an output signal for controlling said control FET and said emulating FET, said output signal causing said control FET and said emulating FET to provide an impedance having a predetermined relationship with respect to said resistance value of said resistor.

11. The terminator recited in Claim 10 wherein said control FET and said series coupled resistor are coupled across said voltage source and wherein said amplifier has a pair of inputs, a first one receiving a reference voltage equal to a predetermined fraction of a voltage provided by said voltage source and a second one coupled to an interconnection between said resistor and said control FET.

12. The circuit recited in Claim 8 wherein said emulating FET is an NMOS device.

13. A circuit for terminating a conductor, said circuit comprising:

a voltage regulator;

an emulating FET having a gate electrode, a source electrode, and a drain electrode, said drain electrode being coupled to said voltage regulator and said source electrode adapted for coupling to said conductor; and

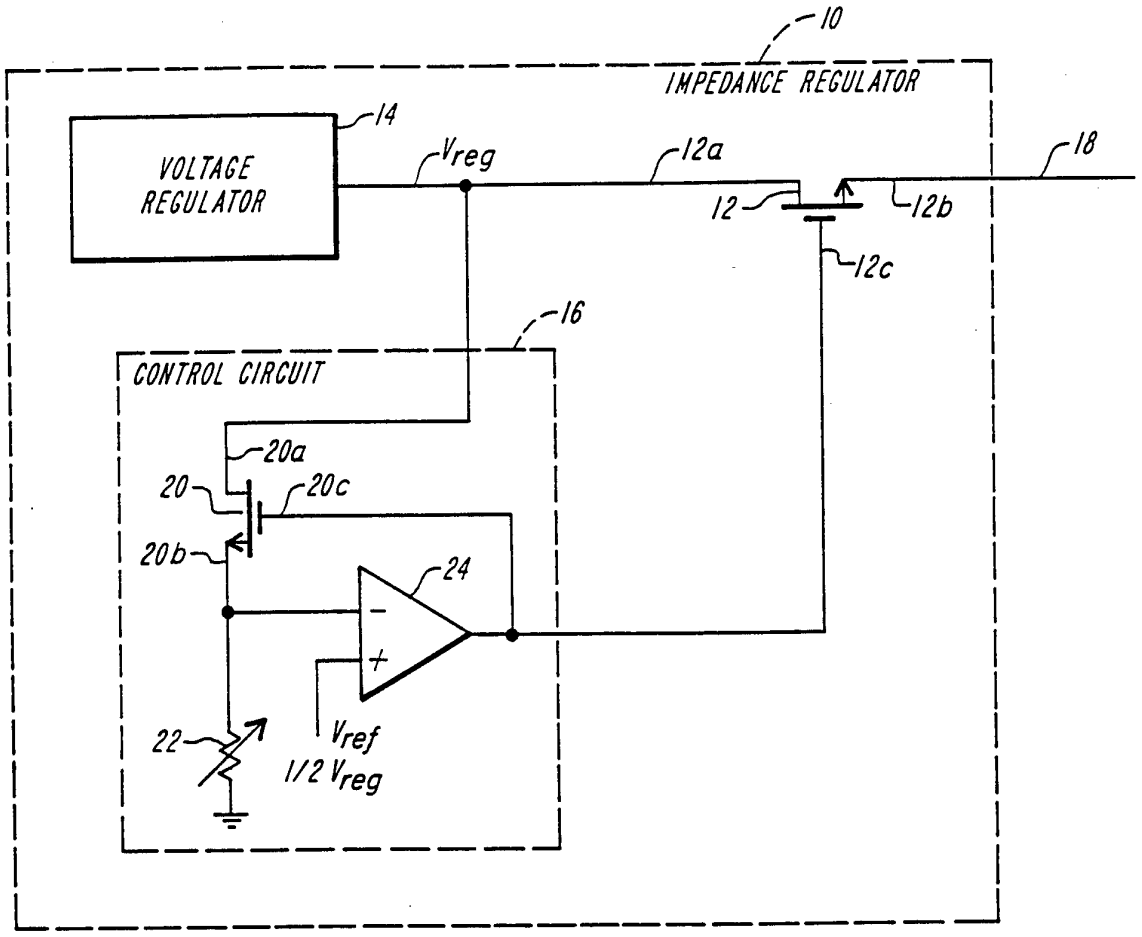
a control circuit coupled to said gate electrode of said emulating FET for providing a control signal to maintain said emulating FET in a linear region of operation, said control circuit comprising:

(a) a control FET having a gate electrode, a source electrode, and a drain electrode coupled to said voltage regulator;

(b) a resistor coupled to said source electrode of said control FET; and

(c) an amplifier having a pair of input terminals and an output terminal, a first one of said pair of input terminals being coupled to a reference voltage, a second one

of said pair of input terminals being coupled to said source electrode of said control FET, and said output terminal being coupled to said gate electrode of said emulating FET and said gate electrode of said control FET.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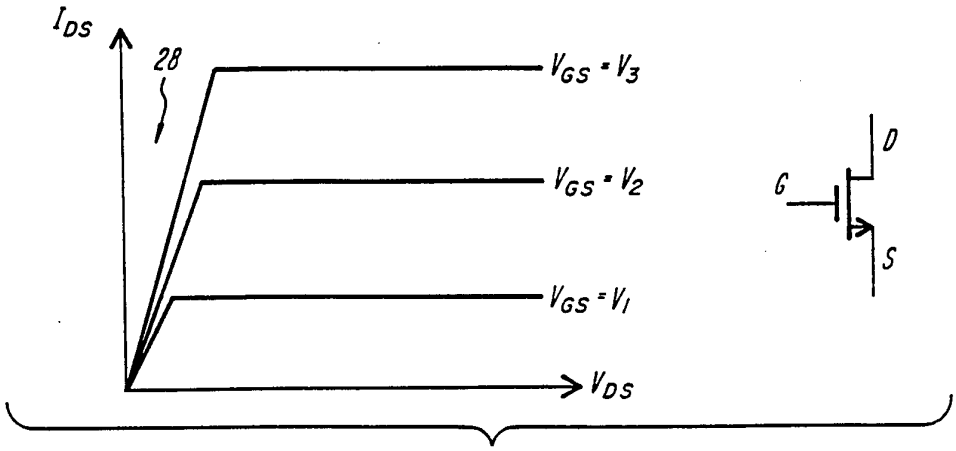
IMPEDANCE REGULATOR
14
VOLTAGE REGULATOR
Vreg
12a
18
12
12b
12c
16
CONTROL CIRCUIT
20a
20
20c
20b
24
22
Vref
1/2 Vreg

FIG. 1


IDS
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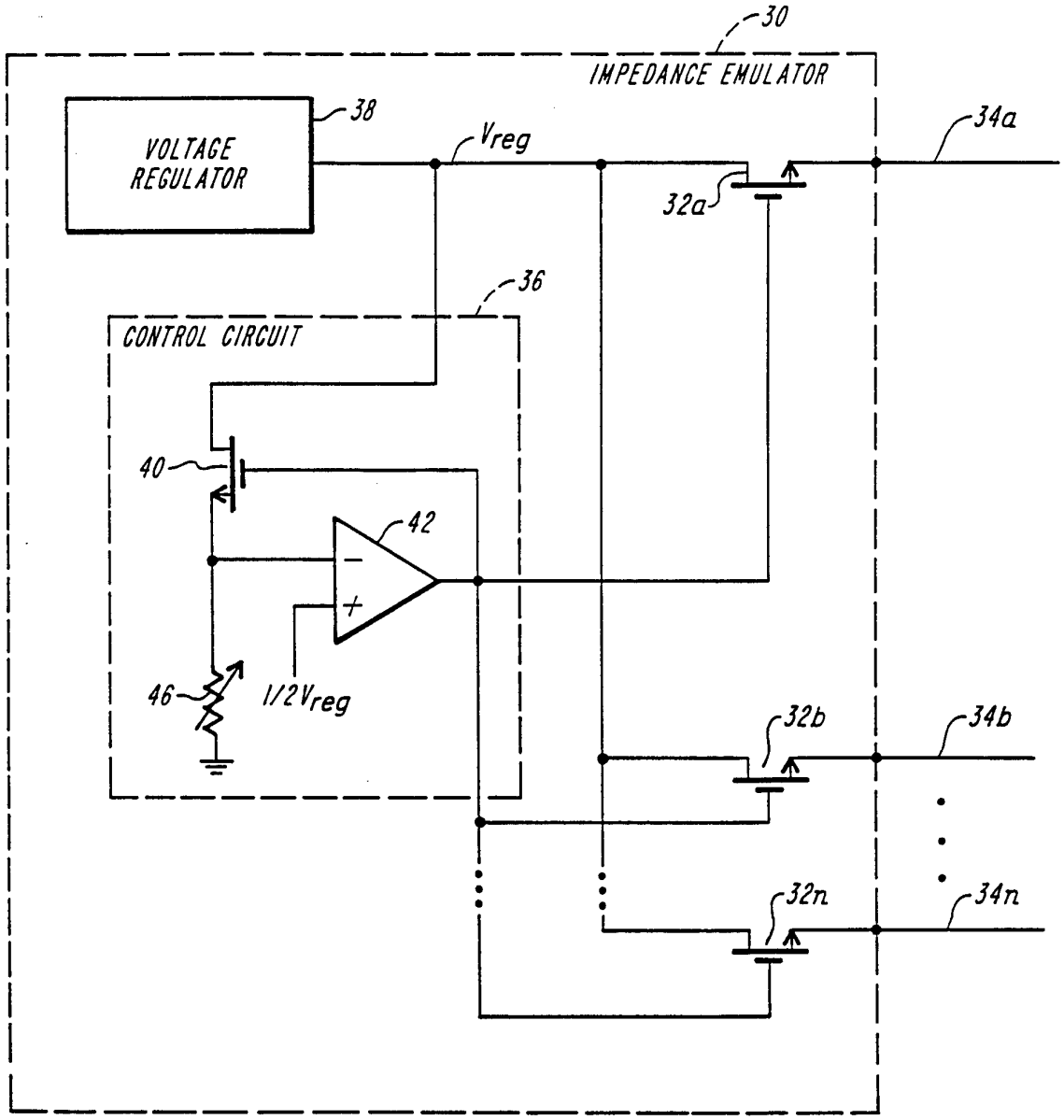
VGS = V3
VGS = V2
VGS = V1
VDS
D
G
S

FIG. 2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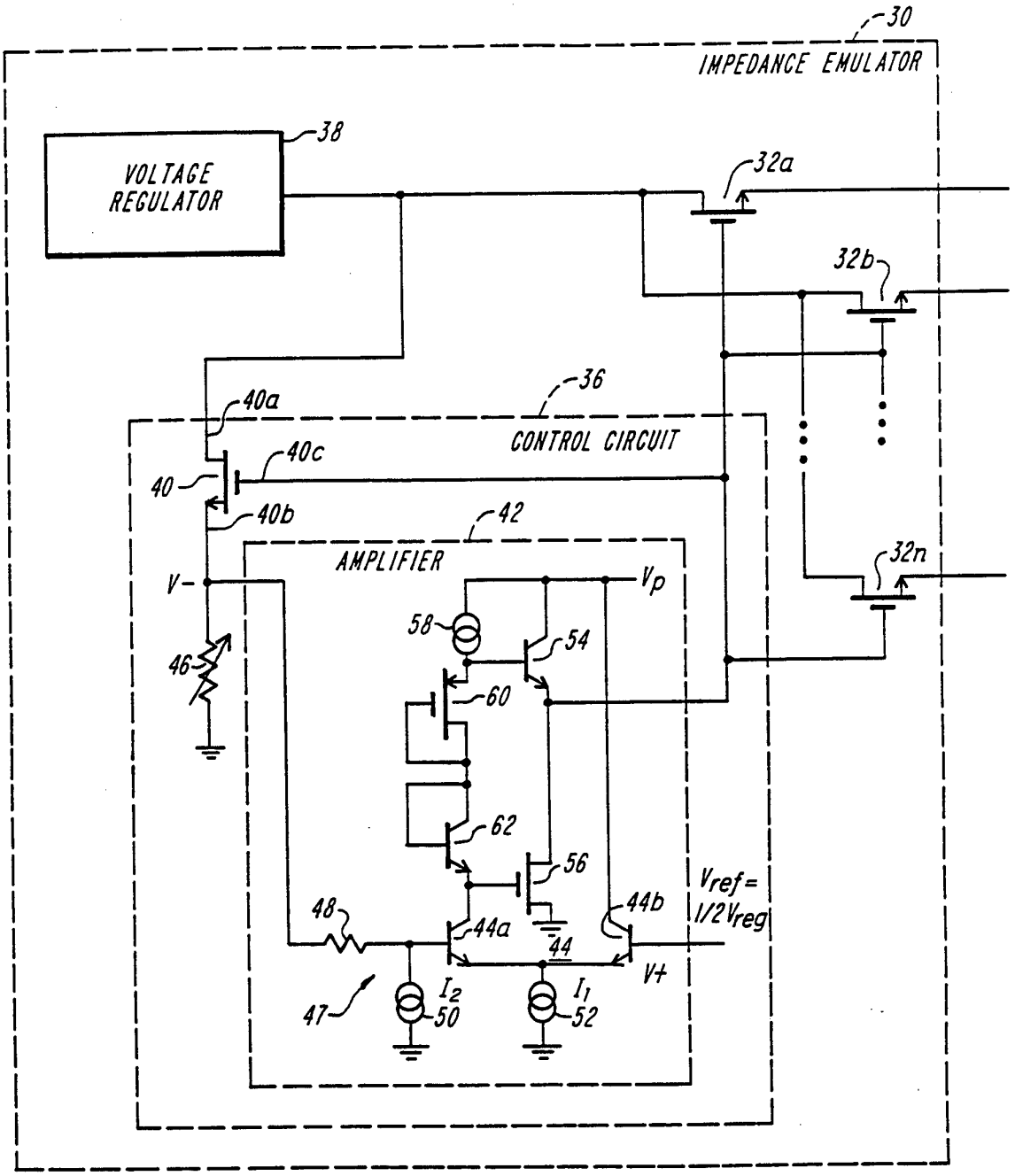
IMPEDANCE EMULATOR
38
VOLTAGE REGULATOR
Vreg
34a
32a
36
CONTROL CIRCUIT
40
42
46
1/2Vreg
32b
34b
32n
34n

FIG. 3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38
VOLTAGE REGULATOR
32a
32b
32n
36
CONTROL CIRCUIT
40a
40c
40
40b
42
AMPLIFIER
V-
Vp
58
54
46
60
62
56
48
44a
44
44b
Vref= 1/2Vreg
V+
47
I2
50
I1
52

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/04844

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H03K 17/16
US CL : 326/30, 32; 333/22R
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 326/30, 32; 333/22R, 32; 375/36, 17

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS
SEARCH TERMS: TERMINAT?, BUS/CONDUCTOR, FET, IMPEDANCE, EMULAT?

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 5,124,580 (MATTHEWS ET AL) 23 JUNE 1992, figures 3-6.	1-13
Y	US, A, 5,136,187 (CECCHERELLI ET AL) 04 AUGUST 1992, figure 1a.	1-7, 13
A	US, A, 4,109,117 (WRENCH, JR. ET AL) 22 AUGUST 1978, figure 1.	1-13
A	US, A, 5,283,479 (ROSSEEL ET AL) 01 FEBRUARY 1994, figures 3-10.	1-13
A, P	US, A, 5,329,184 (REDFERN) 12 JULY 1994, figure 7.	1-13
A	US, A, 4,748,426 (STEWART) 31 MAY 1988, figure 2.	1-13

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search
31 MAY 1995

Date of mailing of the international search report
08 JUN 1995

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