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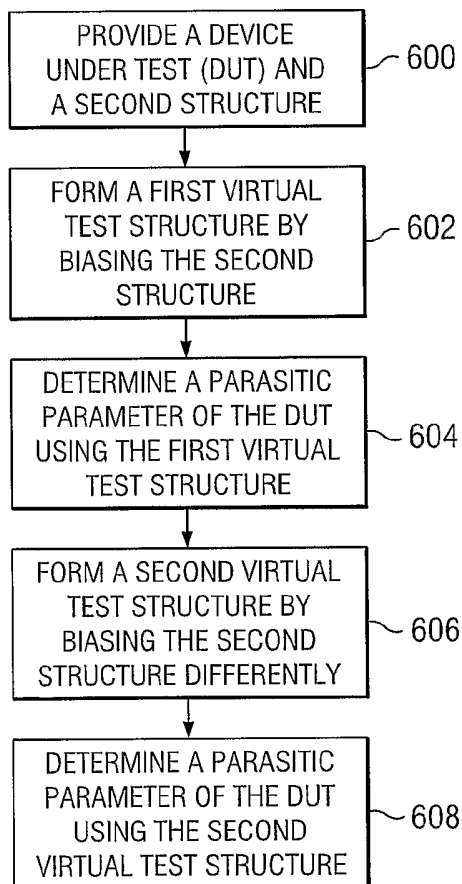
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(54) Title: METHOD FOR CAPACITANCE MEASUREMENT IN SILICON



(57) Abstract: A method (Figure 6) for testing a partially fabricated wafer comprising: providing a plurality of selectable devices under test (DUT) overlying a substrate of the wafer (600); biasing a second structure in proximity to the DUT having a first electrical state such that a first equivalent test structure is formed (602); determining a first parasitic parameter associated with the first equivalent test structure by applying a signal to the DUT while the second structure is in the first electrical state and measuring a response that is indicative of the first parameter (604); biasing the second structure to a second electrical state such that a second equivalent test structure is formed (606); determining a second parasitic parameter associated with the second equivalent test structure by applying a signal to the DUT while the second structure is in the second electrical state and measuring a response that is indicative of the second parameter (608).

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METHOD FOR CAPACITANCE MEASUREMENT IN SILICON

The present invention relates to integrated circuit fabrication, and specifically to structures and methods for electrical testing and/or for process monitoring and/or parasitic extraction accuracy monitoring and/or building statistical interconnect models based on silicon measurements.

BACKGROUND

A critical part of semiconductor manufacturing and design is the testing of integrated circuits. Before the functionality tests at the end of processing, additional testing for process monitoring is also useful. Testing for process monitoring uses special test structures which are not part of the integrated circuit's functionality. Process monitoring helps to detect problems that may cause reliability problems in the field, helps to optimize the process for maximum yield, and helps to catch any process deviations before too much work-in-process is wasted.

Typical electrical test structures for in-process testing are long series-connected chains of similar elements (to test for excessive resistance or open circuits). The test structure will also include two or more "probe pads," which are flat metal surface that electrical connection can be made to them in the test lab. These test structures are manufactured at the same time as the functional circuitry, using the same process steps, but are specially designed to test particular process parameters. (For example, to test for specific contact resistance a chain of thousands of series-connected contacts might be created.) A large variety of test structures are used by process engineers to test various process stages and device portions.

A "wafer" is a flat disk of semiconductor material on which integrated circuits are made by micro-fabrication techniques. After fabrication is complete, the wafer will be separated into rectangular "dice," each of which is the electronics portion of one integrated circuit. The dice will be packaged to provide the end-product integrated circuits. Typically one wafer will provide dozens or hundreds of dice.

When the dice are separated, some of the wafer surface between them is wasted. This space is known as "scribe lines," since the dice were formerly separated by scribing and fracturing; now that diamond sawing has replaced scribing, these spaces are also known as "saw streets."

Test structures are placed within the scribe lines of the wafer (and in other places), typically once or more per photolithographic field. Typical scribe line test structures are individually connected to corresponding probe pads, also located in the scribe lines. Since the area within the scribe lines is densely occupied, the size and number of probe pads is critical.

5 However, probe pad size has not scaled as fast as other process steps, and the space available within the scribe lines is very limited. Placing multiple test structures and probe pads for those test structures within this limited area becomes difficult in many processes, and limits the testing of the wafer fabrication process. Limits to the testing capability lead to less reliable integrated circuits.

10 Scribe line widths are typically less than a tenth of a millimeter. Probe pads are typically made just small enough to fit within the scribe line. These dimensions can be expected to change over time, in dependence on wafer fabrication and separation technologies; but the key point is that each probe pad occupies a very significant fraction of the limited available scribe line area.

15 Since each probe pad nearly fills the width of a scribe line, the layout of test structures in the scribe lines is often somewhat one-dimensional. That is, a test structure in the scribe lines can be allowed to take up nearly the entire width of the scribe line, and extended along the scribe line as far as necessary.

Some space in the corners of the dice themselves is typically also allocated for test
20 patterns, but again the available area is limited. Typically several to several tens of test structures can fit into each corner of a die.

Some space for test structures is also available along the edge of the wafer, where the grid of square or rectangular dice meets the unusable width of the rounded edge. While these spaces are relatively large, they are far from the important central areas of the wafer. Thus
25 test structures in the edge-of-wafer corners cannot provide sufficiently close monitoring of process variation, including spatial variation across the wafer.

One basic tool for process monitoring is the use of pilot wafers. Some manufacturers will start several pilot or dummy wafers for each wafer that will produce actual chips. While some use of pilot wafers will always be common (e.g. at the head of each lot), every pilot
30 wafer start takes the place of a wafer full of salable chips. Thus to the extent that sufficient

process monitoring can be done using on-chip test and monitoring structures, this is greatly preferable to use of pilot wafers. Dummy wafers, on the other hand, are used to ensure that equipment has stabilized, e.g. when a bulk furnace is being ramped up or when a wet processing station has been refilled. Use of such dummy wafers is not motivated by process monitoring needs, and hence would not appear to be subject to trade-off against on-wafer test structures.

U.S. Pat. publication 2002-0047724, entitled "Multi-state test structures and methods," describes a selection capability that radically increases the number of test structures per probe pad. By adding a test selector to the test structure, multiple test structures are multiplexed to one (or more) probe pads. Selection of which test structure is to be accessed from a given probe pad is preferably performed entirely by control of the voltage applied across the probe pads. In one class of embodiments, the applied voltage directly determines which test structure will be accessed. In another class of embodiments, modulation of the applied voltage controls sequential logic that selects one of multiple test structures for access.

In the past, circuit delay has been due mostly to transistors. Today, the dominant source of delay in circuits such as ASICs and microprocessors is metal interconnect. FIG. 1 is a schematic diagram of a prior art charge-based capacitance measurement (CBCM) structure for measuring parasitic capacitance. A paper entitled "An On-Chip, Attofarad Interconnect Charge-Based Capacitance Measurement (CBCM) Technique," Proc. of IEDM 1996, pp. 69-72, discloses an improved test structure for performing CBCM that included an on-chip signal generator and an entirely new measurement scheme as well. The resolution limit of the methodology is estimated to be 0.01 fF, hence making it more than adequate for characterizing parasitic interconnect capacitances.

In this paper, a test structure is disclosed that comprises a pair of NMOS and PMOS transistors connected in a "pseudo" inverter configuration two form two inverters 100, 101. Inverter 100 is a reference inverter used to achieve the highest resolution. Inverter 100 is identical to inverter 101 in every manner except that it does not include the target capacitance to be characterized. Inverter 101 is connected to the target device that is to be measured. For example, in FIG. 1 the target device consists of level 2 metal line 111 and level 1 metal line

112 that form an intersection at 110. This structure is used to measure the resulting interconnect capacitance between the two lines. The reference inverter is connected to metal 1 line 113 that is the same configuration as line 112, but does not contain the metal 1 to metal 2 overlap capacitance that is to be measured.

5 FIG. 2 is a timing diagram illustrating non-overlapping clock signals used by the prior art CBCM structure of FIG. 1. The V1 and V2 signals of FIG. 1 consist of two non-overlapping signals shown in FIG. 2. These signals can be either generated off-chip or on chip. The purpose of these non-overlapping waveforms is to ensure that only one of the two transistors in each test structure inverter is conducting current at any given time. Thus, short-circuit current from Vdd to ground is eliminated. When the PMOS transistor turns on, it will
10 draw charge from Vdd to charge up the target interconnect capacitance.

This amount of charge will then be subsequently discharged through the NMOS transistor into ground. An ammeter can be placed at the source of the PMOSFET (or, alternatively at the source of the NMOSFET) to measure this charging current. The actual
15 waveform of this charging current is of no consequence; only its DC or average current value needs to be measured. DC current can be easily obtained from any modern current meter. The difference between the two DC current values in FIG. 1 is used to extract the target interconnect capacitance as shown by equations 1 and 2 below.

$$I - I_{\text{ref}} = I_{\text{net}} \quad (1)$$

$$20 \quad C = I_{\text{net}} / V_{\text{dd}} * F \quad (2)$$

CBCM can be used in conjunction with simulation at early process development stages to provide designers with accurate parasitic interconnect capacitances; including metal to substrate, interwire, and interlayer capacitances, as discussed in a paper entitled
"Investigation of Interconnect Capacitance using Charge-Based Capacitance Measurement
25 (CBCM) Technique and 3-Dimensional Simulation", IEEE JSSC, pp. 449-453, March 1998. However, this paper teaches that several test structures must be utilized to decouple vertical and horizontal capacitive components from the total capacitance.

Therefore, there is still a need in the art for a way to increase the efficiency of space usage for test structures within the scribe lines of an integrated circuit process.

SUMMARY

An apparatus is provided for testing a partially fabricated wafer using a test structure located within the scribe lines of the wafer. The test structure includes a first structure overlying a substrate and coupled to a first probe pad, such that the first structure has a first parasitic capacitance relative to the substrate. A second structure is located in proximity to the first structure, such that the first structure has a second parasitic capacitance relative to the second structure. A bias circuit is coupled to the second structure and has an input coupled to a second probe pad. The bias circuit is operable to bias the second structure in response to a select signal impressed on the second probe pad. A test signal impressed on the first probe pad is operable to provide a measure of the first parasitic capacitance when the select signal has a first value; and the test signal is operable to provide a measure of the second parasitic capacitance when the select signal has a second value.

A method for testing a partially fabricated wafer is provided that comprises the following steps:

- a) providing a device under test (DUT) overlying a substrate of the wafer;
- b) biasing a second structure located in proximity to the DUT to have a first electrical state such that a first equivalent test structure is formed;
- c) determining a first parasitic parameter associated with the first equivalent test structure by applying a signal to the DUT while the second structure is in the first electrical state and measuring a response that is indicative of the first parameter;
- d) biasing the second structure to have a second electrical state such that a second equivalent test structure is formed; and
- e) determining a second parasitic parameter associated with the second equivalent test structure by applying a signal to the DUT while the second structure is in the second electrical state and measuring a response that is indicative of the second parameter.

Advantages of the disclosed methods and structures, in various embodiments, can include one or more of the following: more test structures can be used on a given wafer; test structures can be made larger; quicker correction of process deviations; increased efficiency of use of wafer area; increased efficiency of use of scribe line area; fewer probe pads are

needed; increased yield; and increased capability for "early warning" testing increases reliability of the integrated circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

The disclosed inventions will be described with reference to the accompanying
5 drawings, which show important sample embodiments of the invention, wherein:

FIG. 1 is a schematic diagram of a prior art charge-based capacitance measurement (CBCM) structure for measuring parasitic capacitance;

FIG. 2 is a timing diagram illustrating non-overlapping clock signals used by the prior art CBCM structure;

10 FIG. 3 is an illustration of a partially completed wafer showing the placement of individual chips and scribe lines in which are located test structures according to the present invention;

FIG. 4 is a schematic illustrating an embodiment of a CBCM test structure according to aspects of the present invention;

15 FIG. 5 is a pictorial representation of various parasitic capacitances that exists in the structure of FIG. 4;

FIG. 6 is a flow chart of a test method using the structure of FIG. 4;

FIG. 7 is a pictorial of a more complex structure illustrating various parasitic capacitances that can be isolated using a single structure, according to aspects of the present
20 invention; and

FIG. 8 is a schematic illustrating use of a common reference circuit for several CBCM measurement circuits.

FIG. 9 is a schematic illustrating the use of demultiplexing circuits to expand the number of DUTs.

25 Corresponding numerals and symbols in the different figures refer to corresponding parts unless otherwise indicated.

DETAILED DESCRIPTION OF THE EMBODIMENTS

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred embodiment. However, it should be understood
30 that this class of embodiments provides only a few examples of the many advantageous uses

of the innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others.

FIG. 3 shows a wafer 100 on which individual chips 102 are being built. The chips 102 are divided by scribe lines 104. As described below, the area of the scribe lines 104 is used to place test structures and test selectors, so that area on the wafer is used efficiently. The test selectors comprise circuit elements that accept a select signal and multiplex one of several biasing signals onto the test structures depending on that input signal. In this way, a single probe pad can be used to effectively vary a test structure on a wafer, thus reducing the number of structures needed to determine parasitic values associated with a three dimensional structure and thereby improving the efficiency of the testing process, as will now be described in more detail.

The test structures and test selectors are made on the wafer surface in the same way that other circuit features are produced. In the preferred embodiment, this includes the typical integrated circuit fabrication processes, such as photolithography, etches, depositions, etc. These features are placed on the wafer area that is later used for scribe lines that separate the several chips on the wafer. When the chips are physically separated from one another (by sawing, breaking, etc.), the test structures and test selectors are destroyed. These test structures and test selectors are normally not connected to any circuitry on the chips themselves.

FIG. 4 is a schematic illustrating an embodiment of a CBCM test structure according to aspects of the present invention. The overall technique is similar to prior art structures, however, in this embodiment reference inverter 400 is located separately from the device under test (DUT) inverter 401. In order to achieve the highest resolution, a null line segment 413 is included with the reference inverter that is identical to null line segment 412. Null line segment 412 is a necessary connection line to the DUT line 410, but its parasitic capacitance is not to be included as part of DUT line 410. An advantage of locating reference inverter separately from DUT inverter 401 will be discussed with reference to FIG. 8. In another embodiment of the present invention, reference inverter 400 may be co-located with DUT inverter 401.

DUT line 410 extends over the substrate of the wafer for some distance and therefore has a parasitic capacitance to the substrate. A second structure 411 is located in proximity to DUT line 410 and is fashioned as side by side tracks on either side of line 410. In another test structure, other configurations may be employed, as will be described later. Second structure 411 also has parasitic capacitive effects with DUT line 410. DUT line 410 and structure 411 are representative of parallel signal lines used for interconnect in a finished circuit. The line to substrate and line-to-line parasitic values are an important factor in the design of the finished circuit and therefore need to be monitored during fabrication of a wafer.

In order to test both parameters with only a single structure, select circuitry 420 is provided along with another inverter 402. Inverter 402 will be referred to as a bias inverter. Reference inverter 400 and test structure inverter 401 identical in every manner. Bias inverter 402 is likewise similar to inverter 401, but may be modified slightly in order to maintain similar signal characteristics between line 410 and structure 411. Selector 420 is controlled by select signal 421 and causes different bias conditions to be selected and applied to structure 411.

By biasing structure 411 to a steady voltage, such as to substrate potential, the combined parasitic capacitance of DUT line 410 to the substrate and also to structure 411 can be measured. Alternatively, another steady voltage, such as V_{dd} could be applied to structure 411 as a bias. In this embodiment, when select is de-asserted (a logical low signal) each multiplexer of select circuit 420 passes a logical one signal to the two gate inputs of bias inverter 402. This causes the PMOS transistor to turn off and the NMOS transistor to connect structure 411 to ground, thereby biasing the structure with a steady ground potential. The CBCM measurement is then made by applying a periodic voltage to the DUT line 410 from test inverter 401 in response to non-overlapping clock signals pclk and nclk. Test voltage V_{test} is applied to a probe pad connected to inverter 401 for this purpose and a resulting DUT current flow I_{DUT} is measured that is representative of the parasitic capacitance value. Similarly, a null current I_{null} is measured by applying reference voltage V_{ref} to a probe pad connected to null inverter 400. Null inverter 400 also is controlled by non-overlapping clock signals pclk and nclk. The parasitic capacitance is then determined using equation 3.

$$C = (I_{DUT} - I_{NULL}) / V_{dd} * F \quad (3)$$

Then, by asserting the select signal (a logical one), each multiplexer of select circuit 420 passes the non-overlapping clock signals pclk, nclk to the two gate inputs of bias inverter 402. This then causes structure 411 to be biased with a periodic voltage that has the same waveform as the periodic voltage applied to DUT line 410. Because of this, no charge will flow between DUT line 410 and structure 411 due to parasitic capacitance. Therefore, the test structure is effectively changed to form a virtual test structure that only comprises the DUT. Thus, when the CBCM measurement process is again performed, as described above, only the parasitic capacitance of DUT line 410 with reference to the substrate will be measured.

Thus, by placing two different bias signals on structure 411, two different virtual test structures are formed and two different parasitic capacitance parameters can be measured using only one physical test structure.

FIG. 5 is a pictorial representation of various parasitic capacitances that exists in the structure of FIG. 4. Capacitance 500 represents a parasitic capacitance between DUT 410 and substrate 510 due to the physical proximity of DUT 410 to substrate 500. Of course, it is to be understood that capacitance 500 is a distributed capacitance along the length of DUT 410, but is shown for simplicity as a single element. After capacitive measurements are taken using the CBCM technique, generally the measured value is normalized to a capacitance/length value based on the length of DUT 410.

Parasitic capacitance 501 and 502 likewise represent distributed parasitic capacitance that occur between DUT 410 and secondary structure 411 represented by 411a, 411b due to the proximity of structure 411 to DUT 410.

By applying a first constant voltage bias signal to structure 411 via signal line 411.1, a CBCM measurement of current drawn into DUT 410 will be indicative of combined capacitance 500, 501 and 502. Advantageously, by applying a periodic bias voltage to structure 411 via 411.1 that mirrors the periodic CBCM voltage applied to DUT 410, a virtual structure is formed that effectively does not include secondary structure 411. CBCM measurement of current drawn into DUT 410 will be indicative of only capacitance 500, since no charge will flow between DUT 410 and structure 411. Thus, capacitance 501 and 502 can be deduced by subtracting the measured value of capacitance 500 from the total measured value of combined capacitance 500, 501, 502. In this embodiment, element 411a

and 411b are identical and equally spaced from DUT, therefore it can further be deduced that capacitance 501 is approximately equal to capacitance 502.

FIG. 6 is a flow chart of a test method using the structure of FIG. 4. In step 600, a device under test (DUT) is provided that overlays a substrate of the wafer. A second structure located in proximity to the DUT is also provided. As discussed above, the DUT has a parasitic parameter relative to the substrate and a parasitic parameter relative to the second structure.

In step 602, a first virtual test structure is formed by biasing the second structure to have a first electrical state. This is done by connecting the second structure to the substrate, for example

In step 604, a first parasitic parameter is determined by applying a signal to the DUT while the second structure is in the first electrical state and measuring a response that is indicative of the first parameter. Using the CBCM technique, measuring the current drawn into the DUT will provide a current value that is indicative of the combined capacitance of the DUT relative to the substrate and relative to the second structure.

In step 606, a second virtual test structure is formed by biasing the second structure to have a second electrical state. This is done by connecting the second structure to periodic voltage that is the same or similar to a periodic voltage applied to the DUT, for example.

In step 608, a second parasitic parameter is determined by applying a signal to the DUT while the second structure is in the second electrical state and measuring a response that is indicative of the second parameter. Using the CBCM technique, measuring the current drawn into the DUT will now provide a current value that is indicative of only the capacitance of the DUT relative to the substrate since the second structure has been virtually removed from the test structure by the periodic bias signal.

FIG. 7 is a pictorial of a more complex structure illustrating various parasitic capacitances that can be isolated using a single structure, according to aspects of the present invention. Element 600 is the DUT and overlays a substrate, not shown for clarity. Elements 601 and 602 proximally located in parallel to DUT 600 on a same level. Element 604 is proximally located in parallel to DUT 600 on a lower level. Elements 603 and 605 are proximally located in a perpendicular arrangement on different levels. Various parasitic

capacitances 611-615 exist between DUT 600 and elements 601-605 due to the close physical spacing. Advantageously, by connecting various combinations of bias voltages to elements 601-605 via respective terminals 601.1-605.5 various virtual structures can be formed. By performing a CBCM measurement on each virtual structure, the various parasitic
5 capacitances 611-615 can be directly measured or deduced, as described previously.

FIG. 8 is a schematic of a test structure 750 that includes many DUT inverters 701.1-701.n and illustrating use of a common reference circuit 700. Referring again to FIG. 4, it was mentioned that reference circuit 400 optionally could be located separately from DUT inverter 401. The inventor of the present invention has discovered that a single reference
10 inverter 700 can be used to improve the resolution of a number of DUT inverters 701.1-701.n, where each DUT inverter 701.x is similar to DUT inverter 401 and reference inverter 700 is similar to reference inverter 400. Non-overlapping clock signals nclk and pclk are routed to each inverter and are provided by dedicated probe pads. Each of DUT inverters 701.1-701.n is designed to be identical. Within a local region that includes all of DUT
15 inverters 701.1-701.n, fabrication repeatability is generally good enough to insure that all of the DUT inverters will have the same electrical characteristics so that a single reference inverter is sufficient. Advantageously, this allows a smaller overall footprint for test structure 750.

Another aspect of test structure 750 is that it is divided into banks, as represented by
20 bank 751 that each contain three or four DUT inverters, for example. In this embodiment, bank 750 has three DUT inverters 701.1-701.3 that each have a respective probe pad 703.1-703.3 for providing a test voltage V_{test} . Bias circuitry that includes selection circuitry 720.1 and bias inverter 702.1 provide a bias voltage to each of the three secondary structures associated with each of respective DUTs 710.1-710.3. Advantageously, a single select signal
25 applied to probe pad 721 controls selection circuitry 720.1 and thereby controls the bias of each of the secondary structures. Note that each of the secondary structures may have a different physical configuration, or they may all be the same.

Additional banks each have another bias circuit, such a selection circuit 720.2 and bias inverter 702.2. All of the selection circuits receive a common select signal from probe
30 721. However, in an alternate embodiment, separate select signals may be provided on

separate probe pads. This may be useful in a complex structure such as that illustrated in FIG. 7.

A representative test structure 750 may contain 20 probe pads. Two are connected to receive the non-overlapping clock signals. One is connected to receive the select signal.

5 Another one is connected to provide Vbias to each of the bias inverters 702.x. Another is connected to provide Vref to the single reference inverter 700. The remaining fifteen probe pads are connected to provide Vtest to each of fifteen DUT inverters 701.x that are organized into five banks. The twenty probe pads are arranged in a linear manner and the entire test structure fits within a scribe line region. Larger test structures can be configured in a similar
10 manner, for example having forty probe pads.

Figure 9 shows a test structure wherein a plurality of DUT's 901 through 904 are connected to demultiplexer 905. Control lines 906 and 907 may be used to select the DUT to be tested. The depth of the demultiplexer chain may be extended to increase the number of DUT's that may be selected for testing.

15 As used herein, the terms "applied," "connected," and "connection" mean electrically connected, including where additional elements may be in the electrical connection path. "Associated" means a controlling relationship, such as a memory resource that is controlled by an associated port. The terms assert, assertion, de-assert, de-assertion, negate and negation are used to avoid confusion when dealing with a mixture of active high and active low
20 signals. Assert and assertion are used to indicate that a signal is rendered active, or logically true. De-assert, de-assertion, negate, and negation are used to indicate that a signal is rendered inactive, or logically false.

While the invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various other
25 embodiments of the invention will be apparent to persons skilled in the art upon reference to this description. For example, in another embodiment, the non-overlapping clock signals are generated by a clock circuit within the test structure, rather than being supplied via a probe pad. In another embodiment, a single clock is provided via a probe pad that is then converted into two non-overlapping clock signals by a circuit included with the test structure.

Various types to DUT structures can be used; for example, active components such as transistors can be included in order to measure parasitic parameters of the transistors.

An operational circuit, such as a ring oscillator can be a DUT and an operation parameter such as frequency can be measured. The select signal can be used to bias a
5 secondary structure proximate to the oscillator and a resulting frequency can be measured to determine sensitivity of the oscillator to the secondary structure.

In another embodiment, multiple ring oscillators may be used both as a DUT and as a reference, and the circuit's inductance may be derived by measuring the frequency of the oscillators.

10 In another embodiment, the select signal may be used to select more than two bias parameters by using a multi-bit select signal, or by encoding a select number using a pulse code or various signal levels, for example.

In another embodiment, one bias circuit may be used to bias all of the secondary structures in a given test structure. Alternatively, one selection circuit having multiple outputs
15 may be connected to several different bias inverters so that a single select signal can cause different bias conditions to be placed on various secondary structures. In this case, the select signal may be a multi-bit select signal, or may be encoded by using a pulse code or various signal levels, for example.

In another embodiment, additional multiplexers or demultiplexers may be provided
20 and used to select from multiple test structures according to an input signal in order to reduce the needed number of probe pads. When a particular DUT test structure is selected, that test structure is connected to the probe pads and its electrical characteristics are tested by further selecting various bias values to configure various effective structures, as described above.

Advantageously, the test methods described herein may be used for measuring
25 capacitance of a variety of structures. For example, the method can be used to monitor memory bit-line and word-line capacitances. Alternatively, the method can be used to measure transistor intrinsic capacitance. Alternatively, the method can be used to separate out capacitances due to contacts and vias in integrated circuits. Many other types of structures may be measured using the methods described herein as is readily apparent to one skilled in
30 the art of semiconductor circuit design and/or fabrication.

It is therefore contemplated that any such modifications of the embodiments fall within the scope of the invention.

CLAIMS

1. A wafer having a plurality of parasitic capacitance test structures, where a single test structure is selectable by means of one or more select signals, with the test structure comprising:

a first structure overlying a substrate and coupled to a first probe pad, the first structure having a first parasitic capacitance relative to the substrate;

a second structure being located in proximity to the first structure, such that the first structure has a second parasitic capacitance relative to the second structure; and

a bias circuit having an input coupled to a second probe pad and an output coupled to the second structure, wherein the bias circuit is operable to bias the second structure in response to a select signal impressed on the second probe pad.

2. The wafer of claim 1, wherein a test signal impressed on the first probe pad is operable to provide a measure of the first parasitic capacitance when the select signal has a first value; and the test signal is operable to provide a measure of the second parasitic capacitance when the select signal has a second value.

3. The wafer of claim 1, wherein the first structure is connected to a switching circuit for periodically switching between the first probe pad and the substrate such that a resulting periodic voltage periodically charges and discharges the parasitic capacitance of the first structure, whereby a current drawn through the first probe pad provides a measure of the parasitic capacitance associated with the first structure.

4. The wafer of claim 3, wherein the bias circuit comprises:

a switching circuit with an output connected to the second structure for periodically switching between a third probe pad and the substrate such that a resulting periodic bias voltage periodically charges and discharges the parasitic capacitance of the second structure to a voltage equal to approximately that of the first structure; and

a selection circuit having the input that is coupled to the second probe pad and an output connected to control the switching circuit.

5. The wafer of claim 4, wherein when the select signal has the first value, the switching circuit is directed to bias the second structure with the periodic bias voltage,

whereby the test signal provides a measure of the first parasitic capacitance exclusive of the second parasitic capacitance.

6. The wafer of claim 5, wherein when select signal has the second value the switching circuit is directed to bias the second structure with a steady potential, whereby the test signal provides a measure of both the first parasitic capacitance and the second parasitic capacitance.

7. The wafer of claim 6, wherein when select signal has the second value the second structure is biased to have a steady potential equal to approximately that of the substrate.

8. The wafer of any of claims 1 - 7, wherein the parasitic capacitance test structure is located in a scribe line of the wafer.

9. A wafer having a plurality of parasitic capacitance test structures, where a single test structure is selectable by means of one or more select signals, the test structure comprising:

a single reference structure, wherein the reference structure comprises a switching circuit;

a plurality of first structures overlying a substrate each coupled to respective one of a plurality of first probe pads, wherein each of the plurality of first structures comprises a switching circuit connected to a device under test (DUT), wherein a test signal impressed on each of the first probe pads is operable to provide a measure of a parasitic capacitance associated with a respective one of the DUTs; and

wherein the switching circuit of the reference circuit and the switching circuit of each of the first structures all have approximately a same topology and size, whereby the single reference circuit is used to improve the resolution of every one of the plurality of first test structures.

10. A method for testing a partially fabricated wafer, comprising the steps of:

a) providing a plurality of devices under test (DUT) overlying a substrate of the wafer where a single DUT is selectable by means of one or more select signals and a second structure located in proximity to the DUT;

b) forming a first virtual test structure by biasing the second structure to have a first

electrical state;

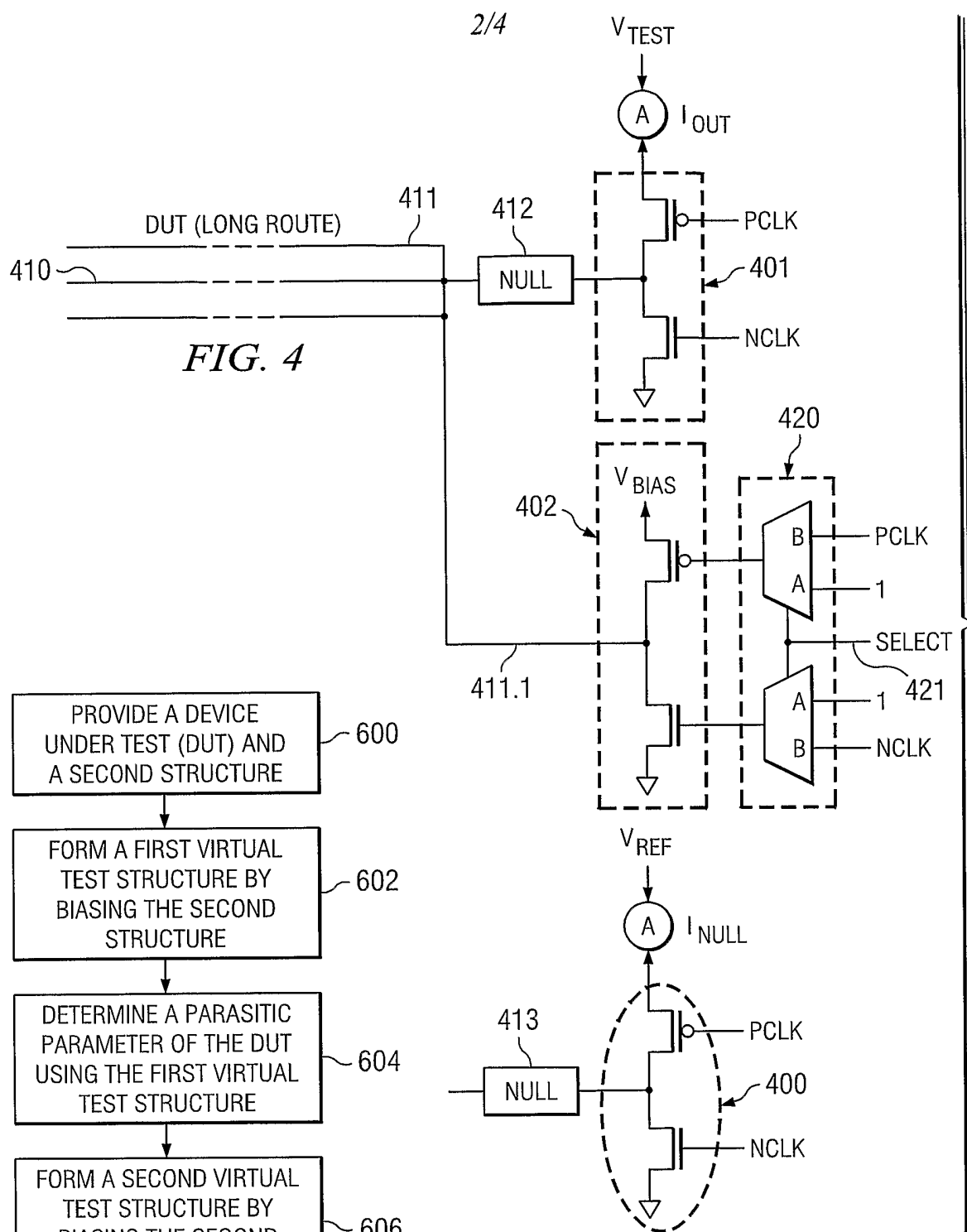
c) determining a first parasitic parameter associated with the first virtual test structure by applying a signal to the DUT while the second structure is in the first electrical state and measuring a response that is indicative of the first parameter;

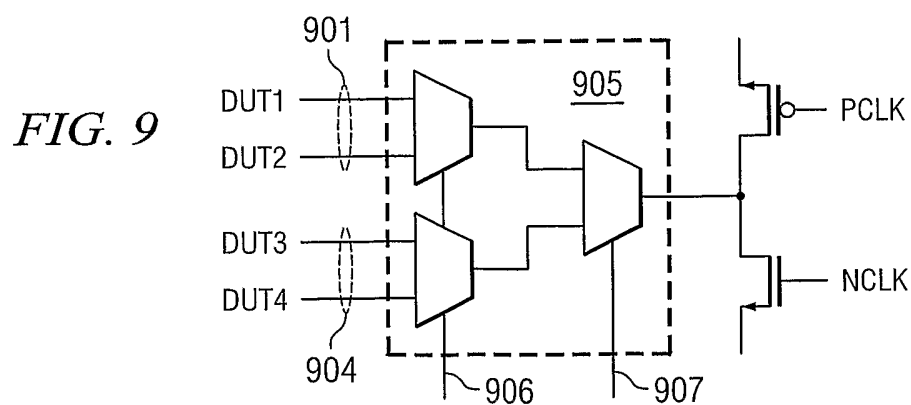
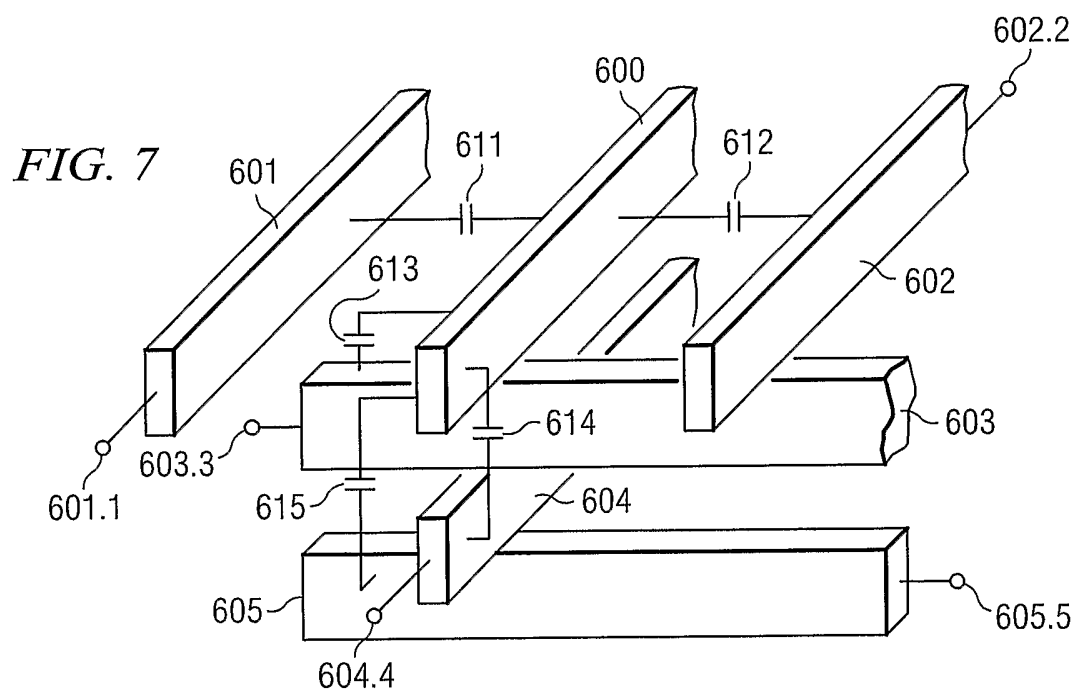
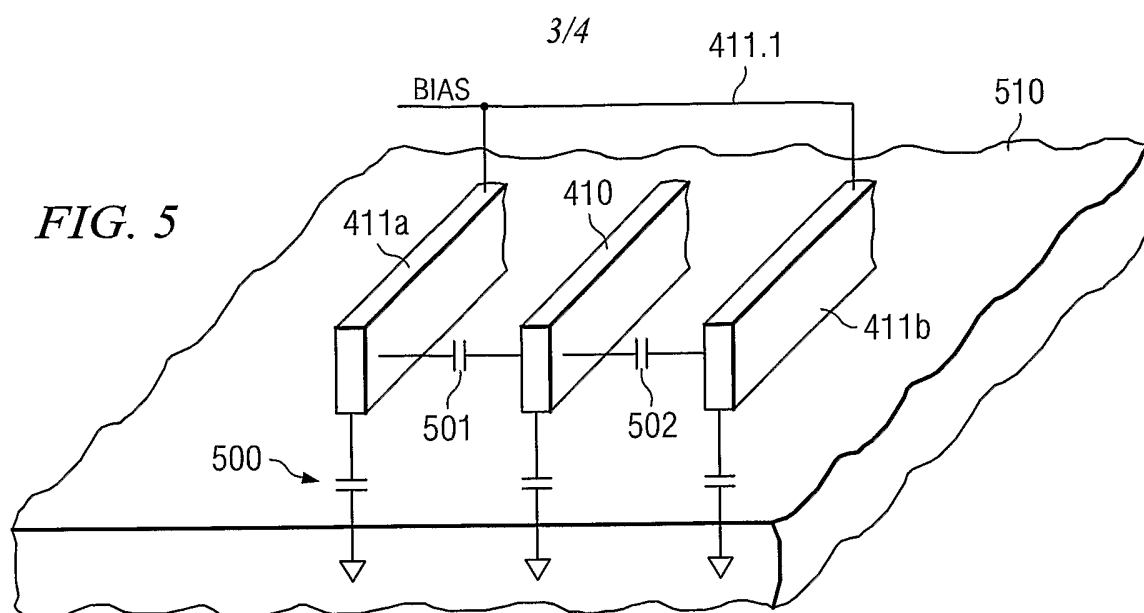
d) forming a second virtual test structure by biasing the second structure to have a second electrical state; and

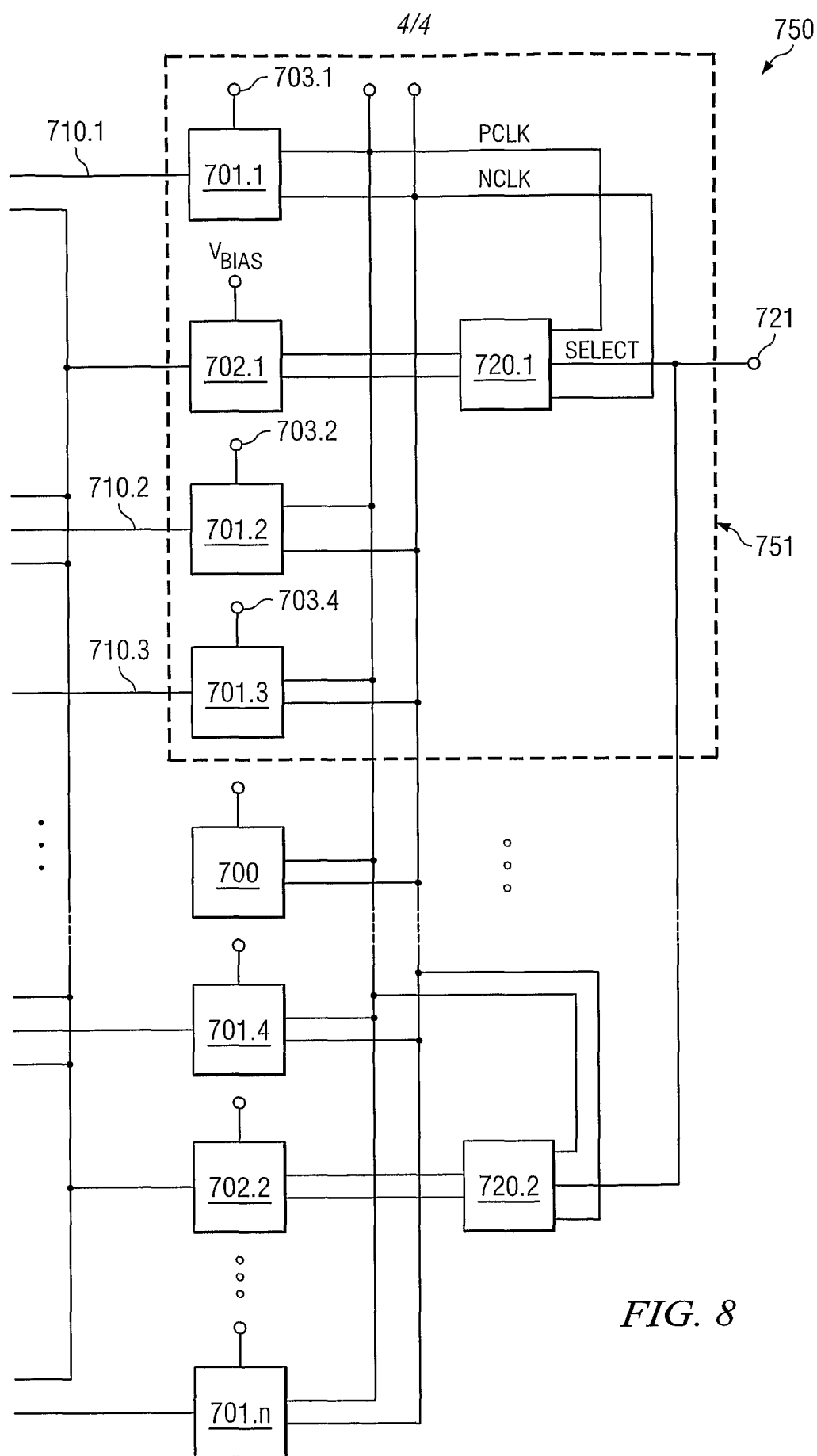
e) determining a second parasitic parameter associated with the second virtual test structure by applying a signal to the DUT while the second structure is in the second electrical state and measuring a response that is indicative of the second parameter.

11. The method of claim 13, wherein step b) biases the second structure with a steady voltage and step d biases the second structure with a periodic voltage.

12. The method of claim 13 or 14, wherein a plurality of second structures are located in proximity to the DUT, and wherein step b biases all of the plurality of structures to have the first electrical state and step d biases a portion of the plurality of structures to have the first electrical state and a different portion of the plurality of structures to have the second electrical state.

**FIG. 6**





INTERNATIONAL SEARCH REPORT

International application No.

PCT/US05/42353

A. CLASSIFICATION OF SUBJECT MATTER IPC: G01R 31/02(2006.01),31/26(2006.01) USPC: 324/761,765;438/18 According to International Patent Classification (IPC) or to both national classification and IPC																				
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) U.S. : 324/158.1,72.5,754,755,761,762,761,765;438/18;439/103,109,219,482,620;174/207;257/48 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)																				
C. DOCUMENTS CONSIDERED TO BE RELEVANT <table border="1"> <thead> <tr> <th>Category *</th> <th>Citation of document, with indication, where appropriate, of the relevant passages</th> <th>Relevant to claim No.</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>US 5,212,454 A (PROEBSTING) 18 May 1993 (18.05.1993), column 8, lines 10-25.</td> <td>1-10</td> </tr> <tr> <td>A</td> <td>US 6,872,583 B1 (WU) 29 March 2005 (29.03.2005), see Abstract.</td> <td>1-10</td> </tr> <tr> <td>X</td> <td>US 6,700,399 B1 (SAVITHRI) 2 March 2004 (02.03.2004), claims 1-10 and column 9, lines 8-10.</td> <td>1-10</td> </tr> </tbody> </table>			Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.	A	US 5,212,454 A (PROEBSTING) 18 May 1993 (18.05.1993), column 8, lines 10-25.	1-10	A	US 6,872,583 B1 (WU) 29 March 2005 (29.03.2005), see Abstract.	1-10	X	US 6,700,399 B1 (SAVITHRI) 2 March 2004 (02.03.2004), claims 1-10 and column 9, lines 8-10.	1-10						
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☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.																				
<table border="0"> <tr> <td colspan="2"> * Special categories of cited documents: </td> <td> "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention </td> </tr> <tr> <td> "A" document defining the general state of the art which is not considered to be of particular relevance </td> <td> "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone </td> <td></td> </tr> <tr> <td> "E" earlier application or patent published on or after the international filing date </td> <td> "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art </td> <td></td> </tr> <tr> <td> "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) </td> <td> "&" document member of the same patent family </td> <td></td> </tr> <tr> <td> "O" document referring to an oral disclosure, use, exhibition or other means </td> <td></td> <td></td> </tr> <tr> <td> "P" document published prior to the international filing date but later than the priority date claimed </td> <td></td> <td></td> </tr> </table>			* Special categories of cited documents:		"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention	"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone		"E" earlier application or patent published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art		"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family		"O" document referring to an oral disclosure, use, exhibition or other means			"P" document published prior to the international filing date but later than the priority date claimed		
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"P" document published prior to the international filing date but later than the priority date claimed																				
Date of the actual completion of the international search 09 March 2006 (09.03.2006)		Date of mailing of the international search report 23 MAR 2006																		
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201		Authorized officer <i>Lydia Devel For</i> Russell M. Kobert Telephone No. 571-272-1650																		

INTERNATIONAL SEARCH REPORT

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Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☒ Claims Nos.: 11 and 12
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
Please See Continuation Sheet
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of any additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

- Remark on Protest**
- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

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Continuation of Box II Reason 2:

Claims 11 and 12 are objected to under PCT Rule 66.2(a)(v) as lacking clarity under PCT Article 6 because claims 11 and 12 are indefinite for the following reason(s):

Claim 11 is dependent on non-existing claim 13.

Claim 12 is dependent on non-existing claims 13 and 14.