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(54) A multichannel television signal recording system

(57) Each line of luminance information (Y) is recorded in a first track (Y) on a magnetic tape (620). Each corresponding line of chrominance information comprises two chrominance components (I, Q), which are time compressed in a compressor (20). The compressor includes switching means controlled to apply both components (I, Q) of each line to a second track (I, Q) on the tape (620).

In this way cross-modulation of the chrominance signals is reduced, and vertical resolution of color is maintained.

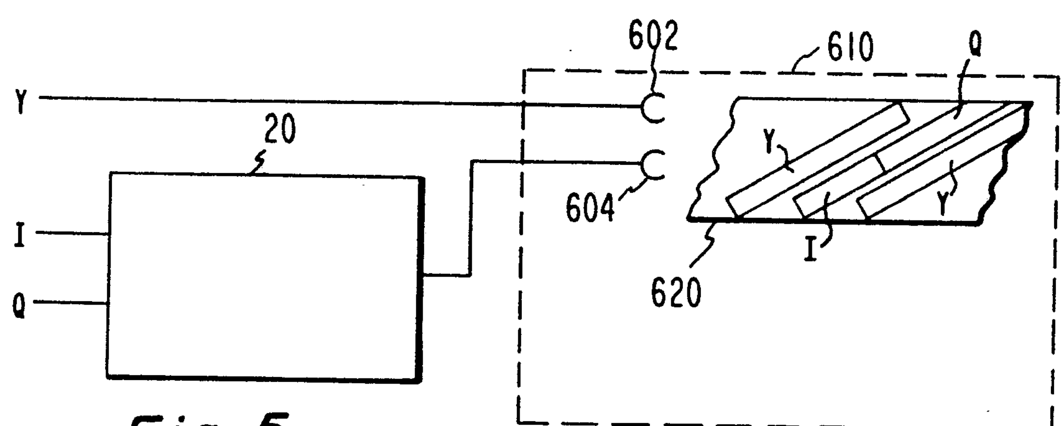

Fig. 5

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The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

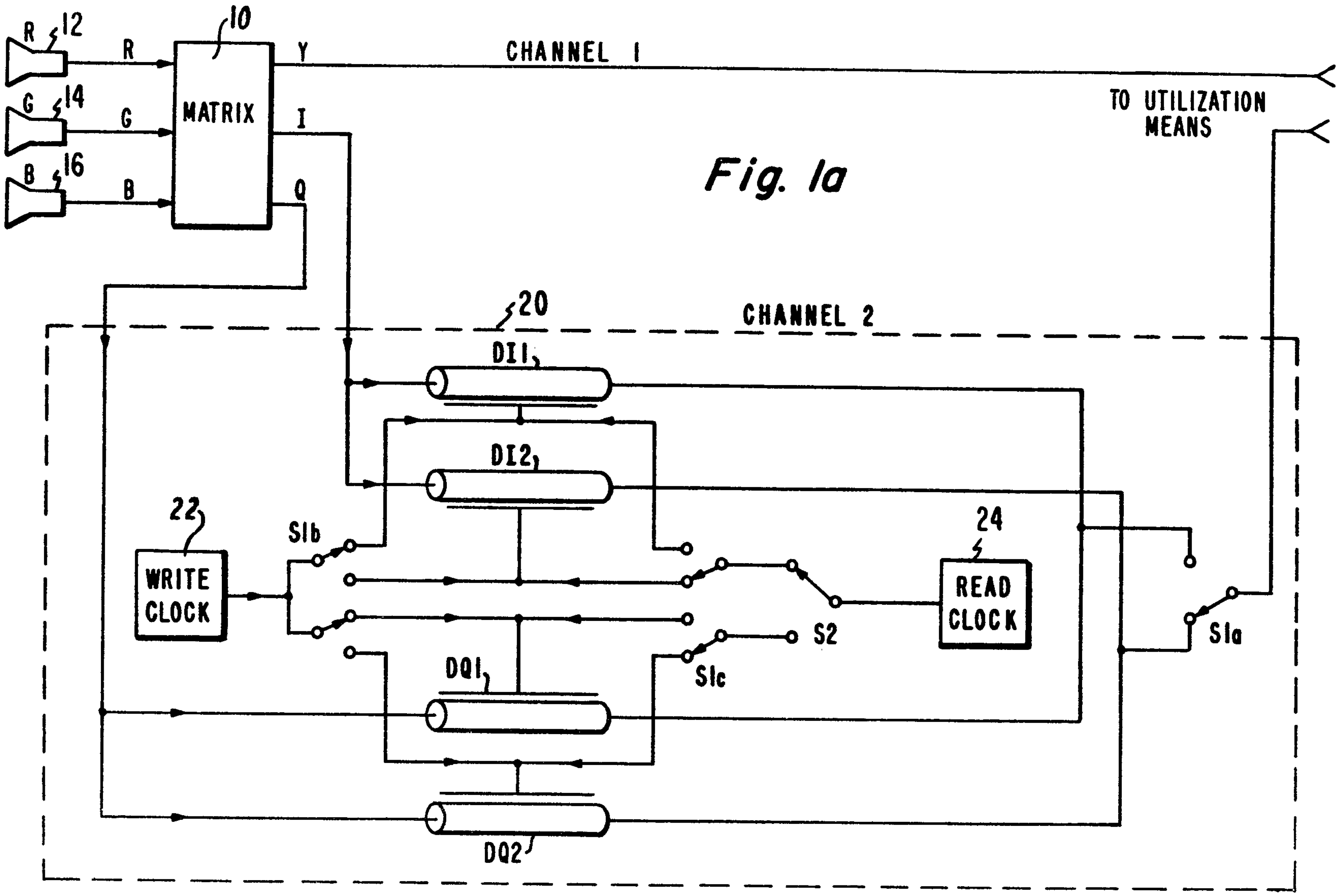
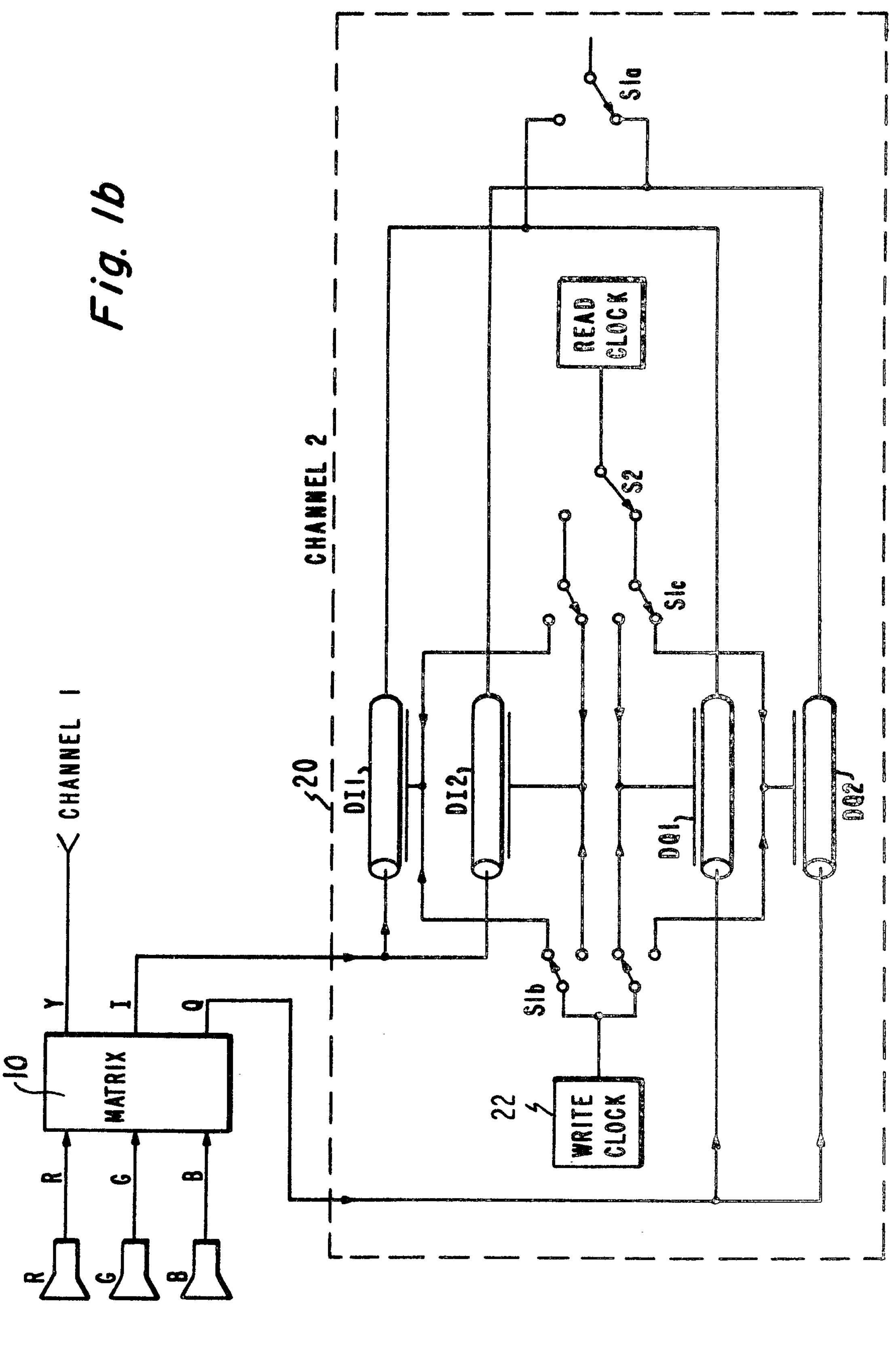

R
12
G
14
B
16
R
G
B
10
MATRIX
Y
I
Q
CHANNEL 1
TO UTILIZATION MEANS
20
CHANNEL 2
DI1
DI2
DQ1
DQ2
22
WRITE CLOCK
S1b
S1c
S2
24
READ CLOCK
S1a

Fig. 1a

Fig. 1b


CHANNEL 1
CHANNEL 2
MATRIX
10
Y
I
Q
R
G
B
20
DI1
DI2
DQ1
DQ2
READ CLOCK
WRITE CLOCK
22
S1a
S1b
S1c
S2

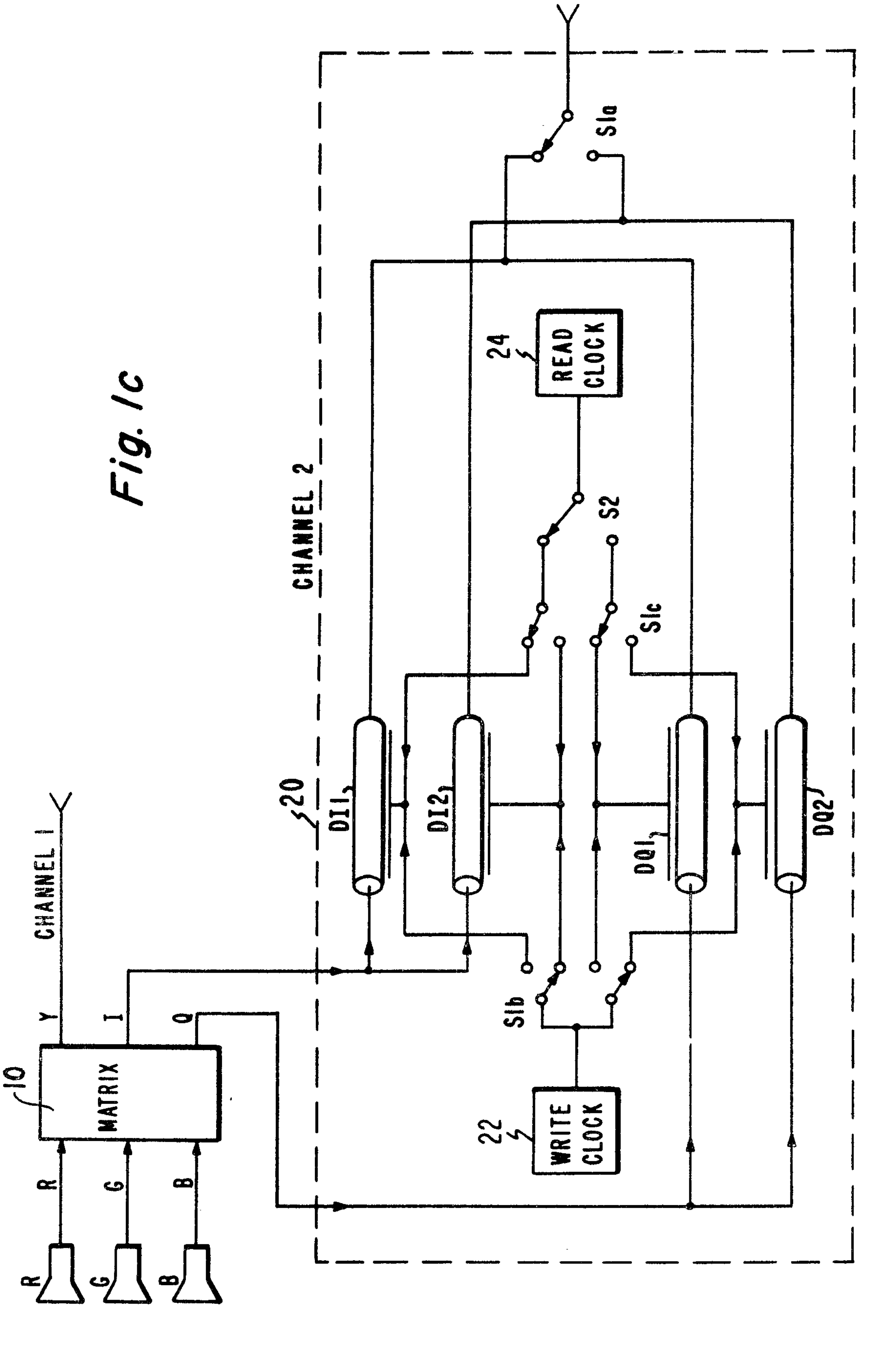

CHANNEL 1
CHANNEL 2
10
MATRIX
R
G
B
Y
I
Q
20
DI1
DI2
DQ1
DQ2
22
WRITE CLOCK
24
READ CLOCK
S1a
S1b
S1c
S2

Fig. 1c

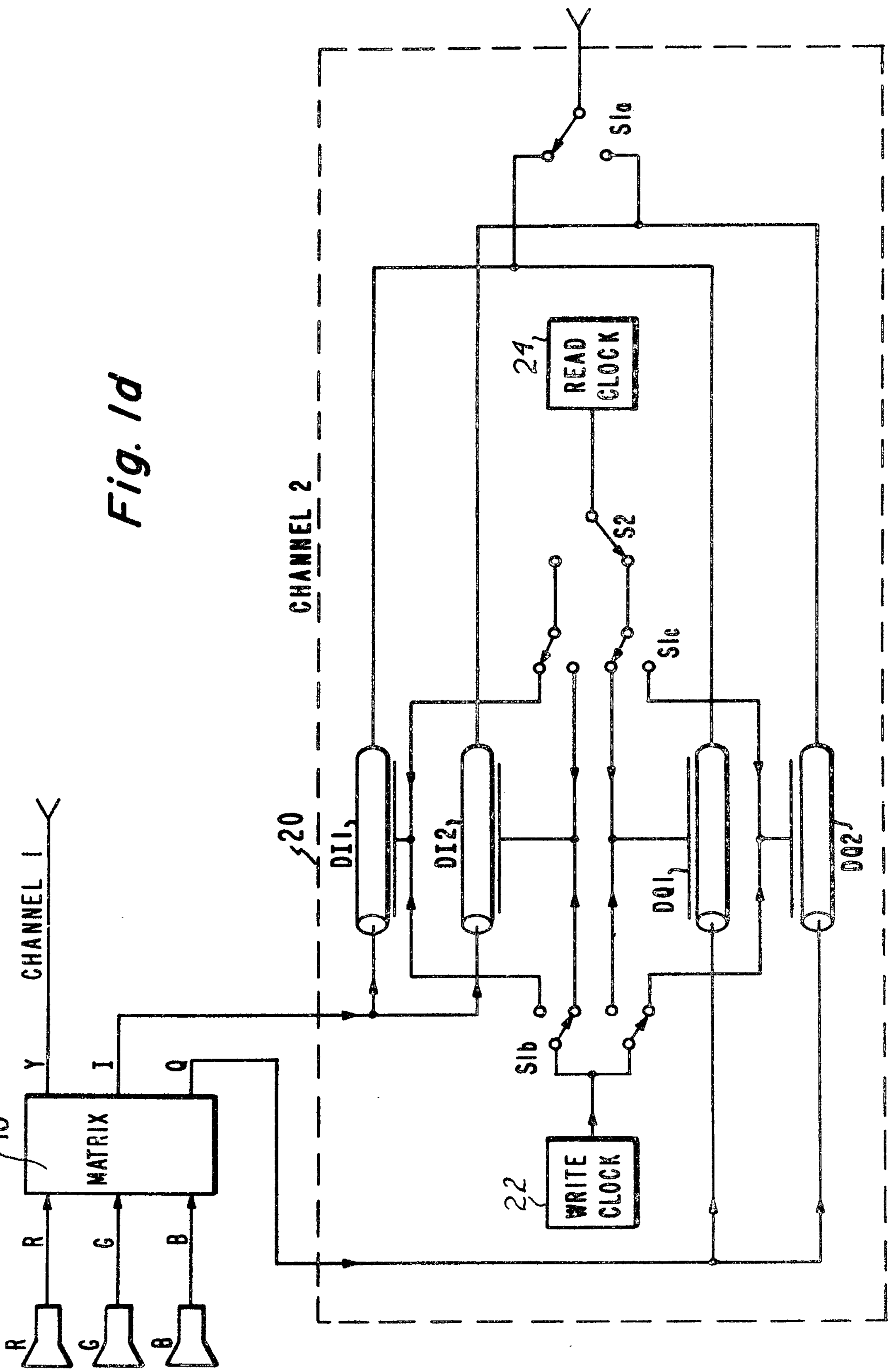

CHANNEL 1
CHANNEL 2
10
MATRIX
Y
I
Q
R
G
B
20
DI1
DI2
DQ1
DQ2
S1a
S1b
S1c
S2
24
READ CLOCK
22
WRITE CLOCK

Fig. 1d

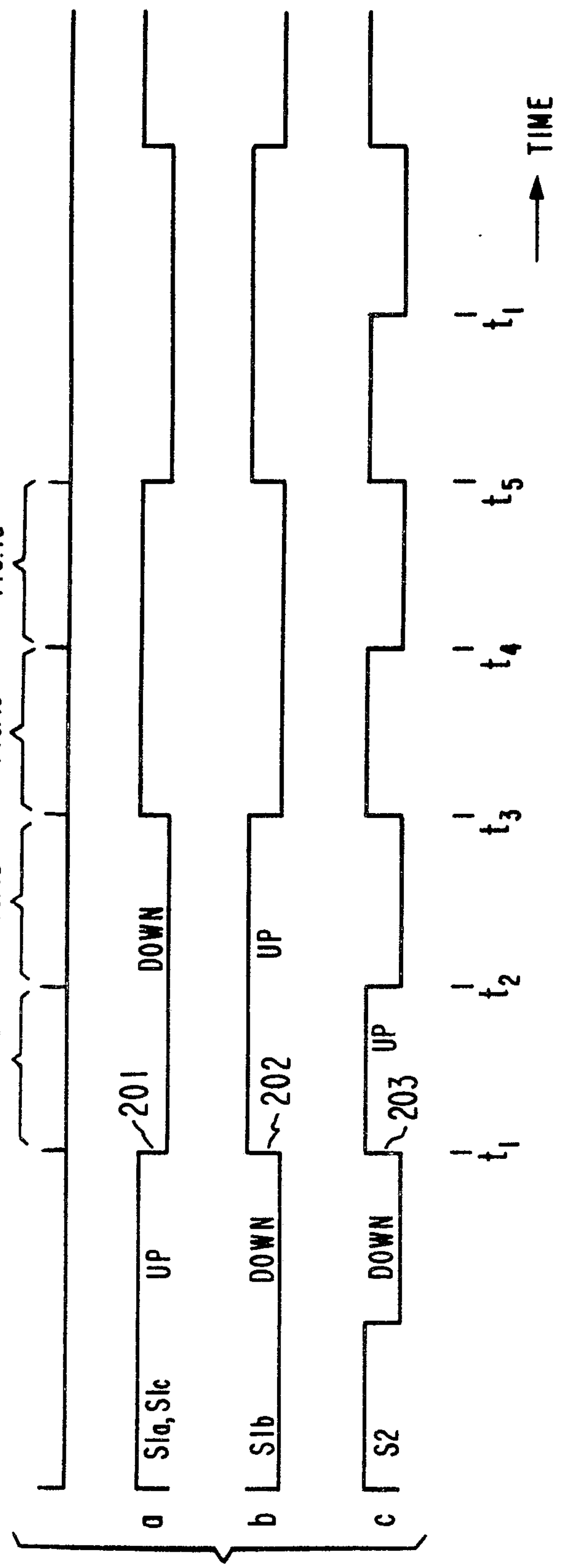


FIG. 1a
FIG. 1b
FIG. 1c
FIG. 1d
a
b
c
S1a, S1c
UP
DOWN
201
S1b
DOWN
UP
202
S2
DOWN
UP
203
t1
t2
t3
t4
t5
t1
TIME

Fig. 2

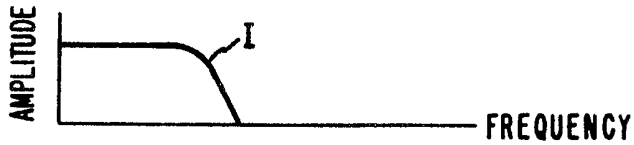


Fig.3a

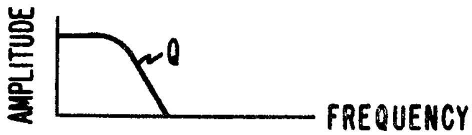


Fig. 3b

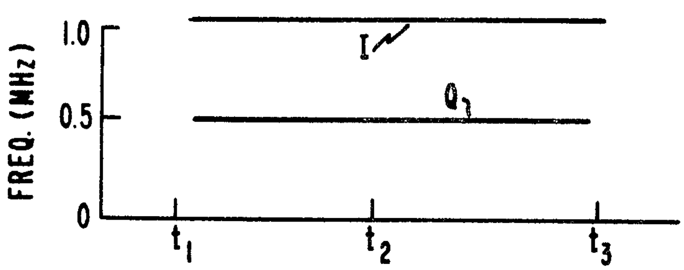


Fig.3c

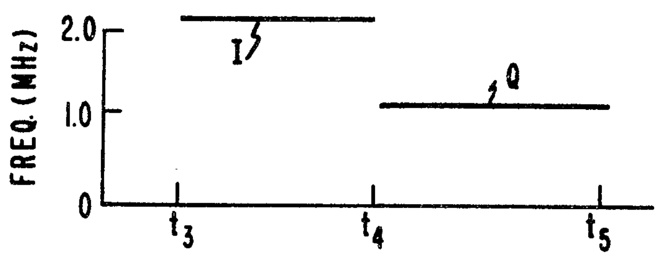


Fig 3d

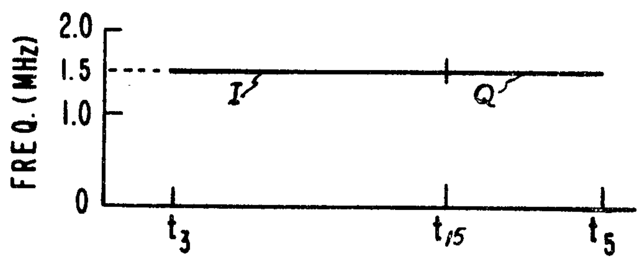


Fig. 3e

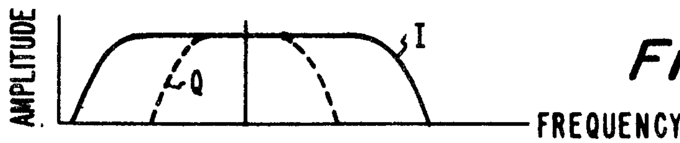


Fig. 3f

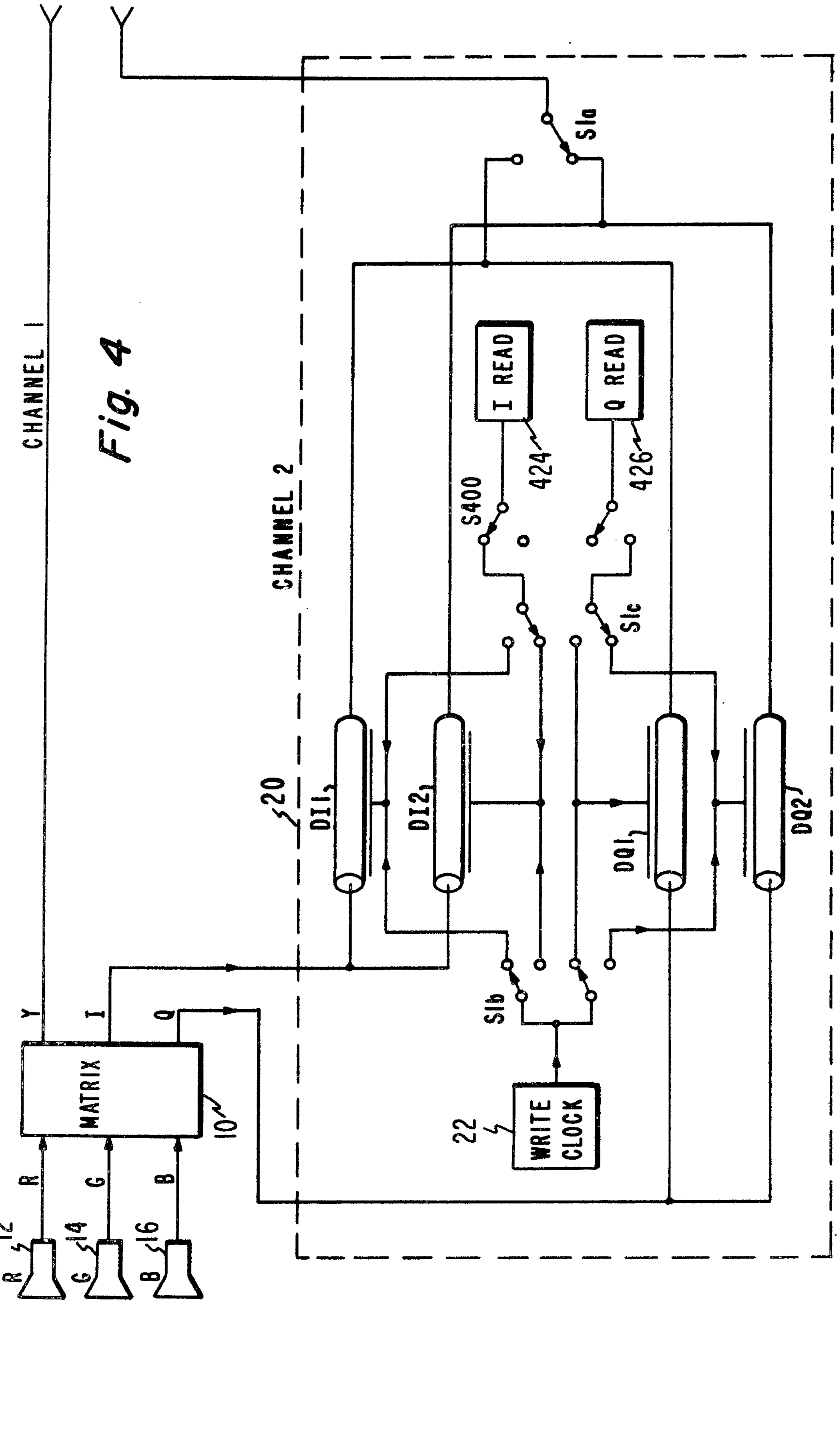

CHANNEL 1
CHANNEL 2
MATRIX
WRITE CLOCK
I READ
Q READ
S1a
S1b
S1c
S400
424
426
DI1
DI2
DQ1
DQ2
20
22
10
12
14
16
R
G
B
Y
I
Q

Fig. 4

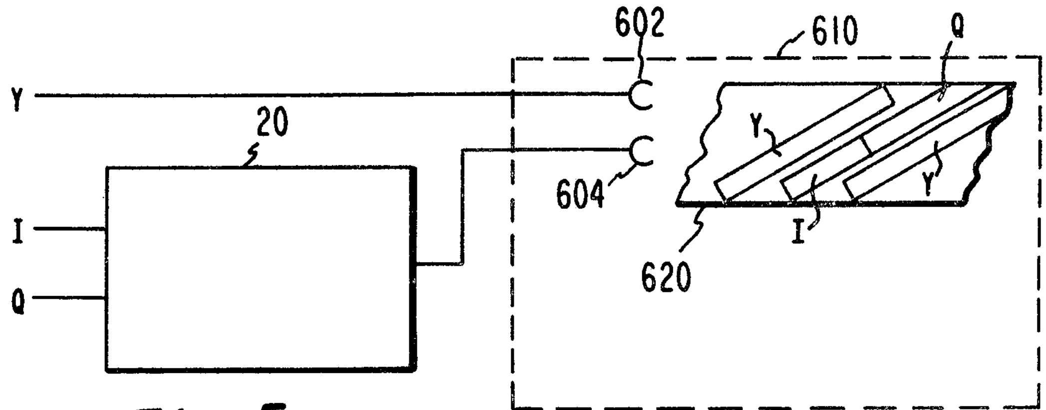


Fig. 5

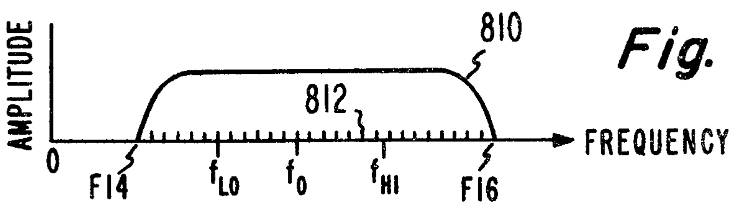


Fig. 6

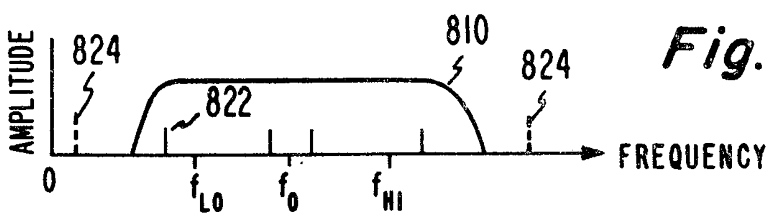


Fig. 7

SPECIFICATION

Multichannel television signal recording system

This invention relates to a multichannel television signal recording system.

In magnetic recording of color television signals by video tape recorders, the record or playback head may occasionally fail to come into contact with the magnetic oxide coating because of variations in tape tension, build up of dirt on the heads and the like. This may cause a reduction in the amplitude of the signal transduced from the tape to the playback head, and may result in objectionable distortion. It is known to frequency-modulate a carrier with the video information to be recorded. Such frequency modulation of the signal translates amplitude changes of the video signal into frequency changes of the carrier. An amplitude limiter coupled to receive the frequency-modulated signal strips away amplitude variations resulting from imperfect head contact, and the frequency-modulated signal when demodulated has an improved signal-to-noise compared with the case of direct recording.

When color television signals encoded in, for example, a standard NTSC manner including luminance components and chrominance components quadrature-modulated onto a color subcarrier are recorded, the total frequency bandwidth of the video signal is large. When it is desired to record such as NTSC signal, it is found that the total bandwidth of the NTSC signal is so large that the sidebands of the frequency-modulated carrier extend over a greater frequency band than can be encompassed within the FM channel of the recorder. Consequently, the "color under" system has been used in the past. In this system, the color subcarrier, quadrature modulated with chroma components, is directly recorded at a low frequency on the same tape track with an FM carrier modulated by video luminance information. To improve linearity, the directly recorded chrominance information is recorded with the aid of a bias signal. To prevent interaction between the bias signal and the frequency-modulated carrier, the FM carrier is often used as the bias signal. While such an arrangement allows recording of a color television signal on a single track of a video tape recorder, certain problems exist, such as poor SN of the chrominance signal, crosstalk between the two quadrature-modulated color signals, and limited frequency bandwidth which necessitates reduction of the desired bandwidth in either the chrominance or luminance information, or possibly both. Furthermore, the FM luminance carrier cannot be modulated to the maximum possible amount because maximum modulation drives the recording medium into saturation, adding distortion to the directly recorded chrominance information.

In order to improve the quality of the television signal to broadcast standards, the luminance information may be recorded on a first track of the tape by the use of a frequency-modulated carrier, while at the same time recording the quadrature-modulated chrominance information onto a second track of the tape adjacent the first. The chrominance information is modulated onto a frequency-modulated carrier for improved signal-to-noise. It has been found, however, that broadcast quality may not be achieved even in such a system using two wideband channels for the recording of the video information. Furthermore, it has been found that cross-modulation occurs between the two components of the chrominance signal.

Figure 6 illustrates an amplitude-frequency diagram. In Figure 6, a frequency F0 illustrates the rest frequency of a frequency-modulated carrier. FLO and FHI represent the lower and upper deviation frequency limits, respectively. An envelope 810 illustrates the amplitude-frequency characteristic of a transmission channel generally including, for example, a tape recorder channel. At frequencies F14 and F16 the response of the channel is reduced due to filters, inherent frequency limitations and the like. A series of spectral lines 812 illustrates generally the distribution of energy which results from modulating the carrier with a relatively low-frequency video signal. Many spectral lines appear, the amplitude of which depends upon the amplitude of the modulating signal. Figure 7 illustrates the response of the same system modulated with a relatively high-frequency video signal. Very few spectral lines 822 appear within the passband defined by curve 810. Other spectral lines illustrated as 824 are cut off and do not appear. It has been established that the signal-to-noise ratio of a frequency-modulated transmission channel such as that described is degraded at higher modulating frequencies. This may be explained by the loss of many of the spectral lines associated with the information of the signal in the case of the high-frequency signal, as compared with the low-frequency situation in which large numbers of spectral lines are carried through the channel.

In order to obtain improved characteristics for a two-channel tape recorder or other transmission system, it is desirable to reduce the frequency of the signal modulating the chrominance channel. Comparison of the bandwidth of the baseband I and Q signals of Figures 3a and 3b with the bandwidth of the I and Q signals quadrature-modulated onto a subcarrier, as illustrated in Figure 3f, reveals that each of the baseband signals alone has a lesser bandwidth than does the modulated signal. The frequency bandwidth of the signal modulating the chrominance channel may be reduced by alternately modualting the frequency-modulated carrier in the chrominance signal channel with one of the two chrominance signals representing the chrominance information. For example, if the chrominance information is represented by I and Q signals, where the I signal has a frequency bandwidth of 1 MHz and the Q signal has a frequency bandwidth of 0.5 MHz, each of these signals is alternately modulated onto the carrier for coupling into the channel. Alternation, however, results in a loss of I signals during that interval in which Q signals are being carried through the system, and similarly Q signals are lost during that interval in which I signals are being processed. Thus, there is a loss in signals similar to that which occurs in a SECAM system. In the SECAM system, the line-to-line alternation of the chrominance information results in a reduced vertical chrominance resolution which degrades the picture. U.S. Patent 4,163,248 issued July 31, 1979 to Heitemann describes a system for alternately processing luminance and chrominance information through a digital field store; the loss of information is concealed by repetition of the stored chrominance information during display of unstored luminance and repetition of stored luminance information during display of unstored chrominance.

A television transmission system, which may include a record, and having high signal-to-noise, low cross-modulation and resolution (no information loss) in the chrominance channel is desirable.

The present invention provides a multichannel television signal recording system as specified in the claims.

In the Drawings:

Figures 1a—1d show in various operating states a signal processor for use in an embodiment of the invention;

Figure 2 illustrates a state diagram useful in understanding the operating cycle;

Figure 3 illustrates bandwidths of signals and the time sequence of the signals useful in understanding certain aspects of the invention;

Figure 4 is a diagram in block and schematic form of another signal processor having certain bandwidth advantages.

Figure 5 illustrates a two-channel recording system including a tape record according to the invention; and

Figures 6 and 7 illustrate amplitude-frequency diagrams and spectra useful in understanding the advantages of the invention.

Figure 1a illustrates a generalised transmission system to which color television signals are applied. In this instance, the television signals are generated by a matrix 10 which receives red (R), green (G) and blue (B) baseband video signals from individual video cameras 12, 14 and 16, respectively. Matrix 10 processes the plurality of baseband components defining luminance and chrominance information to produce luminance (Y) information which is coupled directly by a first channel of the transmission system to a utilizing means (not shown). Matrix 10 also forms further baseband components conventionally known as I and Q signals representative of the chrominance information being processed, and couples them to a signal processor 20 of a second channel of the transmission system. The I signals are coupled in parallel to the inputs of clocked delay lines DI1 and DI2 of processor 20 for further processing, and the Q signals are coupled in parallel to the inputs of further clocked delay lines DQ1 and DQ2. (Delay lines are designated generally by the letter D, those processing I information are also designated by the letter I, those processing Q information by the letter Q.) The outputs of delay lines DI1 and DQ2 are coupled in parallel, and the outputs of delay lines D12 and DQ2 are coupled in parallel. A single-pole, double-throw switch S1A switches alternately between the parallel outputs of the delay lines for selecting the output signal of processing portion 20 of the transmission channel. The remainder of processing portion 20 of the second transmission channel is a clocking arrangement by which sequential processing of the I and Q signals in the delay lines is accomplished without loss of information and the consequent loss of resolution.

A write clock generator 22 is coupled by a double-pole double-throw switch S1B to pairs of delay lines DI, DQ for clocking the delay lines to cause signals to be coupled therethrough. For example, at the time illustrated in Figure 1, switch S1B couples the write clock signal to DI1 and DQ1. A read clock generator 24 is also coupled to delay lines DI, DQ by way of a double-pole double-throw switch S1C and a single-pole double-throw switch S2. A switch drive means (not shown) derives swtiches S1A, S1B, and S1C synchronously at the horizontal rate and drives switch S2 at twice the horizontal rate. Switch S1 toggles at a time during the horizontal blanking interval and switch S2 toggles synchronously with switch S1 and also at a time near the center of each horizontal line interval.

Clocked delay lines D in the emobidment of Figure 1 may include charge-transfer devices of the type known as charge-coupled devices (CCD) which are well known in the art. Each CCD consists of a number of cells which when clocked cause a sequential transfer from cell to cell of charge packets representing analog signals. Thus, each delay line may be considered a sampled analog delay line, the sample rate of which is determined by the clock rate and the delay of which is determined by the clock rate of the number of cells. The clocking rate of generator 22 is selected based upon the maximum frequency which may be expected in the signals being processed through the delay lines so as to provide a faithful reproduction of the signal as determined by Nyquist's criterion. For example, the minimum frequency of write clock generator 22 might be selected to be twice the maximum frequency expected to be processed through a delay line. The number of cells in each delay line D is selected to have a propagation delay of 1H, which is sufficient delay to store an I or Q signal occurring during one horizontal line. Read clock generator 24, in a particular embodiment of the invention, has its frequency selected so as to allow signal to propagate through a delay line at twice the writing rate, thereby allowing the signal representing an entire horizontal line of chrominance information to be read out of a delay line during an interval equal to one-half of a horizontal line.

Prior to time T1, as illustrated in Figure 2, DI2 and DQ2 were clocked at the write rate so as to store the entire I and Q signals, respectively, for the preceding horizontal line. Delay lines DI1 and DQ2 contain material unsuitable for transmission. At time T1, which may occur during a horizontal blanking interval or during a transition from one line to the next, the condition of switches S1 and S2 changes as shown by waveforms 201, 202 and 203 of Figures 2a, 2b and 2c, respectively. A high condition of any of waveforms 201—203 represents an "up" condition of the switch associated with that waveform. Thus, in the interval between time T1 and T2 of Figure 2, switches S1A and S1C are in a "down" position as represented by a low condition of waveform 201; switch S1B is in an "up" position as represented by a high condition of waveform 202; and switch 2 is in an "up" position as represented by waveform 203. Thus, the condition of the switches of Figure 1 in the interval T1—T2 is that condition represented in Figure 1a. Similarly, the condition of the switches in the interval T2—T3 is that condition illustrated in Figure 1b, and Figures 1c and 1d represent the condition of the switches in the intervals T3—T4 and T4—T5, respectively. The condition of the switches repeats cyclically.

In the interval preceding time T1, as mentioned, DI2 and DQ2 were clocked by write clock generator 22 so as to store in DI2 and DQ2 a sampled analog version of the I and Q signals occurring in the preceding line. DI1 and DQ1 contain unsuitable information. At time T1, the switch configuration becomes that of Figure 1a, as indicated by Figure 2. Write clock generator 22 becomes coupled at time T1 and DI1 and DQ1, which begin clocking at the writing rate to progressively store the I and Q signals occurring in the interval T1—T2. The unsuitable material stored therein is simultaneously clocked out, but the unsuitable material is decoupled from the output of transmission processor 20 at switch S1A and does not affect the output signal. Delay line DQ2 remains in a passive storage mode in interval T1—T2. Also in the interval T1—T2, read clock generator 24 is coupled to delay line DI2, and the I signal stored therein is clocked out at twice the rate at which it was clocked in. The signal clocked out of DI2 is coupled by switch S1A to the output of transmission processor 20. While DI2 is clocking out, the I signal at its input is also clocked into cells of delay line DI2. However, the current line I information is not coupled to the output of processor 20 because at the moment that the first of the current line information would begin to exit from DI2, switch drive signal 203 takes a transition representing the switching of S2 to produce the configuration shown in Figure 1b.

As illustrated in Figure 1b, write clock generator 22 continues to be coupled during interval T2—T3 to DI1 and DQ1 for loading or storing the current line I and Q information. However, no clocking signals at all are coupled to DI2, and it becomes passive and retains the stored I information from the first half T1—T2 of the first horizontal line T1—T3. Switch S1C couples read clock 24 to previously passive DQ2. DQ2 contains the Q information from the horizontal line preceding time T1. Beginning at time T2, this I signal is clocked to the output of transmission processor 20. As in the case of DI2, the clocking out of the stored information causes the storage in DI2 of Q information from the current line. However, Q information from the current line cannot begin to exit from DQ2 until after time T3. At time T3, the first horizontal line ends and the second horizontal line begins.

At time T3, the condition of the switches of Figure 1 changes as indicated by waveforms 201—203, and in the interval T3—T4 the condition is as illustrated in Figure 1c. In Figure 1c, DI2 and DQ2 are coupled to the write clock and their parallel outputs are decoupled from the output of processor 20. Consequently, DI2 begins to store currently generated I signal and DQ2 begins to store currently generated Q signal. The unusable half-line information stored therein during the previous line is clocked out as current signal is stored. During the interval T3—T4, DQ1 is not clocked and merely retains the stored Q information from horizontal line T1—T3. DI2, however, is coupled to read clock generator 24, and begins to read out the I information stored during line T1—T3 in a manner similar to that already described. At time T4, when all of the I information relating to horizontal line T1—T3 has been read out, but before I information stored subsequent to time T3 has been read out, the switch configuration again changes to that represented by waveforms 201—203 of Figure 2 in the interval T4—T5. This configuration is illustrated in Figure 1d. In Figure 1d, it will be recognized that the configuration of Figure 1d occurring in the interval T4—T5 allows loading in DI2 and DQ2 of the I and Q signals then being generated, and allows DQ1 to be read so as to couple to the output of processor 20 the Q signal stored during interval T1—T3 of the preceding horizontal line. At time T5, then, DI2 and DQ2 are loaded with information which is not useful for transmission and DI1 and DQ1 are loaded with the I and Q, respectively, information from the preceding line. This will be recognized as the same condition as that which preceded time T1, and that the cycle as described can repeat.

Thus, the arrangement of Figure 1 represents a two-channel transmission system in which the luminance information is transmitted on one channel and the chrominance information is represented by baseband I and Q signals which are generated concurrently, stored and then time compressed by a factor of 2:1 for sequential coupling to the second channel of the transmission system. This transmission system maintains high resolution and has improved signal-to-noise. It should be noted that operation of the delay line D at twice the clock rate for time compression also results in a doubling of the signal frequencies associated with the I and Q signals, and this in turn affects the minimum allowable bandwidth of channel 2 of the arrangement of Figure 1.

Commonly, the I chrominance signal has a greater signal bandwidth than the Q signal. This is illustrated in Figures 3a and 3b. Over the interval T1—T3, the bandwidth remains constant as illustrated in Figure 3c. The I signal has a 1.0 MHz bandwidth and the Q signal has a 0.5 MHz bandwidth. Figure 3d illustrates the result of time-compressing the I and Q signals of Figures 3a—3c equally for sequential presentation in the interval T3—T5. The I signal presented in the interval T3—T4 has a 2 MHz bandwidth representing the doubling of the 1 MHz bandwidth as it was generated, and the doubled frequency of the Q signal is only 1.0 MHz. Consequently, in the interval T4—T5 the bandwidth of channel 2 of the transmission system is under-utilized. By appropriate selection of the duration of the read-out interval and the read-out clock frequency, the bandwidth interval and the read-out clock frequency, the bandwidth of the time-compressed I and Q signals can be made equal, as illustrated in Figure 3e. If the interval T3—T15 during which the I signal is read-out is two-thirds of the available read-out time and the time interval T15—T5 in which the Q signal is read out is one-third the available time, the bandwidth of the I signal as generated is multiplied by 3/2 to 1.5 MHz as illustrated in Figure 3e and the Q signal is multiplied by 3. With such an apportionment of the compression based on the signal bandwidth, the channel bandwidth use is maximized.

Figure 4 illustrates an arrangement by which the I and Q signal as sequentially presented for transmission may have the same bandwidth. In Figure 4, elements corresponding to those of Figure 1 are provided with the same reference numerals. Reference to Figure 2 and to the description of the operation of Figure 1 will reveal that when waveform 203 is high representing an up condition for switch 2, I is being read, and when S2 and waveform 203 are down, Q is being read. Consequently, a double-pole double-throw (DPDT) switch S400 may be substituted for SPDP switch S2 of Figure 1a. A first half of switch S400 connected as shown in Figure 4 is connected to an I read clock generator 424 and a second pole is connected to a Q read clock generator 426. Generators 424 and 426 are at different frequencies. The I read clock is selected to read-out I information from delay lines DI in 2/3 of a horizontal line and Q read clock generator 426 has a frequency selected to read Q information from the DQ delay lines in 1/3 of a line. Thus, in the example given (I bandwidth as generated of 1 MHz and 0.5 MHz for Q and with 2/3 of the transmission time devoted to I and 1/3 to Q), the I read clock would be at a frequency or rate of 1.5 times that of the write clock, while the Q read generator would be at a rate of 3 times the write clock rate.

The descriptions of the embodiments of Figures 1 and 4 are somewhat simplified in that it has been assumed that chrominance information is generated during the horizontal blanking interval. Generally speaking, this is not the case. Thus, the switching of switches S1, S2 and S400 may include a condition in which the delay lines D are not clocked at all, so as to avoid entering or coupling out information during the horizontal blanking interval. Also, it will be obvious to those skilled in the art that signals stored during the active portion of each horizontal line may be read-out during the interval including the blanking interval, thereby allowing a reduction in the bandwidth required for transmission of the sequential I and Q signals by the ratio of the active video time (approximately 53 microseconds) in each horizontal interval to the total horizontal interval (63.5 microseconds).

If the direction of the delay lines D of the transmission processors 20 of Figures 1 and 4 are reversed so that the signals proceed from right to left rather than from left to right, the encoders may be operated in reverse mode as decoders of the sequentially coded signals. Thus, for example, the I and Q signals sequentially encoded with equal times as described in conjunction with Figure 1 may be applied to the common terminal of switch S1A for sequentially writing into a DI and DQ delay line. Clock generator 22 clocks the information out in parallel to produce concurrent I and Q signals from the sequentially stored information.

It will be apparent that R—Y and B—Y chrominance signals representing chrominance information may be processed rather than I and Q signals by an arrangement such as that shown in Figure 1a. However, because the R—Y and B—Y signals ordinarily have equal bandwidths, the arrangement of Figure 4 would not be used unless unequal output bandwidths were desired.

Figure 5 illustrates a 2-channel transmission system in which a first channel carries a luminance signal and which a second channel receives I and Q signals which are processed by a signal processor 20 for sequential coupling of the I and Q signals to a second channel of the system. The first and second channels of the transmission system are coupled to first and second recording heads 602 and 604 in a video tape recorder 610. As illustrated in Figure 5, a tape 620 has scanned thereon in parallel tracks the Y information and the sequential I and Q information. Of course, the I and Q information may be presented in either sequence.

It will be obvious to those skilled in the art that the physical switches described for ease of understanding the invention may instead be solid-state equivalents such as those well-known in the art. Also, any signal source for producing baseband chrominance and luminance information may be used instead of the matrix shown. Instead of CCD delay lines D as illustrated in the embodiments shown, digital memories may be used.

As a further advantage of the described transmission system, the signal is scrambled by comparison with NTSC coded signals and cannot be received by an ordinary receiver. At the current state of the art, the CCD delay lines are expensive and this provides a measure of security from someone who might casually wish to develop a decoder. Thus, the described transmission channel may include a satellite transponding system used for restricted channels.

CLAIMS

1. A multichannel television signal recording system, wherein each line of luminance information is recorded separately from each corresponding line of chrominance information, and wherein said chrominance information comprises first and second signal components and comprising:

a first channel for recording each line of luminance information;

a second channel for recording each line of chrominance information, said second channel being subject to nonlinearities which may cause cross-modulation between said first and second signal components of said chrominance information when said first and second signal components are processed concurrently; and

switching means coupled to said second channel for alternating coupling both first and second signal components of each line of chrominance information for recording in said second channel whereby said first and second signal components are processed alternately rather than concurrently thereby eliminating said cross-modulation.

2. A system in accordance with claim 1, further comprising means for time compressing the said first and second signal components.

3. A system according to claim 2 wherein the time-compressing means are coupled to receive said first and second signal components as they are generated and adapted for generating time-compressed first and second signal components for recording during first and second sequential intervals; and include control clock means coupled to control input terminals of said controllable time-compression means for controlling the writing and reading rates of said controllable time-compression means, for controlling said time compression said clock means having frequencies selected so that the ratio of the duration of said first interval to said second interval equals the ratio of the bandwidth of said first signal component to the bandwidth of said second signal component.

4. A system according to claim 3 wherein said time-compressing means further comprises storage means coupled to said switching means for storing said first signal during said second intervals and for storing said second signal during said first intervals for preventing loss of resolution of said chrominance.

5. A system in accordance with claim 1 further comprising storage means coupled to said second channel and to said switching means for alternately storing said first and second signal components during those intervals in which said second and first signal components, respectively, are coupled for recording.

6. A system according to claim 1, 2 or 5 wherein said switching means couples said first and second signal components of said chrominance information alternately to said second channel during first and second sequential intervals, respectively, and wherein said first and second intervals are of equal duration.

7. A system in accordance with any preceding claim wherein said first and second signal components are R—Y and B—Y signals respectively.

8. A system in accordance with anyone of claims 1 to 6 wherein said first and second signal components are I and Q, respectively.

9. A system according to claim 1 further comprising a matrix for forming said first and second signal components whereby said first and second signal components have the same bandwidth.

10. A multichannel recording system for recording a television signal representing lines of luminance and chrominance information comprising:

a first input for receiving a luminance signal representing a line of the luminance information,

a second input for receiving a first chrominance signal, representing a corresponding line of a first component of the chrominance information and

a third input for receiving a second chrominance signal representing a corresponding line of a second component of the chrominance information,

means coupled to the first input for recording the luminance signal in a first track on a magnetic recording tape,

means coupled to the second and third inputs for concurrently and separately time compressing both the said first and second chrominance signals,

means for recording the time compressed chrominance signals in a second track on the tape, and

switching means for applying both the time compressed chrominance signals sequentially to the chrominance signal recording means.

11. A multichannel television signal recording system substantially as hereinbefore described with reference to Figure 5 or to Figure 5 together with Figs. 1a to 1d or to Figure 5 together with Figure 4.

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