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(71) Applicant: TEXAS INSTRUMENTS INCORPORATED [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(72) Inventors: SESTOK, Charles, Kasimer; 7900 Churchill Way, Apt. 11-205, Dallas, TX 75251 (US). MAGEE, David, Patrick; 1108 Krum Court, Allen, TX 75013 (US).

BARSUKOV, Yevgen, Pavlovich; 3257 Heatherbrook Ln, Richardson, TX 75802 (US).

(74) Agent: ABRAHAM, Ebby et al.; Texas Instruments Incorporated, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

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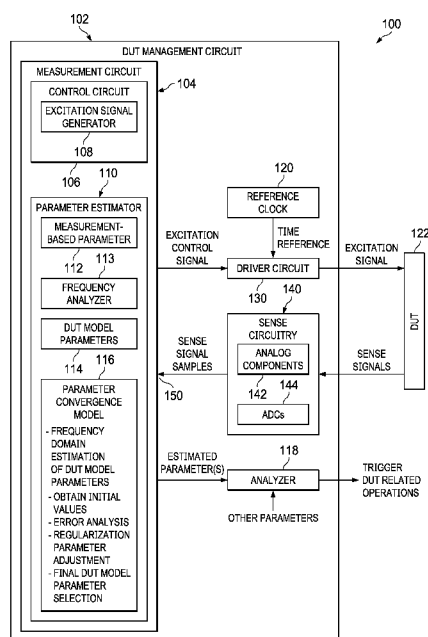


FIG. 1

(57) Abstract: A circuit (104) for determining device under test (DUT) model parameters (114) is described. The circuit (104) includes a parameter estimator circuit (110) configured to: obtain initial values for DUT model parameters (114) based on sense signal samples; execute a parameter convergence model (116) having a regularization parameter and a cost function that accounts for error residuals; and obtain final values for the DUT model parameters (114) by adjusting the regularization parameter in iterations of the parameter convergence model (116) as a function of cost function improvement until the parameter convergence model (116) converges to within a target tolerance.

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MEASUREMENT CIRCUIT HAVING FREQUENCY DOMAIN ESTIMATION OF DEVICE UNDER TEST (DUT) MODEL PARAMETERS

BACKGROUND

[0001] As new electronic devices are developed and integrated circuit (IC) technology advances, new IC products are commercialized. One example IC product for electronic devices is a microcontroller or measurement circuit configured to obtain measurements of a device under test (DUT), analyze the measurements to determine at least one parameter, and provide the parameter or related control signals for DUT management operations.

[0002] Many electronic systems include a battery unit and a related monitoring circuit. In such systems, the battery unit is an example of a DUT and the monitoring circuit includes a microcontroller or measurement circuit configured to obtain voltage and current measurements related to each battery unit. The voltage and current measurements may be used to determine a parameter such as battery unit impedance. The determined battery unit impedance and/or other parameters are used for battery management operations. Example battery management operations include battery unit charging operations, battery unit status management, and battery unit health monitoring.

[0003] In some systems, DUT management involves estimating DUT model parameters in the frequency domain, where the DUT model parameters are based on an equivalent circuit model for the DUT. However, estimating DUT model parameters for varying conditions (e.g., different ICs, temperatures, current flow, and/or DUT age) is problematic. An existing technique relies on a non-linear least squares algorithm to estimate DUT model parameters in the frequency domain. Convergence of DUT model parameters using the non-linear least squares algorithm is time-consuming and/or the results are inaccurate for different conditions.

SUMMARY

[0004] In one example embodiment, a circuit for estimating device under test (DUT) model parameters is described. The circuit comprises a parameter estimator circuit configured to: obtain initial values for DUT model parameters based on sense signal samples; execute a parameter convergence model having a regularization parameter and a cost function that accounts for error

residuals; and obtain final values for the DUT model parameters by adjusting the regularization parameter in iterations of the parameter convergence model as a function of cost function improvement until the parameter convergence model converges to within a target tolerance.

[0005] In another example embodiment, a system comprises sense circuitry adapted to be coupled to a device under test (DUT) and configured to obtain sense signal samples related to the DUT in response to an excitation signal. The system also comprises a measurement circuit coupled to the sense circuitry. The measurement circuit is configured to: obtain initial values for DUT model parameters based on the obtained sense signal samples; execute a parameter convergence model having a regularization parameter and a cost function that accounts for error residuals; and obtain final values for the DUT model parameters by adjusting the regularization parameter in iterations of the parameter convergence model as a function of cost function improvement until the parameter convergence model converges to within a target tolerance.

[0006] In yet another example embodiment, a method for DUT management is described. The method comprises: obtaining, by a measurement circuit, sense signal samples related to the DUT; obtaining, by the measurement circuit, initial values for DUT model parameters as a function of frequency based on the obtained sense signal samples; executing, by the measurement circuit, a parameter convergence model having a regularization parameter and a cost function that accounts for error residuals; obtaining, by the measurement circuit, final values for the DUT model parameters by adjusting the regularization parameter in iterations of the parameter convergence model as a function of cost function improvement until the parameter convergence model converges to within a target tolerance; and using the DUT model parameters to perform DUT management operations.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. 1 is a block diagram of a system in accordance with an example embodiment.

[0008] FIG. 2 is a diagram of battery unit impedance as a function of frequency in accordance with an example embodiment.

[0009] FIG. 3A is a diagram of a battery unit impedance model as a function of frequency in accordance with an example embodiment.

[0010] FIG. 3B is a diagram of another battery unit impedance model as a function of frequency in accordance with an example embodiment.

[0011] FIG. 4A is a graph of imaginary versus real impedance of a battery unit for different state of charge (SOC) values in accordance with an example embodiment.

[0012] FIG. 4B is a graph of imaginary versus real impedance of a battery unit for different state of health (SOH) values in accordance with an example embodiment.

[0013] FIG. 5 is a block diagram of a non-linear least squares algorithm to determine device under test (DUT) model parameters in accordance with a conventional technique.

[0014] FIG. 6 is a graph of mode time constant as a function of degree of discharge of a battery unit in accordance with an example embodiment.

[0015] FIG. 7 is a graph of resistor-capacitor (RC) time constants as a function of state of charge of a battery unit in accordance with an example embodiment.

[0016] FIG. 8 is a graph of normalized absolute error as a function of normalized frequency domain standard deviation for DUT model parameters in accordance with a conventional technique.

[0017] FIG. 9 is a graph of normalized absolute error as a function of normalized frequency domain standard deviation for DUT model parameters in accordance with an example embodiment.

[0018] FIG. 10 is a graph of normalized absolute error as a function of frequency for a conventional DUT model parameter estimation technique and a new DUT model parameter estimation technique in accordance with an example embodiment.

[0019] FIG. 11 is a flowchart of a DUT management method in accordance with an example embodiment.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0020] The same reference numbers (or other reference designators) are used in the drawings to designate the same or similar (structurally and/or functionally) features. FIG. 1 is a block diagram of a system 100 in accordance with an example embodiment. The system 100 represents an electric vehicle, a desktop computer, a laptop computer, a smartphone, or other electrical system. As shown, the system 100 includes a device under test (DUT) 122 coupled to a DUT management circuit 102. The DUT management circuit 102 includes a control circuit 106 and a parameter estimator circuit 110. In some example embodiments, the control circuit 106 includes an excitation signal generator 108 configured to generate an excitation control signal. The excitation signal generator 108 provides the excitation control signal to a driver circuit 130, which is configured to generate an excitation signal based on the excitation control signal and a time reference from a reference clock 120. In some example embodiments, the driver circuit 130 and/or another excitation signal source is external to the DUT management circuit 102. In either case, the excitation signal generated by the driver circuit 130 is provided to the DUT 122 and results in sense signals from the DUT 122. The sense signals

from the DUT 122 are input to sense circuitry 140 coupled to the DUT 122. The sense circuitry 140 samples the sense signals using analog components 142 (e.g., sense resistors, amplifier circuitry, filter circuitry, anti-aliasing circuitry, etc.) and analog-to-digital converters (ADCs) 144. The sense signal samples resulting from the operations of the sense circuitry 140 are provided from the sense circuitry 140 to a sense signal input 150 of the measurement circuit 104. The sense signal samples are used, for example, by the parameter estimator circuit 110.

[0021] In some example embodiments, the DUT management circuit 102 is an integrated circuit (IC). In other example embodiments, the DUT management circuit 102 includes multiple ICs and/or discrete components packaged together or mounted to a printed circuit board (PCB). In one example, the measurement circuit 104 may be in a first IC, while the reference clock 120, driver circuit 130, and sense circuitry 140 are in a second IC.

[0022] In different example embodiments, the parameter estimator circuit 110 may include a processor, a coprocessor, a logic accelerator, or other logic unit configured to perform frequency domain estimation of DUT model parameters. In some example embodiments, the parameter estimator circuit 110 may also include memory (e.g., random-access memory, flash memory, or other memory) with related instructions and/or storage for initial values, iteration results, and final values of a parameter convergence model 116. The parameter convergence model 116 is a model or algorithm that is iteratively executed by the measurement circuit 110 until DUT model parameters converge. The parameter estimator circuit 110 may also include a frequency analyzer circuit 113. In some example embodiments, the frequency analyzer circuit 113 is configured to: convert sense signal samples, including voltage sense signal samples and current sense signal samples, to frequency domain values; and represent the frequency domain values as complex values. In some example embodiments, the frequency analyzer circuit 113 performs discrete Fourier transform (DFT) operations from which the frequency domain values and related complex values are obtained. The frequency analyzer circuit 113 is configured to provide the complex values to the parameter convergence model 116. The measurement circuit 104 may also include a user interface and/or communication interface (not shown) to facilitate the measurement circuit 104 obtaining instructions, a predetermined characterization of the DUT 122, and/or other information.

[0023] In the example of FIG. 1, the parameter estimator circuit 110 obtains (e.g., stores in memory) a measurement-based parameter 112 derived based on the sense signal samples input to the sense signal input 150. In some example embodiments, the measurement-based parameter 112

is the impedance of the DUT 122 as a function of frequency. Without limitation, the impedance of the DUT 122 as a function of frequency is determined by the measurement circuit 104 from sense signal samples (e.g., samples of the voltage across the DUT 122 and samples of the current through the DUT 122) resulting from application of the excitation signal to the DUT 122. In the example of FIG. 1, the parameter estimator circuit 110 also includes DUT model parameters 114. In some example embodiments, initial values of the DUT model parameters 114 are obtained by the parameter estimator circuit 110 based on the measurement-based parameter 112 and a predetermined characterization of the DUT 122. In some example embodiments, the DUT model parameters 114 include: a series resistance, a series capacitance, a series inductance, mode capacitors, mode resistors, and mode time constants. The mode time constants may vary to account for varying conditions of the DUT such as degree of discharge, temperature condition, and age.

[0024] In some example embodiments, the measurement circuit 104 uses the parameter estimator circuit 110 to perform frequency domain of DUT model parameters. Example operations of the measurement circuit 104 (or the parameter estimator circuit 110) include: obtain sense signal samples related to the DUT 122 (e.g., indicating voltage across the DUT 122 and/or current through the DUT 122); obtain initial values for the DUT model parameters 114 based on the obtained sense signals; perform error analysis using the parameter convergence model 116; iteratively adjust a regularization parameter of the parameter convergence model 116 based on the error analysis; and select final values of the DUT model parameters 114 when the parameter convergence model 116 converges to within a target tolerance. In some example embodiments, the measurement circuit 104 is configured to: run the parameter convergence model 116 for multiple initial DUT model parameter settings based on a characterization of the DUT 122; and select final converged values for the DUT model parameters 114 based on minimization of a total residual error metric.

[0025] In some example embodiments, the parameter estimator circuit 110 is configured to adjust the regularization parameter in iterations of the parameter convergence model 116 as a function of a ratio of cost function improvement to expected improvement. For example, the parameter estimator circuit 110 may be configured to compare the ratio to a threshold. The regularization parameter is then adjusted by the parameter estimator circuit 110 based on the comparison. If the ratio is greater than the threshold, the parameter estimator circuit 110 is configured to select the regularization parameter to be a maximum of a first value and a second value. Without limitation, the first value may be fixed and the second value may be a function of the ratio. If the ratio is less than or equal to

the threshold, the parameter estimator circuit 110 is configured to increase the regularization parameter for a next iteration of the parameter convergence model 116 relative to its current value. The final values for the DUT model parameters 114 may be provided by the parameter estimator circuit 110 to an analyzer circuit 118, which is configured to direct or trigger DUT management operations based on the DUT model parameters 114 and possibly other parameters.

[0026] In some example embodiments, the analyzer circuit 118 is a processor, application-specific integrated circuit (ASIC), or programmable logic. The analyzer circuit 118 may use the DUT model parameters and possibly other parameters (e.g., temperature or other conditions) to trigger DUT-related operations. Example DUT-related operations triggered by the analyzer circuit 118 (e.g., when the DUT is a battery unit) include: adjusting battery unit charging operations (turn battery unit charging on/off), updating a battery unit charge indicator status (e.g., 30%, 50%, 70%, 90%, etc.); identifying a battery unit fault condition; and/or other battery management operations.

[0027] FIG. 2 is a diagram 200 of battery unit impedance as a function of frequency in accordance with an example embodiment. In the diagram 200, imaginary impedance versus real impedance of a battery unit are represented as a function of frequency. The diagram 200 also shows different battery unit features (e.g., separator, electrodes, insulating layer, activation, diffusion, electronic conduction, ionic conduction, and phase formation) related to the impedance variations. The plotted curve 202 in diagram 200 represents the impedance as a function of frequency for a particular battery unit. When impedance as a function of frequency for a battery unit is modeled accurately (e.g., using an equivalent circuit model and related values), the performance and timing of various battery management operations is improved.

[0028] FIG. 3A is a diagram of a battery unit equivalent circuit 300 in accordance with an example embodiment. As shown, the battery unit equivalent circuit 300 models a battery unit as various components between a reference voltage (V_r) at the positive terminal of the battery unit and ground. The battery unit model components including a series resistor (R_s), a first mode circuit (having R_1 and C_1), a second mode circuit (having R_2 and C_2), a third mode circuit (having R_3 and C_2), and an open circuit voltage (V_{oc}) in series between the V_r terminal and ground.

[0029] FIG. 3B is a diagram of another battery unit equivalent circuit 310 in accordance with an example embodiment. As shown, the battery unit equivalent circuit 310 models a battery unit as various components in series including: a series inductor (L_s); a series resistor (R_s); a first mode circuit (having R_1 and C_1); a second mode circuit (having R_2 and C_2); a third mode circuit (having

R_3 and C_3); a fourth mode circuit (having R_4 and C_4); a fifth mode circuit (having R_5 and C_5); and a series capacitor (C_s) to represent V_{oc} . Other battery unit equivalent circuits or models are possible. For example, the number of mode circuits and the values of the model components may vary, which affects the impedance at different frequencies.

[0030] FIG. 4A is a graph 400 of imaginary versus real impedance for different battery unit state of charge (SOC) values in accordance with an example embodiment. In graph 400, imaginary and real impedances for different battery unit SOC values are shown. The example battery unit SOC values range from 100% to 5% for the modeled SOC (mod SOC) and the experimental SOC (exp SOC). In some example embodiments, the battery unit SOC is accounted for when estimating DUT model parameters as described herein.

[0031] FIG. 4B is a graph 410 of imaginary versus real impedance for different battery unit state of health (SOH) values in accordance with an example embodiment. In graph 410, imaginary and real impedances for different battery unit SOH values are shown. The example battery unit state of health values are based on charge cycles, which range from 1 cycle to 315 cycles in the example of FIG. 4B. In some example embodiments, the battery unit state of health is accounted for when estimating DUT model parameters as described herein.

[0032] FIG. 5 is a block diagram of a non-linear least squares algorithm 500 to determine DUT model parameters in accordance with a conventional technique. For the example of FIG. 5, $\beta = \{R_s, L, C_s, R_1, R_2, R_3, \dots, C_1, C_2, C_3, \dots\}$. Also, the transfer function model of the impedance as a function of the Laplace domain variable s is given as:

$$Z_{TH}(s) = R_s + Ls + \frac{1}{C_s s} + \frac{R_1}{R_1 C_1 s + 1} + \frac{R_2}{R_2 C_2 s + 1} + \frac{R_3}{R_3 C_3 s + 1} + \dots, \quad \text{Equation (1)}$$

where $R_s, L, C_s, R_1, R_2, R_3, C_1, C_2, C_3$ are example DUT model parameters (see e.g., the DUT model of FIG. 3B). $Z_m(f_n)$ is the measured impedance spectrum, where the variable f_n denotes the measurement frequency for the n^{th} element of the transfer function. Also, the residual $r[n, \beta]$, which is a function of n and β , is given as:

$$r[n, \beta] = Z_m(f_n) - Z_{TH}(f_n, \beta), \quad \text{Equation (2)}$$

denotes the difference between the model and the measurement. Also, r can be written as a vector:

$$r = [r[1, \beta] \quad \dots \quad r[N, \beta]]^T, \quad \text{Equation (3)}$$

where N is the number of samples in the measurements.

[0033] With the non-linear least squares algorithm 500, an initial value for a set of DUT model

parameters (β) is provided to block 502, which linearizes a cost function around current parameters as represented by equations 504. At block 506, the approximate model is solved as represented by equations 508. At block 510, the DUT model parameters are updated from the approximate model solution as represented by equation 512. At block 514, a test for convergence is performed as represented by equation 516. The operations of blocks 502, 506, 510, 514 are repeated until the final estimate for β is within a target tolerance.

[0034] The accuracy of the non-linear least squares algorithm 500 and/or the speed of convergence may suffer depending on the initial value for β and variable conditions for a DUT (e.g., the DUT 122 in FIG. 1). For example, the non-linear least squares algorithm 500 converges rapidly only when the parameter vector (e.g., β) is close to a local optimum. Far from a local optimum, a steepest descent technique (e.g., $\Delta\beta = \alpha J^T r^{(k)}$) would reduce the error criterion faster.

[0035] In the described embodiments, the initial values of the DUT model parameters account for variable conditions of a DUT, including degree of discharge, temperature, and age. FIG. 6 is a graph 600 of mode time constant (in seconds) as a function of degree of discharge (in decimal fractions) of a battery unit in accordance with an example embodiment. Depending on the degree of discharge, the resulting mode time constants vary over two order of magnitude. Referring again to the non-linear least squares algorithm 500, some DUT model parameters (e.g., mode circuit values) do not converge correctly when degree of discharge and temperature are not taken into account.

[0036] FIG. 7 is a graph 700 of resistor-capacitor (RC) time constants (in seconds) as a function of state of charge (in %) of a battery unit in accordance with an example embodiment. In graph 700, RC constants (τ_1, τ_2, τ_3) vary as a function of state of charge and different initial conditions. The initial values of the DUT model parameters may be based on a predetermined characterization of the DUT.

[0037] In some example embodiments, the predetermined characterization of the DUT includes initial values for DUT model parameters based on impedance spectrum measurements (e.g., determined from the obtained sense signals or related samples). In one example, the initial values include:

$$C_{s,init} = \max_{SOC,T} C_s(SOC, T), \quad \text{Equation (4)}$$

$$R_{s,init} = Re(Z_m(f_{max})), \quad \text{Equation (5)}$$

$$R_{p,init} = (R_{min} - R_{max})/N, \quad \text{Equation (6)}$$

$$\tau_{min} = \frac{\gamma}{f_{max}}, \quad \text{Equation (7)}$$

$$\tau_{max} = \frac{1}{\gamma f_{min}} \text{ with } \gamma = 2, \quad \text{Equation (8)}$$

$$\tau_{p,init} = \kappa \tau_{min} e^{\left(\frac{p}{M} \ln\left(\frac{\tau_{max}}{\tau_{min}}\right)\right)} \quad p = 1, \dots, M, \text{ and} \quad \text{Equation (9)}$$

$$C_{p,init} = \tau_p / R_{p,init}. \quad \text{Equation (10)}$$

For Equation 4, $C_{s,init}$ is the initial value of C_s , $\max_{SOC,T} C_s$ is a maximum value for C_s , SOC is the state of charge, and T is temperature. For Equation 5, $R_{s,init}$ is the initial value of R_s , $\text{Re}()$ is the real part of the argument, and $Z_m(f_{max})$ is the measured impedance for a maximum frequency. For Equation 6, $R_{p,init}$ is the initial value of R_p is resistance value of the p^{th} mode, R_{min} is the minimum possible resistance value, and R_{max} is the maximum possible resistance value. For Equation 7, τ_{min} is the minimum mode time constant, and γ is a scale factor applied to the system frequency range. For Equation 8, τ_{max} is the maximum mode time constant, and f_{min} is a minimum frequency. For Equation 9, $\tau_{p,init}$ is the initial value of τ_p , κ is a parameter used to select the initial starting condition, p is the mode number, and M is the total number of modes. For Equation 10, $C_{p,init}$ is the initial value of C_p . In some example embodiments, κ enables mode time constant variance to account for different degree of discharge (DOD), temperature, and age conditions.

[0038] FIG. 8 is a graph 800 of normalized absolute error as a function of normalized frequency domain standard deviation for DUT model parameters in accordance with a conventional technique (e.g., the non-linear least squares technique in FIG. 5). In graph 800, the DUT model parameters include: R_s ; L_p ; R_1 ; R_2 ; R_3 ; C_1 ; C_2 ; and C_3 . Due to convergence to a false local minimum there is a large error increase 802 in the DUT model parameters.

[0039] FIG. 9 is a graph 900 of normalized absolute error as a function of normalized frequency domain standard deviation (i.e., the standard deviation of the noise added in the frequency domain) for DUT model parameters in accordance with an example embodiment. In graph 900, the DUT model parameters includes: R_s ; L_p ; R_1 ; R_2 ; R_3 ; C_1 ; C_2 ; and C_3 . With the parameter convergence model described herein, false local minimums and related errors are avoided or reduced. Compared to the conventional technique, the parameter convergence model described herein provides improved accuracy (e.g., 100 times more accurate) and maintains estimation error linearity over the frequency range of interest (e.g., nonlinear discontinuities due to signal-to-noise ratio (SNR) and convergence to incorrect minima are avoided).

[0040] In some example embodiments, a parameter convergence model (e.g., the parameter convergence model 116 in FIG. 1) is given as:

$$(J^T J + \lambda I) \Delta \beta = J^T r^{(k)}, \quad \text{Equation (11)}$$

where J is a Jacobian matrix (i.e., the gradient of the model with respect to the unknown parameters), J^T is the transpose of the Jacobian matrix, λ is a regularization parameter, I is the identity matrix, $\Delta \beta$ is the change in β , and $r^{(k)}$ is the residual for the k^{th} iteration of the model. With the parameter convergence model, the regularization parameter is adjustable. At the beginning of optimization, large values are used for the regularization parameter and the parameter convergence model behaves like a steepest descent algorithm. As fit quality improves, the regularization parameter is reduced to expedite convergence near the local optimum. Use large values at beginning of optimization to get behavior like steepest descent. As fit quality improves, reduce it to get fast convergence of near the local optimum.

[0041] In some example embodiments, a parameter convergence model (e.g., the parameter convergence model 116 in FIG. 1) uses a ratio of cost function improvement to expected improvement to update the regularization parameter. For example, the ratio may be given as:

$$\rho = \frac{\ell^2(r^{(k)}) - \ell^2(r^{(k+1)})}{\Delta \beta^T (\lambda^{(k)} \Delta \beta + J^T r)}, \quad \text{Equation (12)}$$

where $\ell^2(r^{(k)}) - \ell^2(r^{(k+1)})$ is the cost ratio improvement and $\Delta \beta^T (\lambda^{(k)} \Delta \beta + J^T r)$ is the expected improvement for the linearized model. In some example embodiments, ρ is compared to an acceptance threshold ϵ . If $\rho > \epsilon$, the regularization parameter is selected to be a maximum of a first value and a second value. The first value may be fixed while the second value is a function of the ratio. In some example embodiments, if $\rho > \epsilon$, $\lambda^{(k+1)} = \lambda^{(k)} \max[1/3, 1 - (2\rho - 1)^3]$. If the ratio is less than or equal to the threshold, the regularization parameter is increased for a next iteration of the parameter convergence model relative to its current value. In some example embodiments, if $\rho \leq \epsilon$, $\lambda^{(k)} = 2\lambda^{(k)}$. With the parameter convergence model, faster convergence to more accurate parameter estimates is achieved relative to the non-linear least squares technique.

[0042] As shown in graph 700 of FIG. 7, a parameter convergence model (e.g., the parameter convergent model 116 in FIG. 1) is computed by a parameter estimator circuit (e.g., the parameter estimator circuit 110 in FIG. 1) for multiple values of the initial conditions. These different choices of the initial condition are parameterized by values of κ , as shown in Equation 9. For each starting point, the parameter convergence model will converge to a final value of the DUT model parameters.

The DUT model parameters are a function of κ , and are denoted by the vector $\beta(\kappa)$. A parameter estimator circuit (e.g., the parameter estimator circuit 110) circuit is configured to determine the best set of converged parameter estimates by comparison of the residual errors. In some example embodiments, the total residual error metric for an individual set of initial conditions is a function of κ , and is given by:

$$\ell^2(r, \beta(\kappa)) = \sum_{a=1}^N r^2[a, \beta(\kappa)]. \quad \text{Equation (13)}$$

The final set of converged parameter estimates is associated by a parameter estimator circuit (e.g., the parameter estimator circuit 110 in FIG. 1) with the smallest total residual error metric, and is denoted as:

$$\beta_{final} = \arg \min_{\beta(\kappa)} \ell^2(r, \beta(\kappa)). \quad \text{Equation (14)}$$

The parameters contained in the vector β_{final} are provided by the parameter estimator circuit to an analyzer circuit (e.g., the analyzer circuit 118 in FIG. 1) for use in subsequent DUT management operations performed or triggered by the analyzer circuit 118.

[0043] FIG. 10 is a graph 1000 of normalized absolute error as a function of frequency for a conventional DUT model parameter estimation technique and a new DUT model parameter estimation technique in accordance with an example embodiment. In graph 1000, the parameter convergence model provides greater than 30x improvement in impedance accuracy at high frequency and 5x improvement in impedance accuracy at low frequency compared to the conventional technique. For a DUT model with additional mode circuits, impedance accuracy at low frequency improves.

[0044] FIG. 11 is a flowchart of a DUT management method 1100 in accordance with an example embodiment. The method 1100 is performed, for example, by a measurement circuit (e.g., the measurement circuit 104 in FIG. 1) or DUT management circuit (e.g., the DUT management circuit 102 in FIG. 1). At block 1102, sense signal samples related to the DUT are obtained. At block 1104, initial values for DUT model parameters are obtained based at least on the obtained sense signal samples. At block 1106, a parameter convergence model having a regularization parameter and a cost function that accounts for error residuals is executed. At block 1108, final values for the DUT model parameters are obtained by adjusting the regularization parameter in iterations of the parameter convergence model as a function of cost function improvement until the parameter convergence model converges to within a target tolerance. At block 1110, the final values for the DUT model parameters are used to perform DUT management operations.

[0045] In some example embodiments, the method 1100 includes: determining a ratio of cost function improvement to expected improvement; and comparing the ratio to a threshold. If the ratio is greater than the threshold, the regularization parameter for a next iteration of the parameter convergence model is selected to be a maximum of a first value and a second value. If the ratio is less than or equal to the threshold, the value of the regularization parameter for a next iteration of the parameter convergence model is increased relative to its current value. In some examples, the first value is fixed and the second value is a function of the ratio. Without limitation, the DUT model parameters may include: a series resistance, a series capacitance, a series inductance, mode capacitors, and mode resistors, and the method further comprises using initial values for the series resistance, the series capacitance, the series inductance, the mode capacitors, the mode resistors, and mode time constants based on a predetermined characterization of the DUT.

In some example embodiments, the mode time constants vary to account for degree of discharge, temperature, and age of the DUT. In some example embodiments, the method 1100 includes running the parameter convergence model for multiple initial DUT model parameter settings based on a characterization of the DUT; and selecting final converged values for the DUT model parameters based on minimization of a total residual error metric. Also, the method 1100 may include: converting the obtained sense signal samples, including voltage sense signal samples and current sense signal samples, to frequency domain values; representing the frequency domain values as complex values; and using the complex values with the parameter convergence model. With the method 1100, the accuracy and convergence speed of solving for DUT model parameters is improved relative to conventional frequency domain estimation of DUT model parameters.

[0046] Some example embodiments include a measurement circuit for a DUT. The measurement circuit is configured perform frequency domain estimation of DUT model parameters. In some example embodiments, the measurement circuit is configured to: obtain sense signal samples related to the DUT (e.g., voltage across the DUT and/or current through the DUT); obtain initial values for the DUT model parameters based on the obtained sense signals; execute a parameter convergence model having a regularization parameter and a cost function that accounts for error residuals; and obtain final values for the DUT model parameters by adjusting the regularization parameter in iterations of the parameter convergence model as a function of cost function improvement until the parameter convergence model converges to within a target tolerance.

[0047] In some example embodiments, the regularization parameter is adjusted in iterations of the

parameter convergence model as a function of a ratio of cost function improvement to expected improvement. For example, the ratio may be compared to a threshold. If the ratio is greater than the threshold, the regularization parameter is selected to be the maximum of a first value and a second value. Without limitation, the first value may be fixed and the second value may be a function of the ratio. If the ratio is less than or equal to the threshold, the regularization parameter is increased relative to its current value for a next iteration of the parameter convergence model.

[0048] The final values for the DUT model parameters may be provided by a parameter estimator circuit to an analyzer circuit configured to provide DUT management operations based on the DUT model parameters and possibly other parameters (e.g., temperature or other conditions). In some example embodiments, the DUT model parameters include: a series resistance, a series capacitance, a series inductance, mode capacitors, mode resistors, and mode time constants. In such case, the parameter estimator operations are based on initial values for the series resistance, the series capacitance, the series inductance, the mode capacitors, the mode resistors, and mode time constants obtained from a characterization of the DUT. The mode time constants vary to account for varying conditions of the DUT such as DOD, temperature condition, and age.

[0049] In some example embodiments, the DUT is a battery unit and the DUT model parameters are used to characterize battery unit impedance as a function of frequency. In different example embodiments, a battery unit refers to a battery cell or multiple battery cells (e.g., battery cells coupled in series and/or in parallel). The number of battery cells included in a battery unit may vary (e.g., 1 to 20 cells). As desired, a number of battery units may be connected in series to form a battery module. Without limitation, a battery module may include from 10 to 40 battery units.

[0050] In some example embodiments, the battery unit impedance as a function of frequency as well as related parameters (e.g., temperature, SOC, SOH, and/or other parameters) may be used to provide the battery management operations. Example battery management operations include: charging operations (e.g., turn battery charging on/off); degree of discharge operations (e.g., adjust current flow to one or more loads); fault condition monitoring (e.g., disconnect or replace battery cells or groups of battery cells); and/or other battery-related operations. As desired, battery management operations are performed for a battery module, each battery unit of the battery module, and/or each battery cell of each battery unit. Suitable measurement circuit ICs and related sense circuitry are used to perform sampling and parameter estimation operations as described herein for a battery module, each battery unit, or each battery cell. With the described parameter convergence

model, the accuracy and convergence speed of DUT model parameters is improved relative to a conventional non-linear least squares algorithm, which improves the battery management operations.

[0051] In this description, the term “couple” may cover connections, communications, or signal paths that enable a functional relationship consistent with this description. For example, if device A generates a signal to control device B to perform an action: (a) in a first example, device A is coupled to device B by direct connection; or (b) in a second example, device A is coupled to device B through intervening component C if intervening component C does not alter the functional relationship between device A and device B, such that device B is controlled by device A via the control signal generated by device A.

[0052] As used herein, the terms “electrode,” “node,” “interconnection,” “pin,” “contact,” and “connection” are used interchangeably. Unless specifically stated to the contrary, these terms are generally used to mean an interconnection between or a terminus of a device element, a circuit element, an integrated circuit, a device or other electronics or semiconductor component.

[0053] The example embodiments above may utilize switches in the form of n-type or p-type metal-oxide semiconductor field-effect transistors (“NMOS” or “PMOS”) transistors. Other example embodiments may utilize NPN bipolar junction transistors (BJTs), PNP BJTs, or any other type of transistor. Hence, when referring to a current electrode, such electrode may be an emitter, collector, source or drain. Also, the control electrode may be a base or a gate.

[0054] A device that is “configured to” perform a task or function may be configured (e.g., programmed and/or hardwired) at a time of manufacturing by a manufacturer to perform the function and/or may be configurable (or re-configurable) by a user after manufacturing to perform the function and/or other additional or alternative functions. The configuring may be through firmware and/or software programming of the device, through a construction and/or layout of hardware components and interconnections of the device, or a combination thereof.

[0055] A circuit or device that is described herein as including certain components may instead be adapted to be coupled to those components to form the described circuitry or device. For example, a structure described as including one or more semiconductor elements (such as transistors), one or more passive elements (such as resistors, capacitors, and/or inductors), and/or one or more sources (such as voltage and/or current sources) may instead include only the semiconductor elements within a single physical device (e.g., a semiconductor die and/or integrated circuit (IC) package) and may

be adapted to be coupled to at least some of the passive elements and/or the sources to form the described structure either at a time of manufacture or after a time of manufacture, for example, by an end-user and/or a third-party.

[0056] Circuits described herein are reconfigurable to include the replaced components to provide functionality at least partially similar to functionality available prior to the component replacement. Components shown as resistors, unless otherwise stated, are generally representative of any one or more elements coupled in series and/or parallel to provide an amount of impedance represented by the shown resistor. For example, a resistor or capacitor shown and described herein as a single component may instead be multiple resistors or capacitors, respectively, coupled in parallel between the same nodes. For example, a resistor or capacitor shown and described herein as a single component may instead be multiple resistors or capacitors, respectively, coupled in series between the same two nodes as the single resistor or capacitor.

[0057] Uses of the phrase “ground” in this description include a chassis ground, an Earth ground, a floating ground, a virtual ground, a digital ground, a common ground, and/or any other form of ground connection applicable to, or suitable for, the teachings of this description. Unless otherwise stated, “about,” “approximately,” or “substantially” preceding a value means +/- 10 percent of the stated value.

[0058] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A circuit for determining device under test (DUT) model parameters, the circuit comprising:
 - a parameter estimator circuit configured to:
 - obtain initial values for DUT model parameters based on sense signal samples;
 - execute a parameter convergence model having a regularization parameter and a cost function that accounts for error residuals; and
 - obtain final values for the DUT model parameters by adjusting the regularization parameter in iterations of the parameter convergence model as a function of cost function improvement until the parameter convergence model converges to within a target tolerance.
2. The circuit of claim 1, wherein the parameter estimator circuit is configured to adjust the regularization parameter in iterations of the parameter convergence model as a function of a ratio of cost function improvement to expected improvement.
3. The circuit of claim 2, wherein the parameter estimator circuit is configured to:
 - compare the ratio to a threshold; and
 - if the ratio is greater than the threshold, adjust the regularization parameter to be a maximum of a first value and a second value.
4. The circuit of claim 3, wherein the first value is fixed and the second value is a function of the ratio.
5. The circuit of claim 2, wherein the parameter estimator circuit is configured to:
 - compare the ratio to a threshold; and
 - if the ratio is less than or equal to the threshold, increase the regularization parameter relative to its current value for a next iteration of the parameter convergence model.
6. The circuit of claim 1, further comprising a frequency analyzer circuit included with or coupled to the parameter estimator circuit, the frequency analyzer circuit is configured to:
 - convert the sense signal samples, including voltage sense signal samples and current sense signal samples, to frequency domain values; and
 - represent the frequency domain values as complex values, wherein the complex values are used with the parameter convergence model.
7. The circuit of claim 1, wherein the parameter estimator circuit is configured to obtain initial values

for DUT model parameters including a series resistance, a series capacitance, a series inductance, mode capacitors, mode resistors and mode time constants, and the mode time constants vary to account for degree of discharge, temperature, and age of the DUT.

8. The circuit of claim 1, wherein the parameter convergence model is run for multiple initial DUT model parameter settings based on a characterization of the DUT, and final converged values for the DUT model parameters are selected based on minimization of a total residual error metric.

9. The circuit of claim 1, further comprising:

an excitation signal generator configured to generate an excitation control signal;

a driver circuit coupled to the excitation signal generator and the DUT, the driver circuit is configured to apply an excitation signal to the DUT based on the excitation control signal; and

sense circuitry coupled to the sense signal input and the DUT, the sense circuitry is configured to provide the sense signal samples in response to the excitation signal being applied to the DUT.

10. A system comprising:

sense circuitry adapted to be coupled to a device under test (DUT) and configured to obtain sense signal samples related to the DUT in response to an excitation signal; and

a measurement circuit coupled to the sense circuitry, the measurement circuit is configured to:

obtain initial values for DUT model parameters based on the obtained sense signal samples;

execute a parameter convergence model having a regularization parameter and a cost function that accounts for error residuals; and

obtain final values for the DUT model parameters by adjusting the regularization parameter in iterations of the parameter convergence model as a function of cost function improvement until the parameter convergence model converges to within a target tolerance.

11. The system of claim 10, wherein measurement circuit is configured to adjust the regularization parameter in iterations of the parameter convergence model based on a ratio of cost function improvement to expected improvement.

12. The system of claim 11, wherein the measurement circuit is configured to:

- compare the ratio to a threshold;
 - if the ratio is greater than the threshold, the regularization parameter is selected to be a maximum of a first value and a second value; and
 - if the ratio is less than or equal to the threshold, the regularization parameter is increased relative to its current value.
13. The system of claim 12, wherein the first value is fixed and the second value is a function of the ratio.
14. The system of claim 10, wherein the measurement circuit is configured to:
- convert the sense signal samples, including voltage sense signal samples and current sense signal samples, to frequency domain values; and
 - represent the frequency domain values as complex values, wherein the complex values are used with the parameter convergence model.
15. The system of claim 10, wherein the measurement circuit is configured to obtain initial values for DUT model parameters including a series resistance, a series capacitance, a series inductance, mode capacitors, mode resistors and mode time constants, and the mode time constants vary to account for degree of discharge, temperature conditions and age of the DUT.
16. The system of claim 10, wherein the measurement circuit is configured to:
- run the parameter convergence model for multiple initial DUT model parameter settings based on a characterization of the DUT; and
 - select final converged values for the DUT model parameters based on minimization of a total residual error metric.
17. A method for device under test (DUT) management, the method comprising:
- obtaining, by a measurement circuit, sense signal samples related to the DUT;
 - obtaining, by the measurement circuit, initial values for DUT model parameters based on the obtained sense signal samples;
 - executing, by the measurement circuit, a parameter convergence model having a regularization parameter and a cost function that accounts for error residuals;
 - obtaining, by the measurement circuit, final values for the DUT model parameters by adjusting the regularization parameter in iterations of the parameter convergence model as a function of cost function improvement until the parameter convergence model converges to within a target tolerance; and

using the DUT model parameters to perform DUT management operations.

18. The method of claim 17, wherein methods further comprises:

determining a ratio of cost function improvement to expected improvement;

comparing the ratio to a threshold;

if the ratio is greater than the threshold, selecting the regularization parameter for a next iteration of the parameter convergence model to be a maximum of a first value and a second value; and

if the ratio is less than or equal to the threshold, increasing a value of the regularization parameter for a next iteration of the parameter convergence model relative to its current value.

19. The method of claim 18, wherein the first value is fixed and the second value is a function of the ratio.

20. The method of claim 17, wherein the method further comprises obtaining initial values of DUT model parameters including a series resistance, a series capacitance, a series inductance, mode capacitors, mode resistors and mode time constants, and the mode time constants vary to account for degree of discharge, temperature, and age of the DUT.

21. The method of claim 20, wherein the method further comprises:

running the parameter convergence model for multiple initial DUT model parameter settings based on a characterization of the DUT; and

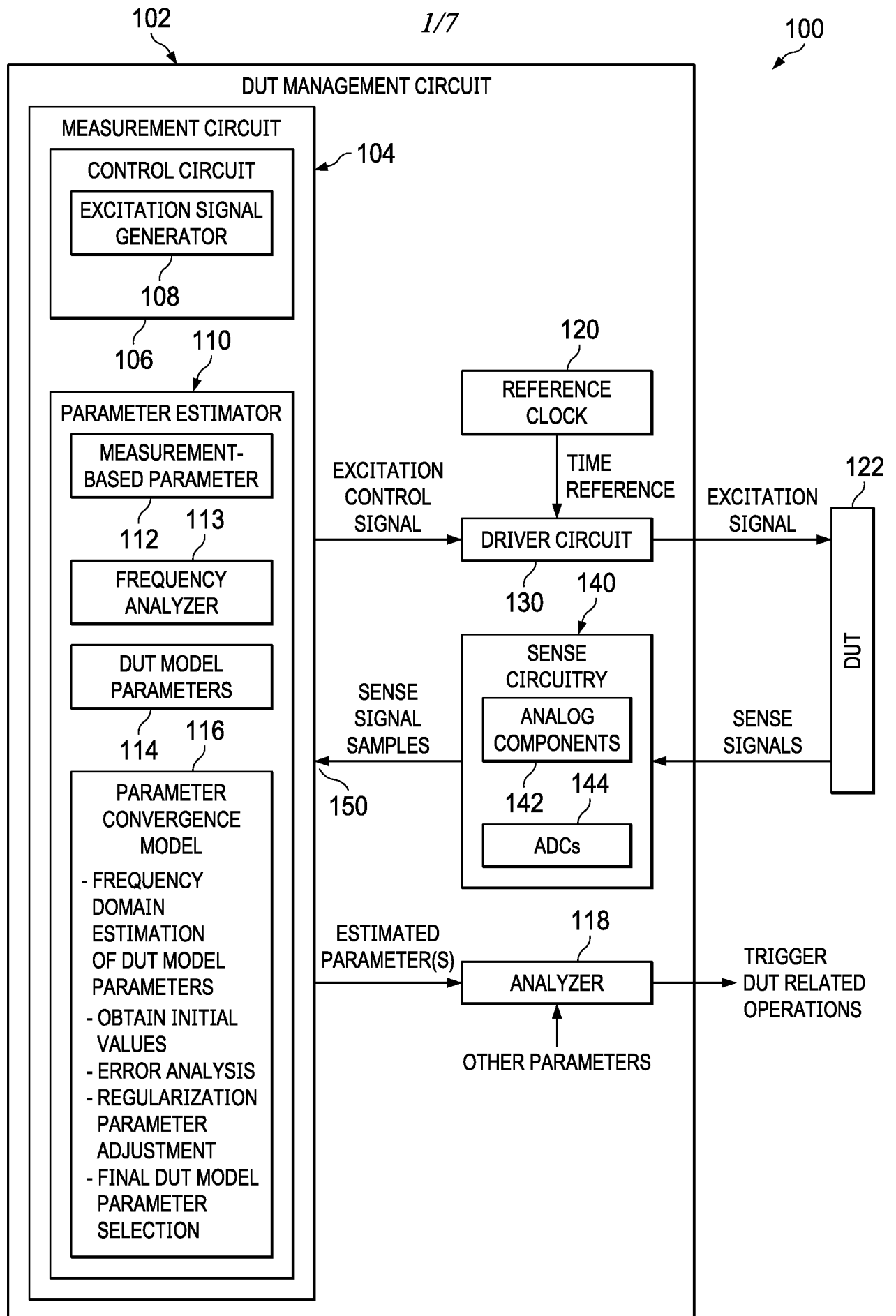
selecting final converged values for the DUT model parameters based on minimization of a total residual error metric.

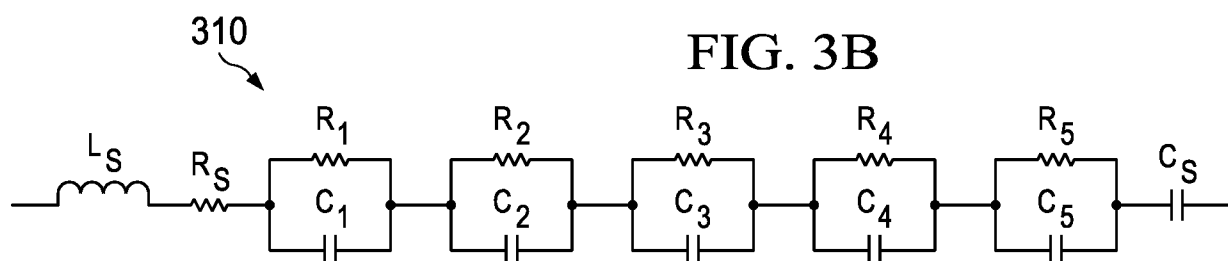
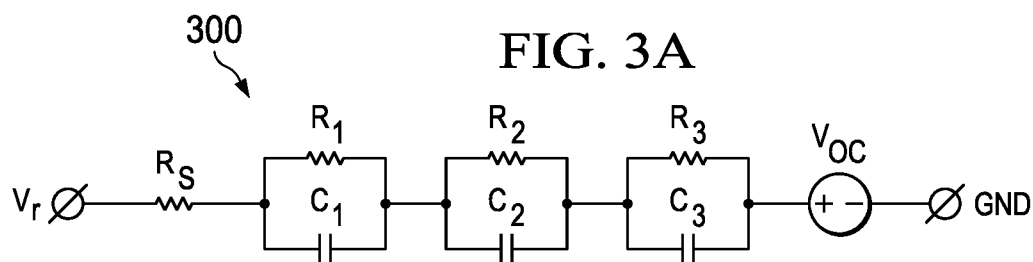
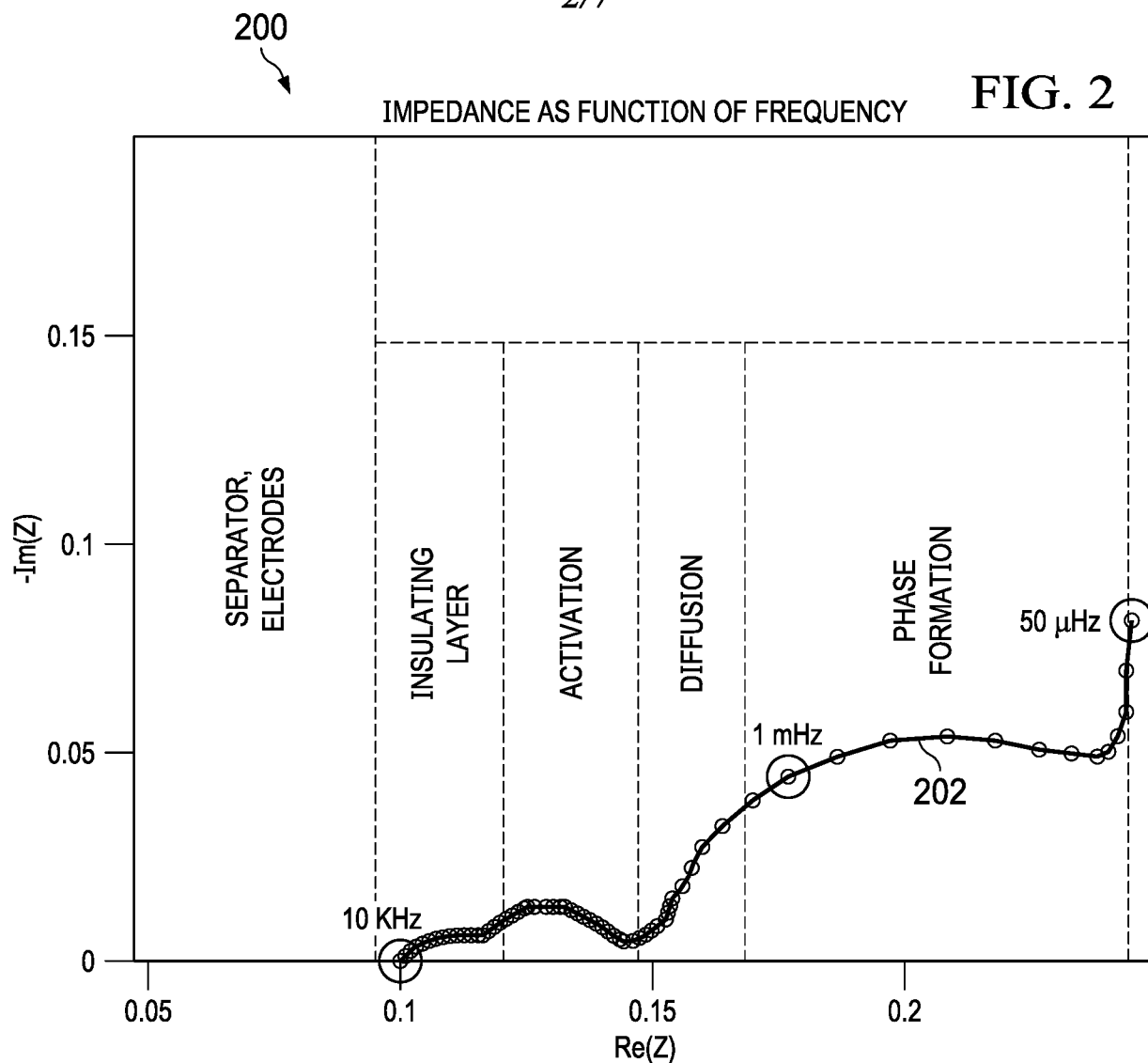
22. The method of claim 17, further comprising:

converting the obtained sense signal samples, including voltage sense signal samples and current sense signal samples, to frequency domain values;

representing the frequency domain values as complex values; and

using the complex values with the parameter convergence model.





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FIG. 4A

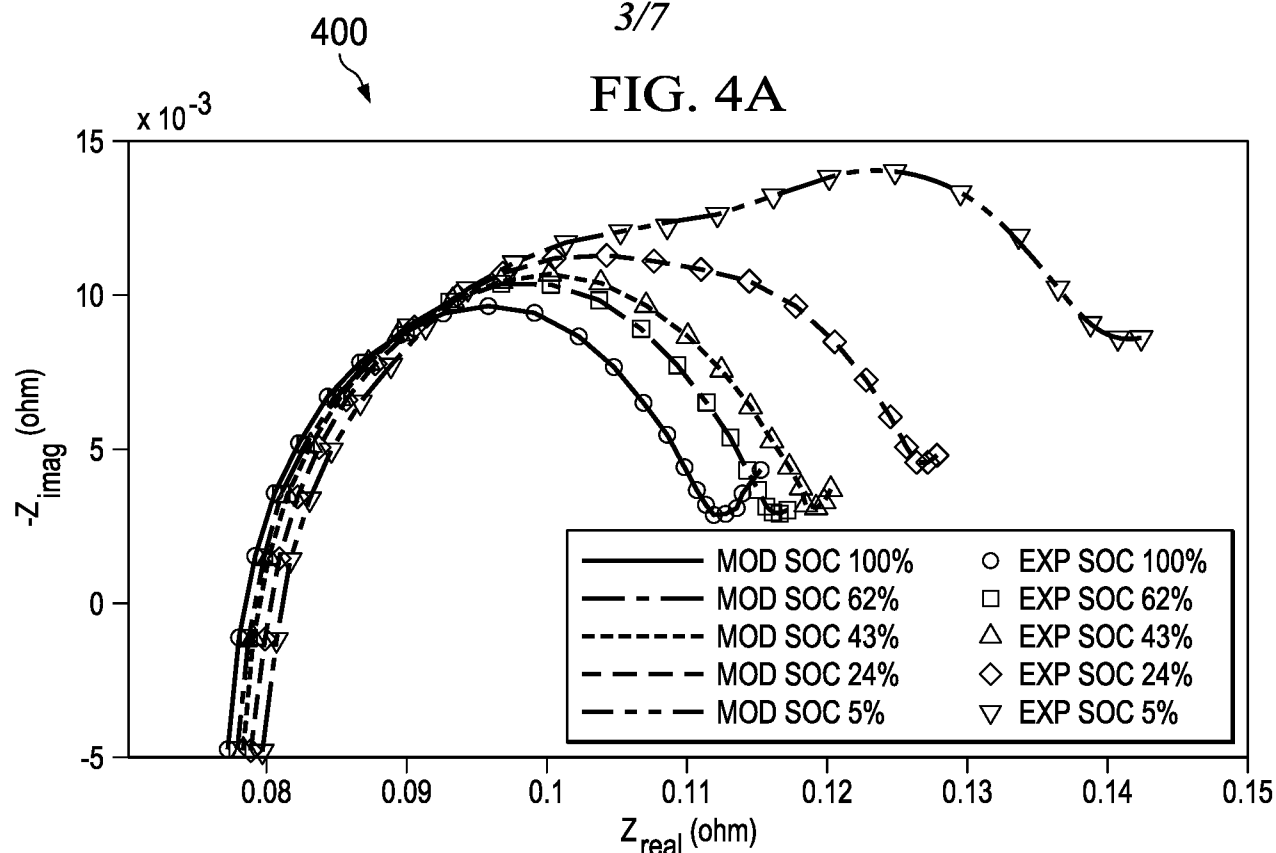
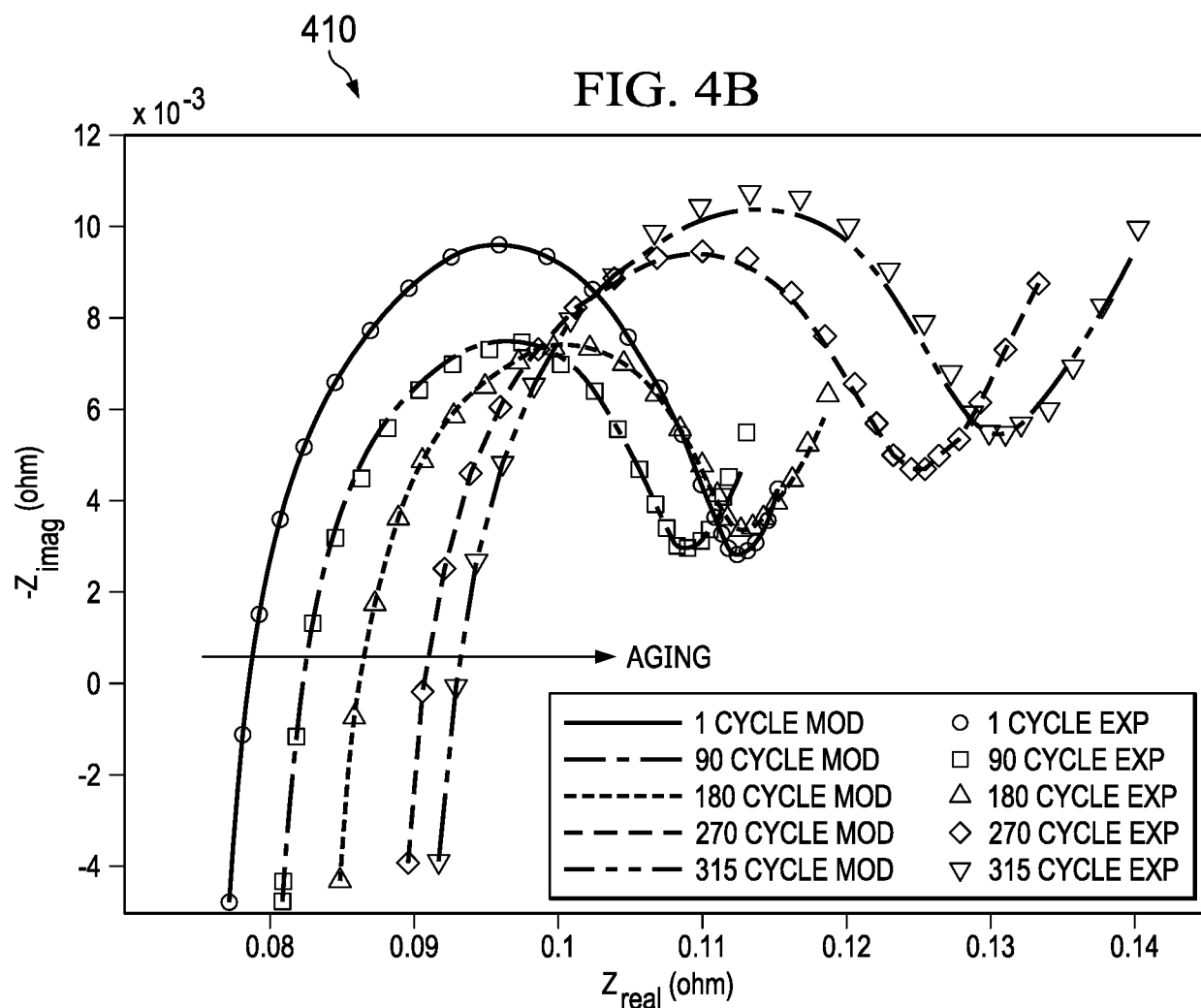
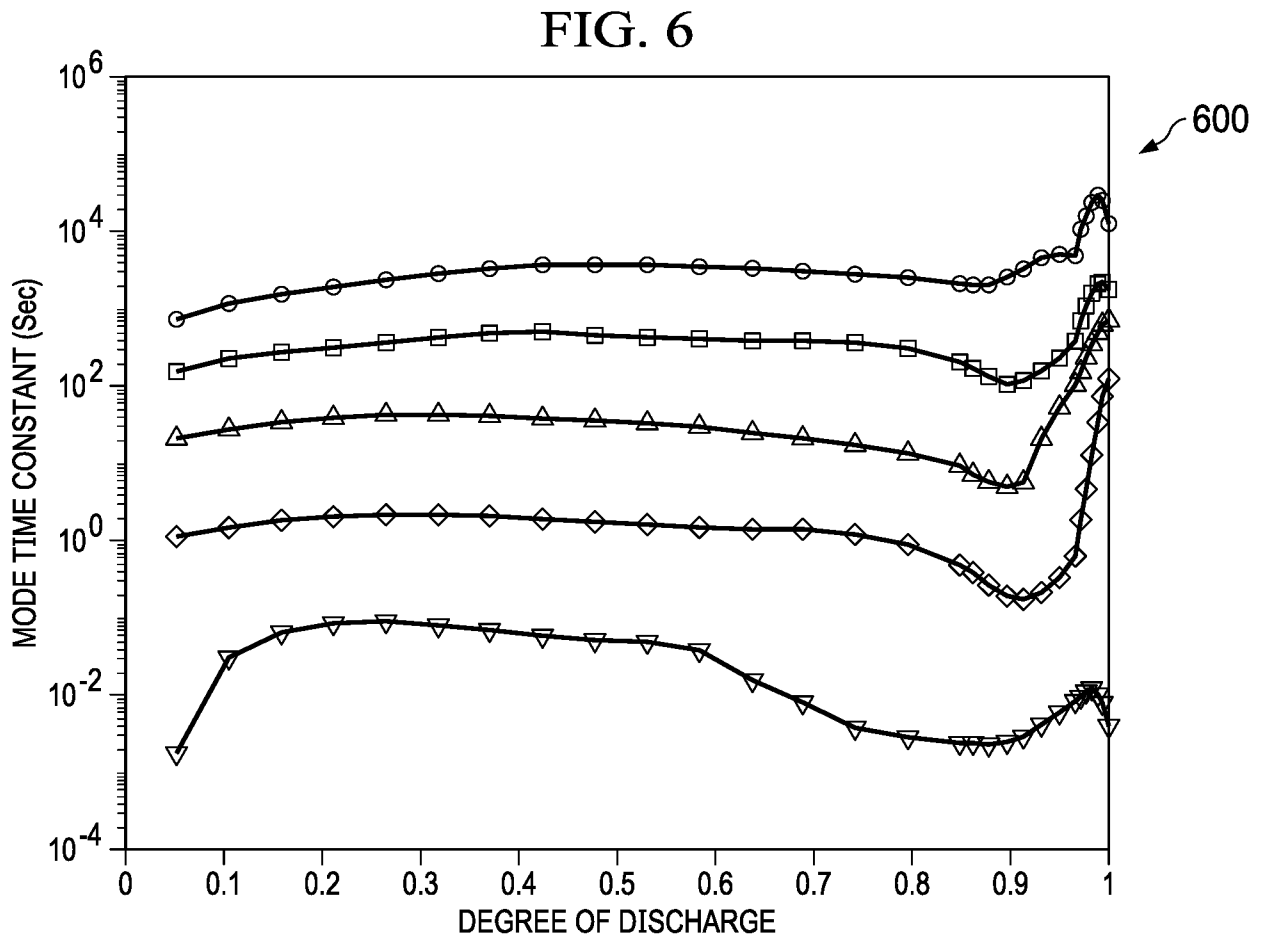
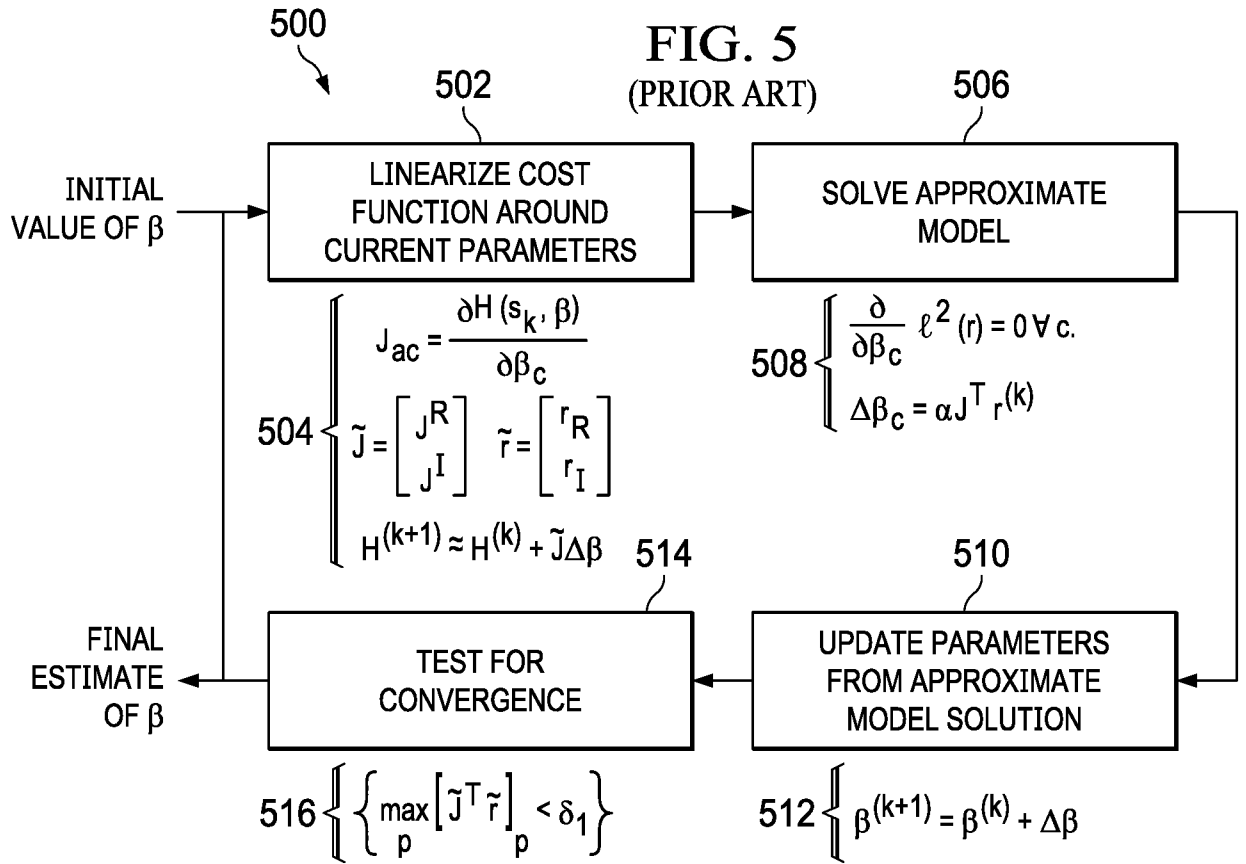


FIG. 4B



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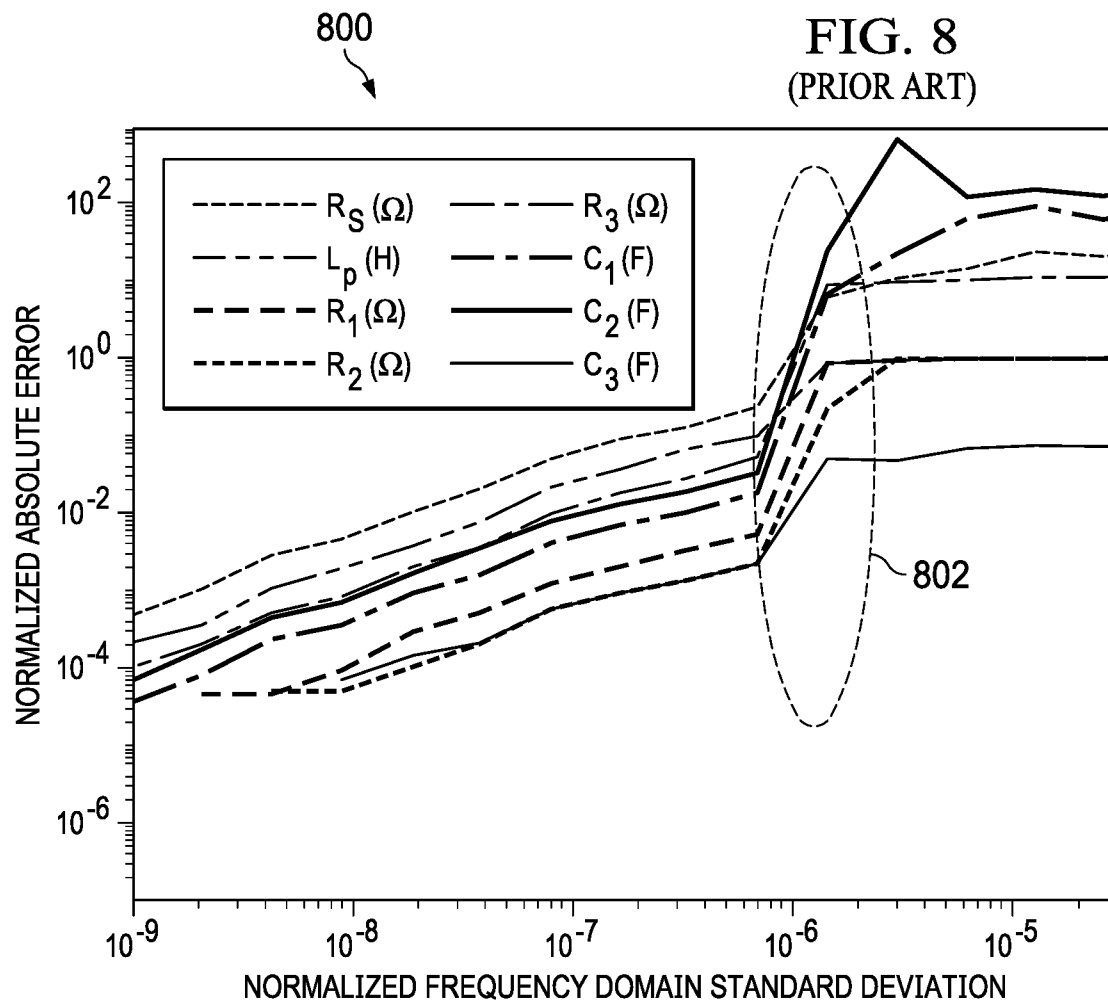
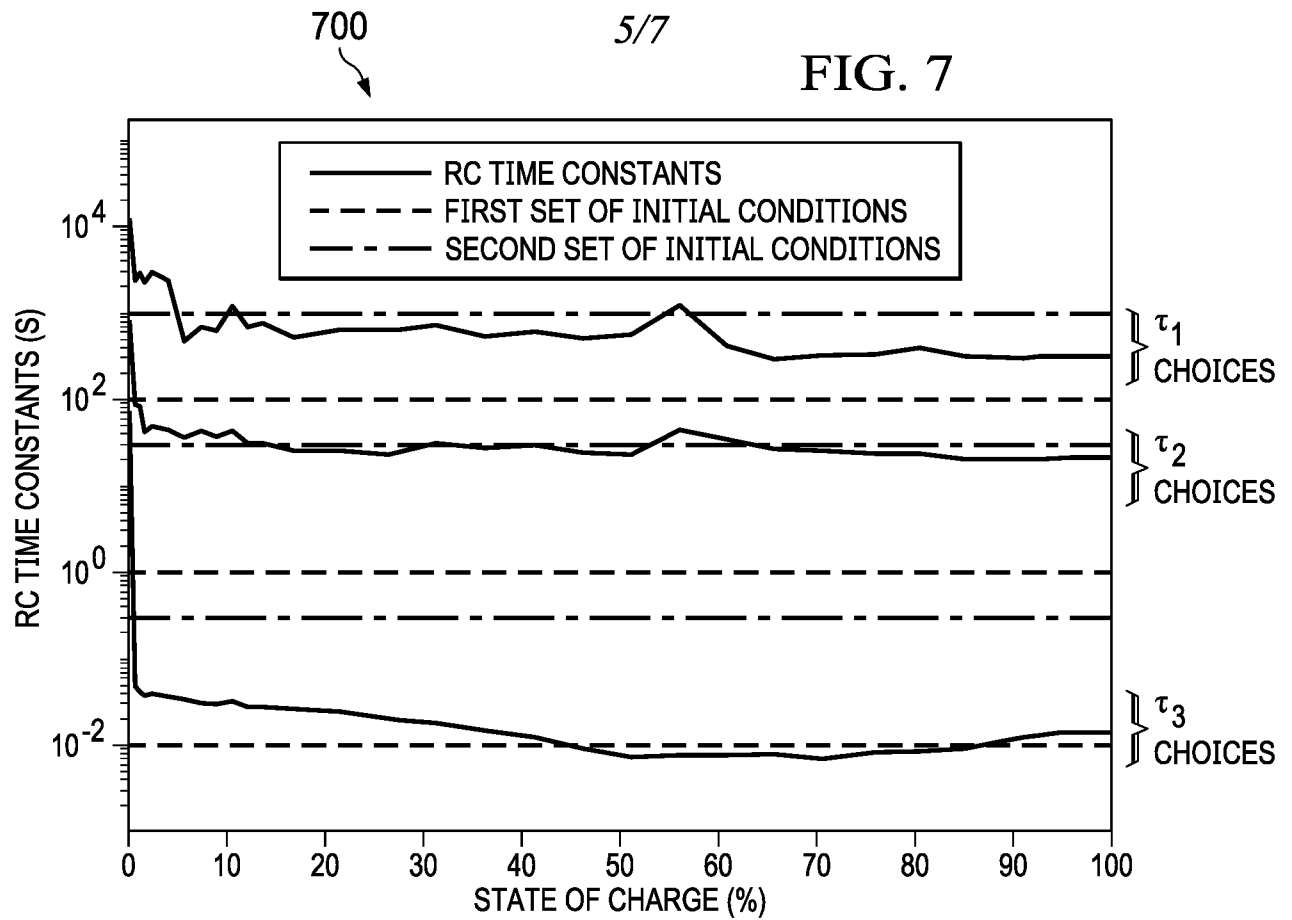


FIG. 9

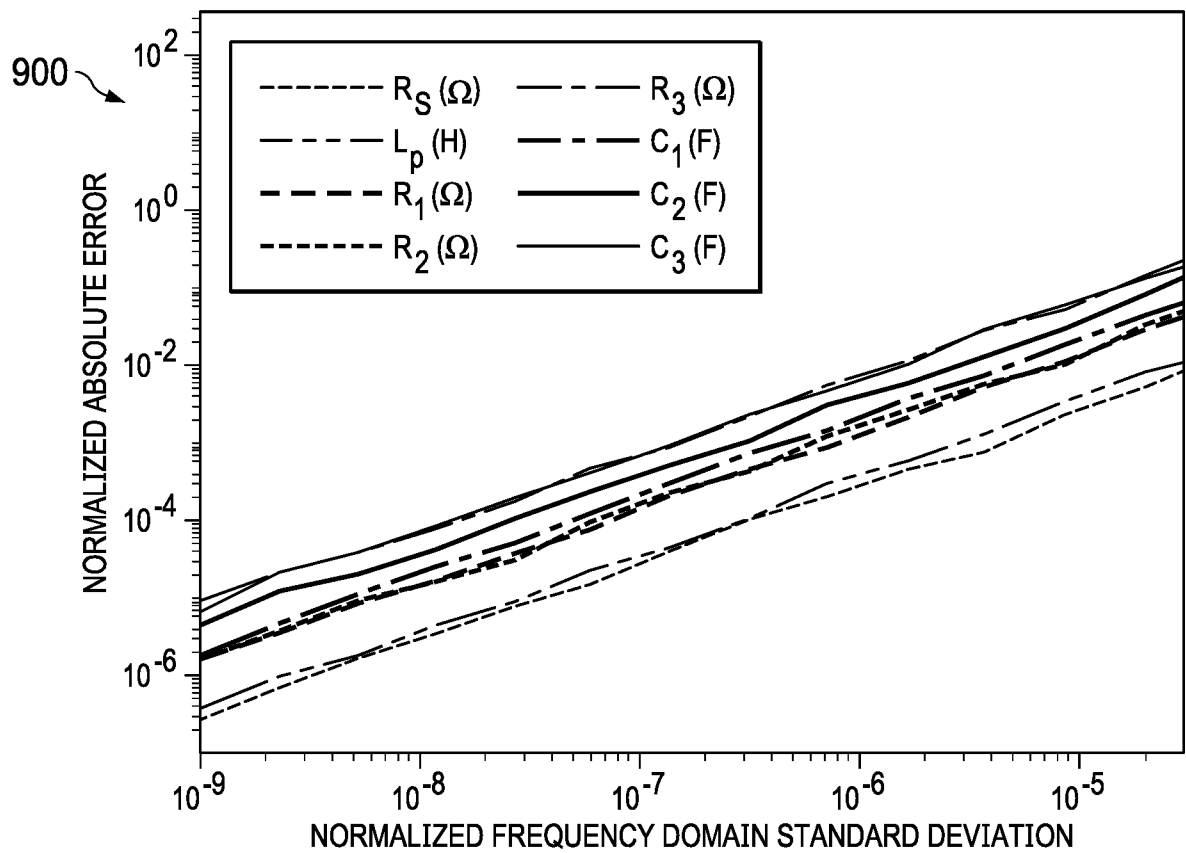
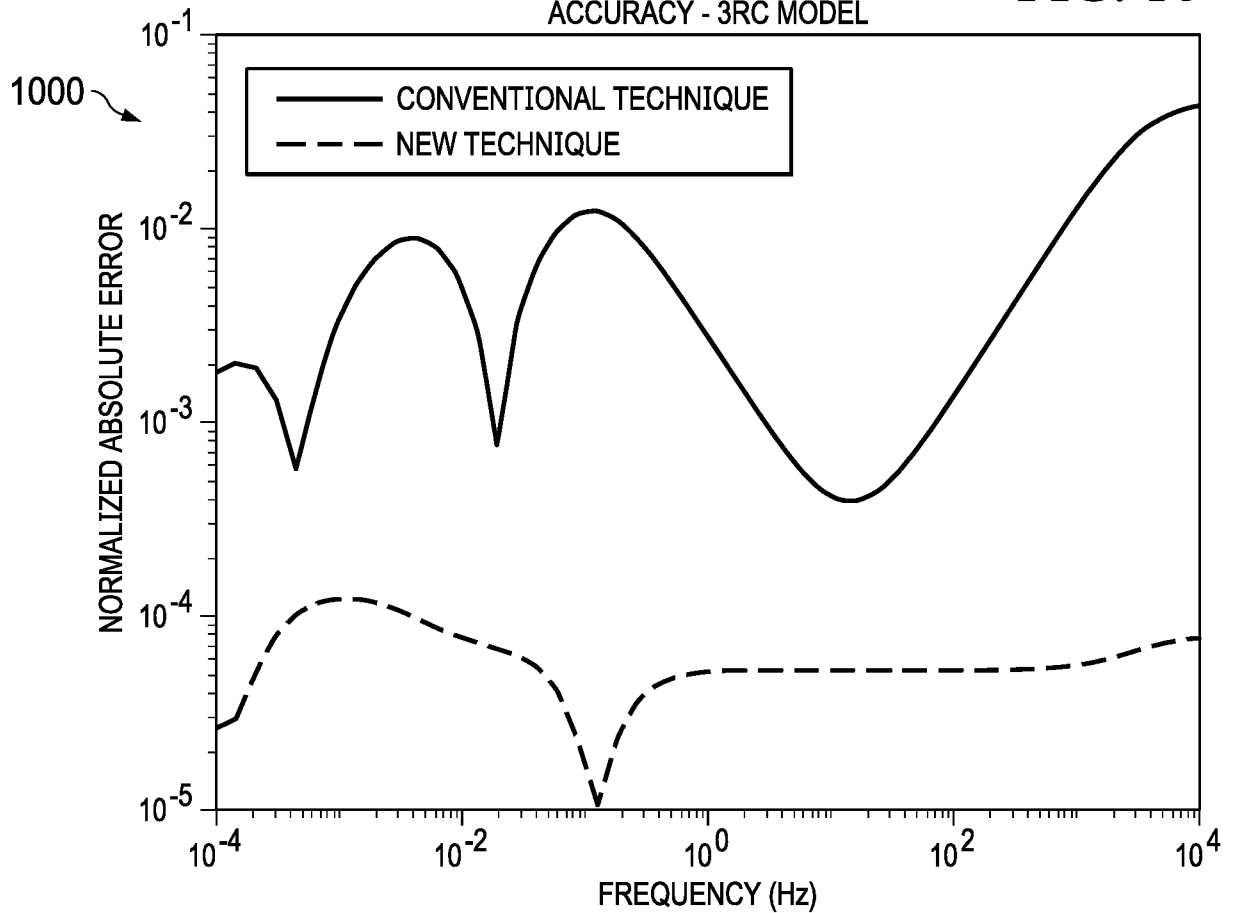
IMPEDANCE ESTIMATION
ACCURACY - 3RC MODEL

FIG. 10



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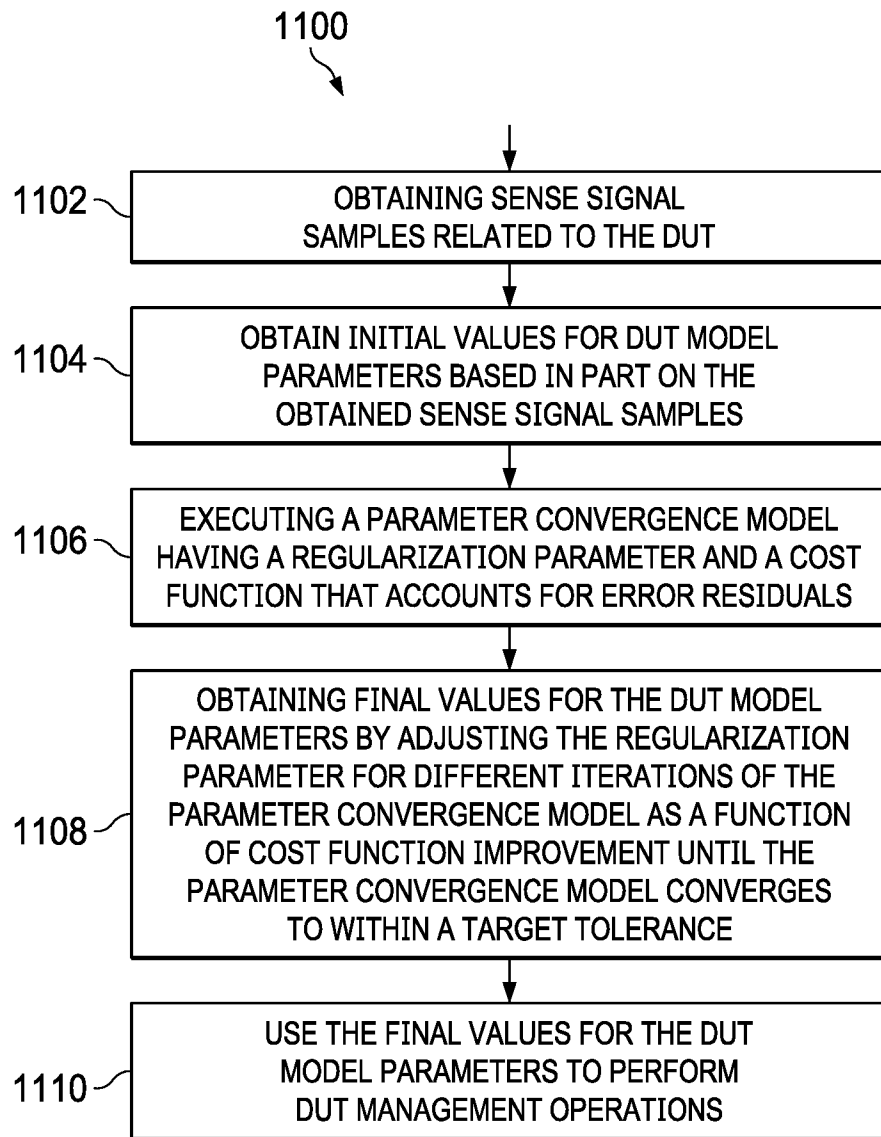


FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2021/060562

A. CLASSIFICATION OF SUBJECT MATTER		
G01R 31/367 (2019.01) G01R 31/374 (2019.01) G01R 31/3842 (2019.01)		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
G01R 31/367, G01R 31/374, G01R 31/3842		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 10191098 B2 (ROHDE & SCHWARZ GMBH & CO. KG) 29.01.2019	1-22
A	EP 0525124 B1 (EDWARDS LIFESCIENCES CORPORATION IRVINE) 05.03.2003	1-22
A	US 2015/0084576 A1 (TEXAS INSTRUMENTS INCORPORATED) 26.03.2015	1-22
☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.		
* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family	
"A" document defining the general state of the art which is not considered to be of particular relevance		
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"O" document referring to an oral disclosure, use, exhibition or other means		
"P" document published prior to the international filing date but later than the priority date claimed		
Date of the actual completion of the international search	Date of mailing of the international search report	
15 February 2022 (15.02.2022)	17 February 2022 (17.02.2022)	
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer T. Plotnikov Telephone No. (499) 240-25-91	