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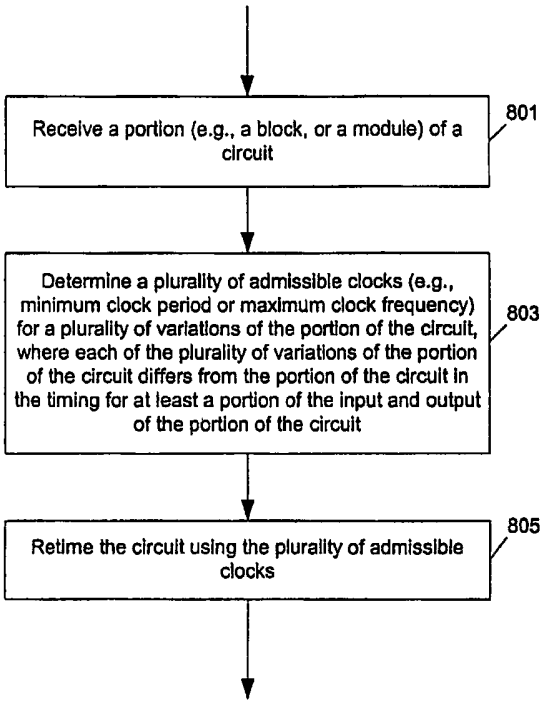
[Continued on next page]

(54) Title: METHOD AND APPARATUS FOR CIRCUIT DESIGN AND RETIMING



(57) Abstract: Methods and apparatuses to hierarchically retime a circuit. In at least one embodiment of the present invention, a module of a circuit is designed with a plurality of different latencies to have a plurality of different minimum clock periods (e.g., through retiming at the module level). In one example, the minimum clock periods are determined from detailed timing analyses after the placement and routine for the module; and, in retiming the circuit that contains the module, a data flow graph representation of the module is constructed based on the target clock period of the circuit and the correlation between the latencies and the minimum clock periods. In at least one embodiment of the present invention, hierarchical retiming is performed in which portions of the circuit is retimed to generate results (e.g., for different latencies), which are selectively used for the retiming of the entire circuit based on the target clock period.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

International Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F17/50

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 898 742 A (VAN DER WERF ET AL) 27 April 1999 (1999-04-27) column 1, line 7 - column 4, line 38 -----	1-17, 34-50, 67-83
X	EP 0 769 738 A (KABUSHIKI KAISHA TOSHIBA) 23 April 1997 (1997-04-23) column 1, line 5 - column 7, line 25 column 11, line 50 - column 13, line 49 ----- -/--	1-17, 34-50, 67-83

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 July 2005	10.10.05

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Anticoli, C

Form PCT/ISA/210 (second sheet) (January 2004)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	KUEHLMANN A ET AL: "Timing analysis in high-level synthesis" PROCEEDINGS OF THE IEEE/ACM INTERNATIONAL CONFERENCE ON COMPUTER AIDEDDESIGN (ICCAD). SANTA CLARA, NOV. 8 - 12, 1992, LOS ALAMITOS, IEEE COMP. SOC. PRESS, US, vol. CONF. 10, 8 November 1992 (1992-11-08), pages 349-354, XP010094525 ISBN: 0-8186-3010-8 abstract paragraphs [0001], [0002], [02.1], [0003]	1-17, 34-50, 67-83
X	GEBOTYS C H ET AL: "Optimal mapping of DSP application to architectures" SYSTEM SCIENCES, 1993, PROCEEDING OF THE TWENTY-SIXTH HAWAII INTERNATIONAL CONFERENCE ON WAILEA, HI, USA 5-8 JAN. 1993, LOS ALAMITOS, CA, USA,IEEE, US, vol. i, 5 January 1993 (1993-01-05), pages 116-123, XP010640453 ISBN: 0-8186-3230-5 abstract paragraph [0001] - paragraph [0003]	1-17, 34-50, 67-83

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2004/014225

Box II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-17, 34-50, 67-83

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-17, 34-50,67-83

Generating a plurality of circuit designs for a module all having deiffenrent latencies and corresponding feasable clock periods.

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2. claims: 18-33,51-66,84-99

Generating one circuit design by retiming a portion and then retiming the design which uses the retimed portion.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2004/014225

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5898742 A	27-04-1999	DE 69323692 D1	08-04-1999
		DE 69323692 T2	16-09-1999
		JP 6232735 A	19-08-1994
EP 0769738 A	23-04-1997	DE 69626596 D1	17-04-2003
		DE 69626596 T2	18-12-2003
		US 6101621 A	08-08-2000