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Dildy, Jr.

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[54] **HELIUM SPEECH DECODER**

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[52] **U.S. Cl.** ..... **179/1 SH**, 179/15.55 T

[51] **Int. Cl.** **G10l 1/00**

[58] **Field of Search** ..... 179/15 A, 15.55 T, 15.55 R

[56] **References Cited**

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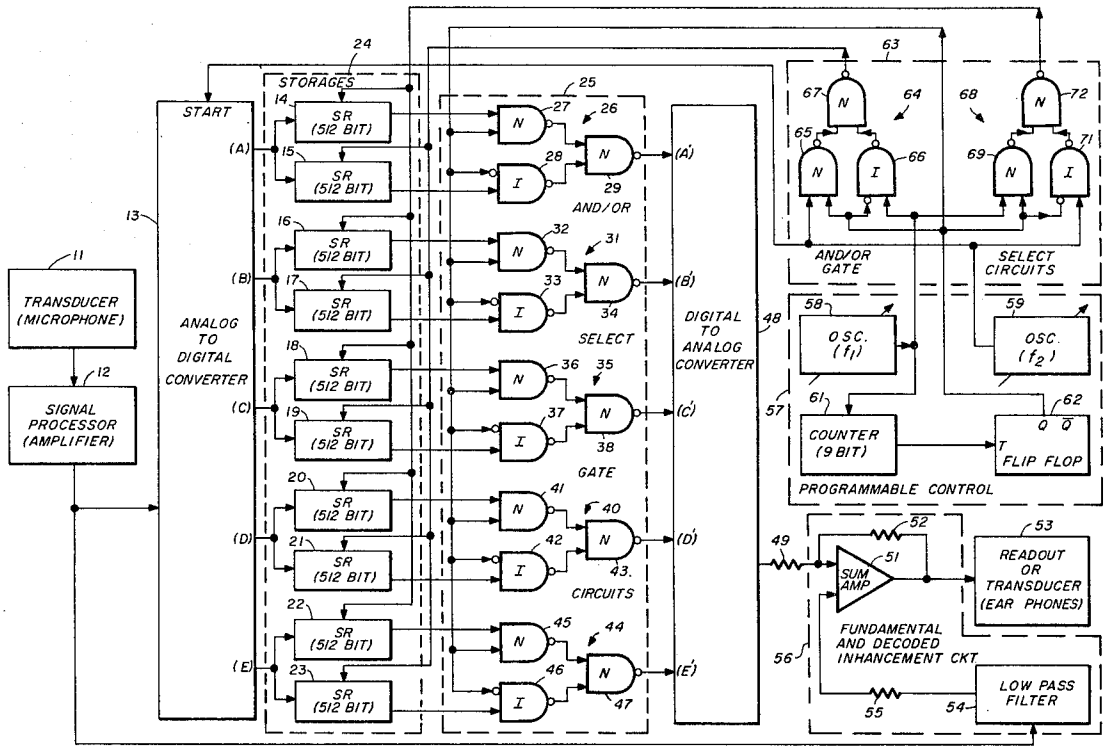
3,621,150	11/1971	Pappas	179/15.55 T
3,634,625	1/1972	Geohegan, Jr. et al.	179/SA

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[57] **ABSTRACT**

A helium speech decoder of the type that may be used to an advantage by divers living, working, and communicating in and from deep water habitats is disclosed as including a microphone, a digital-to-analog converter, a battery of pairs of shift registers, a like battery of select gate circuits, an analog-to-digital converter, and earphones. A programmable generator produces a plurality of control signals which are timely supplied to the aforementioned components as necessary to effect the concerted operation thereof in such manner as to cause a pitch scaling, reduction, or decoding of the human speech that is spoken in a pressurized helium-oxygen environment, without substantially changing the syllabic or word rate thereof. A filtered fundamental frequency of said human speech is optionally added to the decoded portion thereof to enhance the fidelity thereof.

2 Claims, 1 Drawing Figure



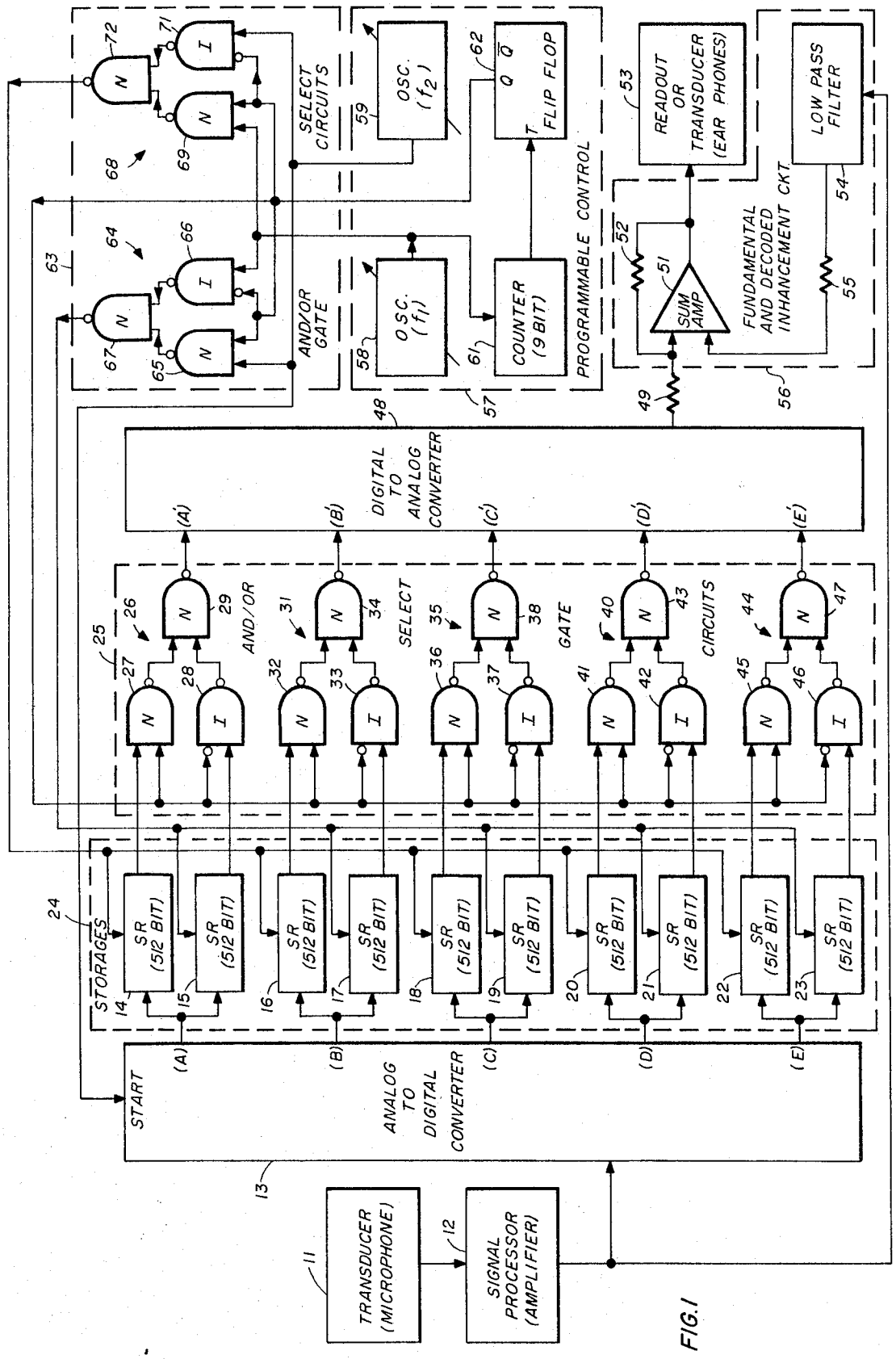

TRANSDUCER (MICROPHONE)
SIGNAL PROCESSOR (AMPLIFIER)
START
ANALOG TO DIGITAL CONVERTER
STORAGES
SR (5/2 BIT)
AND/OR GATE
SELECT CIRCUITS
DIGITAL TO ANALOG CONVERTER
SELECT CIRCUITS
OSC. (f1)
OSC. (f2)
COUNTER (9 BIT)
FLIP FLOP
PROGRAMMABLE CONTROL
SUM AMP
READOUT OR TRANSDUCER (EAR PHONES)
LOW PASS FILTER
FUNDAMENTAL AND DECODED INHANCEMENT CKT

FIG. 1

HELIUM SPEECH DECODER

STATEMENT OF GOVERNMENT INTEREST

The invention described herein may be manufactured and used by or for the Government of the United States of America for Governmental purposes without the payment of any royalties thereon or therefor.

FIELD OF THE INVENTION

The present invention relates, in general, to time compression and expansion of multi-frequency signals by sampling methods and means and, in particular, is an improved method and means for rescaling the pitch of human speech and other signals without adversely effecting the syllabic rate, word rate, or other intelligence parameters thereof. In even greater particularity, the subject invention is a speech processor which decodes the speech of a human diver or other being located in a helium-oxygen environment — such as, for instance, those environments found in undersea habitats disposed at various and sundry water depths or other ambient pressure environments that are considerably greater than the earth's typical atmospheric pressure — and reproduces it in a form that is intelligible to the human ear and intellect.

DESCRIPTION OF THE PRIOR ART

Heretofore, a number of techniques have been employed to expand speech in time. One of the simplest techniques used, to date, is to record the speech and then play it back at a speed that is slower than that used for the original recording. Unfortunately, the use of such technique resulted in a decrease in pitch in an amount that was proportional to the difference in the record and playback speeds. Of course, if the pitch of the speech were decreased enough to be operative for most practical purposes, the intelligibility thereof was adversely affected, often times to the extent that it was useless. Moreover, communication using such record-playback techniques could not, in many instances, be accomplished in real time, although it is recognized that the time delay involved, in most cases, could be relatively small, as far as recording and playback are concerned.

Another device of the prior art is shown in U.S. Pat. No. 3,621,150, entitled Speech Processor For Changing Voice Pitch, by George W. Pappas. The device taught therein purports to make speech of a diver located in a helium-oxygen atmosphere intelligible. In such case, the speech processor thereof makes use of the principle that normal speech may be chopped or segmented at certain rates and still retain its intelligibility. Once it is segmented into very small pieces, every other piece thereof is then discarded and the remaining pieces thereof are then recombined. The recombined pieces are then played back at a lower speed dependent upon the length of the discarded pieces by means of digital shift registers, the number of which may be considerable, in order to be effective. Hence, the number of components incorporated therein could be considerable, indeed, and the monetary cost and manufacturing complexities could be prohibited for many practical purposes.

U.S. Pat. No. 3,634,625, entitled Speech Unscrambler, by Geohagen, Jr., and Sherian, also discloses a prior art device which purports to covert shifted frequency speech which is relatively unintelligible into speech which is intelligible to human beings. In some respects, it is similar to the present invention and the aforesaid U.S. Pat. No. 3,621,150 to Pappas, in that it periodically samples speech signals which are converted to digital form, placed in storage, unloaded from said storage, and converted back to analog form before being read out or otherwise used. Of course, in spite of such similarities with the instant invention, there are also some dissimilarities, both structurally and functionally, which are significant, inasmuch as they constitute improvements in the speech processing effected thereby, thus effecting improved speech intelligence and fidelity.

Other prior art methods and means for processing speech are discussed in the aforementioned patents, but none thereof appear to anticipate the subject invention.

SUMMARY OF THE INVENTION

The subject invention is a new and unique speech processing device which renders frequency-shifted human speech within a predetermined pressurized helium-oxygen environment more intelligible than it otherwise would be if it were left in its unnatural, frequency-shifted, squeaky, "Donald Duck" form. Such speech processing occurs when speech signals are applied to a microphone for conversion from acoustical signals to electrical signals proportional thereto and the latter are then converted from analog signals to digital signals which are stored in a plurality of pairs of shift registers, alternate ones of which are then unloaded by a plurality of And/Or select gate circuits into a digital-to-analog converter for conversion of the digital signals alternately stored therein into analog signals proportional thereto, respectively. Said alternations are timely effected by another pair of And/Or select gate circuits which, in turn, are timely enabled by a programmable control circuit. In order to enhance the data output signal from the aforesaid digital-to-analog converter, and thus make the output signal therefrom more intelligible, a filtered fundamental signal from the aforesaid microphone is effectively combined therewith prior to be supplied to a readout, a transducer such as earphones, or the like, or to some other utilization apparatus. As a result, the communications between divers between a pressurized habitat and the communications between undersea divers and surface support people are facilitated.

It is, therefore, an object of this invention to provide an improved helium speech processor and decoder.

Another object of this invention is to provide an improved speech scaler.

Another object of this invention is to provide an improved signal expander, without adversely effecting the pitch or frequency thereof to the extent that it is no longer intelligible or useful.

A further object of this invention is to provide an improved method and means for discretely segmenting, delaying, and reconstructing predetermined portions of acoustical and electrical signals.

Another object of this invention is to provide an improved method and means for eliminating the squeaky "Donald Duck" effect from human speech that is spoken in pressurized helium-oxygen atmospheres, such as, for example, those which are employed as life-support atmospheres for divers or other air breathing

mammals working and living in deep underwater habitats.

Another object of this invention is to provide an improved method and means for sampling and expanding a speech or other acoustical or electrical signal containing a rather broadband of frequencies while retaining the essential pitch characteristics thereof which make them intelligible to the human ear and intellect.

Another object of this invention is to provide an improved signal scaler that may be miniaturized by means of hybrid technology, so that it may be easily carried and operated in otherwise inconvenient, difficult, or hazardous environments by swimmers, divers, or others.

Another object of this invention is to effect the reduction of the pitch of human speech signals without substantially changing the syllabic or word rates thereof.

Other objects and many of the attendant advantages will be readily appreciated as the subject invention becomes better understood by reference to the following detailed description, when considered in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1, the sole FIGURE of the drawing, is a combination block and schematic diagram of a preferred embodiment of the subject invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIG. 1, there is shown a transducer 11 which, in this particular instance, is preferably a microphone suitable for converting acoustical signals to a proportional electrical signals. However, it should be understood that transducer 11 may be an underwater electroacoustical transducer or any other device which is appropriate for converting any signals supplied thereto into signals which are suitable for being further processed by the subject invention.

The output of transducer 11 is connected to the input of a suitable signal processor 12 which may be, for instance, an amplifier or such other circuit arrangement which would facilitate the further processing thereof. The output of signal processor 12 is connected to the data signal input of an analog to digital converter 13 which, in this particular instance, also includes a start input and a quintet of outputs labeled (A), (B), (C), (D), and (E), respectively.

To the (A) output of analog-to-digital converter 13 are the data inputs of a first pair of 512 bit shift registers 14 and 15; to the (B) output of analog-to-digital converter 13 are the data inputs of a second pair of 512 bit shift registers 16 and 17; to the (C) output of analog-to-digital converter 13 are the data inputs of a third pair of 512 bit shift registers 18 and 19; to the (D) output of analog-to-digital converter 13 are the data inputs of a fourth pair of 512 bit shift registers 20 and 21; and to the (E) output of analog-to-digital converter 13 are connected the data signal inputs of a fifth pair of 512 bit shift registers 22 and 23. Of course, in this particular instance, the aforesaid shift registers 14 through 23, in fact, constitute storages 24.

The data signal outputs of each of the aforesaid shift registers 14 through 23 are connected to a like plurality of inputs of a quintet of And/Or select gate circuits 25 in the following manner:

A first And/Or select gate 26 includes a NAND gate 27 having a pair of inputs and an output, with one of the inputs thereof connected to the data signal output of shift register 14; an inhibit gate 28 having a pair of inputs and an output, with one of the inputs thereof connected to the data output of shift register 15; and another NAND gate 29 having a pair of inputs and an output, with the inputs thereof respectively connected to the outputs of NAND gate 27 and inhibit gate 28.

A second And/Or select gate 31 has a NAND gate 32 having a pair of inputs and an output, with one of the inputs thereof connected to the data output of shift register 16; an inhibit gate having a pair of inputs and an output, with one of the inputs thereof connected to the data output of shift register 17; and another NAND gate having a pair of inputs and an output, with the inputs thereof respectively connected to the outputs of NAND gate 32 and inhibit gate 33.

A third And/Or select gate 35 has a NAND gate 36 having a pair of inputs and an output, with one of the inputs thereof connected to the data output of shift register 18; an inhibit gate having a pair of inputs and an output, with one of the inputs thereof connected to the output of shift register 19; and a NAND gate 38 having a pair of inputs and an output, with the inputs thereof respectively connected to the outputs of NAND gate 36 and inhibit gate 37.

A fourth And/Or select gate 40 has a NAND gate 41 having a pair of inputs and an output, with one of the inputs thereof connected to the data signal output of shift register 20; an inhibit gate having a pair of inputs and an output, with one of the inputs thereof connected to the data output of shift register 21 and another NAND gate having a pair of inputs and an output, with the inputs thereof respectively connected to the outputs of NAND gate 41 and inhibit gate 42.

A fifth And/Or select gate 44 includes a NAND gate 45 having a pair of inputs and an output, with one of the inputs thereof connected to the data outputs of shift register 22; an inhibit gate 46 having a pair of inputs and an output, with one of the inputs thereof connected to the data output of shift register 23; and another NAND gate 47 having a pair of inputs and an output, with the inputs thereof respectively connected to the outputs of NAND gates 45 and inhibit gate 46.

The five outputs from NAND gates 29, 34, 38, 43, and 47 constitute the outputs from And/Or select gate circuits 25 and are respectively connected to a like number of inputs of a digital-to-analog converter 48, hereby designated as being (A'), (B'), (C'), (D'), and (E'), respectively.

The data signal output of digital-to-analog converter 48 is connected through a voltage dropping resistor 49 to one of the inputs of a summing amplifier 51, with said one input thereof also connected through a voltage dropping resistor 52 to the output thereof. The output of summing amplifier 51 is connected to the input of a readout or transducer 53 which, in this particular instance, is preferably a pair of earphones. Of course, readout or transducer 53 may be such as would enable it to interface with the input of any suitable utilization apparatus (not shown).

The data signal output of signal processor (amplifier) 12 includes the fundamental frequency signal which is processed by the aforementioned combination of components. Hence, it is also connected to the input of a low pass filter 54, the output of which is connected

through a voltage dropping resistor **55** to the other input of the aforesaid summing amplifier **51.** As may readily be seen, such arrangement of summing amplifier **51,** low pass filter **54,** and voltage dropping resistor **55** constitute an ancillary but important circuit **56** which enhances both the fundamental and decoded signals supplied from signal processor **12** and digital-to-analog converter **48,** respectively. Such enhancement is intended and does improve the fidelity and intelligence of the equivalent of the original speech signal supplied to earphone of transducer **53.**

A programmable controller **57** is employed to provide the proper timing signals for the subject invention. It includes a read clock oscillator **58** which produces a first frequency (f_1) of, for example, 10,000 cycles per second. It also includes a write clock oscillator **59** which generates a second frequency signal (f_2) having a frequency of, for example, 20,000 cycles per second. The output of read clock oscillator **58** is connected to the input of a nine bit counter **61,** the output of which is connected to the toggle input of the bistable multivibrator or flip-flop **62,** the latter of which has both a Q output and a Q output. The output of read clock oscillator **58,** the output of write clock oscillator **59,** and the Q output of flip-flop **62** are all connected to a like plurality of inputs of a pair of And/Or select gate circuits **63.**

Included in said And/Or select gate circuit **63** is a first select gate **64** which includes a NAND gate **65** having a pair of inputs and an output, with one of the inputs thereof connected to the output of the aforesaid write clock oscillator **59;** an inhibit gate **66** having a pair of inputs and an output, with one of the inputs thereof connected to the output of the aforesaid read clock oscillator **58;** and another NAND gate **67** having a pair of inputs and an output, with the inputs thereof respectively connected to the outputs of NAND gate **65** and inhibit gate **66.** Also included is another And/Or select gate **68** which includes a NAND gate **69** having a pair of inputs and an output, with one of the inputs thereof connected to the output of the aforesaid read clock oscillator **58,** and with the other input thereof connected to the Q output of the aforesaid flip-flop. An inhibit gate **71** has a pair of inputs and an output, with one of the inputs thereof connected to the Q output of the aforesaid flip-flop **62** and the remaining inputs of the aforsaid NAND gate **65** and inhibit gate **66** of And-/Or select gate **64,** and with the other inputs thereof connected to the output of the aforesaid write clock oscillator **59;** and a NAND gate **72** having a pair of inputs and an output, with the inputs thereof respectively connected to the outputs of NAND gate **69** and inhibit gate **71.**

The outputs of NAND gates **67** and **72,** in this particular instance, constitutes the outputs of And/Or select gate circuit **63.** Hence, the output of NAND gate **67** is connected to the shift inputs of shift registers **15, 17, 19, 21,** and **23.** And, the output of NAND gate **72** is connected to the shift inputs of shift registers **14, 16, 18, 20,** and **22.**

The Q output of flip-flop **62** is also connected to the remaining inputs of the aforesaid NAND gate **27,** inhibit gate **28,** NAND gate **32,** inhibit gate **33,** NAND gate **36,** inhibit gate **37,** NAND gate **41,** inhibit gate **42,** NAND gate **45,** and inhibit gate **46.**

The output of write clock oscillator **59** is also connected to the start input of the aforesaid analog-to-digital converter **13** for the timely starting thereof.

MODE OF OPERATION

The operation of the invention will now be discussed briefly in conjunction with FIG. **1,** the sole FIGURE of the drawing.

Due to the physiological limitations of human beings and other beings that breathe air at typical earth atmospheric pressures, it is necessary to replace air with mixtures of helium-oxygen or helium-nitrogen-oxygen, in order to eliminate or reduce the effects of narcosis on divers living and working in deep water habitats or other abnormally pressurized vessels. But, unfortunately, such gaseous mixtures adversely affect the speech of such divers, in that it becomes sufficiently frequency shifted in helium atmospheres to be high-pitched, even making it unintelligible under certain conditions. In such instances, although the fundamental voice frequency remains substantially unaffected at approximately 100 hertz, the voice harmonics are shifted upward in frequency, with the amount of shift effected being contingent upon the helium gas mixture involved, its pressure, and the length of time the diver has been living or working in such helium gas mixture environment. More particularly, as a result of such frequency up-shiftig of the diver's speech, to the ear and intellect of a person with whom he is attempting to communicate, such speech becomes high-pitched, squeaky, and Donald Duck-like, sometimes to the extent that it is not understandable, at least in part.

It is, thus, the primary intended function of the subject helium speech decoder invention to process such highly pitched speech in such manner that the pitch thereof will be reduced to a frequency that is readily discerned by people, including the person speaking, and the person or persons listening thereto, and to do it in real time, thereby allowing substantially normal communication to occur between two or more people located with a pressurized helium habitat or between two or more people located at differently pressurized habitats, such as, for example, between a deep water diver and a surface located human associate.

With this in mind, the operation of the subject invention will be discussed in such context; however, it should be understood that its uses — and, hence, the scope of its operations — are numerous and, therefore, may be entirely different, depending upon the structural combination within which it is incorporated during any given operational circumstance. Of course, it would be well within the purview of the artisan having the benefit of the teachings presented herewith to employ the subject invention in conjunction with and in combination with whatever other apparatus he desires for his intended purpose, even though such purpose and the operations concomitant therewith are not discussed at this time.

For the purpose of keeping this disclosure as simple as possible, but without limitation, it will be assumed that transducer **11** is a microphone into which a diver located in a pressurized helium-oxygen environment speaks, and transducer **53** is a pair of earphones worn by some other person located at any given place who wants to hear what the aforesaid diver says. Of course, it should be understood that any other communication arrangements or situations may occur in which the in-

stant invention may be used to an advantage, including its use as telemtering links betwen two or more otherwise incompatible pieces of apparatus.

As the diver's frequency-shifted, squeaky, "Donald Duck" sounding speech is supplied to microphone **11**, it is converted into electrical signals that are proportional thereto. Then, said speech equivalent electrical signals are conventionally processed by signal processor **12** — as by amplifying, filtering, etc. — to the state where they are optimized or at least suitable to be supplied as an analog signal to the input of analog-to-digital converter **13**.

In this particular preferred embodiment, analog-to-digital (A/D) converter **13** is a five bit word parallel A/D converter; however, if so desired, it may be a larger bit word parallel A/D converter, too.

As a result of the A/D conversion, the speech signal is now in digital form with its amplitude represented by five bits — that is, a five bit word — at the outputs thereof, all of which are supplied for a timely storage in alternate shift registers of five pairs of shift registers, respectively. Of course, said shift registers are always operatively storing signals whenever the entire invention is in an operative condition, although some of said storage may be zero.

In order to more fully understand the operation of shift registers **14** through **23** — that is, storages **24** — and their associated And/Or select gate circuits **25**, reference is now made to programmable controller **57** and its associated And/Or select gate circuits **63**. Two clock oscillators, herein defined as being read clock oscillator **58** and write clock oscillator **59**, produce two basic clock signals having frequencies f_1 and f_2 of, for example, 10 KHz and 20 KHz, respectively.

The f_1 signal is supplied to **9** stage counter **61**, which produces an output signal every 512 cycles (or bits) of f_1. Because said output signal from counter **61** is supplied to the toggle input of flip-flop **62**, said flip-flop **62** changes state every 512 cycles of read clock **58**.

As may readily be seen, the output of read clock oscillator **58** supplies a signal with an f_1 frequency to one of the inputs of inhibit gate **66** and Nand gate **69**, and the output of write clock oscillator **59** is connected to supply a signal with an f_2 frequency to one of the inputs of NAND gate **65** and inhibit gate **71**. Moreover, the Q output of flip-flop **62** is connected to alternately supply a 1 or a 0 signal to the remaining inputs of NAND gate **65**, inhibit gate **66**, NAND gate **69**, and inhibit gate **71** every 512 cycles of f_1, as a result of its changing state at such times.

Whenever Q of flip-flop **62** is a 1, for example, said 1 signal enables NAND gates **65** and **69** and disables inhibit gates **66** and **71**, thereby allowing the f_2 signal (20 KHz) to pass through NAND gate **65** and NAND gate **67** (which, in effect, acts like an OR gate) to become the output signal from And/Or select gate **64**, and also thereby allowing the f_1 signal (10 KHz) to pass through NAND gate **69** and NAND gate **72** (which, in effect, also acts like an OR gate) to become the output signal from And/Or select gate **68**. Of course, when Q of flip-flop **62** is a 0, the opposite occurs, and f_1 becomes the output signal from And/Or select gate **64** and f_2 becomes the output signal from And/Or select gate **68**. Thus, it may readily be seen that for every 512 cycles of read oscillator **58**, the outputs from select gates **64** and **68** alternate from f_2 to f_1 to f_2 to f_1, and so on, in such manner (or with such program) that when one is f_2 to other is f_1 and vice versa.

In the example being discussed, when a 1 occurs at Q of flip-flop **62**, f_2 is supplied to the shift inputs of odd numbered shift registers **15, 17, 19, 21,** and **23**, and f_1 is supplied to the shift inputs of even numbered shift registers **14, 16, 18, 20,** and **22**. At such instance, the odd numbered shift registers would be shifted at the rate of 20 KHz, and the even numbered shift registers would be shifted at the rate of 10 KHz.

Because the start sample input of the aforesaid parallel analog-to-digital converter **13** is connected to the output of write clock oscillator **59**, the speech will be effectively sampled at the rate of f_2 by said analog-to-digital converter **13**.

The five parallel output signals from analog-to-digital converter **13** are simultaneously supplied to the inputs of five pairs of 512 bit shift register storage devices; however, since the shifting of the odd numbered shift registers alternate with the shifting of the even numbered shift registers, the signals received from the aforesaid five parallel outputs of analog-to-digital converters **13** are alternately stored therein while they are being shifted therethrough. For example, the digital signals from output (A) is alternately stored in shift registers **14** and **15**, the digital signal from output (B) is alternately stored in shift registers **16** and **17**, and so on.

As a result of the alternate 0 and 1 output signals from the Q of output of flip-flop **62** being supplied to the control inputs of the respective NAND and inhibit gates of And/Or select gates **26, 31, 35, 40,** and **44**, alternate ones of pairs of shift registers **14** and **15, 16** and **17, 18** and **19, 20** and **21,** and **22** and **23** are unloaded every **512** cycles of the f_1 output signal from read clock oscillator **58** into the (A'), (B'), (C'), (D'), and (E') inputs of digital-to-analog converter **48**, where they are converted back to a single continuous analog signal that is proportional thereto. Of course, said single continuous analog signal constitutes the reconstructed speech signal and, thus, has a lower frequency or pitch than the original speech signal supplied by the diver to transducer **11**.

After suitable voltage regulation for optimization purposes has been effected by resistor **49**, the reconstructed speech (or data) signal is supplied to summing amplifier **51**, where it has added thereto the fundamental frequency portion of the original speech signal from signal processor **12** after it has been likewise optimized by filtering in low pass filter **54** and voltage regulated by resistor **55**. The output signal from summing amplifier **51** is, thus, an enhanced representation of the reconstructed speech signal which by comparison with the original speech signal is considerably more intelligible and, therefore, more useful to the listeners thereof who may be listening by means of transducer or earphones **53**.

From the foregoing, it may readily be seen that all signal frequencies below $f_1/512$ are unchanged, but that all signal frequencies above $f_1/512$ are shifted downward by a factor equal to f_2/f_1. This, of course, means that, for the most part, the signal frequencies in the speech will be lowered but the syllabic and word rates will remain unchanged, thereby causing the intelligibility thereof to be retained sufficiently to be understood by human beings.

Obviously, other embodiments and modifications of the subject invention will readily come to the mind of

one skilled in the art having the benefit of the teachings presented in the foregoing description and the drawings. It is, therefore, to be understood that this invention is not to be limited thereto and that said modifications and embodiments are intended to be included within the scope of the appended claims.

What is claimed is:

1. A data signal decoder, comprising in combination:

means for receiving and transducing a predetermined data signal into an electrical analog signal that is proportional thereto;

means having a data signal input, a start signal input, and a plurality of outputs, with the data signal input thereof effectively connected to the output of said receiving and transducing means for converting said electrical analog signal into a digital word signal represented by a plurality of bits respectively available at the aforesaid plurality of outputs thereof in response to a predetermined start signal supplied to the start signal input thereof;

a plurality of pairs of shift registers, each pair of shift registers of which include an odd numbered shift register and an even numbered shift register, each shift register of which has a data signal input, a shift signal input, and a data signal output, with the odd and even numbered shift registers of each pair of shift registers of said plurality of pairs of shift registers having their data signal inputs interconnected and respectively connected to the plurality of outputs of said analog-to-digital signal converting means in such manner as to timely receive and store said plurality of bits therein in response to a predetermined pair of shift signals respectively supplied to the shift signal inputs thereof, with the shift signal inputs of said odd numbered shift registers being interconnected for simultaneous response to one of the aforesaid predetermined pair of shift signals, and with the shift signal inputs of said even numbered shift registers being interconnected for simultaneous response to the other of the aforesaid predetermined pair of shift signals;

a plurality of And/Or select gates, each of which has a pair of data signal inputs, a pair of interconnected gating control signal inputs, and a data signal output, with the pairs of data signal inputs of each And/Or select gate thereof respectively connected to the outputs of the odd and even numbered shift registers of each pair of shift registers of said plurality of pairs of shift registers for timely passing therethrough the bits stored in said odd and even numbered shift registers in response to a predetermined programmed gating control signal supplied to the interconnected gating control signal inputs thereof;

means having a plurality of inputs responsive to a digital word signal that contains the same number of bits as the number of inputs thereof respectively connected to the data signal outputs of said plurality of And/Or select gates for converting the digital word signal received therefrom into an electrical analog signal that is proportional thereto; and

programmable means connected to the start signal input of said electrical analog signal to digital word signal converting means, to the interconnected shift signal inputs of the odd and even numbered shift registers of the pairs of shift registers of said plurality of pairs of shift registers, to the interconnected gating control signal inputs of the afroresaid plurality of And/Or select gates for timely supplying said start signal, said predetermined pair of shift signals, and the aforesaid predetermined programmed signal thereto respectively, wherein said programmable means connected to the start signal input of said electrical analog signal to digital word signal converting means, to the interconnected shift signal inputs of the odd and even numbered shift registers of the pairs of shift registers of said plurality of pairs of shift registers, to the interconnected gating control signal inputs of the aforesaid plurality of And/Or select gates for timely supplying said start signal, said predetermined pair of shift signals, and the aforesaid predetermined programmed signal thereto comprises:

a read clock oscillator for producing a first clock signal having a predetermined first frequency at the output thereof;

a write clock oscillator for producing a second clock signal having a predetermined second frequency at the output thereof, with the output thereof connected to the start signal input of the aforesaid electrical analog signal to digital word signal converting means;

a counter connected to the output of said read clock oscillator;

a flip-flop having a toggle input, a Q output, and a Q output, with the toggle input thereof connected to the output of said counter, and with the Q output thereof connected to the interconnected gating inputs of the aforesaid plurality of And/Or select gates;

another And/Or select gate having a pair of data signal inputs, a pair of interconnected gating control signal inputs, and an output with one of the data signal inputs thereof connected to the output of said write clock oscillator, with the other data signal input thereof connected to the output of said read clock oscillator, with the interconnected gating control signal inputs thereof connected to the Q output of said flip-flop, and with the output thereof connected to the interconnected shift signal inputs of the aforesaid odd numbered shift registers; and

still another And/Or select gate having a pair of data signal inputs, a pair of interconnected gating control signal inputs, and an output, with one of the data signal control inputs thereof connected to the output of said read clock oscillator, with the other data signal input thereof connected to the output of said write clock oscillator, with the interconnected gating control signal inputs thereof connected to the Q output of said flip-flop, and with the output thereof connected to the interconnected shift signal inputs of the aforesaid even numbered shift registers.

2. The device of claim 1, wherein:

the first frequency of the first clock signal from the read clock oscillator is of the order of 10,000 cycles per second;

the second frequency of the second clock signal from the write clock oscillator is of the order of 20,000 cycles per second; and

said counter connected to the output of said read clock oscillator is a nine stage counter.

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