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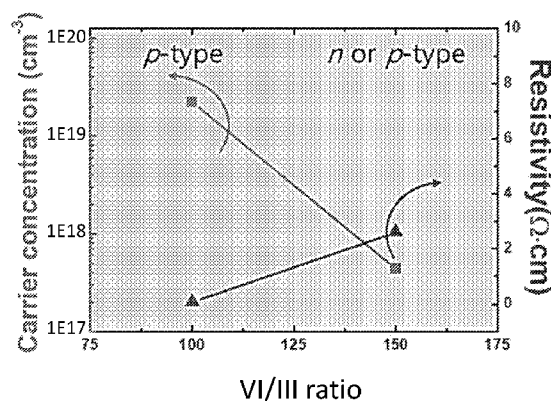


FIG. 1A

(57) Abstract: Methods of forming a p-type IV-doped III-VI semiconductor are provided which comprise exposing a substrate to a vapor composition comprising a group III precursor comprising a group III element, a group VI precursor comprising a group VI element, and a group IV precursor comprising a group IV element, under conditions to form a p-type IV-doped III-VI semiconductor via metalorganic chemical vapor deposition (MOCVD) on the substrate. Embodiments make use of a flow ratio defined as a flow rate of the group VI precursor to a flow rate of the group III precursor wherein the flow ratio is below an inversion flow ratio value for the IV-doped III-VI semiconductor.



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AMPHOTERIC P-TYPE AND N-TYPE DOPING OF GROUP III-VI SEMICONDUCTORS WITH GROUP-IV ATOMS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims priority to U.S. Provisional Patent Application No. 62/623,183 that was filed January 29, 2018, the entire contents of which are hereby incorporated by reference.

REFERENCE TO GOVERNMENT RIGHTS

[0002] This invention was made with government support under ECCS-1748339 awarded by the National Science Foundation. The government has certain rights in the invention.

BACKGROUND

[0003] $(\text{Al}, \text{In}, \text{Ga})_2\text{O}_3$ represents a newly developing III-VI family of semiconducting oxide materials. It holds great promise, but currently suffers from an inability to achieve effective p-type doping. The material is typically doped using silicon (Group-IV) to substitute for gallium (or aluminum or indium) to achieve a n-type material. Magnesium (Group-II) has been used to substitute for the same gallium (or aluminum or indium) to achieve a p-type material. However, this requires the addition of a separate magnesium source. In addition, magnesium exhibits a large memory effect in metalorganic chemical vapor deposition (MOCVD) growth which means it is difficult to obtain p-n heterojunctions where the p-type material is grown first.

SUMMARY

[0004] Provided are methods of forming IV-doped III-VI semiconductors, including p-type III-VI semiconductors doped with Si. Also provided are the IV-doped III-VI semiconductors and devices incorporating the IV-doped III-VI semiconductors.

[0005] In an aspect, methods of forming a p-type IV-doped III-VI semiconductor are provided which comprise exposing a substrate to a vapor composition comprising a group III precursor comprising a group III element, a group VI precursor comprising a group VI element, and a group IV precursor comprising a group IV element, under conditions to form a p-type IV-doped III-VI semiconductor via metalorganic chemical vapor deposition

(MOCVD) on the substrate. Embodiments make use of a flow ratio defined as a flow rate of the group VI precursor to a flow rate of the group III precursor wherein the flow ratio is below an inversion flow ratio value for the IV-doped III-VI semiconductor.

[0006] In another aspect, a p-type IV-doped III-VI semiconductor is provided which comprises a group III element, a group VI element and a group IV element.

[0007] Other principal features and advantages of the disclosure will become apparent to those skilled in the art upon review of the following drawings, the detailed description, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Illustrative embodiments of the present disclosure will hereafter be described with reference to the accompanying drawings.

[0009] FIG. 1A shows a plot of carrier concentration as a function of VI-III flow ratio for $\text{Ga}_3\text{O}_2\text{:Si}$ formed according to an illustrative embodiment. FIG. 1B shows a plot of Hall mobility as a function of VI-III flow ratio for $\text{Ga}_3\text{O}_2\text{:Si}$ formed according to an illustrative embodiment.

[0010] FIG. 2A shows a cross-sectional view of a schematic of a field effect transistor (FET) with a fin structure fabricated using p-type $\text{Ga}_3\text{O}_2\text{:Si}$ according to an illustrative embodiment. FIG. 2B shows a perspective view of the fin-FET.

[0011] FIG. 3A is a plot of the I-V curve and FIG. 3B is a plot of the transfer characteristics at $V_{\text{DS}} = 20 \text{ V}$ of a p-type $\text{Ga}_2\text{O}_3\text{:Si}$ $3 \mu\text{m}$ by $3 \mu\text{m}$ fin array fin-FET (shown in FIGs. 2A and 2B). The fin-FET shows an on/off ratio of 10^6 and a breakdown voltage of over 150 V.

[0012] FIG. 4A shows an XRD omega/2theta scan of $\sim 150 \text{ nm}$ thick $\text{Ga}_2\text{O}_3\text{:Si}$ grown using a VI/III ratio of 150 (top), at a VI/III ratio of 100 (middle) and an XRD omega/2theta scan of a $\beta\text{-Ga}_2\text{O}_3$ substrate (TAMURA Corp) (bottom). FIG. 4B shows a TEM image of typical morphology of the $\sim 150 \text{ nm}$ thick $\text{Ga}_2\text{O}_3\text{:Si}$ on sapphire. The inset shows SAED patterns obtained along the $[5\text{-}10]$ zone axis at the $\kappa\text{-Ga}_2\text{O}_3/\text{Al}_2\text{O}_3$ interface.

[0013] FIG. 5A shows the carrier concentration and resistivity of $\text{Ga}_2\text{O}_3\text{:Si}$ on sapphire (0001) as a function of growth temperature at VI/III ratio of 150 and FIG. 5B shows the same

at a VI/III ratio of 100. FIG. 5C shows the Hall mobility of Ga₂O₃:Si on sapphire (0001) as a function of growth temperature at VI/III ratio of 100 and 150.

[0014] FIG. 6 shows I-V curves of ~ 150 nm thick *p*-type Ga₂O₃:Si on sapphire (0001) from V_{GS} = -10 to 40 V and the inset is an optical microscope image of the fabricated device.

[0015] FIG. 7A show schematic illustrations of 2D *p*-type Ga₂O₃:Si channel microstrip array FETs with details of device scale FIG. 7B shows an optical micrograph of the fabricated device.

[0016] FIG. 8A shows I-V curves from V_{GS} = -50 to 100 V. The inset is an optical micrograph of the probing. FIG. 8B shows simulation data of I-V curves from V_{GS} = -40 to 40 V. FIG. 8C shows transfer characteristics at V_{DS} = 10 to 40 V.

[0017] FIG. 9A shows a schematic illustration of the 2D Ga₂O₃:Si channel microstrip array FETs. FIG. 9B shows a schematic illustration of three portions of the Ga₂O₃ channel.

DETAILED DESCRIPTION

[0018] Provided are methods of forming IV-doped III-VI semiconductors, including *p*-type III-VI semiconductors doped with Si. Also provided are the IV-doped III-VI semiconductors and devices incorporating the IV-doped III-VI semiconductors.

[0019] The present methods are based on the technique of metalorganic chemical vapor deposition (MOCVD). As such, any reactor system suitable for carrying out MOCVD may be used to carry out the methods. An embodiment of a method of forming an IV-doped III-VI semiconductor comprises a step of exposing a substrate to a vapor composition comprising a group III precursor comprising a group III element, a group VI precursor comprising a group VI element, and a group IV precursor comprising a group IV element. The exposure takes place under conditions sufficient to form a compound semiconductor from the group III, group VI, and group IV precursors via MOCVD. That is, the group III, group VI, group IV precursors adsorb to the surface of substrate where they react to form the compound semiconductor, typically as a layer on the surface of the substrate. The method may include a predeposition step to form a wetting layer on the substrate prior to exposure to the vapor composition. The predeposition step may comprise exposing the substrate to the group III precursor (i.e., without the group VI precursor and without the group IV precursor).

[0020] The group III precursors are metalorganic compounds comprising a group III element. In embodiments, the group III element is selected from Ga, Al, and In. A variety of group III precursors may be used, e.g., trimethylgallium, trimethylaluminum, trimethylindium, triethylgallium, triethylaluminum, triethylindium, triisopropylgallium, triisopropylaluminum, triisopropylindium, triisobutylgallium, and triisobutylaluminum. In embodiments, a single group III precursor is used, e.g., a gallium-containing group III precursor to provide a Ga-group VI compound semiconductor. In embodiments, more than one group III precursor is used so as to facilitate alloying of the group III elements in the formation of the compound semiconductor. By way of illustration, a gallium-containing group III precursor, an aluminum-containing group III precursor and an indium-containing group III precursor may be used to provide a GaAlIn-group VI compound semiconductor. In such a compound semiconductor, the ratios of Ga, Al, In may vary, depending upon the desired properties and application for the semiconductor. As another illustration, a gallium-containing group III precursor and an indium-containing group III precursor may be used to provide a GaIn-group VI compound semiconductor. Again, in such a compound semiconductor, the ratios of Ga and In may vary.

[0021] The group VI precursors are compounds comprising a group VI element. In embodiments, the group VI element is O. A variety of group VI precursors may be used, e.g., water, oxygen, N₂O, and ozone.

[0022] The group IV precursors are compounds comprising a group IV element. In the present methods, the group IV precursors are used as dopants, i.e., to provide an IV-doped III-VI. In embodiments, the group IV element is Si. A variety of group IV precursors may be used, e.g., SiH₄, tetraethylorthosilicate, Si₂H₆, SiCl₄.

[0023] Because one or more of the group III, group VI, and group IV precursors may be provided in a carrier gas (e.g., N₂, Ar, H₂), the vapor composition may also comprise one or more such carrier gases.

[0024] By “conditions” as that term is used with respect to the present methods, refers to the growth temperature, the pressure of the vapor composition, the flow ratio of the group VI precursor to the group III precursor, and the carrier gas. The present methods are based, at least in part, on the finding that certain of these conditions may be adjusted to tune the doping type of the compound semiconductor from n-type to p-type, even when using the same dopant, i.e., the same group IV precursor. That is, certain of these conditions may be adjusted

so that the group IV element of the group IV precursor substitutes for the group VI element in the forming compound semiconductor to provide a p-type IV-doped III-VI semiconductor or so that the group IV element substitutes for the group III element to provide an n-type IV-doped III-VI semiconductor.

[0025] These findings are particularly surprising given the widely accepted challenges in the field for obtaining p-type III-VI semiconductors such as p-type Ga₂O₃. Specifically, for p-type Ga₂O₃ thin films, shallow donor level (due to oxygen vacancy) with low formation energy can influence the efficiency of doping and compensate for native acceptors. This requires high formation energy, which makes it difficult to grow the p-type material. See also Mastro *et al.*, “Opportunities and Future Directions for Ga₂O₃,” *ECS Journal of Solid-State Science and Technology*, 6 (5) p. 356-359 (2017), which provides additional evidence of these challenges.

[0026] By way of illustration, it has been found that the flow ratio of the group VI precursor to the group III precursor may be adjusted to provide both an n-type IV-doped III-VI semiconductor (at certain flow ratios) and a p-type IV-doped III-VI semiconductor (at other flow ratios) even when using the same group IV precursor. Similarly, an inversion flow ratio value has been found, below which value a p-type IV-doped III-VI semiconductor is formed and above which value a n-type IV-doped III-VI semiconductor is formed even when using the same group IV precursor. The inversion flow ratio value for a particular material system may be referenced at a particular growth temperature, pressure, and carrier gas being used in the method.

[0027] These findings are demonstrated in the Examples below using trimethylgallium (group III precursor), water (group VI precursor) and silane (group IV precursor) to provide both n-type Ga₃O₂:Si and p-type Ga₃O₂:Si simply by adjusting the flow ratio of the O precursor to the Ga precursor. In other words, it has been found that Si acts as an amphoteric dopant for Ga₃O₂ via adjustments of the VI-III flow ratio. This vastly simplifies manufacturability of doped Ga₂O₃, thereby enabling many applications of this important material. Moreover, it has been found that the inversion flow ratio value for this material system is about 125. That is, for VI-III flow ratios below 125, the compound semiconductor formed is p-type (silicon substitutes for oxygen, taking up two extra electrons from the lattice, thus acting as a doubly ionized acceptor to achieve very effective p-type doping). For VI-III flow ratios above 125, the compound semiconductor formed is n-type (silicon

substitutes for gallium). (See FIG. 1A.) This inversion flow ratio value of 125 may be referenced, e.g., at a growth temperature of 1000 °C, a pressure of 50 mbar, and N₂ as the carrier gas.

[0028] FIGs. 5A-5C further support the findings described above. Moreover, these figures show the growth temperature does not changing the nature of doping, only the ratio of the flows of the group III and VI precursors.

[0029] Thus, the present methods may comprise carrying out the step of exposure to the vapor composition under conditions (e.g., VI-III flow ratio) selected to achieve a desired doping type (either p-type or n-type) for the IV-doped III-VI semiconductor being formed. Since both doping types may be achieved using the same group IV precursor, the methods may further comprise forming a second IV-doped III-VI semiconductor having the opposite doping type to provide a p-n heterojunction. For example, the method can be used to form an n-type IV-doped III-VI semiconductor on a p-type IV-doped III-VI semiconductor or vice versa.

[0030] With reference back to the growth temperature and pressure described above, illustrative growth temperatures include those in the range of from about 500 °C to about 1500 °C, including from about 600 °C to about 1000 °C, or from about 700 °C to about 1000 °C. Illustrative pressures include those in the range of from about 10 mbar to about 100 mbar, including from about 50 mbar to about 150 mbar. A variety of substrates may be used in the present methods, e.g., sapphire (a-sapphire, m-sapphire, c-sapphire), Al₂O₃, silicon (Si(111), Si(100)), native β-Ga₂O₃, MgO, ZnO, etc.

[0031] The IV-doped III-VI semiconductors formed using the present methods are also encompassed by the present disclosure. The IV-doped III-VI semiconductors may be characterized by their carrier concentrations. In embodiments, the IV-doped III-VI semiconductor is p-type having a carrier concentration in the range of from about 10¹⁵ cm⁻³ to about 10²⁰ cm⁻³, from about 10¹⁶ cm⁻³ to about 10²⁰ cm⁻³, from about 10¹⁷ cm⁻³ to about 10²⁰ cm⁻³ or from about 10¹⁸ cm⁻³ to about 10²⁰ cm⁻³. In embodiments, the IV-doped III-VI semiconductor is n-type having a carrier concentration in any of the ranges disclosed above. The IV-doped III-VI semiconductors may be characterized by their Hall mobility. In embodiments, the Hall mobility may be in the range of from about 5 to about 300 cm²/Vs, about 10 to about 300 cm²/Vs, or from about 5 to about 150 cm²/Vs. Known techniques may be used to measure carrier concentration and Hall mobility.

[0032] The IV-doped III-VI semiconductors may be characterized by the phase of the III-VI semiconductor. By way of illustration, for Ga_2O_3 , the phase of the material may be, e.g., β or κ .

[0033] Also encompassed by the present disclosure are p-n heterojunctions formed from any of the disclosed p-type IV-doped III-VI semiconductor and another n-type semiconductor or from any of the disclosed p-type IV-doped III-VI semiconductors and any of the disclosed n-type IV-doped III-VI semiconductors.

[0034] Devices incorporating the IV-doped III-VI semiconductors are also encompassed by the present disclosure. Illustrative devices include photodetectors (including solar-blind UV photodetectors), field effect transistors (including fin structured transistors see FIGs. 2A-2B and 7A-7B), light emitting diodes and combinations thereof. Other applications include use of the IV-doped III-VI semiconductors in high voltage direct current transmission lines, variable frequency drives and switch mode power supplies.

[0035] Additional information regarding MOCVD, techniques for characterizing the IV-doped III-VI semiconductors, and devices in which the IV-doped III-VI semiconductors may be incorporated may be found in the Appendix I (entire document), Appendix II (especially Section 2.2 and Section 4), and Appendix III (entire document) included in U.S. Provisional Application No. 62/623,183, the entire contents of which are hereby incorporated by reference.

EXAMPLE

[0036] Example 1

[0037] A commercial horizontal-flow MOCVD reactor (AIXTRON 200/4 RF) was used to grow doped Ga_2O_3 thin films on c-plane sapphire (0001) at a growth temperature of about 1000 °C using a conventional trimethylgallium (TMGa) bubbler and high purity deionized water loaded in a custom quartz bubbler as the gallium and oxygen precursors, respectively. Silane (SiH_4) was used as the silicon precursor. H_2 was used as the carrier gas. First, TMGa was flowed for 1 minute to predeposit gallium on the substrate before introducing the water. Doped Ga_2O_3 thin films were investigated using VI / III flow ratios in the range of from 100 to 150.

[0038] FIG. 1A shows the carrier concentration as a function of the III-VI flow ratio. For VI-III flow ratios below ~125 the as-grown material is p-type (silicon substitutes for oxygen).

At an VI-III flow ratio of ~ 125 an inversion takes place and the material becomes compensated. At an VI-III- flow ratio higher than ~ 125 the material becomes n-type (silicon substitutes for gallium). The only aspect of the growth that was changed was the VI-III flow ratio. In all cases, the growth temperature was $1000\text{ }^{\circ}\text{C}$ and the only variable changed was the ratio of the trimethylgallium and water flow rate being introduced into the reaction chamber. The Hall mobility of the as-grown material as a function of the VI-III flow ratio is plotted in FIG. 1B.

[0039] In order to verify that the as-grown material is indeed p-type at low VI-III flow ratios, a series of field effect transistors (FETs) with a fin structure were fabricated using the p-type material (see FIGs. 2A and 2B). An insulated gate consisting of $\sim 100\text{ nm}$ of silicon dioxide was deposited over the semiconductor material (i.e., p-type Ga_2O_3) and source, drain, and gate contacts were deposited. The epitaxial layer of Ga_2O_3 was only $\sim 1.2\text{ nm}$ thick. Hall mobility measurements indicated the layer was p-type with a carrier concentration of $3.423 \times 10^{18}\text{ cm}^{-3}$. The source-drain spacing was $20\text{ }\mu\text{m}$ and the gate was just $5\text{ }\mu\text{m}$ wide.

[0040] The fin-FET transistors were then experimentally characterized using an HP 4155C semiconductor parameter analyzer to measure the family of curves. The results are shown in FIGs. 3A and 3B. The measured results show the excellent conductivity of the p-type layer achieved with the novel doping technique used in this Example.

[0041] Example 2

[0042] Ga_2O_3 has emerged as a next generation semiconductor material for high power electronic devices. This is in great part due to its high breakdown electric field ($\sim 8\text{ MV/cm}$), which largely surpasses that of competing materials systems such as SiC or GaN.

Furthermore, the emergence of *n*-type doping capacity and single crystal Ga_2O_3 substrates has allowed the development of various unipolar electronic devices including metal oxide semiconductor field effect transistors (MOSFETs), Schottky diodes, metal semiconductor field effect transistors (MESFET).¹⁻³ The vast majority of this work has focused on homoepitaxial growth of monoclinic $\beta\text{-Ga}_2\text{O}_3$, which is the most stable of five common polymorphs (α , β , γ , δ and ϵ). A major drawback of Ga_2O_3 till present, however, has been lack of a method to obtain *p*-type conduction. This is a key limitation for its adoption in a whole range of semiconductor device applications. Moreover, the relatively low thermal conductivity of Ga_2O_3 and the problem of Ga_2O_3 substrate cost being two orders of

magnitude higher than sapphire are both currently hindering the fuller development of Ga₂O₃ based power electronics.

[0043] κ -Ga₂O₃ (an orthorhombic polymorph which is normally considered to be transient) can be stabilized in heteroepitaxial growth on sapphire (0001) substrates by MOCVD.⁴ In this Example, it is shown that high levels of shallow acceptor *p*-type conduction may be achieved in such layers using silicon impurity doping under Ga rich growth conditions. 2D layers of such *p*-type Ga₂O₃:Si are then processed into microstrip array ring FETs using conventional photolithography. The operational characteristics of the FETs proved to be consistent with *p*-type conduction. This is the first demonstration of both shallow acceptor doping of Ga₂O₃ and a *p*-type Ga₂O₃ channel FET. A phenomenological model coherent with a *p*-type channel is also presented.

[0044] A commercial MOCVD reactor (AIXTRON 200/4 RF) was used to grow Ga₂O₃ on sapphire (0001) substrates at growth temperatures ranging from 730 to 1000 °C. Trimethylgallium (TMGa), high purity deionized water and SiH₄ were adopted as the Ga, O and Si precursors, respectively. N₂ was used as the carrier gas. Total pressure was 50 mbar. VI/III ratio was either 100 (Ga-rich) or 150 (O-rich). The SiH₄ flow rate was fixed at 15 sccm.

[0045] As shown in FIG. 4A, XRD analysis was performed to analyze the phases of the grown ~ 150 nm thick Ga₂O₃:Si with different VI/III ratio 100 and 150 (top and middle). The XRD results show three peaks for each Ga₂O₃:Si layer. These three peaks were observed, similar to the results of the β -Ga₂O₃ substrate (bottom). However the TEM analysis in FIG. 4B showed the result of κ -phase with the space group of *Pna*²1.⁴ The κ -phase Ga₂O₃:Si was grown in the (002) direction and the 6 rotated domains were observed in the ~ 150 nm thick Ga₂O₃:Si.

[0046] Electrical properties were measured using Van der Pauw Hall measurements. Ohmic contacts were obtained using a Ga/In eutectic. FIGs. 5A and 5B show the results as a function of growth temperature for both VI/III ratios. At a VI/III ratio of 150, Ga₂O₃:Si grown at 730 °C shows *n*-type characteristics. As growth temperature was increased from 730 °C to 1000 °C, the carrier concentration decreased linearly to ~ 4.4 × 10¹⁷ cm⁻³. FIG. 5B shows that the lower VI/III ratio (100) consistently gave *p*-type characteristics. Assuming that the Si dopant acts as a shallow acceptor by substituting on the O-site of the Ga₂O₃, the VI/III ratio of 100 growth condition would generate a higher density of oxygen vacancies (V_O) by

virtue of the Ga-rich nature of the growth which lets the Si substitute more readily at the O-sites. This assumption is consistent with FIG. 2C which shows the Hall mobility of the $\text{Ga}_2\text{O}_3\text{:Si}$ as a function of growth temperature for VI/III ratios of 150 and 100. For a VI/III ratio of 150, a (*n*-type) mobility near $50 \text{ cm}^2/\text{Vs}$ was observed for a growth temperature of 1000°C . For a VI/III ratio of 100, a (*p*-type) mobility of $\sim 3.3 \text{ cm}^2/\text{Vs}$ was observed. This demonstrates Si is acting as an amphoteric dopant in $\kappa\text{-Ga}_2\text{O}_3$. Si impurity doping is generally incorporated so as to substitute for Ga where it acts as a shallow donor so as to create heavily doped *n*-type Ga_2O_3 . But as the density of V_O increases under Ga-rich growth conditions, the above results suggest that Si can act as a shallow acceptor by substituting on the O-sites in $\kappa\text{-Ga}_2\text{O}_3$, and thus promote a transformation to predominantly *p*-type conduction. These *p*-type results were confirmed via multiple independent measurements.

[0047] Ring type FETs were fabricated and evaluated for the characteristics of the FET device of $\sim 150 \text{ nm}$ thick *p*-type $\text{Ga}_2\text{O}_3\text{:Si}$ with VI/III ratio of 100. FIG. 6 shows the I-V curves. It is observed that the drain current decreases with increasing gate voltage. However, it was not possible to achieve pinch-off due to the gate electrode burning at gate voltages higher than 50 V . To avoid this issue the channel thickness was reduced to $\sim 1.2 \text{ nm}$ and the ring pattern FETs were patterned with microstrips. $\text{Ga}_2\text{O}_3\text{:Si}$ channel layers were grown at 1000°C with a VI/III ratio of 100. The channel thickness was estimated to be $\sim 1.2 \pm 0.5 \text{ nm}$ based on interferometric growth rate calibration and AFM step-edge profilometry. Hall measurements confirmed the *p*-type nature of the layers with a resistivity of $\sim 0.007 \Omega\cdot\text{cm}$, a carrier concentration of $\sim 1.7 \times 10^{20} \text{ cm}^{-3}$ and a mobility of $\sim 5.7 \text{ cm}^2/\text{V}\cdot\text{s}$.

[0048] Standard photolithography and lift-off were employed to deposit source and drain metal contacts. Before their deposition, $3 \mu\text{m} \times 3 \mu\text{m}$ microstrip patterns were formed by electron cyclotron resonance-reactive ion etching (ECR-RIE) with CF_4 for 5 minutes. The metal contacts were Ti (20 nm) / Au (150 nm) deposited by e-beam evaporation. SiO_2 of 100 nm thick gate dielectric material was formed by plasma-enhanced chemical vapor deposition (PECVD). After dielectric and passivation film deposition, the gate metal contact was formed with Pt(20 nm) / Ti(20 nm) / Au(150 nm) on the SiO_2 film. The gate length, and the spacing between the source/drain and the inside source circular pad were 15 , 20 and $100 \mu\text{m}$, respectively. FIG. 7A shows schematic illustrations of the device with top- and cross-sectional views illustrating the device scale. FIG. 7B shows an optical microscope image of the fabricated device.

[0049] Next, the FETs were fabricated and tested using a semiconductor parameter analyzer and probe station. FIG. 8A shows the DC source-drain current versus source-drain voltage (I_{DS} - V_{DS}) output characteristics for the depletion-mode FETs measured by increasing gate-source voltage (V_{GS}) stepwise from -50 to 100 V. The maximum I_{DS} was 2.19 mA and it was effectively modulated by V_{GS} from -50 to 100 V, which is consistent with a p -type channel. Because of the heavy p -doping, the 2D microstrip channel is normally-on, and the channel off-state was observed for a gate bias of 50 V ($I_{DS} = 0.1$ pA at V_{DS} of 40 V). In addition, because of the high sheet resistance, even with a drain voltage as high as 40 V, the voltage drop in the FET channel is still lower than $|V_G - V_T|$, which is the condition for current saturation in long channel FETs. So the I_{DS} - V_{DS} characteristics remain linear. FIG. 8B displays a similar set of curves obtained from the simulation. It can be seen that the theoretical model is consistent with the experimental data in showing an output resistance increase with positive gate voltage, and I_{DS} bunching with little variation of the output resistance for $V_{GS} < 0$. This is also consistent with a p -type channel. FIG. 8C shows transfer characteristics at V_{DS} of 10 to 40 V in a logarithmic scale. The device achieved an *on/off* ratio of $\sim 10^8$ by minimizing the thickness and width of the channel. A plot of the gate current as a function of drain-source voltage (not shown) showed that I_G increases above a V_{GS} of 50 V because of a gate leakage current. It is expected that the *on/off* ratio can be further improved through optimization of the dielectric layer.

[0050] A phenomenological model was developed based on the device configuration displayed in FIGs. 7A-7B. FIGs. 9A-9B show the schematic of the model device that consists of a linear array of $\delta = 3$ μm wide micro-strips separated from each other by $\delta = 3$ μm . They are covered by a disk-shaped source contact of 200 μm in diameter, and separated from a square shaped drain by a 30 μm wide circular channel. So, in each quadrant, the channel length, L_i , varies between a minimum value when it is perpendicular to the disk and a maximum value when it is tangential to the disk. The position of the i^{th} microstrip is identified by its distance, d_i , from the center of the source disk.

[0051] At $V_G = 0$ V, the channel is uniform and the current between source and drain in the i^{th} micro-strip channel is given by

$$I_i = e p_S \delta v_i \quad (1)$$

[0052] where e is the electron charge (C), p_s is the 2D hole concentration (carriers/cm²), δ the wire width (cm) and v_i is the hole velocity in the i^{th} channel (cm/s). In the absence of saturation velocity (long channel-low mobility),

$$v_i = \frac{\mu V_{DS}}{L_i} \quad (2)$$

[0053] where μ is the hole mobility (cm²/Vs) and L_i is the channel length (cm).

[0054] If $d_i = 2i\delta$ with $0 \leq i \leq N$, Equ.1 becomes for top and bottom right quadrants

$$I_{right} = 2 \sum_{i=0}^N I_i = ep_s \mu V_{DS} \sum_{i=0}^N 1 / \left[\sqrt{(N+5)^2 - i^2} - \sqrt{N^2 - i^2} \right] = 2.84 ep_s \mu V_{DS} \quad (3)$$

[0055] Because of the relatively big gate pad on the left side of the source, channel lengths are longer for a sizeable portion of the FIN-microstrips, so it is estimated that the total current should be multiplied by a factor $\eta \sim 1.8-1.9 < 2$. Finally,

$$I = I_{Right} + I_{Left} = \eta I_{Right} \quad (4)$$

[0056] At $V_G \neq 0$, the channel is made of three portions with different conductances (FIG. 9B). By neglecting the contact resistance, for each channel,

$$I_i(V_G) = \frac{V_{DS}}{\frac{1}{G_1^i} + \frac{1}{G_2^i} + \frac{1}{G_3^i}} \quad \text{with} \quad G_{1,3}^i = \frac{ep_s(V_G=0)\delta\mu}{L_{1,3}^i} \quad G_2^i = \frac{ep_s(V_G \neq 0)\delta\mu}{L_2^i} \quad (5)$$

[0057] If $p_s(V_G \neq 0) = p_s(V_G = 0) \exp\left(-\frac{eV_C}{kT}\right)$, where $V_C(V_G)$ is the channel potential induced by the gate bias, the expression for the current reads

$$I_i(V_G) = ep_s(V_G = 0)\delta\mu V_{DS} / (L_1^i + L_2^i \exp(eV_C/kT) + L_3^i) \quad (6)$$

or after summation over all channels,

$$I(V_G) = \frac{2I(V_G=0)}{1 + \exp\left(\frac{eV_C}{kT}\right)} \quad (7)$$

[0058] This equation shows that for $V_C < 0$ ($V_G < 0$) the drain current decreases, whereas for $V_C > 0$ ($V_G > 0$) the drain current increases in agreement with the experimental data. This is consistent with the channel being p -type. In quantitative terms, it shows that current decreases by several orders of magnitude under positive V_G compared to a limiting increase by a factor 2 under negative V_G . This asymmetry in the variation of the I-V characteristics for $V_G < 0$ and $V_G > 0$ is also consistent with the experimental data.

[0059] From the Poisson equation, one can derive an expression of V_C for intermediate gate bias:

$$V_C(y) = \frac{V_G \lambda_D \exp\left(-\frac{y-D}{\lambda_D}\right)}{D + \lambda_D} \quad (8)$$

[0060] where D is the thickness of the SiO_2 barrier, y is the vertical coordinate inside the Ga_2O_3 layer, and λ_D is the Debye length in the Ga_2O_3 layer fitted to reproduce the experimental I-V characteristics. FIG. 8B displays simulation data of I-V curves from $V_{GS} = -40$ to 40 V, for which a channel mobility $\mu = 23 \text{ cm}^2/\text{Vs}$ and hole concentration $p_S = 2.35 \times 10^{12}/\text{cm}^2$ was used.

[0061] In conclusion, $\kappa\text{-Ga}_2\text{O}_3\text{:Si}$ layers grown on sapphire (0001) substrates by MOCVD showed consistent p -type Hall signal for layers grown with lower VI/III ratios during growth. Room temperature mobilities were up to $7 \text{ cm}^2/\text{Vs}$, resistivities were as low as $0.007 \text{ }\Omega\cdot\text{cm}$ and carrier concentrations were up to $\sim 10^{20} \text{ cm}^{-3}$ for thinner layers. Ring mesa FETs were fabricated based on $\sim 1.2 \text{ nm}$ thick $p\text{-Ga}_2\text{O}_3\text{:Si}$ channels formed into a number of $3 \text{ }\mu\text{m}$ wide microstrips. The devices achieved a maximum drain current density of 2.19 mA and an *on/off* ratio of $\sim 10^8$ and showed characteristics consistent with a p -type conduction in the channel.

[0062] The p -type Ga_2O_3 demonstrated in this Example represents a significant advance in the state of the art, which may herald the fabrication of a range of p - n junction based devices. These may be smaller/thinner and bring both cost (more devices/wafer and less growth time) and operating speed advantages (due to miniaturisation) than current isotype FETs. Moreover the demonstration of the first functioning devices based on scaling down to 2D device channels in Ga_2O_3 based FETs opens up the perspective of faster devices and improved heat evacuation.

[0063] References for Example 2

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[0064] The word "illustrative" is used herein to mean serving as an example, instance, or illustration. Any aspect or design described herein as "illustrative" is not necessarily to be construed as preferred or advantageous over other aspects or designs. Further, for the purposes of this disclosure and unless otherwise specified, "a" or "an" means "one or more."

[0065] The foregoing description of illustrative embodiments of the disclosure has been presented for purposes of illustration and of description. It is not intended to be exhaustive or to limit the disclosure to the precise form disclosed, and modifications and variations are possible in light of the above teachings or may be acquired from practice of the disclosure. The embodiments were chosen and described in order to explain the principles of the disclosure and as practical applications of the disclosure to enable one skilled in the art to utilize the disclosure in various embodiments and with various modifications as suited to the particular use contemplated. It is intended that the scope of the disclosure be defined by the claims appended hereto and their equivalents.

WHAT IS CLAIMED IS:

1. A method of forming a p-type IV-doped III-VI semiconductor, the method comprising:

exposing a substrate to a vapor composition comprising a group III precursor comprising a group III element, a group VI precursor comprising a group VI element, and a group IV precursor comprising a group IV element, under conditions to form a p-type IV-doped III-VI semiconductor via metalorganic chemical vapor deposition (MOCVD) on the substrate.

2. The method of claim 1, wherein the conditions comprise use of a flow ratio defined as a flow rate of the group VI precursor to a flow rate of the group III precursor and the flow ratio is below an inversion flow ratio value for the IV-doped III-VI semiconductor so as to provide the p-type IV-doped III-VI semiconductor.

3. The method of claim 1, further comprising exposing the substrate to the vapor composition under conditions to form an n-type IV-doped III-VI semiconductor via MOCVD from the vapor composition.

4. The method of claim 3, wherein the n-type IV-doped III-VI semiconductor is in contact with the p-type IV-doped III-VI semiconductor, thereby forming a p-n heterojunction.

5. The method of claim 3, wherein the conditions comprise use of a flow ratio defined as a flow rate of the group VI precursor to a flow rate of the group III precursor and the flow ratio is above an inversion flow ratio value for the IV-doped III-VI semiconductor so as to provide the n-type IV-doped III-VI semiconductor.

6. The method of claim 1, wherein the conditions comprise use of a first flow ratio defined as a flow rate of the group VI precursor to a flow rate of the group III precursor to provide the p-type IV-doped III-VI semiconductor;

wherein the method further comprises exposing the substrate to the vapor composition under conditions to form an n-type IV-doped III-VI semiconductor via MOCVD from the vapor composition, wherein the conditions comprise use of a second, different flow ratio to provide the n-type IV-doped III-VI semiconductor.

7. The method of claim 6, wherein the n-type IV-doped III-VI semiconductor is in contact with the p-type IV-doped III-VI semiconductor, thereby forming a p-n heterojunction.

8. The method of claim 1, wherein the group III precursors are selected from a Ga-containing group III precursor, an Al-containing group III precursor, an In-containing group III precursor and combinations thereof.

9. The method of claim 1, wherein the group III precursor is a Ga-containing group III precursor.

10. The method of claim 1, wherein the group VI precursor comprises O.

11. The method of claim 1, wherein the group IV precursor comprises Si.

12. The method of claim 1, wherein the carrier gas comprises N₂, H₂, Ar, or combinations thereof.

13. The method of claim 1, wherein the group III precursors are selected from a Ga-containing group III precursor, an Al-containing group III precursor, an In-containing group III precursor and combinations thereof; wherein the group VI precursor comprises O; and wherein the group IV precursor comprises Si.

14. The method of claim 13, wherein the p-type IV-doped III-VI semiconductor formed is p-type Si-doped Ga₂O₃.

15. The method of claim 13, wherein the p-type IV-doped III-VI semiconductor formed is p-type Si-doped (Ga,In)₂O₃.

16. The method of claim 13, wherein the carrier gas comprises N₂, H₂, Ar, or combinations thereof.

17. A p-type IV-doped III-VI semiconductor comprising a group III element, a group VI element and a group IV element.

18. A p-n heterojunction comprising a layer of an n-type semiconductor in contact with the p-type IV-doped III-VI semiconductor of claim 17.

19. The p-n heterojunction of claim 18, wherein the n-type semiconductor is an n-type IV-doped III-VI semiconductor comprising the group III element, the group VI element and the group IV element.

20. A device comprising the p-type IV-doped III-VI semiconductor of claim 17 and another material layer in contact with the p-type IV-doped III-VI semiconductor.

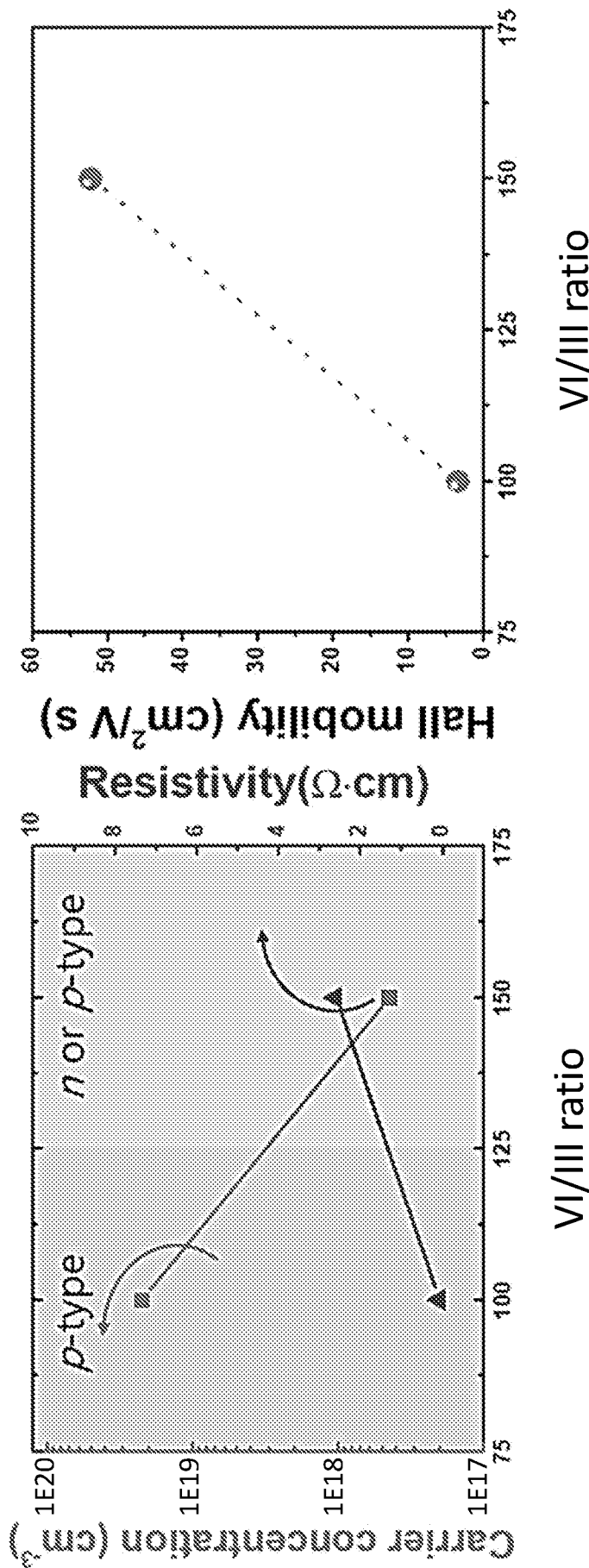


FIG. 1B

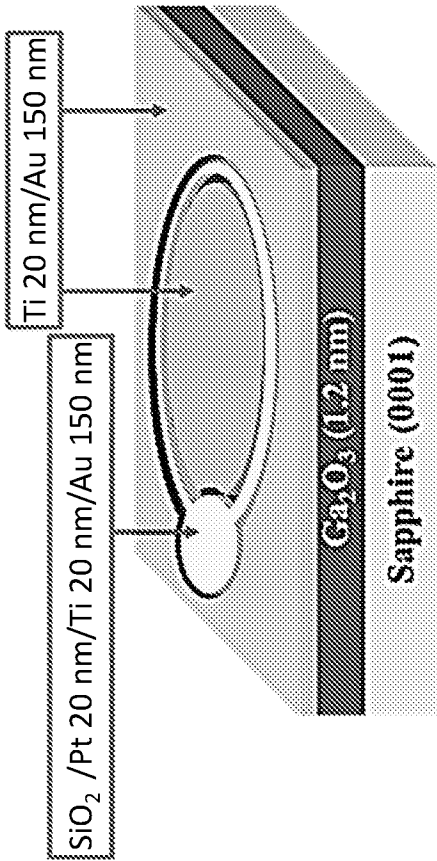


FIG. 2B

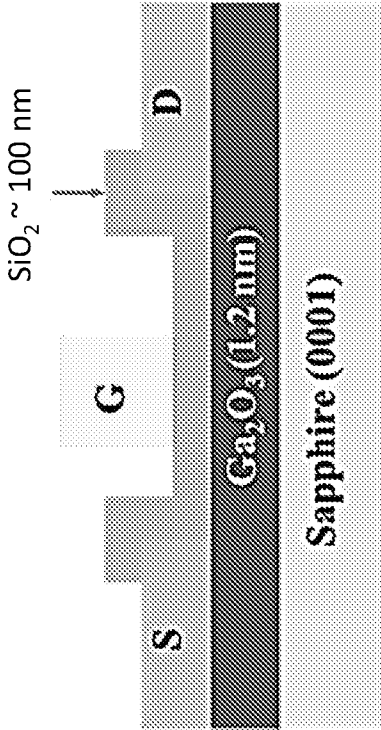


FIG. 2A

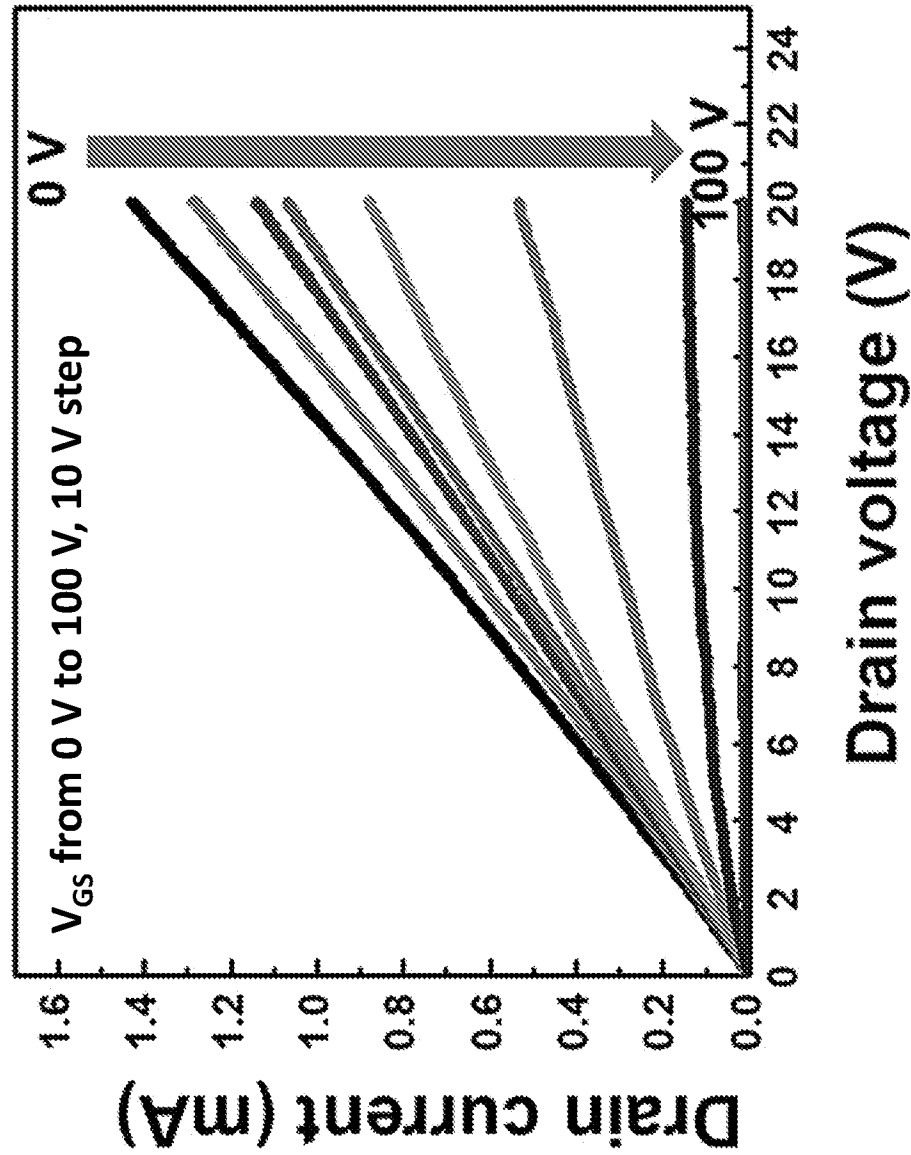


FIG. 3A

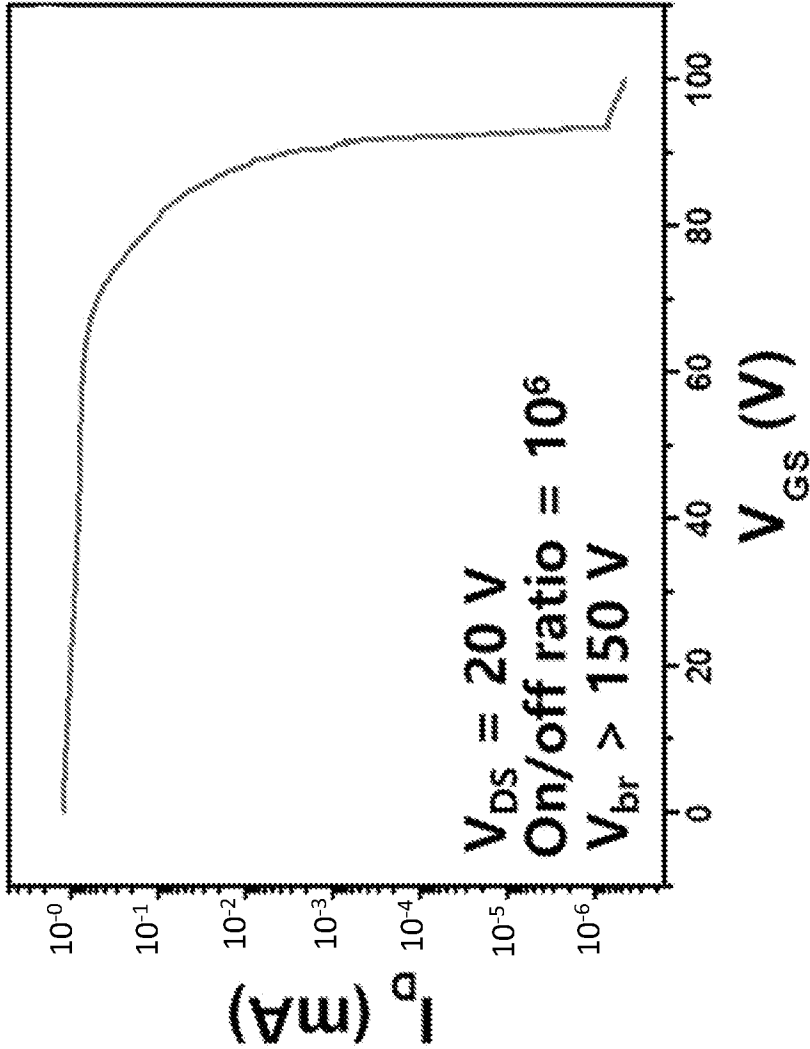


FIG. 3B

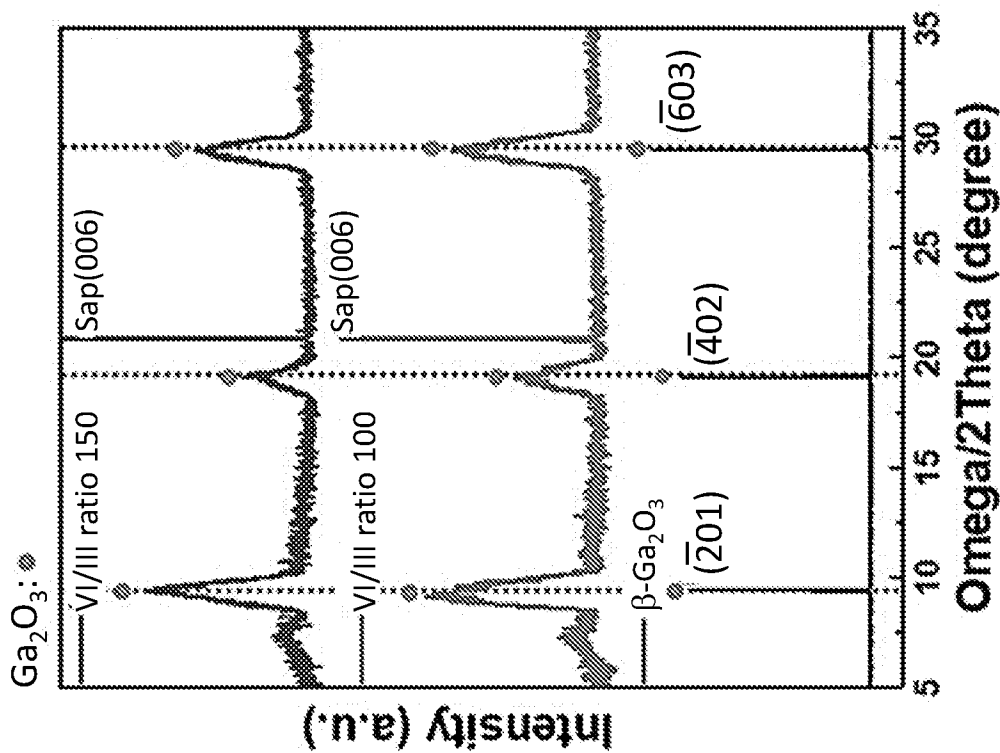


FIG. 4A

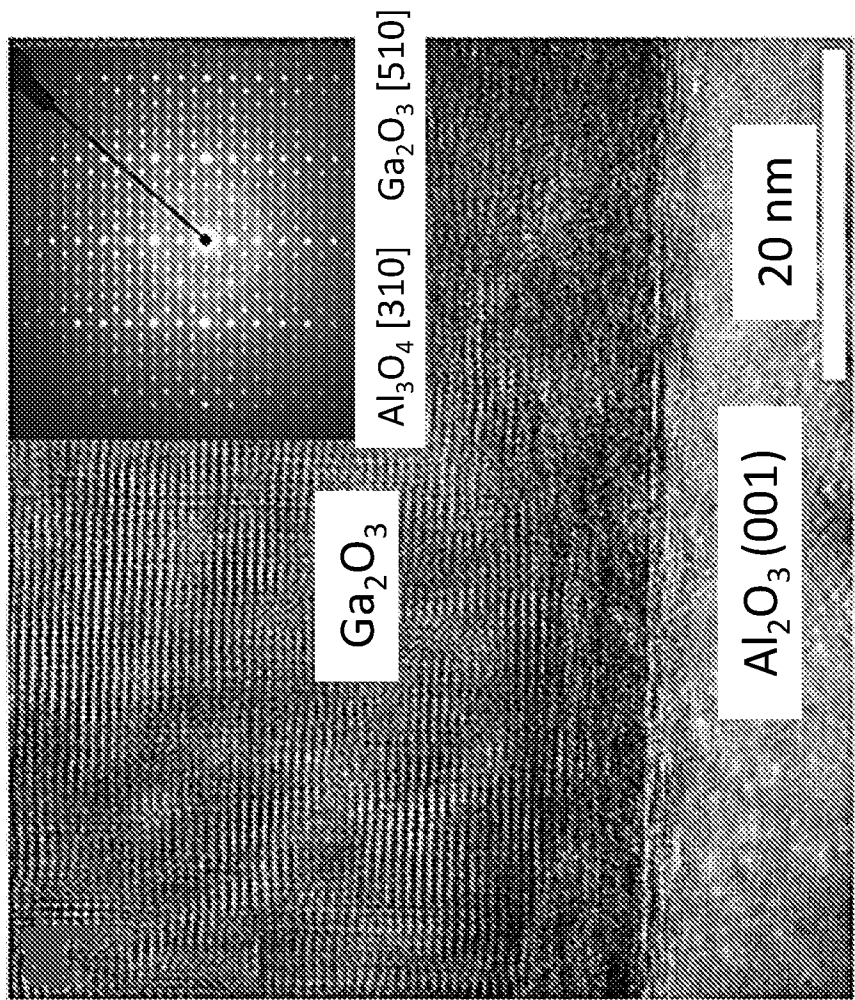


FIG. 4B

FIG. 5B

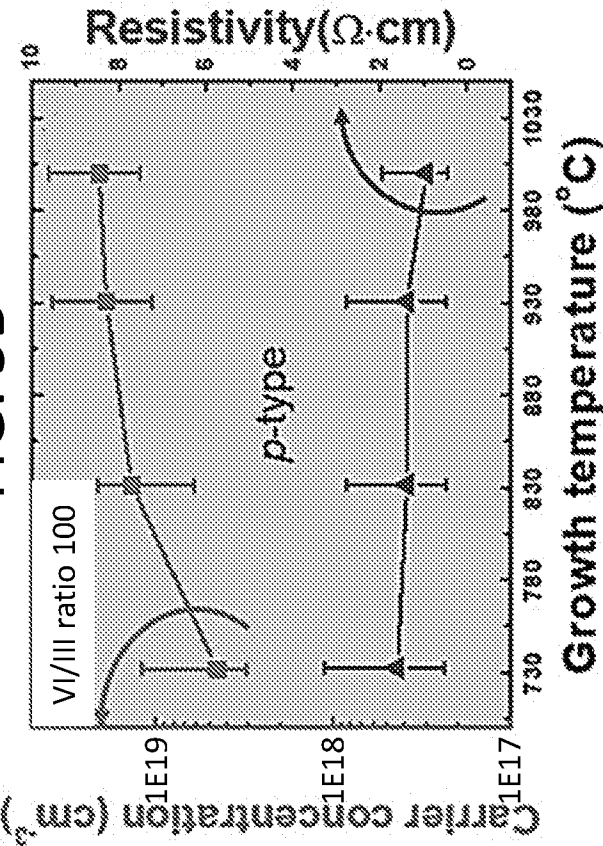


FIG. 5A

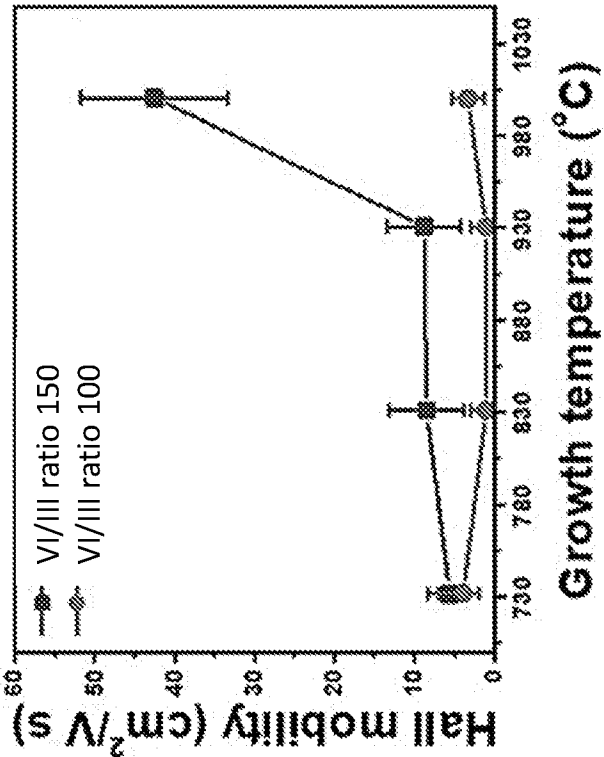
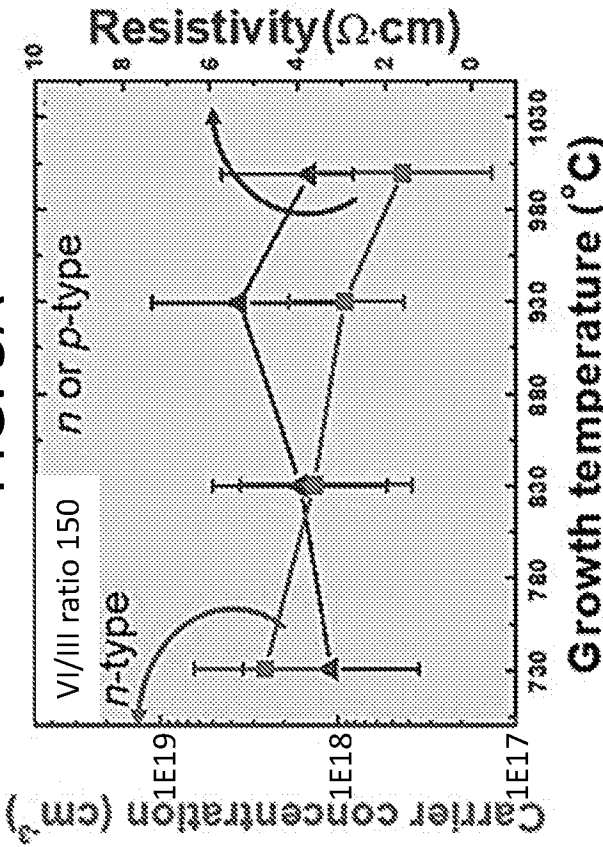


FIG. 5C

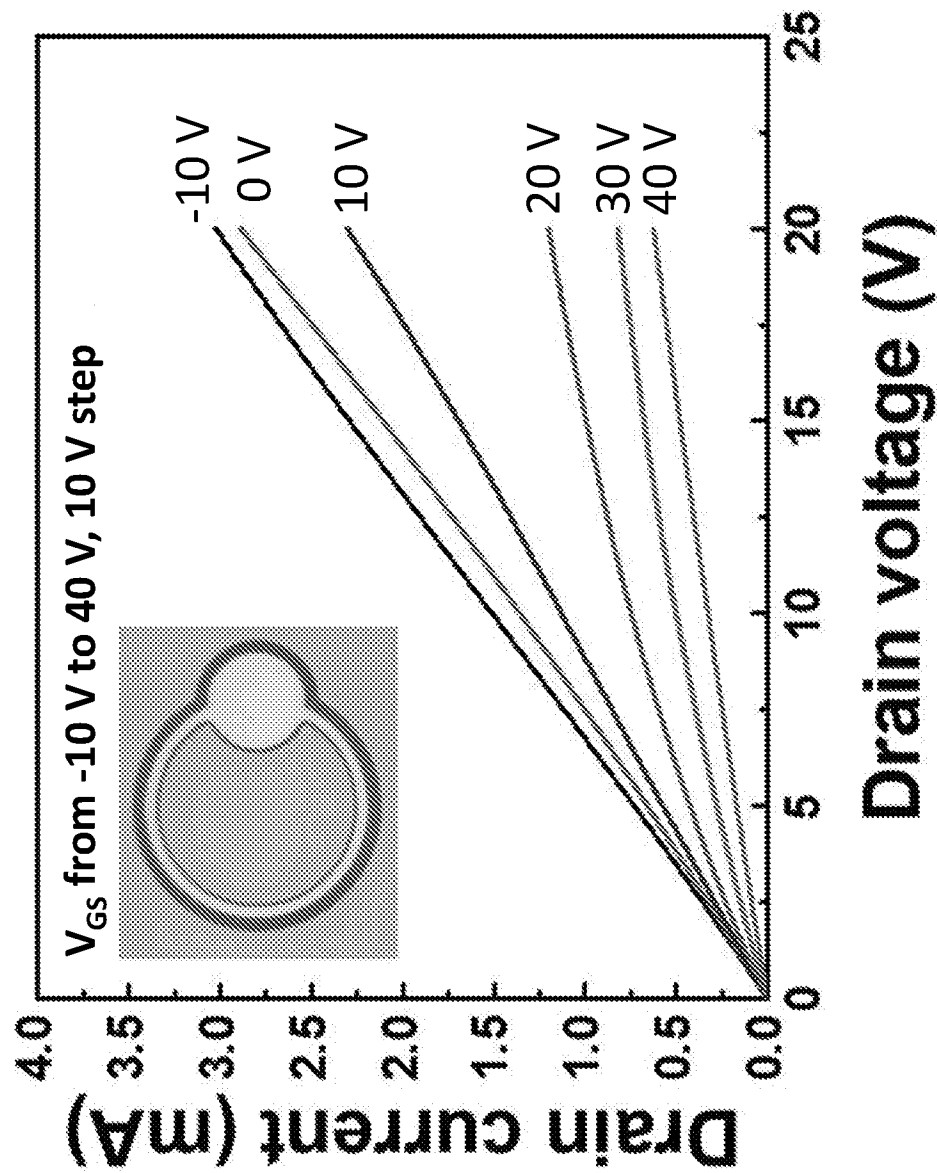


FIG. 6

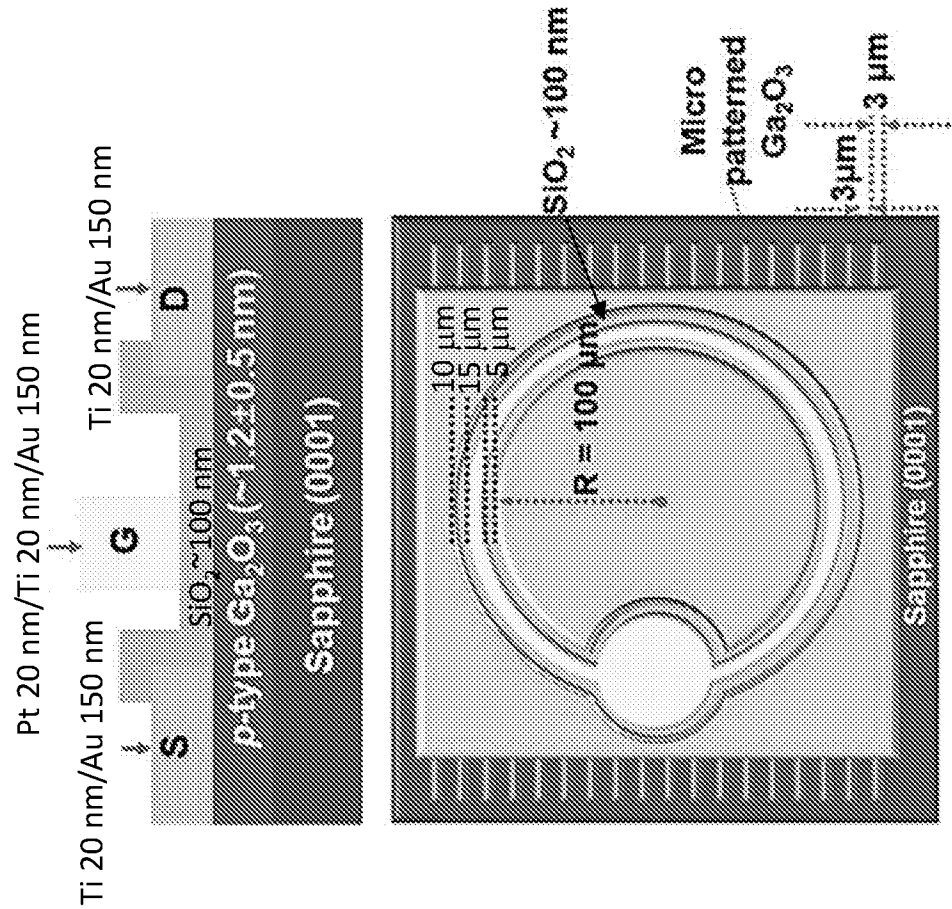


FIG. 7A

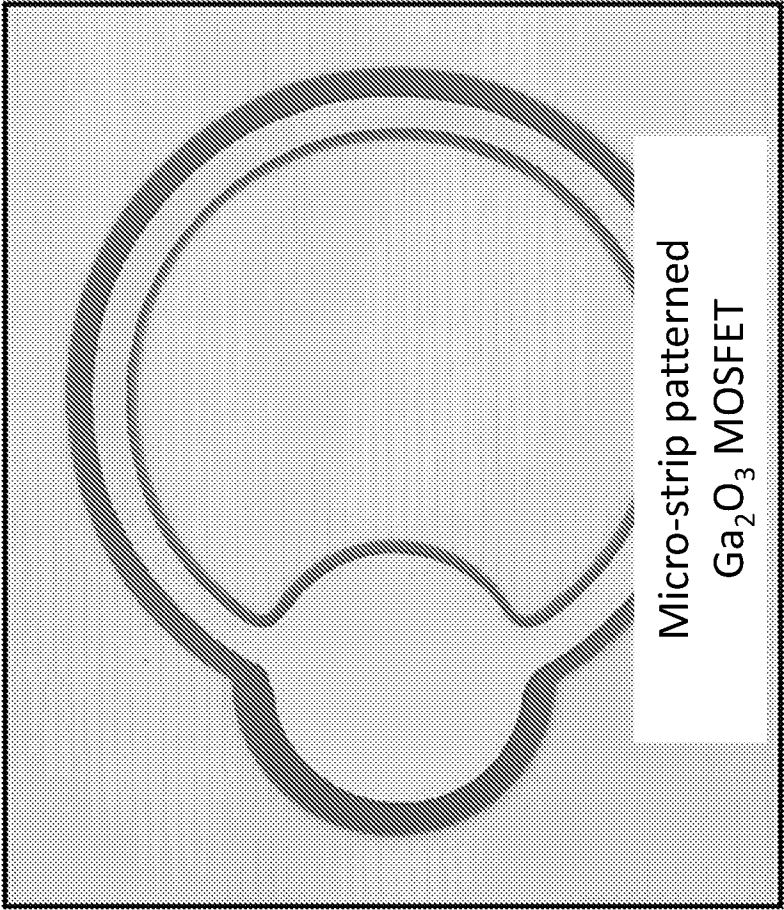


FIG. 7B

FIG. 8B

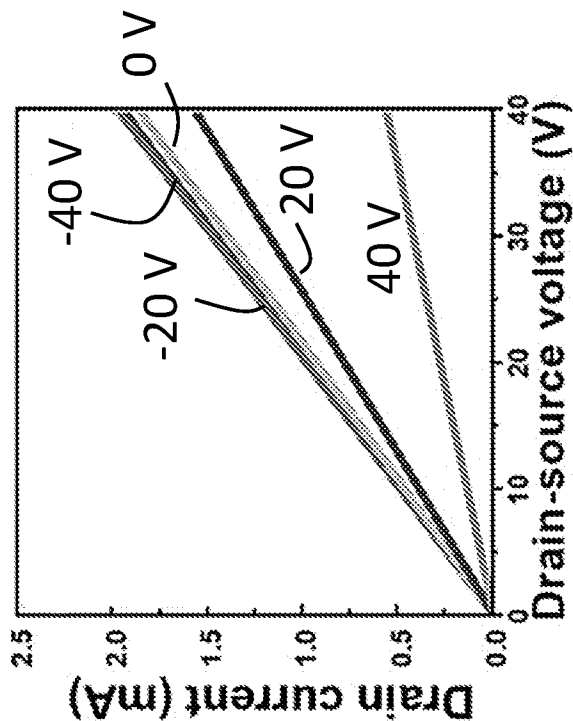


FIG. 8A

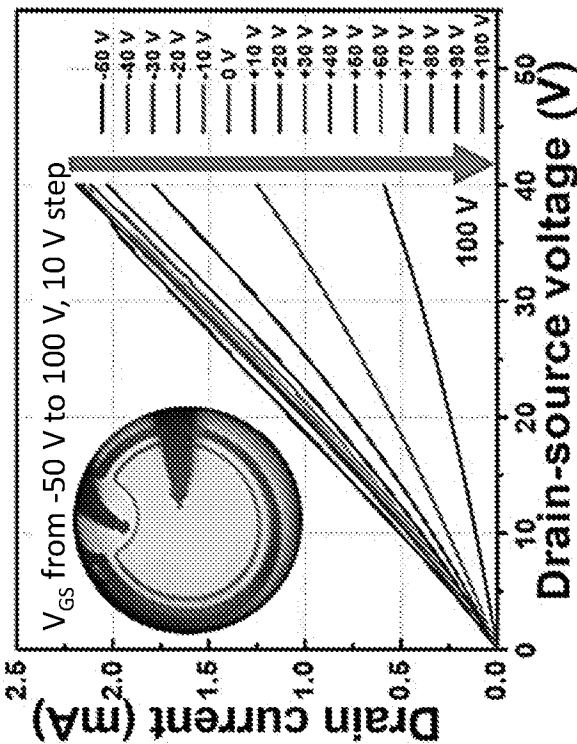
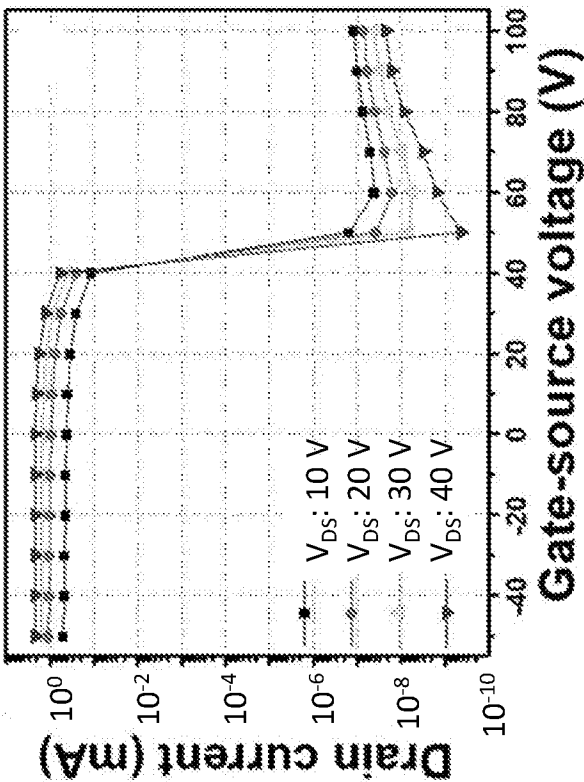


FIG. 8C



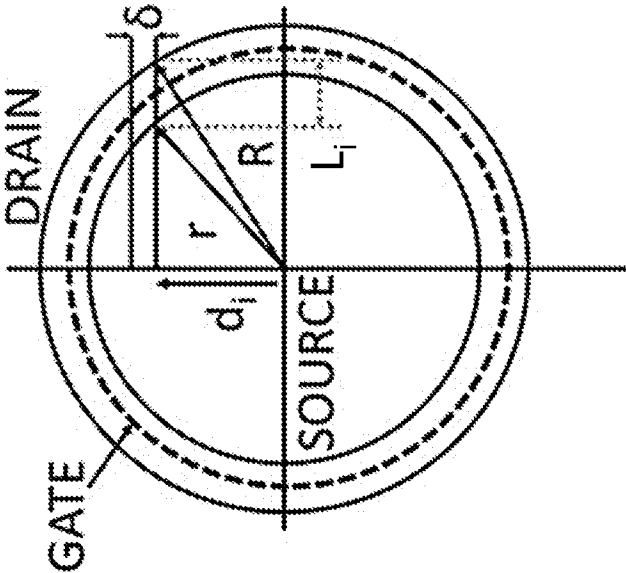


FIG. 9A

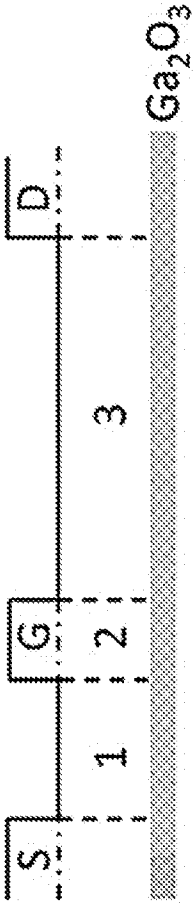


FIG. 9B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 19/14650

A. CLASSIFICATION OF SUBJECT MATTER
 IPC(8) - H01L 31/02, H01L 31/0232, H01L 31/0264 (2019.01)
 CPC - H01L 31/0443, H01L 31/0687, H01L 31/0725

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History Document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History Document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History Document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ----- A	US 2011/0186856 A1 (Huang et al.) 04 August 2011 (04.08.2011); Abstract, para[0025], para[0021], para[0023], para[0017], para[0018], Figure 5	1, 3-4, 8-20 ----- 2, 5-7
A	Niu "Epitaxial systems and combining oxides and semiconductors" 2013 (2013); paragraph 1 https://www.sciencedirect.com/topics/chemistry/metal-organic-chemical-vapor-deposition (col 2, article 2)	1
A	US 2017/0077330 A1 (Taiwan Semiconductor Manufacturing Company, Ltd.) 16 March 2017 (16.03.2017); para[0058]	12, 16
A/P	US 2018/0287001 A1 (International Business Machines Corporation) 04 October 2018 (04.10.2018); entire document	1-20
A	US 2008/0092954 A1 (Choi) 24 April 2008 (24.04.2008); entire document	1-20
A	US 2006/027814 A1 (Watanabe et al.) 09 February 2006 (09.02.2006); entire document	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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Date of the actual completion of the international search

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Date of mailing of the international search report

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