

Dec. 29, 1970

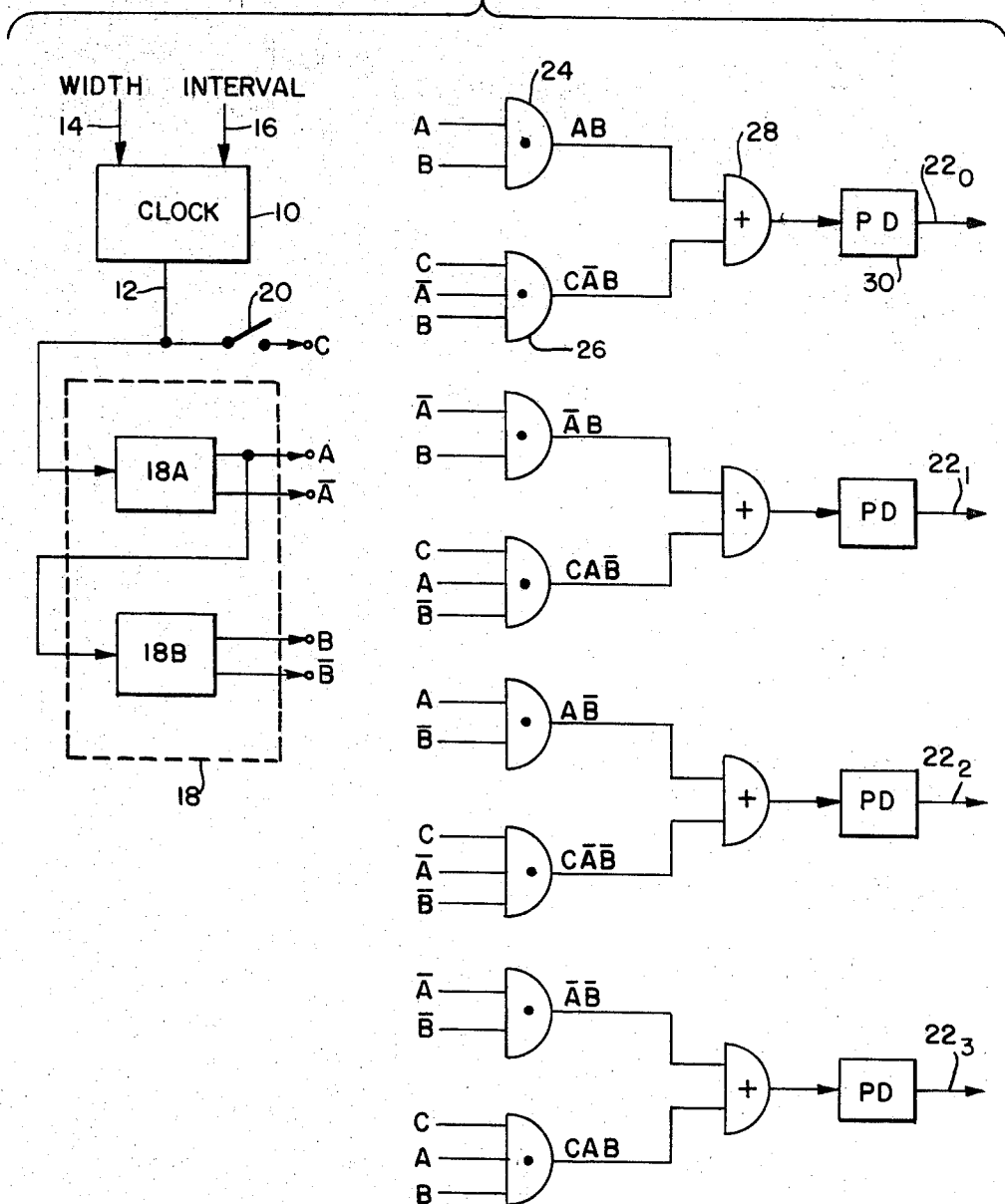
P. M. McNELIS
TIMING DEVICE FOR GENERATING A PLURALITY
OF CONTROLLABLE PULSE TRAINS

3,551,822

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2 Sheets-Sheet 1

FIG. 1



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FIG. 2

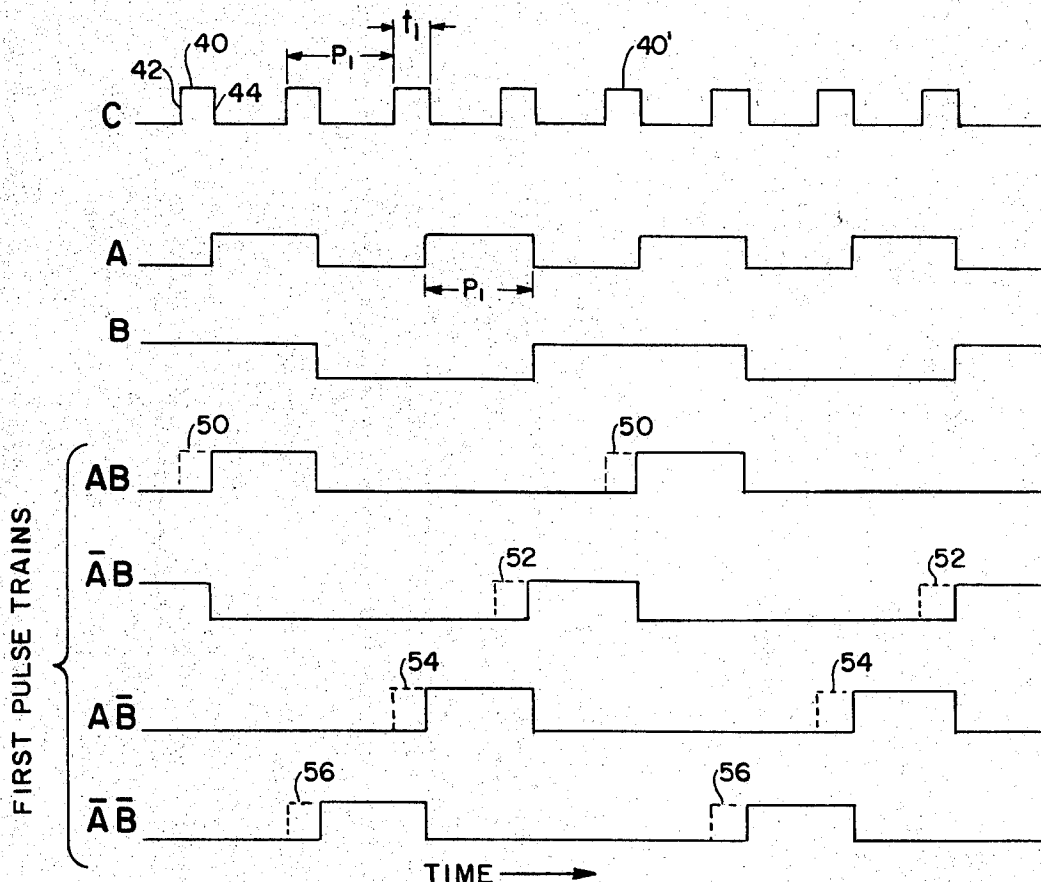
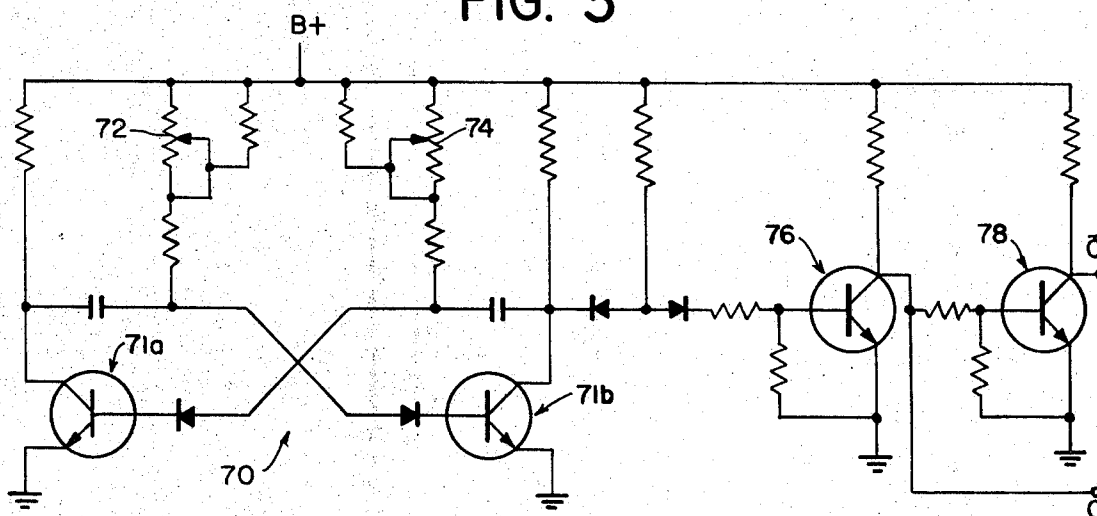


FIG. 3



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1

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TIMING DEVICE FOR GENERATING A PLURALITY OF CONTROLLABLE PULSE TRAINS

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2 Claims

ABSTRACT OF THE DISCLOSURE

A timing device for producing a plurality of output pulse trains which are delayed in time with respect to each other, comprises a source of clock pulses wherein the time interval between pulses as well as the duration of the pulses can be varied, and a gating circuit for combining selected ones of the clock pulses with each of a plurality of first pulse trains to produce output pulse trains wherein the pulses of successive trains overlap each other in time and wherein the extent of the overlap can be adjusted along with the pulse width and the time interval between pulses.

The present invention relates to timing circuits of a type which may be used to control the sequential operation of cyclical devices such as pumps.

There are certain types of pumps which require a sequence of electrical control signals which cannot readily be obtained by conventional mechanical means. An example of such a pump is the Slurrymaster brand pump manufactured and sold by Foster Pump Works, Inc. of Brooklyn, N.Y. This pump is used to pump abrasives and corrosives and includes two or more pumping chambers which are operated in sequence to receive and discharge the material to be pumped under the control of pressurized air or steam which can be introduced into the chamber through a suitable valve.

In order to provide continuous pumping action, a plurality of pumping chambers are employed in which case a chamber is always being discharged while the remaining chambers are being filled through an inlet manifold. Where a plurality of chambers are employed, it is important that the operation of the respective valves be adjustable to assure continuous pulse-free flow. This requires that the valve of each of the chambers be opened slightly before the valve of the preceding chamber is closed. Since opening of a valve initiates the discharge of the contents of the chamber associated with that valve, a continuous flow from the pump is assured despite the cyclical operation of the different chambers.

For different materials to be pumped, the optimum overlap in operation of successive chambers will vary depending upon various known factors.

For example, it is generally desirable to minimize the overlap period during which successive chambers operate concurrently since this increases the volume capacity of the pump. On the other hand, to ensure pulse free operation, the overlap interval may have to be increased to accommodate viscous fluids (which will tend to start flowing less readily than non-viscous fluids), higher differential pressure across the pump (requiring a greater intake of gas to initiate flow), and materials of high specific gravity (which require a longer period of time to attain the velocity of the material being pumped from the preceding chamber).

The required valve control cannot readily be achieved by cam operated mechanisms or the like. It is therefore desirable to employ electrically controlled valves which are capable of selectively applying the discharge pressure

2

to each of the pump chambers as required. This requires the generation of a pulse train for each of the individual pump chambers wherein the duration of the pulses and the time interval between pulses can be adjusted to operate the valves in any required cyclical relationship. Furthermore, the pulses of each train must overlap in time the pulses of at least one other train to assure continuous pulse-free pumping, and the extent of such overlap must be adjustable to accommodate different materials as described above.

Accordingly, the object of this invention is to provide an electrical timing device capable of providing a plurality of pulse trains wherein the duration of the pulses in the individual trains, the time interval between adjacent pulses, and the overlap of the pulses in successive trains can be adjusted over wide limits.

Briefly, in accordance with the invention, a source of clock pulses is provided wherein the duration of the pulses and the interval between pulses can be separately adjusted. A binary counter responsive to the clock pulses produces a plurality of first pulse trains in which the duration of the individual pulses is determined by the time interval between successive clock pulses, and the time interval between the pulses is determined by the time interval between a preselected number of the clock pulses. A gating circuit responsive to the clock pulses and the first pulse trains produces the desired output pulse trains.

The invention is described in detail below with reference to the attached drawings, wherein:

FIG. 1 is a block diagram of a preferred timing device in accordance with the invention;

FIG. 2 is a timing chart showing the various time relationship between the clock pulses and the pulse trains produced by the circuit of FIG. 1; and

FIG. 3 is a schematic diagram of a preferred clock pulse generator.

The following description relates to a device capable of producing four separate pulse trains which would be used in combination with a pump having four separate chambers. Obviously, however, the invention is in no respects limited to a specific number of output pulse trains and would generally have utility in the production of two or more pulse trains of the type described.

Referring to FIG. 1, a source of clock pulses 10 produces a pulse train on its output line 12, the width and duration of the clock pulses on line 12 being separately controllable as indicated by the arrows 14 and 16. The output of the clock source 10 is coupled to a binary divider 18 which is a standard binary counter including two bi-stable flip-flops indicated at 18A and 18B. As will become apparent from the following description, the maximum number of output pulse trains equals 2^n , where n equals the number of stages of counter 18.

Each of the stages 18A and 18B produces two outputs, one of which is the complement of the other as indicated at A and $\bar{A}$ and B and $\bar{B}$, respectively. A switch 20 may be selectively closed to apply the output on the clock pulse line 12 to the output line labelled C in FIG. 1.

The output lines which are coupled to the solenoids which operate the pump valves are shown at 22, 22₁, 22₂, and 22₃, respectively. Each of these output lines derives a pulse train from the outputs of the clock source 10 and the divider 18 by means of identical gating circuits which are connected to these outputs. These gating circuits include two AND gates 24 and 26 and an OR gate 28 connected to the outputs of the AND gates 24 and 26. The output of the OR gate 28 is coupled to a standard pulse driver 30 which produces a pulse of the required magnitude to operate the solenoid or other device which controls the valve.

The inputs to the AND gates 24 and 26 are labelled

to correspond to the output lines from the clock 10 and the divider stages 18A and 18B. Thus, the AND gate 24 is connected to the output lines A from stage 18A and output lines b from stage 18B. AND gate 26 is connected to output lines C, A, and B.

The operation of the circuit is further described with reference to the timing chart of FIG. 2. In FIG. 2, the different wave forms are indicated by the same letters used to designate the lines on which the wave forms appear in FIG. 1.

The clock pulse train C comprises a plurality of pulses 40 having a leading edge 42 and a trailing edge 44. Each of the pulses 40 is identical and may be considered to have a pulse width equal to t_1 with the time interval between the leading edges 42 of adjacent pulses being equal to P_1 . As noted previously, both of these parameters are separately adjustable. The two stages 18A and 18B of divider 18 change state in response to the trailing edge 44 of the clock pulses 40. Consequently, each of the pulses of pulse train A will have a pulse width equal to the time interval P_1 . In the same fashion, the divider stage 18B changes states at each of the trailing edges of the pulses of pulse train A thereby counting two of the pulses in the pulse train A and four of the pulses 40 in the clock pulse train C.

The outputs from the gates 24 indicated as $\overline{AB}$, $\overline{AB}$, $\overline{AB}$ and $\overline{AB}$, may be considered to be a plurality of first pulse trains, the wave forms of which are illustrated in FIG. 2. Each of these pulse trains is identical and includes a plurality of pulses having a width equal to P_1 with the time interval between the leading edges of successive pulses being equal to $4P_1$, that is, four times the interval between the leading edges of a clock pulse 40 and the fourth succeeding clock pulse 40'.

As shown in FIG. 2, the leading edges of the pulses in one first pulse train occur concurrently with the trailing edges of the pulses in a successive first pulse train. That is, there is no overlap between the pulses of train $\overline{AB}$ and $\overline{AB}$.

The respective gates 26 introduce the overlap into the respective first pulse trains produced on the output of the gates 24. Each of the AND gates 26 is responsive to the clock pulse train C and the next adjacent first pulse train. In other words, considering the pulse trains illustrated in FIG. 2, the AND gate 26 in the first output channel passes those clock pulses which occur concurrently with the pulses of the first pulse train $\overline{AB}$. Consequently, each of the clock pulses 50 (illustrated in dashed lines) will be passed through the AND gate 26 and combined with the first pulse train $\overline{AB}$ in the OR gate 28.

In like fashion, the clock pulses 52 will be combined with the pulse train $\overline{AB}$, clock pulses 54 will be combined with pulse train $\overline{AB}$, and clock pulses 56 will be combined with the pulse train $\overline{AB}$. Since the pulse width of the clock pulses 50, 52, 54 and 56 is adjustable, it is possible to effectively increase the width of the pulses in each of the four first pulse trains by a substantial amount which can be varied from zero (by opening switch 20) to almost twice the width of the pulses illustrated in FIG. 2. In effect, the pulses of each train overlap the pulses of an adjacent train by an amount equal to the pulse width of the clock pulses. Each of the output pulse trains appearing on lines 22 will be identical except there will be a fixed time relationship between the corresponding pulses of successive trains with the extent to which such pulses overlap each other in time being adjustable by controlling the time duration (t_1) of the pulses of the clock pulse train C. The frequency of the output pulse trains is adjustable by controlling the frequency of the clock pulse train C, that is by adjusting the time interval P_1 between adjacent clock pulses. Hence, these output pulse trains have the relationship required to suitably control the valves associated with the individual pump chambers of a multi-chamber pump of the type described above.

FIG. 3 is a schematic diagram of a preferred embodiment of the clock pulse generator. It comprises a standard monostable multi-vibrator 70 including two transistors 71 and 73 and respective potentiometers 72 and 74 in the feedback loops between the collector of each transistor and the base of the other transistor. By adjusting the value of potentiometer 72, the duration of the pulse output at the collector of transistor 71b can be controlled. Similarly, potentiometer 74 adjusts the time interval between adjacent pulses.

The output at the collector of transistor 71b comprises a train of negative going clock pulses. These negative going clock pulses are then passed through two inverter stages 76 and 78 each of which comprises a grounded emitter transistor. The output from the collector of inverter 76 will be the desired clock pulse train C with the output from the collector of transistor 78 comprising the complementary output $\overline{C}$.

Although a preferred embodiment of the invention has been illustrated and described, the invention is not necessarily so limited. For example, although in its preferred embodiment, it is intended specifically for use with a pump of the type described above, the control circuit alone would have utility in other related situations where a series of individual control pulses is required wherein the pulses of adjacent trains overlap each other in time. As an example, a system of this nature might have utility in controlling a plurality of conveyor members wherein successive members should be started just prior to the stopping of a preceding member.

Although the control of the pulse duration and interval between the clock pulses has been shown manually controllable, a transducer or other sensing means may be used to generate an electrical control signal which could be used to automatically compensate for a change in operating conditions (e.g., fluid viscosity or inertia, etc.) and to use the signal to adjust the clock pulse generator as described previously. For the presently contemplated purposes, the ability to adjust the overlap interval in millisecond intervals is considered sufficient although the principles of the invention would have utility with coarser or finer control. Obviously, the amount of amplification provided by the pulse drivers in the individual output channels can be adjusted to provide any desired ultimate power output drive for whatever purposes the invention is used. The device may be A.C. or battery powered as required. Accordingly, the invention should be defined primarily with reference to the attached claims.

What is claimed is:

1. A timing device for producing an output pulse train on each of a plurality of output channels, wherein each pulse train is identical to the other pulse train and successive pulse trains are delayed in time by the same amount, comprising
 - means for producing a train of identical clock pulses, said means including means for varying the time interval between said clock pulses and means for varying the time duration of said clock pulses,
 - divider means responsive to said clock pulses for producing a plurality of identical first pulse trains, the leading edges of the pulses in each train occurring substantially simultaneously with the trailing edges of the pulses in a successive train, the duration of the pulses in said first pulse trains being determined by the time interval between successive clock pulses and the time interval between adjacent pulses in each of said first pulse trains being equal to the time interval between a preselected number of said clock pulses, and
 - gating means in each of said output channels for combining the pulses of one of said first pulse trains with respective time adjacent clock pulses to provide said output pulse trains, wherein the pulses of any one of said output pulse trains overlap in time the pulses of a successive one of said output pulse trains.

5

2. A timing device according to claim 1, wherein the gating means in each one of said output channels includes an AND gate responsive to said clock pulses and the first pulse train associated with the output pulse train overlapped by the pulse train in said one output channel.

References Cited

UNITED STATES PATENTS

2,790,900	4/1957	Feissel -----	328—62X	
3,327,225	6/1967	Schell -----	328—62	10
3,478,273	11/1969	Duncan et al. -----	328—62X	

6

OTHER REFERENCES

"Clock," by Carnevale and Howe in IBM Technical Disclosure Bulletin, vol. 9, No. 10, dated March 1967, pp. 1313-1314.

5

STANLEY D. MILLER, JR., Primary Examiner

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