(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
8 December 2011 (08.12.2011)

PCT

(10) International Publication Number
WO 2011/150496 A1

(51) International Patent Classification:
G06F 12/02 (2006.01) *G06F 9/44* (2006.01)

(21) International Application Number:
PCT/CA2011/000614

(22) International Filing Date:
31 May 2011 (31.05.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/349,943 31 May 2010 (31.05.2010) US
13/012,754 24 January 2011 (24.01.2011) US

(71) Applicant *(for all designated States except US)*: **MOSAID TECHNOLOGIES INCOPORATED** [CA/CA]; 11 Hines Road, Suite 203, Ottawa, Ontario K2K 2X1 (CA).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **CHOI, Byoung Jin** [CA/CA]; 104 Brady Avenue, Kanata, Ontario K2K 0B1 (CA).

(74) Agents: **DONNELLY, Victoria** et al.; 11 Hines Road, Suite 203, Ottawa, Ontario K2K 2X1 (CA).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

[Continued on next page]

(54) Title: HIGH SPEED INTERFACE FOR DAISY-CHAINED DEVICES

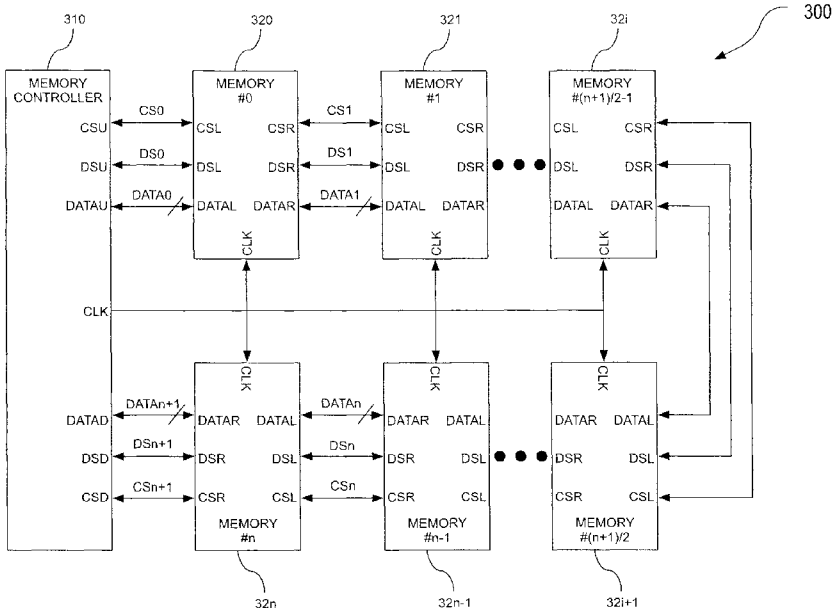


FIG. 3

(57) Abstract: A plurality of devices are operated by storing at a device a first ID number received at a first port of the device and a second ID number received at a second port of the device. The device receives a data command through at least one of the first and second ports. The data command has a command ID number. The device executes the data command when at least one of the command ID number is equal to the first ID number when the data command is received at the first port and the command ID number is equal to the second ID number when the data command is received at the second port.

WO 2011/150496 A1

Published:

— *with international search report (Art. 21(3))*

HIGH-SPEED INTERFACE FOR DAISY-CHAINED DEVICES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a utility application claiming priority to co-pending U.S. Provisional Application Serial No. 61/349,943 filed on May 31, 2010 and US Application Serial No. 13/012,754 filed on January 24, 2011, the entirety of which is incorporated by reference herein.

FIELD OF THE INVENTION

[0002] The invention relates generally to a memory interface. More specifically, the invention relates to a high-speed interface that provides bidirectional communications in a loop-chained memory.

BACKGROUND

[0003] Memory devices are used to store data. The demand for large memory systems with high bandwidth has increased during recent years. For large memory systems, several devices may share a common bus. For example, the data bus or the clock signal may share a single bus, or a set of conductive elements. This bus sharing causes an increase in the capacitive loading of each device. The increased loading degrades signal quality as well as the switching speed of signals, which then requires slower clocking and consequently reduced bandwidth.

[0004] A daisy-chained interconnection 100, is shown in FIG. 1, and a loop chained interconnection 200 is shown in FIG. 2, wherein memory devices are connected in series to reduce capacitive loading on the bus. However each memory device does not use the full

channel but rather just half of the channel to write or read data because data flows only in one direction when the write command or the read command issues.

BRIEF SUMMARY

[0005] In one aspect, the invention features a method for operating a plurality of devices comprising storing at a device a first ID number received at a first port of the device and a second ID number received at a second port of the device. The device receives a data command through at least one of the first and second ports. The data command has a command ID number. The device executes the data command when at least one of the command ID number is equal to the first ID number when the data command is received at the first port and the command ID number is equal to the second ID number when the data command is received at the second port.

[0006] In another aspect, the invention features a high-speed interface device comprising a command state machine in communication with a first port, a second port and a device resource. The command state machine controls data flow therebetween in response to at least one of a first data command received at the first port and a second data command received at the second port. The first port further comprises a first data buffer in communication with a data register and a page buffer, a first data strobe buffer in communication with a data strobe register and a first command strobe buffer in communication with a command strobe register. The data buffer and the command state machine receive a command in response to the first command strobe buffer. The second port further comprises a second data buffer in communication with the data register and the page buffer, a second data strobe buffer in communication with the data strobe register and a second command strobe buffer in communication with the command strobe register. The data buffer and the command state machine receive a command in response to the second

command strobe buffer. The device resource is in communication with the page buffer. The page buffer receives a data in response to at least one of the first data strobe buffer and the second data strobe buffer.

[0007] In another aspect, the invention features a daisy-chained system comprising a plurality of a device connected in a daisy-chain to a controller including a first controller port and a second controller port. Each controller port is capable of communicating a data and a command to each of the device. Each device comprises a command state machine in communication with a first port, a second port and a device resource. The command state machine controls data flow therebetween in response to at least one of a first data command received at the first port and a second data command received at the second port. The first port further comprises a first data buffer in communication with a data register and a page buffer, a first data strobe buffer in communication with a data strobe register and a first command strobe buffer in communication with a command strobe register. The data buffer and the command state machine receive a command in response to the first command strobe buffer. The second port further comprises a second data buffer in communication with the data register and the page buffer, a second data strobe buffer in communication with the data strobe register and a second command strobe buffer in communication with the command strobe register. The data buffer and the command state machine receive a command in response to the second command strobe buffer. The device resource is in communication with the page buffer. The page buffer receives a data in response to at least one of the first data strobe buffer and the second data strobe buffer.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0008] The above and further advantages of this invention may be better understood by referring to the following description in conjunction with the accompanying drawings, in which like numerals indicate like structural elements and features in various figures. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

[0009] FIG. 1 is a conventional memory system with daisy-chained interconnections.

[0010] FIG. 2 is a conventional memory system with loop-chained interconnections.

[0011] FIG. 3 is a memory system with bidirectional loop chained interconnections, according to an embodiment of the invention.

[0012] FIG. 4 is a block diagram of a memory device shown in FIG. 3, according to an embodiment of the invention.

[0013] FIG. 5A is a block diagram of a data input/output block shown in FIG. 4, according to an embodiment of the invention.

[0014] FIG. 5B is a block diagram of a control signal input/output block shown in FIG. 4, according to an embodiment of the invention.

[0015] FIGs. 6A and 6B are schematic diagrams showing the directions of signals when the SETID command issues, according to an embodiment of the invention.

[0016] FIGs. 6C and 6D are schematic diagrams showing the directions of signals when the WRITE command issues, according to an embodiment of the invention.

[0017] FIGs. 6E and 6F are schematic diagrams showing the directions of signals when the READ command issues, according to an embodiment of the invention.

[0018] FIGs. 7A to 7G are flowcharts of the methods performed by a memory device, according to an embodiment of the invention.

[0019] FIGs. 8A to 8D are timing diagrams of the method performed by a memory device, according to an embodiment of the invention.

[0020] FIGs. 9A and 9B are schematic diagrams showing the directions of signals for simultaneous READ and WRITE operations, according to an embodiment of the invention.

[0021] FIG. 9C is a schematic diagram showing the directions of signals for simultaneous WRITE operations, according to an embodiment of the invention.

[0022] FIG. 9D is a schematic diagram showing the directions of signals for simultaneous READ operations, according to an embodiment of the invention.

[0023] FIG. 9E is a block diagram of a memory device shown in the embodiments shown in FIGs 9A to 9D.

[0024] FIG. 10A is a schematic diagram showing the directions of signals, according to an embodiment of the invention.

[0025] FIG. 10B is a block diagram of a memory device shown in the embodiment in FIG. 10A.

DETAILED DESCRIPTION

[0026] Embodiments of the present invention provide bidirectional loop-chained connections between a memory controller and a plurality of devices to optimize communication bandwidth for operations including writing and reading. Reducing capacitive loading on signals shared by the devices improves signal slew rate and thus affords a faster system clock rate and bandwidth. Communication bandwidth is improved in a loop-chained arrangement by transmitting information over multiple preexisting communication paths. A loop-chain is a daisy-chain that begins and ends at the same functional block, for example the memory controller 310 shown in FIG. 3.

[0027] In one example, the communication over multiple paths is concurrent. In another example, the communication over one path temporally overlaps with the communication over another path. The loop-chained connections shown in the various figures and application show two communication ports to and from each device. It is envisioned that each device could have any number of ports. For example, a two-dimensional array would have four ports allowing overlapping communication with the device over all four ports. In another example, a three-dimensional array would have six ports to each device allowing overlapping communication with the device over all six ports.

[0028] A device shown in the various figures and application shows a memory device. It is envisioned that each device could be a transducer device, used for image sensing, radar beam forming, or an acoustic system for example. The device could also be a transceiver device used in a mesh communication network.

[0029] FIG. 3 shows a memory system 300 according to an embodiment of the invention. A memory controller 310 provides overall control of a plurality of memory devices 320, 321, 32i, 32i+1, 32n-1 and 32n. Control signals and data signals are communicated in a bidirectional manner between the controller and the memory devices. For example, in FIG. 3 a command strobe CS0, a data strobe DS0 and a data signal DATA0 communicate between the controller 310 and one port of a memory device 320. A command strobe CS1, a data strobe DS1 and a data signal DATA1 communicate between the memory device 320 and the next memory device 321 in the daisy-chain. The width of the data signal is any feasible width, such as but not limited to 4, 8 or 16. The memory controller 310 provides a clock signal CLK to each device.

[0030] FIG. 4 shows a block diagram of one of the memory devices 320 shown in FIG. 3. Each memory device includes bi-directional buffers DATAL 410, DATAR 411, DSL 420, CSL 421, DSR 422 and CSR 423 for receiving and providing corresponding signals. A state machine 430 receives the CLK signal and provides control signals to the bi-directional buffers 410, 411, 420, 421, 422, 423 and internal registers 440, 441, 442, 443, 444 and 445. A page buffer 460 and 461 provides temporary data storage for data write and read operations to a memory array 470. In another embodiment, where the memory device 320 is substituted for another device, such as a transducer or transceiver, the memory array 470 is a device resource. For example, when the device is a transducer device, the device resource is a transducer converting between electric signals (such as voltage) and pressure. When the device is a transceiver device, the device resource is a transceiver converting between radio frequency emissions and electric signals (such as voltage).

[0031] The memory device 320 can receive a WRITE command with a device ID number from both ports at CSL 421, DSL 420, and DATAL 410 and at CSR 423, DSR 422, and DATAR 411. If the received device ID number is the same as the device ID number registered in the memory device 320, the memory device 320 writes the input data into a page buffer 460 and 461. If the received device ID number is different from the device ID number registered in the memory device 320, the memory device 320 passes the data from DATAL 410 to DATAR 411 or from DATAR 411 to DATAL 410.

[0032] The memory device 320 can also receive a READ command with device ID number from both ports at CSL 421, DSL 420 and DATAL 410 and at CSR 423, DSR 422, and DATAR 411. If the received device ID number is same as the device ID number registered in the memory device 320, the memory device 320 reads out from the page buffer 460 and 461 to DATAL 410 and DATAR 411. If the received device ID number is different from the device ID number registered in the memory device 320, the memory device 320 passes the data from DATAL 410 to DATAR 411 or from DATAR 411 to DATAL 410.

[0033] FIG. 5A is a block diagram of the DATAL input/output block 410 shown in FIG. 4. Tri-state buffers 510 and 520 are controlled by the state machine 430 and an inverter 550. A multiplexer 530 selects data from the register 445 or the buffer 460 for output to DATAL 410. A de-multiplexer 540 provides input data from DATAL 410 to the state machine 430, register 444 or the buffer 460. A person of skill in the art will understand that the DATAR block 411 has a similar structure and works in a similar manner to the DATAL block 410.

[0034] FIG. 5B is a block diagram of the DSL input/output block 420 shown in FIG. 4. Tri-state buffers 511 and 521 are controlled by the state machine 430 and an inverter 551. A

multiplexer 531 selects output from the state machine 430 or the register 443. A de-multiplexer provides data from DSL to the state machine 430 or register 442. A person of skill in the art will understand that the CSL 421, DSR 422 and CSR 423 blocks have a similar structure and work in a similar manner to the DSL block 420.

[0035] FIGs. 6A and 6B show the directions of the command strobe, data strobe and data signals when the SETID command issues. Note the signal directions are all clockwise, FIG. 6A, or all counter-clockwise, FIG. 6B, between the controller 310 and each of the memory devices 320, 321, 32i, 32i+1, 31n-1 and 32n.

[0036] FIGs. 6C and 6D show the directions of signals when a WRITE command issues. Note that the signal directions are from the controller 310 towards the first memory device 320 in FIG. 6C, and from the controller 310 towards the last memory device 32n in FIG. 6D.

[0037] FIGs. 6E and 6F show the directions of signals when a READ command issues. Note that the signal directions are from the first memory device 320 towards the controller 310 in FIG. 6E, and from the last memory device 32n towards the controller 310 in FIG. 6F.

[0038] FIGs. 7A and 7B are flowcharts for a SETID command shown in FIGs. 6A and 6B. At step 700, the controller 310 assigns a device ID corresponding to the device in the loop-chain shown in FIG. 6A, that the controller 310 will write to or read from. At step 700, the controller 310 assigns a reverse device ID corresponding to the device in the loop-chain shown in FIG. 6B, that the controller 310 will write to or read from. In one embodiment, if the device ID and the reverse device ID refer to the same device in the loop-chain then a WRITE command will write a half of a word to one port of the device and the other half of the word to the other port of the device, in a split transaction. In another embodiment, if the device ID and reverse device ID

refer to different devices, then one device is written to or read from with a full word, and a second device is written to or read from with a different full word. At step 700, the controller 310 assigns a latency variable Z and a latency control flag L. If the latency control flag is enabled, then the aforementioned split transaction will delay half of the word being read so that both halves of the word arrive at the controller 310 in the same clock cycle.

[0039] At steps 701, 702 and 703, the controller 310 communicates a SETID command and a device ID to a device as shown in FIG. 6A, for example device 320. Device 320 receives both the SETID command and the device ID at DATAL when the CSL strobe is activated. In one embodiment, CSL is high when active. At steps 711, 712 and 713, the controller 310 communicates a SETID command and a reverse device ID to a device as shown in FIG. 6B, for example device 320. Device 320 receives both the SETID command and the reverse device ID at DATAR when the CSR strobe is activated. In one embodiment, CSR is high when active.

[0040] If the latency control flag is enabled (e.g. L=1) then the latency variable Z is assigned the absolute numerical difference between the device ID and the reverse device ID. For example in FIG. 6A if device 320 was the first of six devices in a loop-chain, then the device ID is assigned to one, the reverse device ID is assigned to six, and the latency variable is five. When device 320 is read with a split transaction then half of a word is read from DATAR passing through five devices until it reaches the controller 310. The other half of the word is read from DATAL after a five cycle delay, thereby reaching the controller 310 in the same cycle as the first half of the word. After calculating the latency variable if the latency control flag is enabled, the SETID command is transmitted to the other port of the device, DATAR at step 709 and DATAL at step 719. At step 710, the device ID is incremented by one and transmitted to the next device

in a clockwise manner shown in FIG. 6A. Similarly, at step 720, the reverse device ID is incremented by one and transmitted to the next device in a counter-clockwise manner shown in FIG. 6B.

[0041] FIGs. 7C, 7D and 7E are flowcharts for a WRITE command. At steps 721 and 722, if the data command ID, for either a WRITE or READ command, does not match the device ID, or similarly a reverse command ID does not match a reverse device ID, then the command is retransmitted to the other port from which is was received as shown in steps 726, 727 and 728.

[0042] If the command is a WRITE command at step 723, with a command ID matching the device ID or a reverse command ID matching the reverse device ID, then the WRITE command is processed. In one embodiment, where both the device ID and the reverse command ID match their respective command ID and reverse command ID, the WRITE commands execute a split transaction as shown in FIG. 7E. In FIG. 7E, a write data received into data buffer 410 as shown in FIG. 4 is first transferred into page buffer 460 at step 730. The write data received into data buffer 411 is then transferred into page buffer 461 at step 732. The contents of pager buffer 460 and 461 are then transferred to the memory array 470 at step 736. Conversely if the write data is first received into data buffer 411, then transferred to page buffer 461 at step 733, then the write data received into data buffer 410 is transferred to pager buffer 460 at step 735. The two half words contained in pager buffer 460 and 461 are then transferred tot he memory array 470 at step 736. In another embodiment, the page buffers 460 and 461 are a dual ported memory that can received data from data buffer 410 and data buffer 411 in the same clock cycle. In another embodiment, the memory array 470 is a multi-ported memory that can communicate directly with the data buffers 410 and 411.

[0043] FIGs. 7C, 7D, 7F and 7G are flowcharts for a READ command. If the command is a READ command at step 724, with the command ID matching the device ID or the reverse command ID matching the reverse device ID, then the READ command is processed as shown in FIGs. 7F and 7G. If a command ID matches the device ID or the reverse command ID matches the reverse device ID and the command is neither a READ nor a WRITE command, then an OTHER command is processed. In one embodiment, the OTHER command is firmware configurable and provides test mode access to the memory array 470.

[0044] At steps 737 and 738, if the data to be read is not available in the page buffers it is transferred from the memory array 470 to the page buffers 460 and 461. In another embodiment the data to be read is read directly from the memory array 470 with multiple ports. At step 739, if the latency control flag is not enabled, then the data from page buffer 460 is transferred to data buffer 410 to be read of one port of the device, and the data from page buffer 461 is transferred to data buffer 411 to be read out of the other port of the device.

[0045] At step 739, if the latency control flag is enabled, and the device ID (X) is less than the reverse device ID (Y), as shown in FIG. 6E, then the data is transferred from the page buffer 461 to the data buffer 411 to be read out of the device 320, and the data from the page buffer 460 is transferred to the data buffer 410 to be read out after a delay equal to the absolute numerical difference between the device ID and the reverse device ID. This ensures that the data from both page buffers 460 and 461 arrive at the controller 310 in the same clock cycle.

[0046] At step 739, if the latency control flag is enabled, and the device ID (X) is not less than the reverse device ID (Y), as shown in FIG. 6F, then the data is transferred from the page buffer 460 to the data buffer 410 to be read out of the device 32n, and the data from the page

buffer 461 is transferred to the data buffer 411 to be read out after a delay equal to the absolute numerical difference between the device ID and the reverse device ID. This ensures that the data from both page buffers 460 and 461 arrive at the controller 310 in the same clock cycle.

[0047] FIGs. 8A is a timing diagram for the SETID command as described in the flowcharts of FIGs. 7A and 7B. First, the memory controller 310 sends the SETID command at CSU, DSU and DATAU with an ID number that may be 0. The memory device 320 in FIG. 3 registers the ID number as 0, and passes the SETID command with the ID number that may be incremented by 1 to the next memory device 321. The SETID command is passed sequentially from each memory device to the next memory device in the loop-chain until it reaches the memory controller 310 resulting in the memory devices 320 through 32n having a register ID numbered from 0 to n respectively. Then, the memory controller 310 sends the SETID command at CSD, DSD and DATAD with a reverse ID number that may be 0. The memory device 32n registers the reverse ID number, 0, and passes the SETID command with reverse ID number that may be incremented by 1 to the next memory device 32n-1. The SETID command is passed sequentially from each memory device to the next memory device in the loop-chain until it reaches the memory controller 310 resulting in the memory devices 32n through 320 having a register reverse ID number from 0 to n respectively. After two SETID commands issue, each of the memory devices have an ID number and a reverse ID number, which indicate the number of devices and the position of each device in the loop-chain. Accordingly, each device can transmit a half word from one port delayed relative to the transmission of the other half word at the second port such that both half words arrive at the controller 310 in the same clock cycle. It is envisioned that when more than two ports exist on each device, for example six ports in a three-

dimensional array, the various device ports can be delayed by different amounts such that data read from each port arrives at the controller in the same cycle.

[0048] FIG. 8B is a timing diagram for the WRITE command as described in the flowcharts of FIGs. 7C, 7D and 7E. The memory controller sends a WRITE command at CSU, DSU and DATAU with a command ID number that may be between 0 and n followed by a half word to be written to a device. The memory controller also sends a WRITE command at CSD, DSD and DATAD with a reverse command ID number corresponding to the same device followed by the other half of the data to be written. The WRITE command is sent through the loop-chain until the command ID number matches the device ID number. The WRITE command is also sent through the loop-chain in the opposing direction until the reverse command ID number matches the reverse device ID number. By not propagating the WRITE command further than is necessary, overall system power is reduced. In another embodiment, the WRITE command is allowed to propagate through the entire loop-chain, which reduces the logic complexity of each device. After a successful match of a command ID number to a device ID number, or a reverse command ID number to a reverse device ID number, the respective command ID numbers read into the device by activating the command strobe, a one or more data is read into the device by activating the data strobe.

[0049] FIGs. 8C and 8D show timing diagrams for a READ command as described in the flowcharts of FIGs. 7C, 7D, 7F and 7G. In one embodiment, to minimize latency while reading out data from memory devices close to the memory controller's CSU, DSU and DATAU, including devices with a registered ID number from 0 to [(n+1)/2]-1, the memory controller sends a READ command at CSU, DSU, and DATAU with an ID number that may be from 0 to

[(n+1)/2]-1. Similarly, to read out data from memory devices close to the memory controller's CSD, DSD and DATAD, including devices with a registered ID number from (n+1)/2 to n, the memory controller sends a READ command at CSD, DSD and DATAD with an ID number that may be from (n+1)/2 to n.

[0050] In another embodiment, to optimize read bandwidth, a READ command with a command ID number is sent at CSU, DSU and DATAU and passed from memory device to memory device until it reaches the memory device where the command ID number and the device ID number match. A READ command with a reverse command ID number is also issued at CSD, DSD and DATAD a passed from memory device to memory device until it reaches the memory device where the reverse command ID number and the reverse device ID number match. The device then reads out half of the data word from page buffer 460 to DATAL as shown in FIG.4 and the other half of the data word from page buffer 461 to DATAR.

[0051] FIGs. 9A and 9B show the directions of signals for a concurrent READ and WRITE. In FIG. 9A, the memory controller 910 sends a WRITE command at CSU, DSU and DATAU with a device ID number i that may be between 0 and n and a READ command at CSD, DSD and DATAD with a reverse device ID number that may be between i and n. For example, the memory controller 910 can write to device 921 while reading from device 92n-1. In FIG. 9B, the memory controller 910 sends a READ command at CSU, DSU and DATAU with device ID number i that may be between 0 and n and a WRITE command at CSD, DSD and DATAD with device ID number that may be between i and n. The memory controller 910 simultaneously writes data into and reads data from one single memory device or two different memory devices.

For example, the memory controller 910 can read from device 921 while writing to device 92n-1, or the memory controller 910 could read and write from device 921.

[0052] FIG. 9C shows the directions of signals for two concurrent WRITE commands. The memory controller 910 sends a WRITE command at CSU, DSU and DATAU with a device ID number, i, that may be between 0 and n-1 and a WRITE command at CSD, DSD and DATAD with a reverse device ID number that may be between i+1 and n. The memory controller 910 simultaneously writes data into two different memory devices.

[0053] FIG. 9D shows the directions of signals for two concurrent READ commands. The memory controller 910 sends a READ command at CSU, DSU and DATAU with a device ID number, i, that may be between 0 and n-1 and a READ command at CSD, DSD and DATAD with a reverse device ID number that may be between i+1 and n. The memory controller 910 simultaneously reads data from two different memory devices.

[0054] FIG. 9E is an embodiment of a block diagram of a memory device 920 for simultaneous access. In another embodiment, the page buffers 940 and 941 are a single dual ported memory.

[0055] FIG. 10A shows the directions of signals for a loop-back system with a source synchronous clock. FIG. 10B shows a block diagram of a memory device 1020 for source synchronous clock shown in Fig. 10A. In FIG. 10A the memory controller 1010 sends a clock at CLK. Memory devices 1020 to 102n pass a clock (CLK) from CLKLi to CLKRo and from CLKRi to CLKLo. The memory controller 1010 sends commands synchronized with the clock thereby minimizing clock skew and affording high clock rates.

[0056] Memory devices 1020 to 102n receive commands at the command strobe buffer 421, data strobe buffer 420 and data buffer 410 synchronized with CLKLi and if required then sends commands at command strobe buffer 423, data strobe buffer 422 and data buffer 411 synchronized with CLKRo.

[0057] While the invention has been shown and described with reference to specific preferred embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the following claims.

[0058] What is claimed is:

CLAIMS

1. A method for operating a plurality of devices comprising:

storing at a device a first ID number received at a first port of the device and a second ID number received at a second port of the device;

receiving, by the device, a data command through at least one of the first and second ports, the data command having a command ID number; and

executing, by the device, the data command when at least one of the command ID number is equal to the first ID number when the data command is received at the first port, and the command ID number is equal to the second ID number when the data command is received at the second port.

2. The method of claim 1 further comprising transmitting the data command without execution from the device through the second port, when the data command is received at the first port and the command ID is not the same as the first ID number, and transmitting the data command without execution from the device through the first port when the data command is received at the second port and the command ID is not the same as the second ID number.

3. The method of claim 1 further comprising writing a word to the device in response to executing the data command received at either the first port or the second port.

4. The method of claim 1 further comprising writing, in response to executing a data command, a first half-word to the first port of the device, and a second half-word to the second port of the device.

5. The method of claim 1 further comprising reading a word from the device in response to executing the data command.

6. The method of claim 1 further comprising reading, in response to executing a data command, a first half-word from the first port of the device, and a second half-word from the second port of the device.

7. The method of claim 1 further comprising reading, in response to executing a data command, a first half-word from the first port of the device, a second half-word from the second port of the device, and delaying one of the first half-word and the second half-word by a number of clock cycles equal to the absolute numerical difference between the first ID number and the second ID number.

8. The method of claim 1 wherein the data command is a read data command and the method further comprises receiving a write data command at one of the first and second ports not receiving the read data command, reading a word from the device in response to executing the read data command and writing a word to the device in response to executing the write data command.

9. A high-speed interface device comprising:

a command state machine in communication with a first port, a second port and a device resource, the command state machine controlling data flow therebetween in response to at least one of a first data command received at the first port and a second data command received at the second port;

the first port further comprising a first data buffer in communication with a data register and a page buffer, a first data strobe buffer in communication with a data strobe register and a first command strobe buffer in communication with a command strobe register, the data buffer and the command state machine receiving a command in response to the first command strobe buffer;

the second port further comprising a second data buffer in communication with the data register and the page buffer, a second data strobe buffer in communication with the data strobe register and a second command strobe buffer in communication with the command strobe register, the data buffer and the command state machine receiving a command in response to the second command strobe buffer; and

the device resource in communication with the page buffer, the page buffer receiving a data in response to at least one of the first data strobe buffer and the second data strobe buffer.

10. The high-speed interface device of claim 9 wherein the device resource is a memory.

11. The high-speed interface device of claim 9 wherein the device resource is a transceiver.

12. The high-speed interface device of claim 9 wherein one of the first data command and the second data command is a write command.

13. The high-speed interface device of claim 9 wherein the first data command is a write command and the second data command is a write command.

14. The high-speed interface device of claim 9 wherein one of the first data command and the second data command is a read command.

15. The high-speed interface device of claim 9 wherein the first data command is a read command and the second data command is a read command.

16. The high-speed interface device of claim 9 wherein the page buffer is capable of simultaneous access by the first data buffer and the second data buffer.

17. The high-speed interface device of claim 9 wherein the command state machine includes source synchronous clocking for each of the first port and the second port.

18. A daisy-chained system comprising:

a plurality of a device connected in a daisy-chain to a controller including a first controller port and a second controller port, each controller port capable of communicating a data and a command to each of the device,

each device comprising a command state machine in communication with a first port, a second port and a device resource, the command state machine controlling data

flow therebetween in response to at least one of a first data command received at the first port and a second data command received at the second port,

the first port further comprising a first data buffer in communication with a data register and a page buffer, a first data strobe buffer in communication with a data strobe register and a first command strobe buffer in communication with a command strobe register, the data buffer and the command state machine receiving a command in response to the first command strobe buffer,

the second port further comprising a second data buffer in communication with the data register and the page buffer, a second data strobe buffer in communication with the data strobe register and a second command strobe buffer in communication with the command strobe register, the data buffer and the command state machine receiving a command in response to the second command strobe buffer, and

the device resource in communication with the page buffer, the page buffer receiving a data in response to at least one of the first data strobe buffer and the second data strobe buffer.

19. The daisy-chained system of claim 18 wherein each device comprises a memory.

20. The daisy-chained system of claim 18 wherein each device transmits a clock signal to an adjacent device in the daisy-chain.

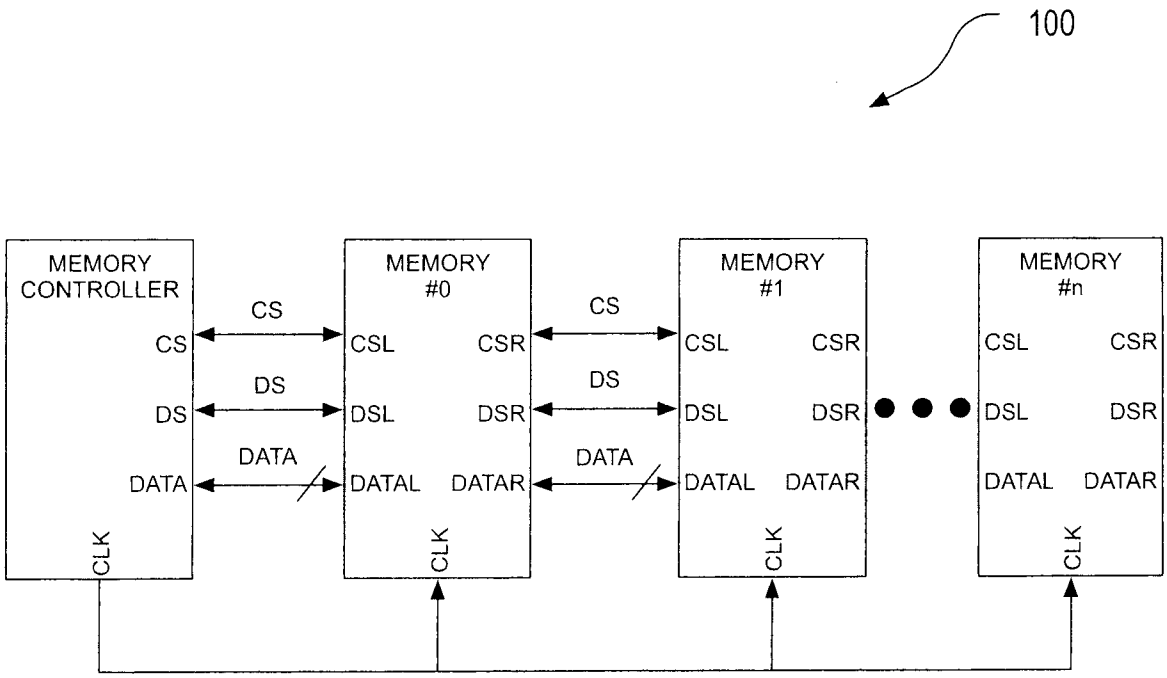


FIG. 1
Prior Art

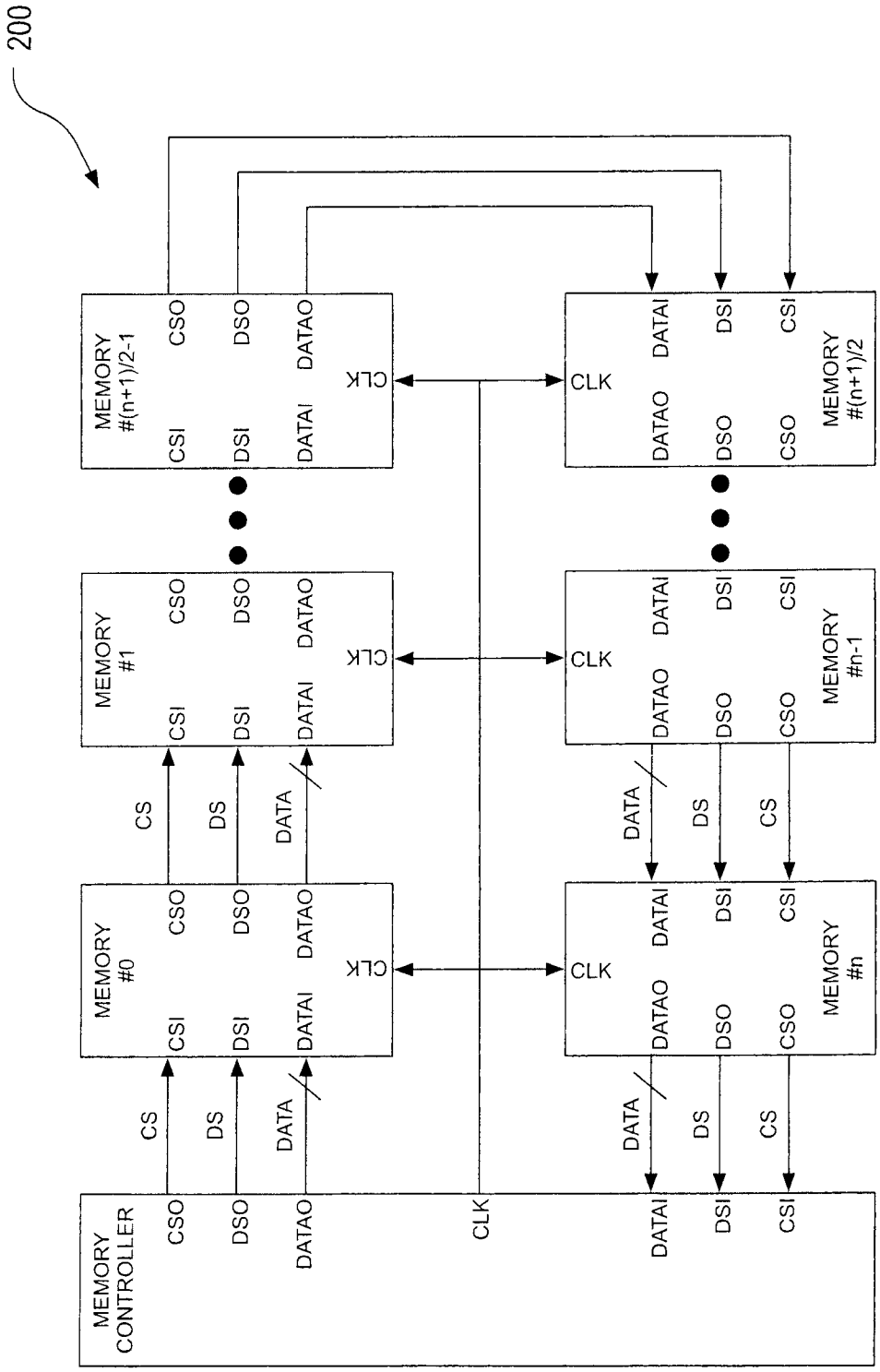


FIG. 2
Prior Art

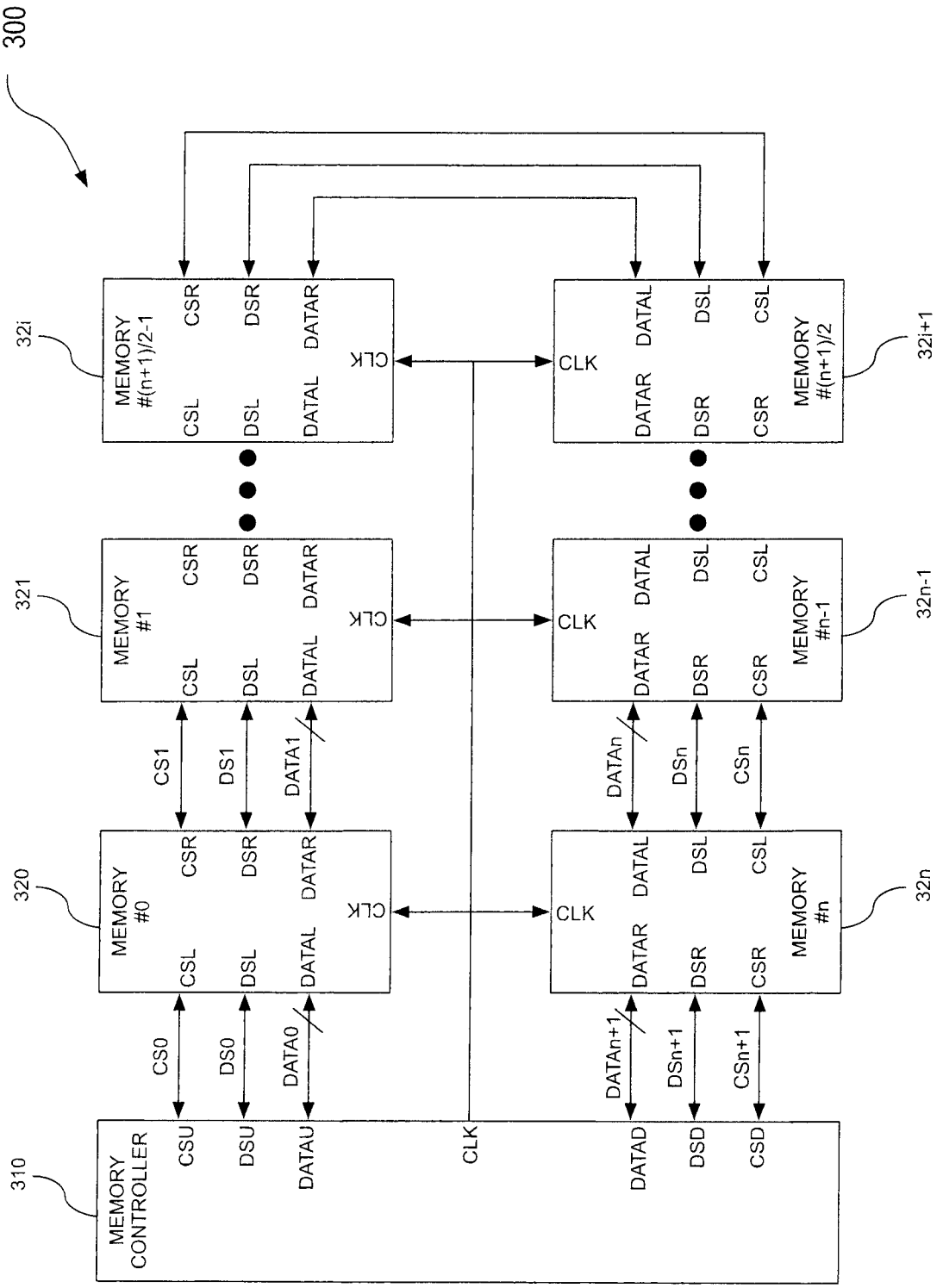

300
MEMORY CONTROLLER
310
CSU
DSU
DATAU
CLK
DATAD
DSD
CSD
CS0
DS0
DATA0
CS1
DS1
DATA1
DATAn+1
DSn+1
CSn+1
DATAn
DSn
CSn
MEMORY #0
320
MEMORY #1
321
MEMORY #(n+1)/2-1
32i
MEMORY #n
32n
MEMORY #n-1
32n-1
MEMORY #(n+1)/2
32i+1
CSL
DSL
DATAL
CSR
DSR
DATAR
CLK

FIG. 3

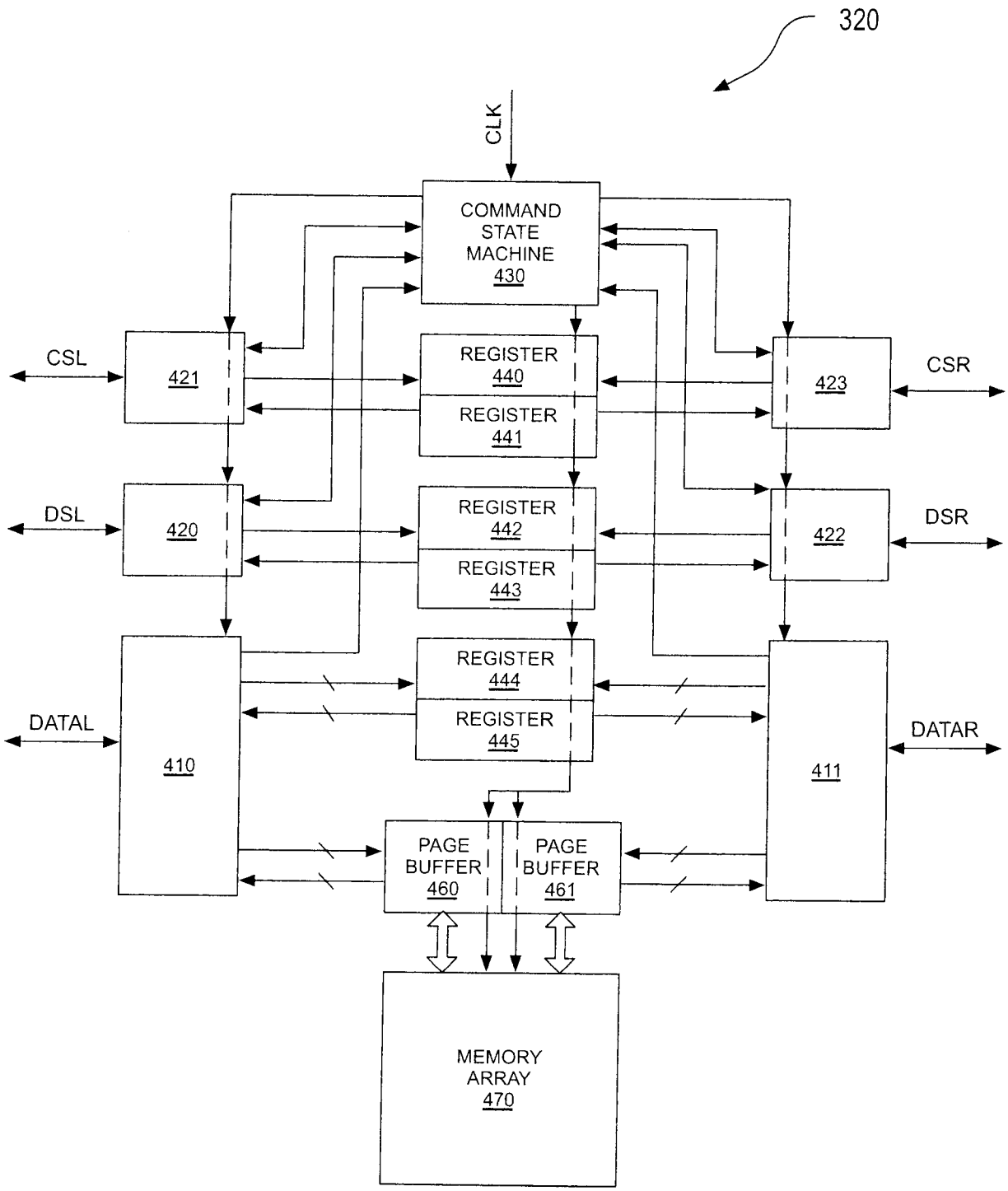

320
CLK
COMMAND STATE MACHINE 430
CSL
421
REGISTER 440
REGISTER 441
423
CSR
DSL
420
REGISTER 442
REGISTER 443
422
DSR
REGISTER 444
REGISTER 445
DATAL
410
411
DATAR
PAGE BUFFER 460
PAGE BUFFER 461
MEMORY ARRAY 470

FIG. 4

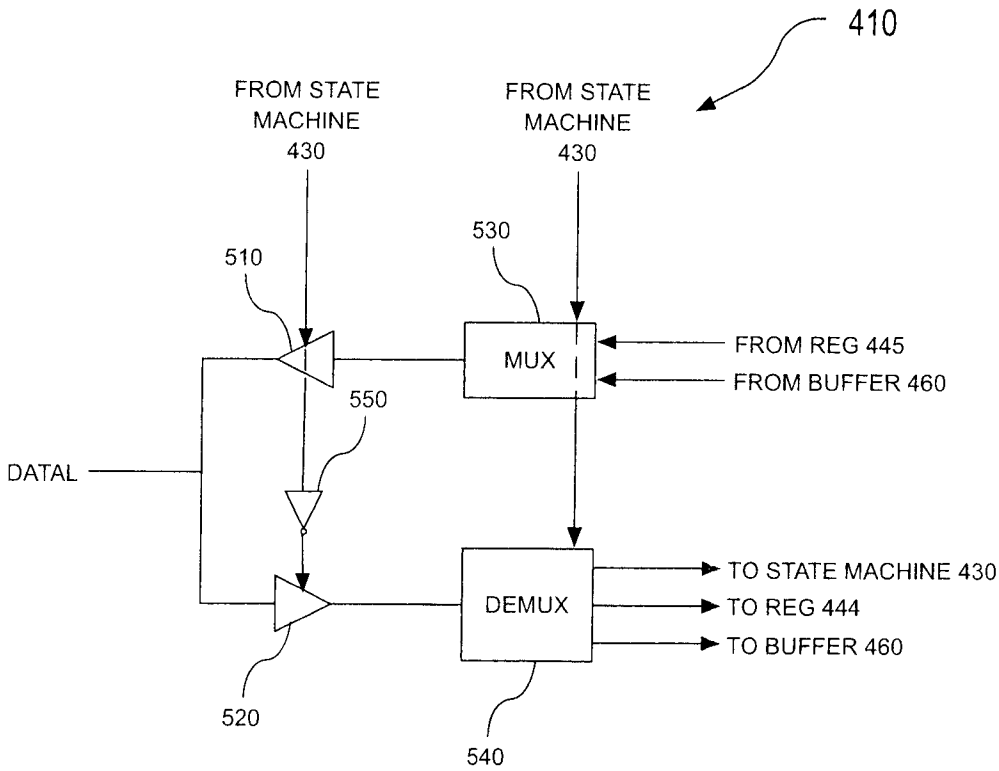

410
FROM STATE MACHINE 430
FROM STATE MACHINE 430
530
510
MUX
FROM REG 445
FROM BUFFER 460
550
DATAL
DEMUX
TO STATE MACHINE 430
TO REG 444
TO BUFFER 460
520
540

FIG. 5A

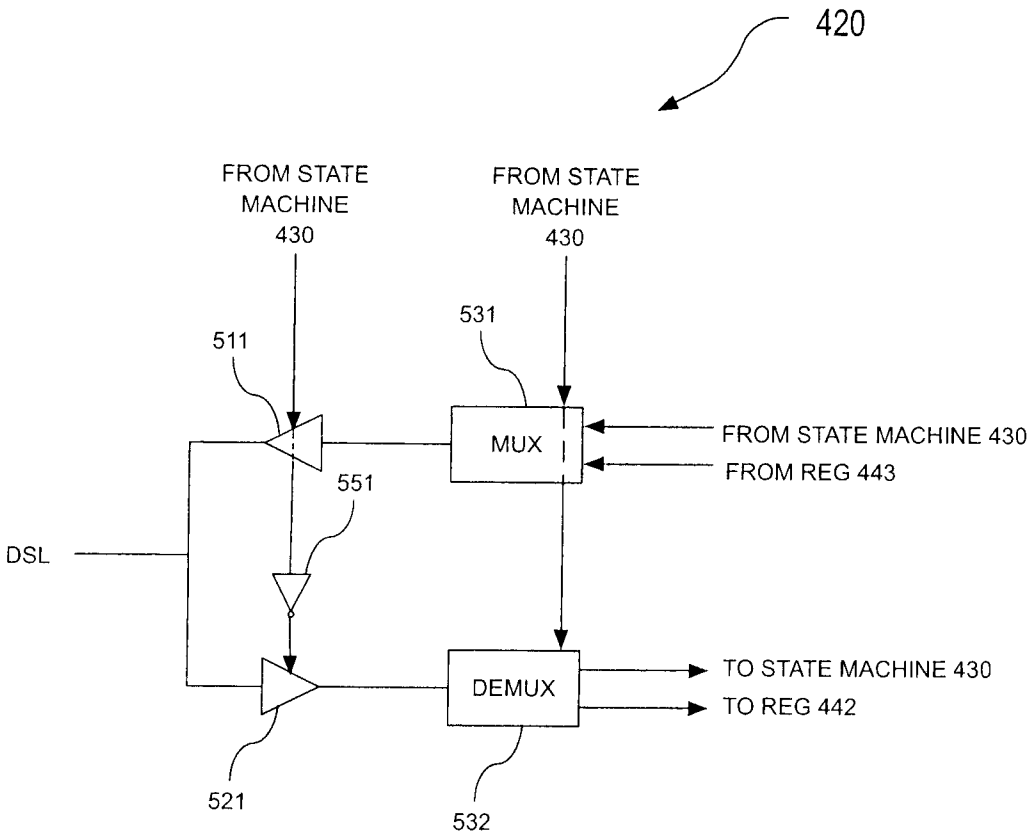

420
FROM STATE MACHINE 430
FROM STATE MACHINE 430
511
531
MUX
FROM STATE MACHINE 430
FROM REG 443
551
DSL
DEMUX
TO STATE MACHINE 430
TO REG 442
521
532

FIG. 5B

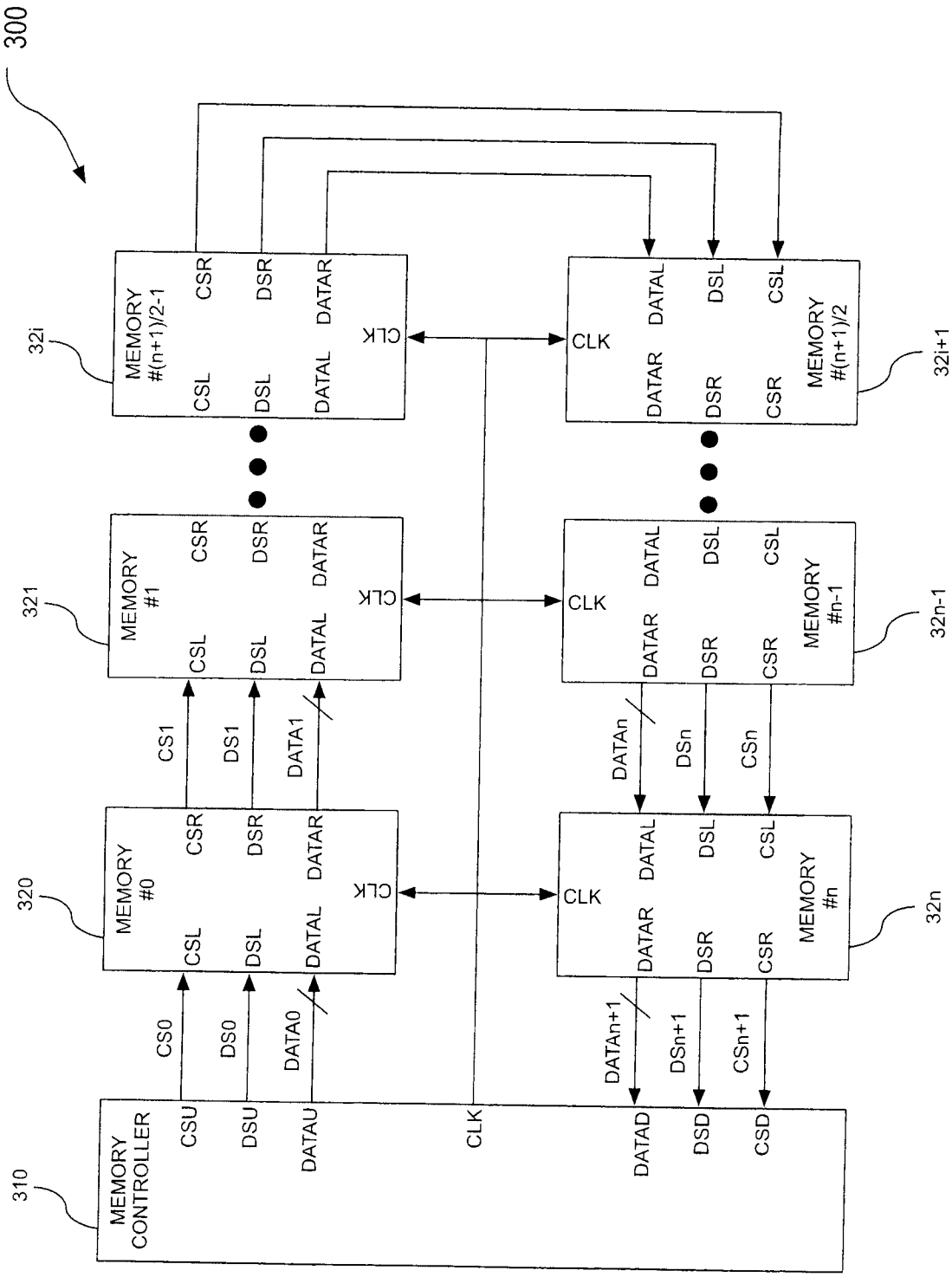

300
MEMORY CONTROLLER
310
CSU
DSU
DATAU
CS0
DS0
DATA0
CLK
DATAD
DSD
CSD
MEMORY #0
320
MEMORY #1
321
MEMORY #(n+1)/2-1
32i
MEMORY #(n+1)/2
32i+1
MEMORY #n-1
32n-1
MEMORY #n
32n
CS1
DS1
DATA1
DATAn
DSn
CSn
DATAn+1
DSn+1
CSn+1
CSR
DSR
DATAR
CSL
DSL
DATAL
CLK

FIG. 6A

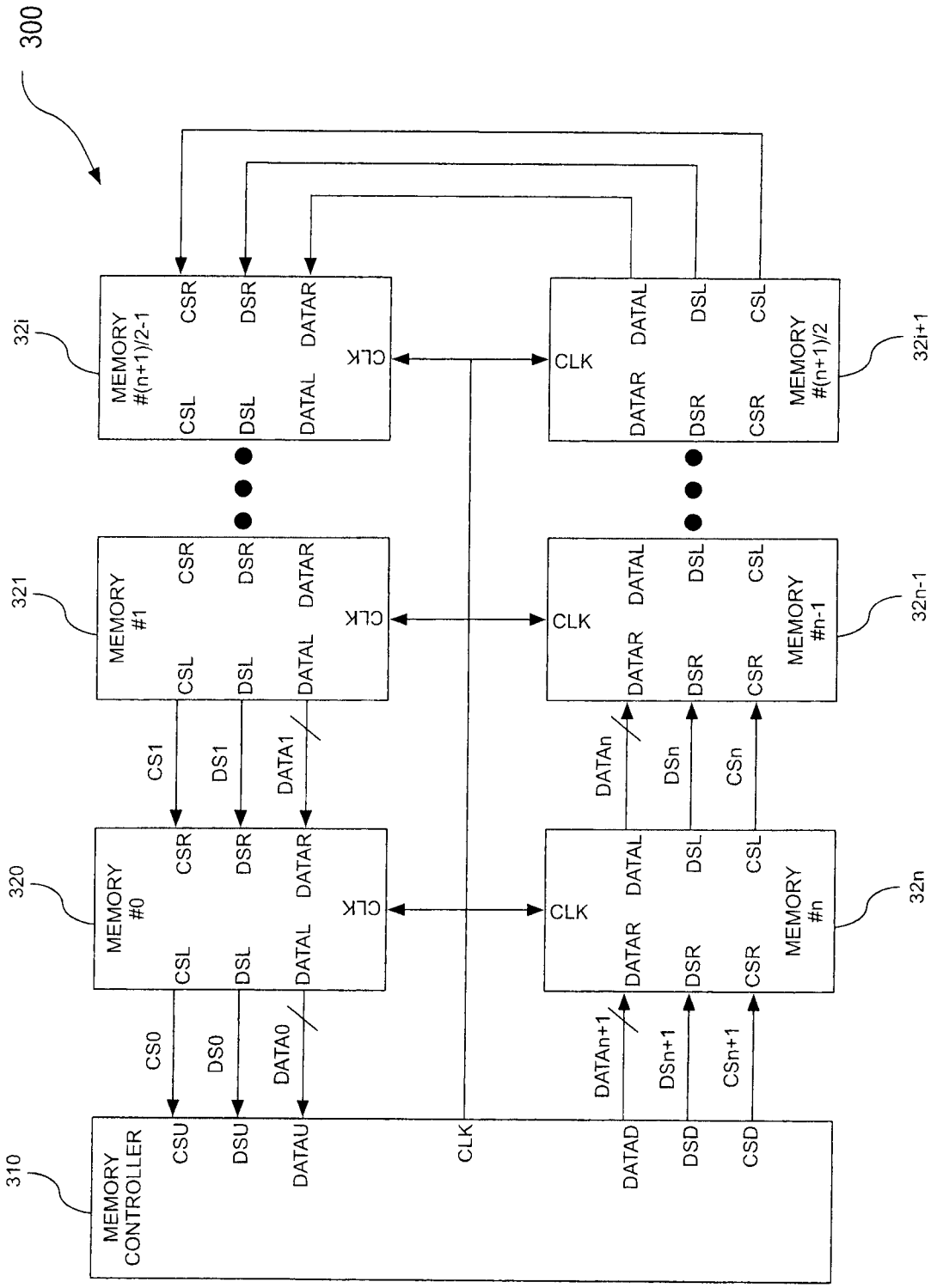

300
MEMORY CONTROLLER
310
CSU
DSU
DATAU
CS0
DS0
DATA0
CS1
DS1
DATA1
CLK
DATAD
DSD
CSD
DATAn+1
DSn+1
CSn+1
DATAn
DSn
CSn
MEMORY #0
320
MEMORY #1
321
MEMORY #(n+1)/2-1
32i
MEMORY #(n+1)/2
32i+1
MEMORY #n-1
32n-1
MEMORY #n
32n
CSR
DSR
DATAR
CSL
DSL
DATAL
CLK

FIG. 6B

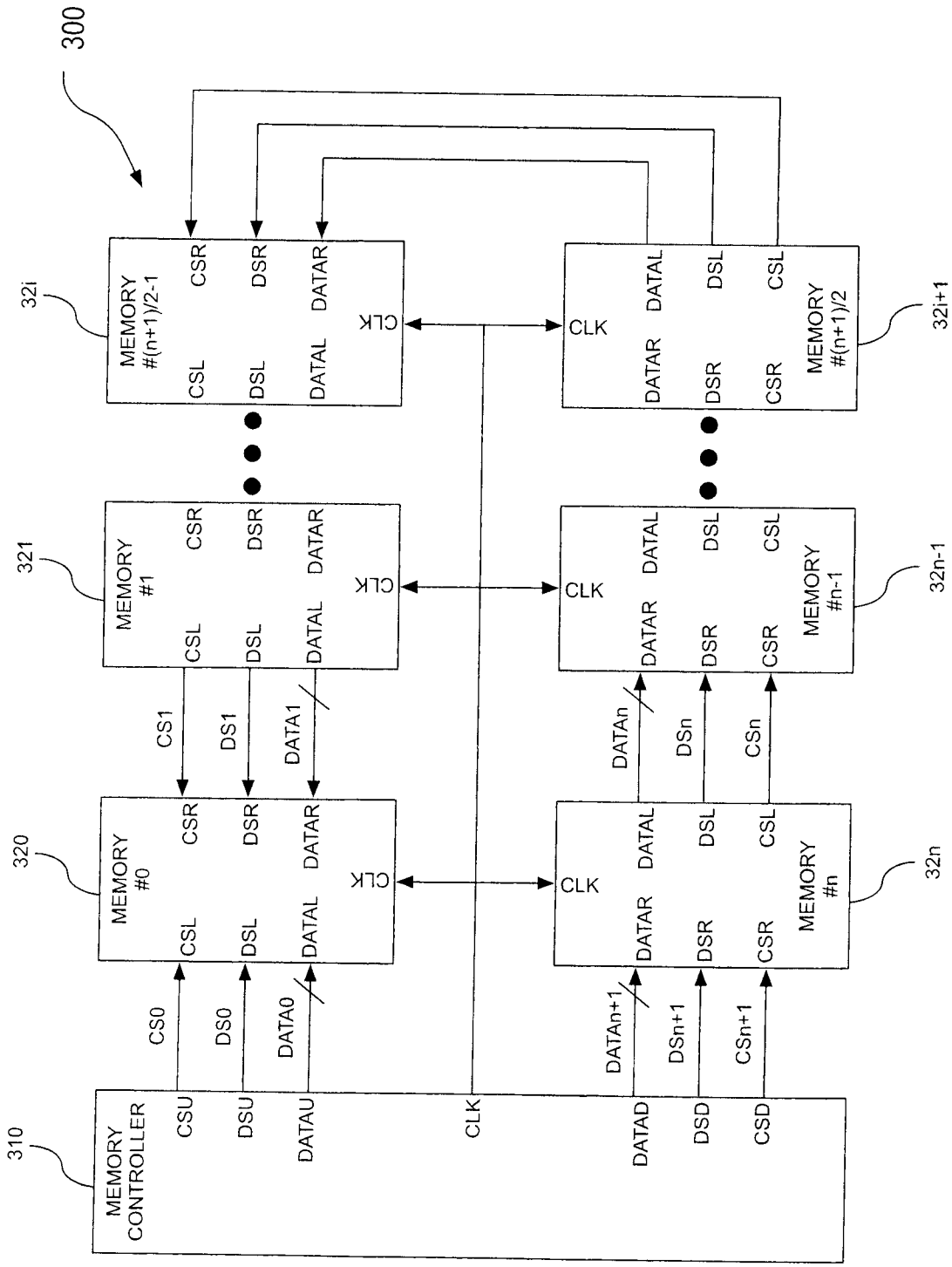

300
MEMORY CONTROLLER
310
MEMORY #0
320
MEMORY #1
321
MEMORY #(n+1)/2-1
32i
MEMORY #(n+1)/2
32i+1
MEMORY #n-1
32n-1
MEMORY #n
32n
CSU
DSU
DATAU
CS0
DS0
DATA0
CS1
DS1
DATA1
CSD
DSD
DATAD
CSn+1
DSn+1
DATAn+1
CSn
DSn
DATAn
CLK
CSR
DSR
DATAR
CSL
DSL
DATAL

FIG. 6C

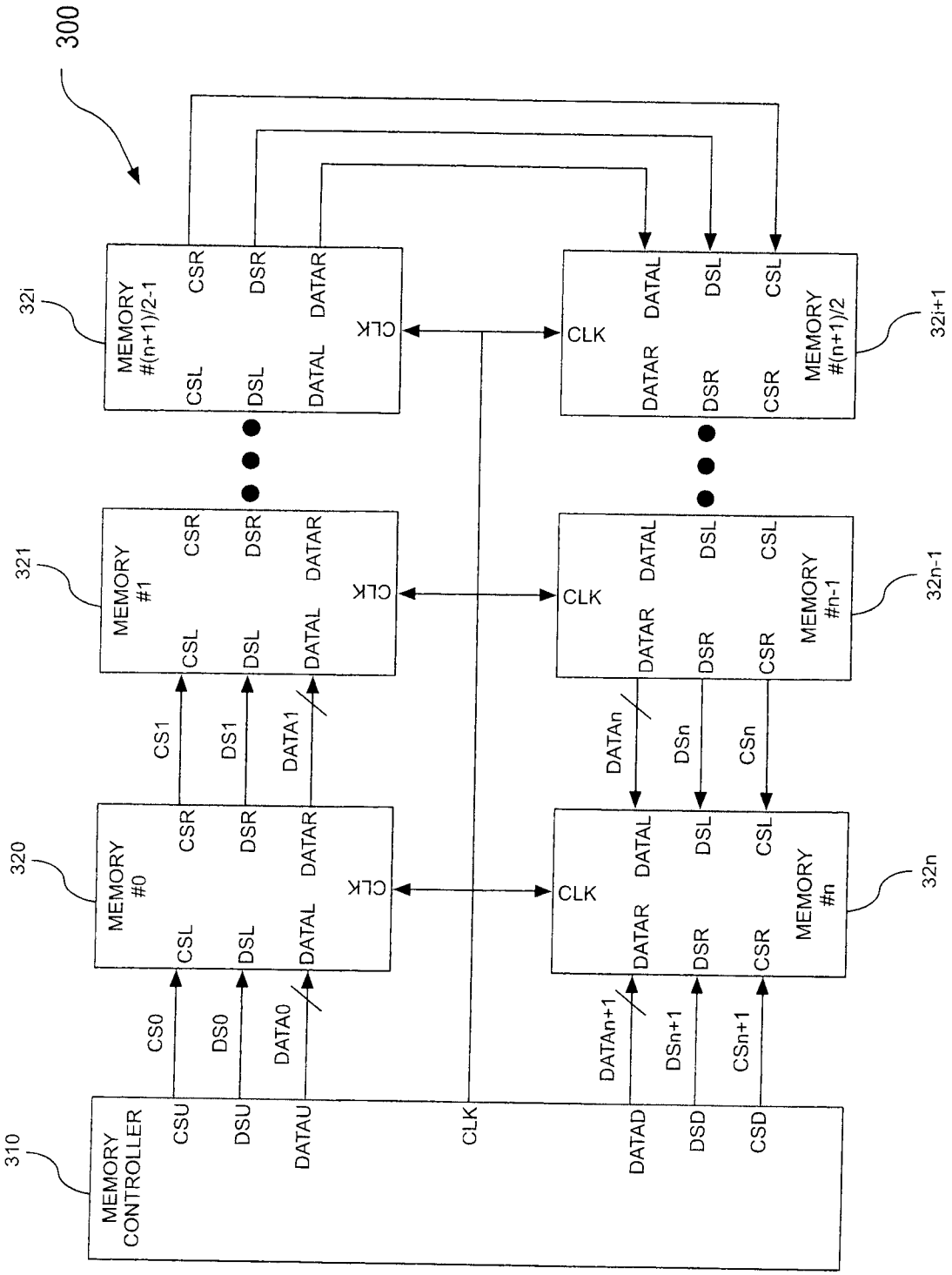

300
310
MEMORY CONTROLLER
CSU
DSU
DATAU
CLK
DATAD
DSD
CSD
CS0
DS0
DATA0
CS1
DS1
DATA1
DATAn
DSn
CSn
DATAn+1
DSn+1
CSn+1
320
MEMORY #0
321
MEMORY #1
32i
MEMORY #(n+1)/2-1
32i+1
MEMORY #(n+1)/2
32n-1
MEMORY #n-1
32n
MEMORY #n
CSR
DSR
DATAR
CSL
DSL
DATAL
CLK

FIG. 6D

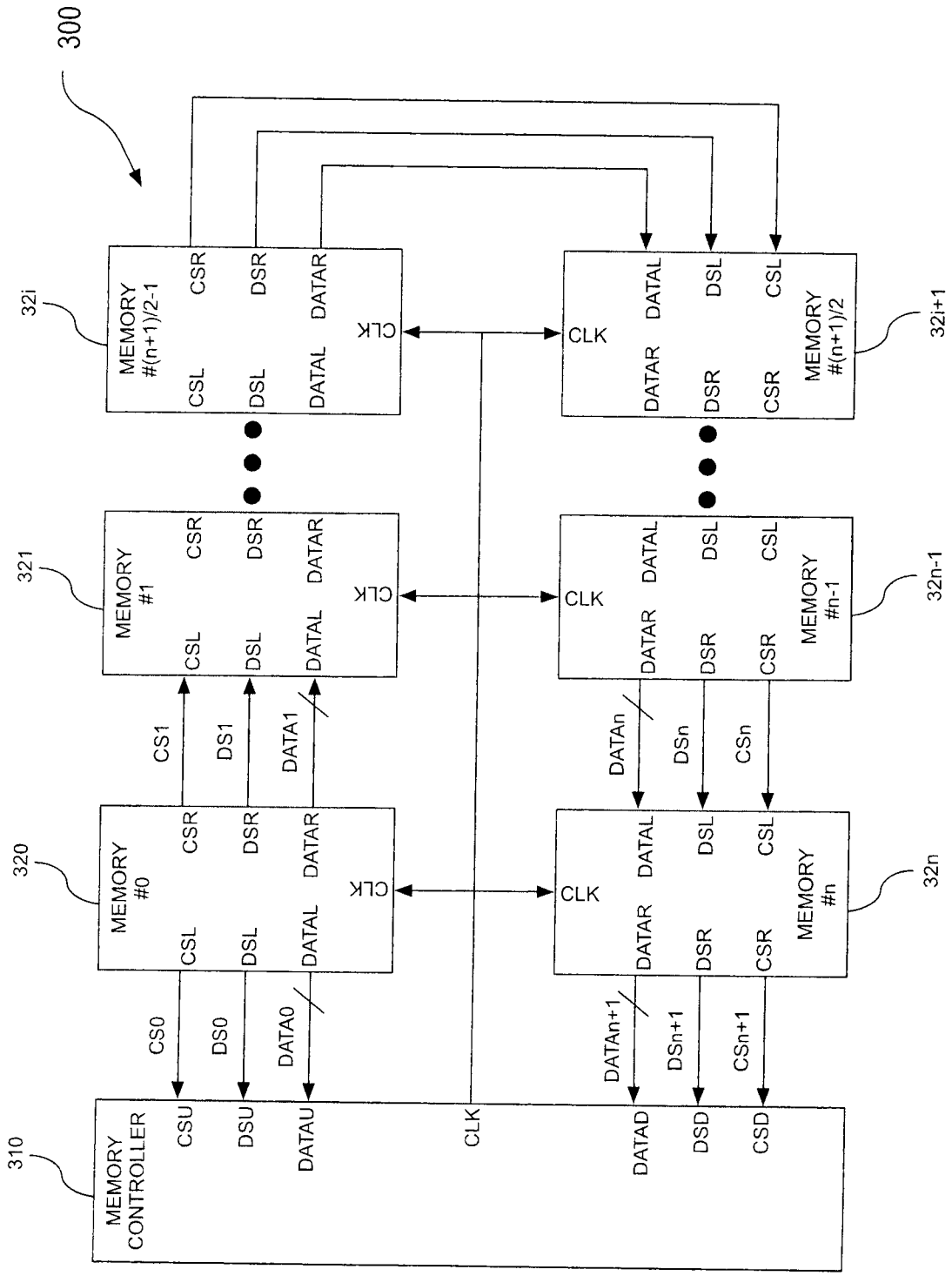

300
MEMORY CONTROLLER
310
MEMORY #0
320
MEMORY #1
321
MEMORY #(n+1)/2-1
32i
MEMORY #(n+1)/2
32i+1
MEMORY #n-1
32n-1
MEMORY #n
32n
CSU
DSU
DATAU
CS0
DS0
DATA0
CS1
DS1
DATA1
CSD
DSD
DATAD
CSn+1
DSn+1
DATAn+1
CSn
DSn
DATAn
CLK
CSR
DSR
DATAR
CSL
DSL
DATAL

FIG. 6E

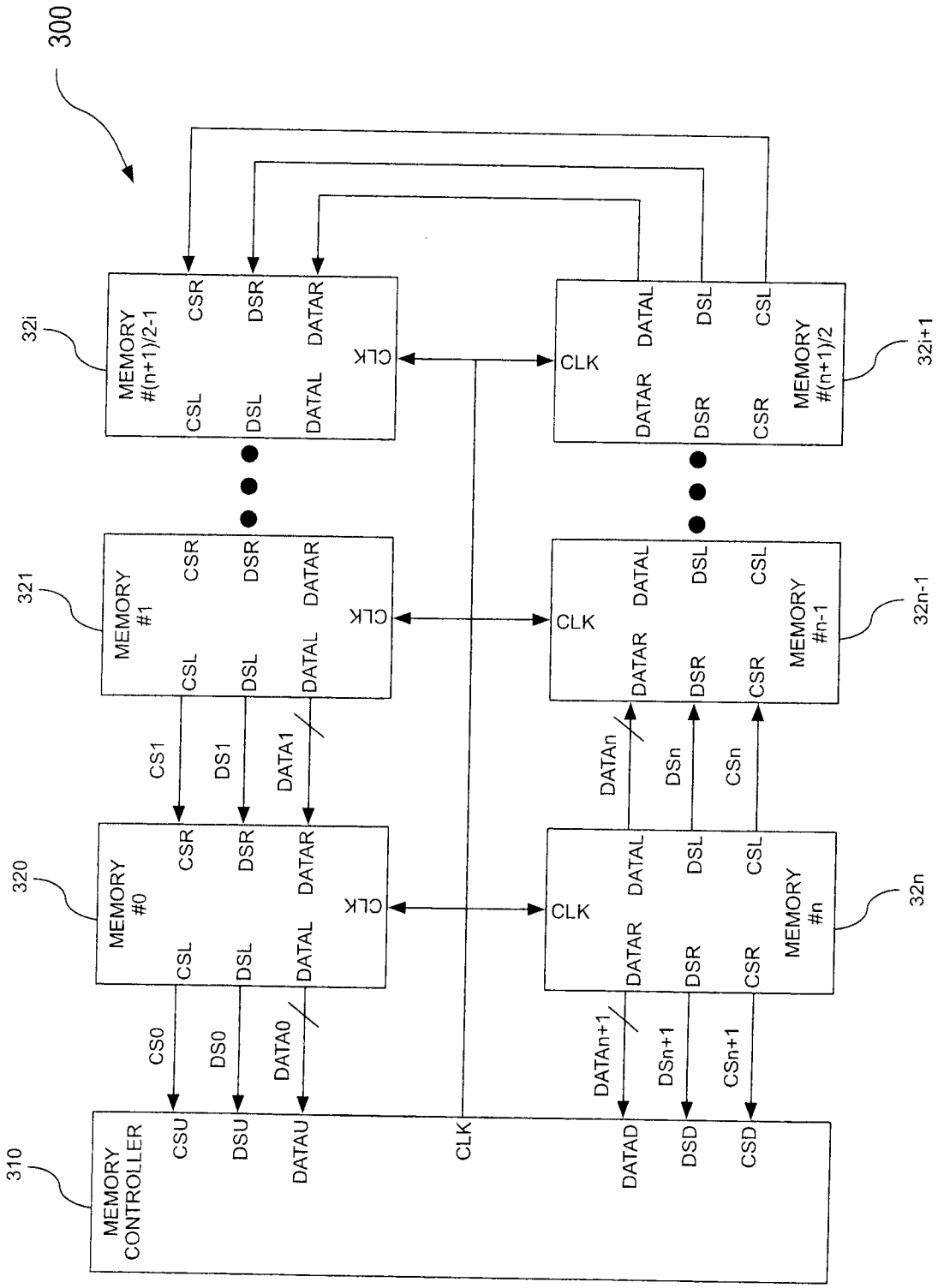

300
MEMORY CONTROLLER
310
MEMORY #0
320
MEMORY #1
321
MEMORY #(n+1)/2-1
32i
MEMORY #(n+1)/2
32i+1
MEMORY #n-1
32n-1
MEMORY #n
32n
CSR
DSR
DATAR
CSL
DSL
DATAL
CLK
CS0
DS0
DATA0
CS1
DS1
DATA1
CSn
DSn
DATAn
CSn+1
DSn+1
DATAn+1
CSU
DSU
DATAU
CSD
DSD
DATAD

FIG. 6F

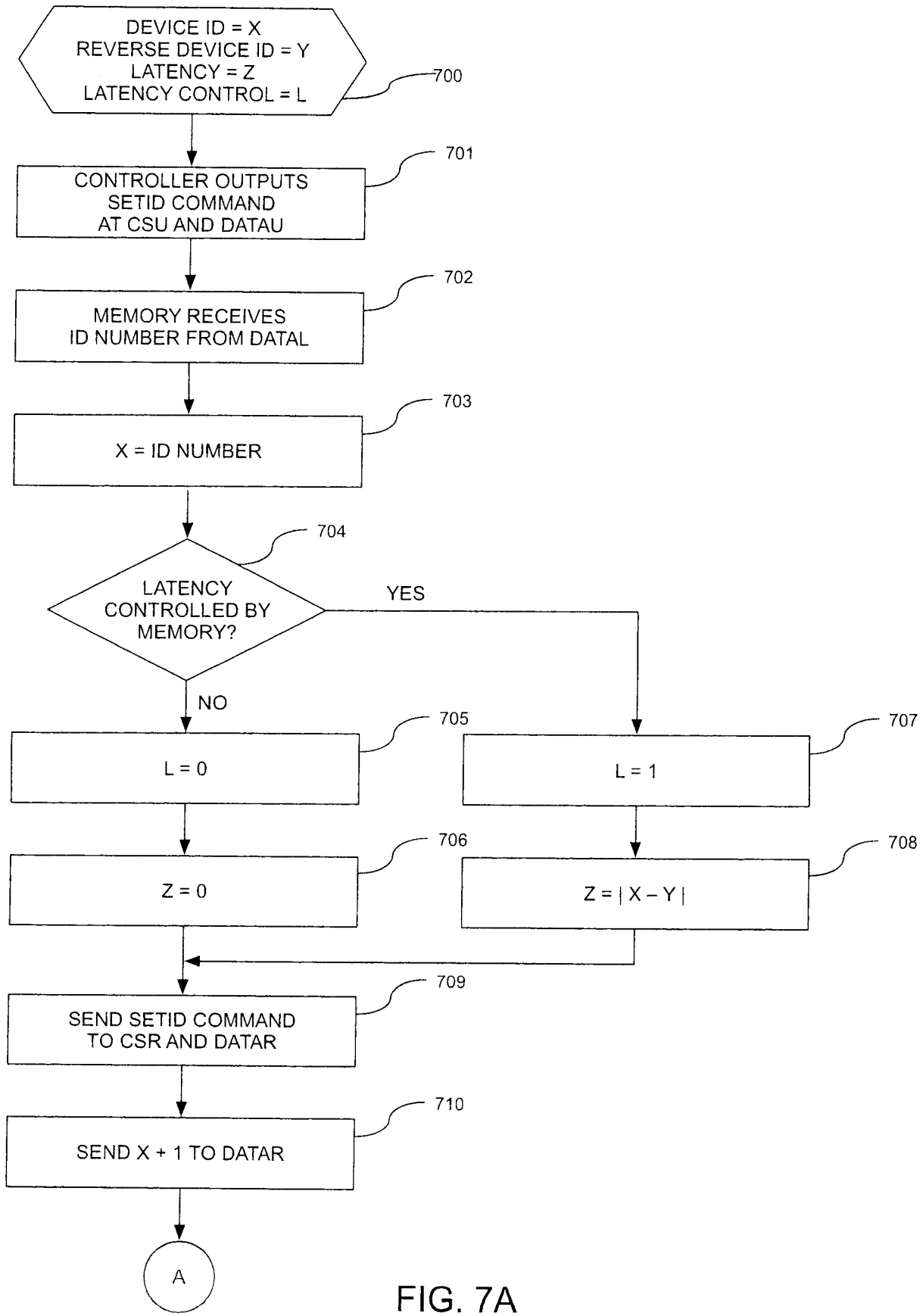

DEVICE ID = X
REVERSE DEVICE ID = Y
LATENCY = Z
LATENCY CONTROL = L
700
CONTROLLER OUTPUTS SETID COMMAND AT CSU AND DATAU
701
MEMORY RECEIVES ID NUMBER FROM DATAL
702
X = ID NUMBER
703
LATENCY CONTROLLED BY MEMORY?
704
YES
NO
L = 0
705
L = 1
707
Z = 0
706
Z = | X – Y |
708
SEND SETID COMMAND TO CSR AND DATAR
709
SEND X + 1 TO DATAR
710
A

FIG. 7A

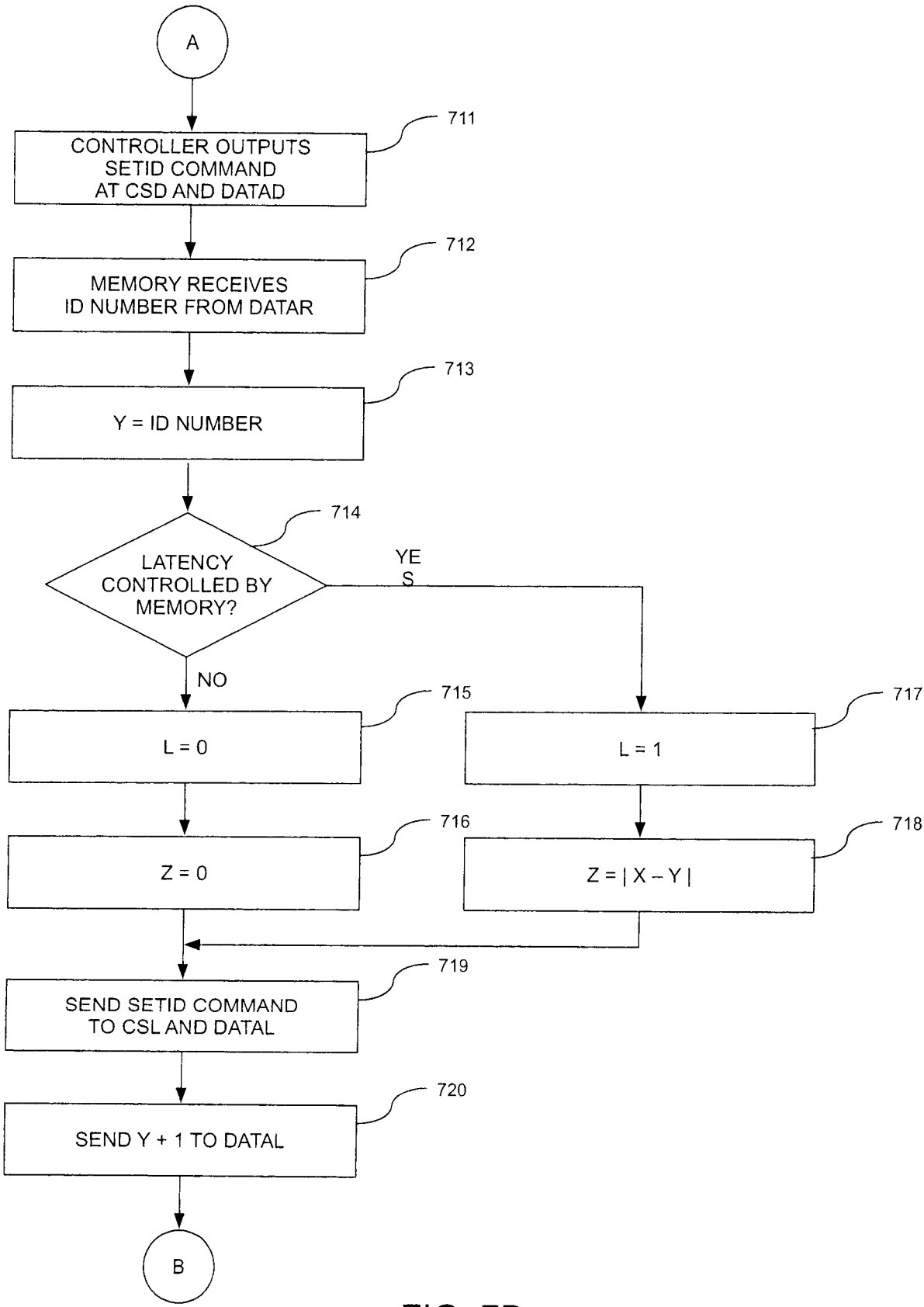

A
CONTROLLER OUTPUTS SETID COMMAND AT CSD AND DATAD
711
MEMORY RECEIVES ID NUMBER FROM DATAR
712
Y = ID NUMBER
713
LATENCY CONTROLLED BY MEMORY?
714
YES
NO
L = 0
715
L = 1
717
Z = 0
716
Z = | X – Y |
718
SEND SETID COMMAND TO CSL AND DATAL
719
SEND Y + 1 TO DATAL
720
B

FIG. 7B

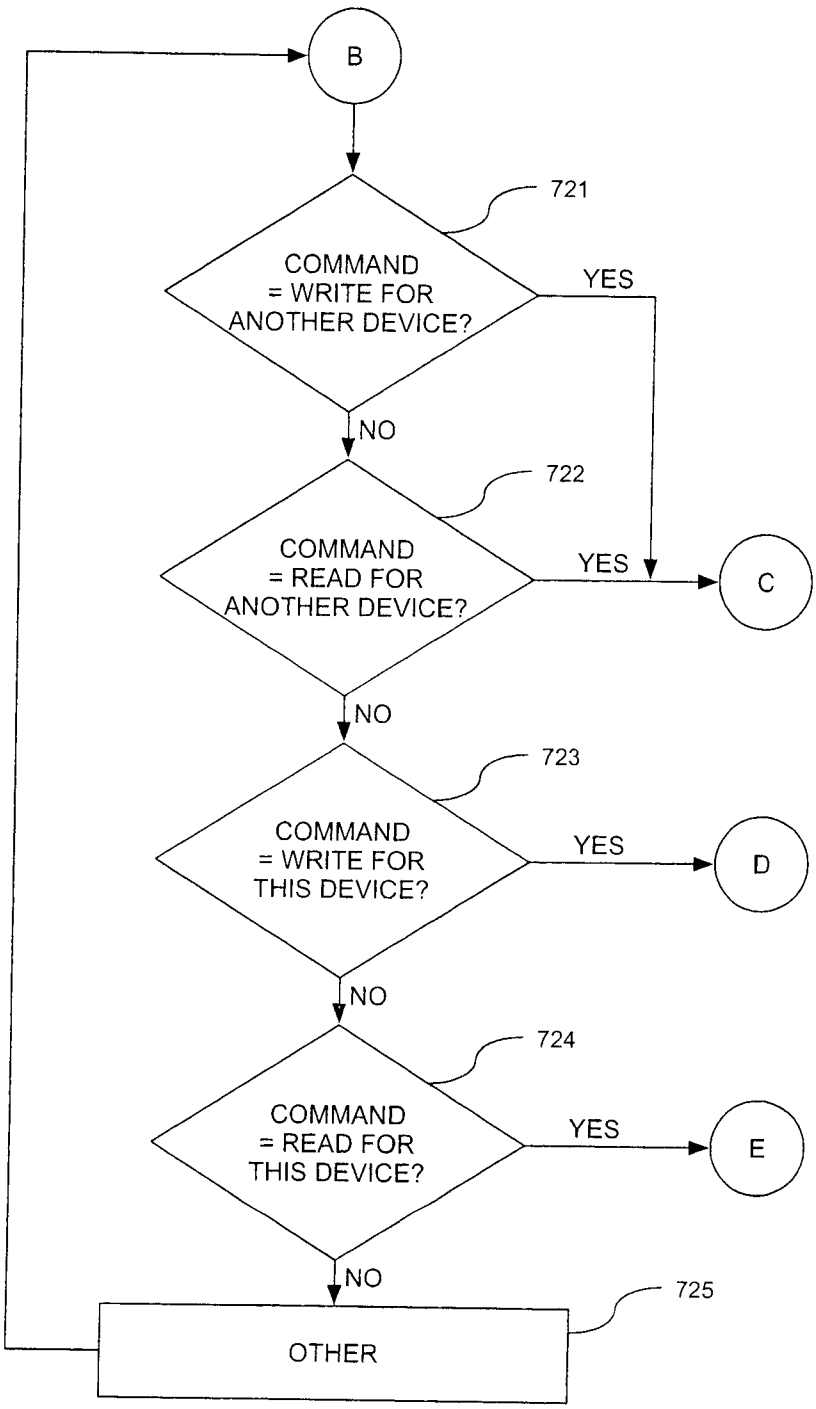

B
721
COMMAND
= WRITE FOR
ANOTHER DEVICE?
YES
NO
722
COMMAND
= READ FOR
ANOTHER DEVICE?
YES
C
NO
723
COMMAND
= WRITE FOR
THIS DEVICE?
YES
D
NO
724
COMMAND
= READ FOR
THIS DEVICE?
YES
E
NO
725
OTHER

FIG. 7C

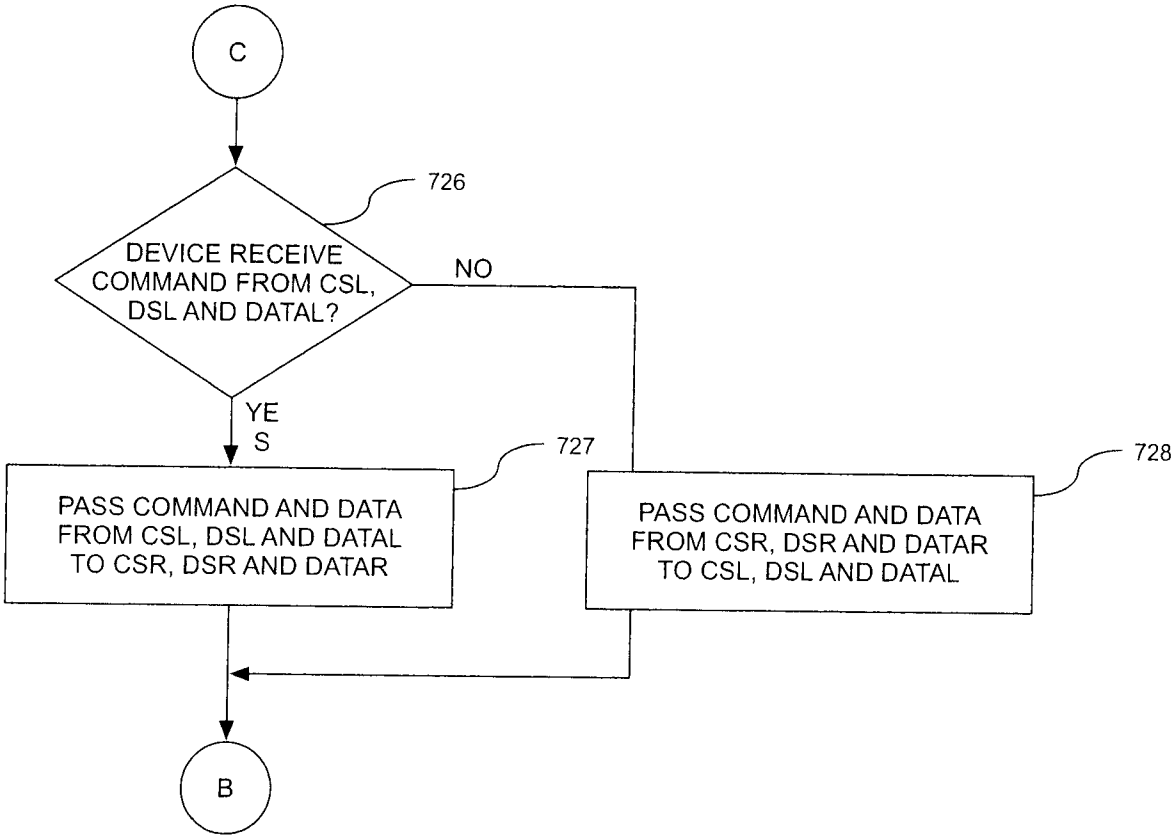

C
726
DEVICE RECEIVE COMMAND FROM CSL, DSL AND DATAL?
NO
YE
S
727
PASS COMMAND AND DATA FROM CSL, DSL AND DATAL TO CSR, DSR AND DATAR
728
PASS COMMAND AND DATA FROM CSR, DSR AND DATAR TO CSL, DSL AND DATAL
B

FIG. 7D

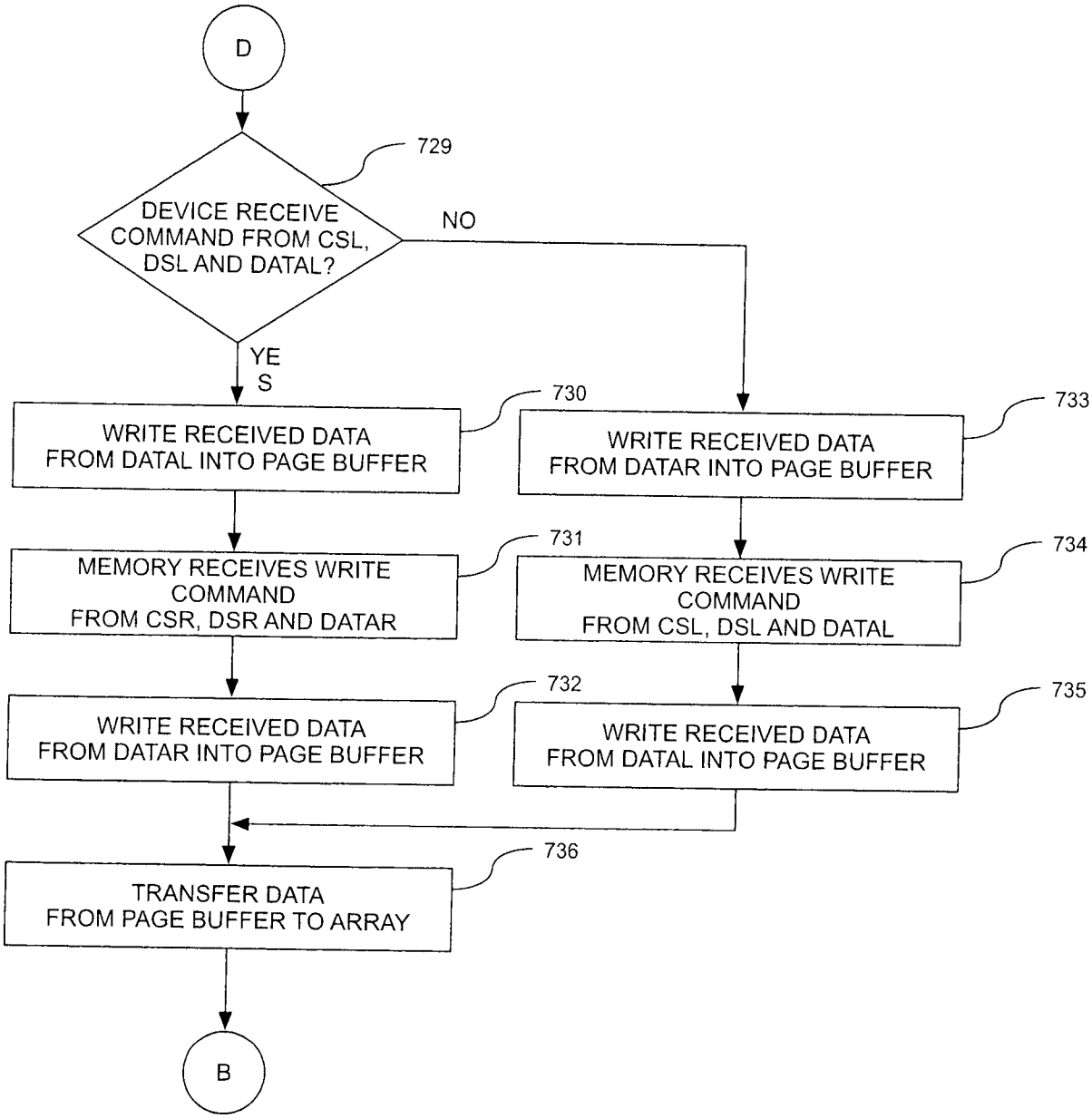

D
729
DEVICE RECEIVE COMMAND FROM CSL, DSL AND DATAL?
NO
YE
S
730
WRITE RECEIVED DATA FROM DATAL INTO PAGE BUFFER
733
WRITE RECEIVED DATA FROM DATAR INTO PAGE BUFFER
731
MEMORY RECEIVES WRITE COMMAND FROM CSR, DSR AND DATAR
734
MEMORY RECEIVES WRITE COMMAND FROM CSL, DSL AND DATAL
732
WRITE RECEIVED DATA FROM DATAR INTO PAGE BUFFER
735
WRITE RECEIVED DATA FROM DATAL INTO PAGE BUFFER
736
TRANSFER DATA FROM PAGE BUFFER TO ARRAY
B

FIG. 7E

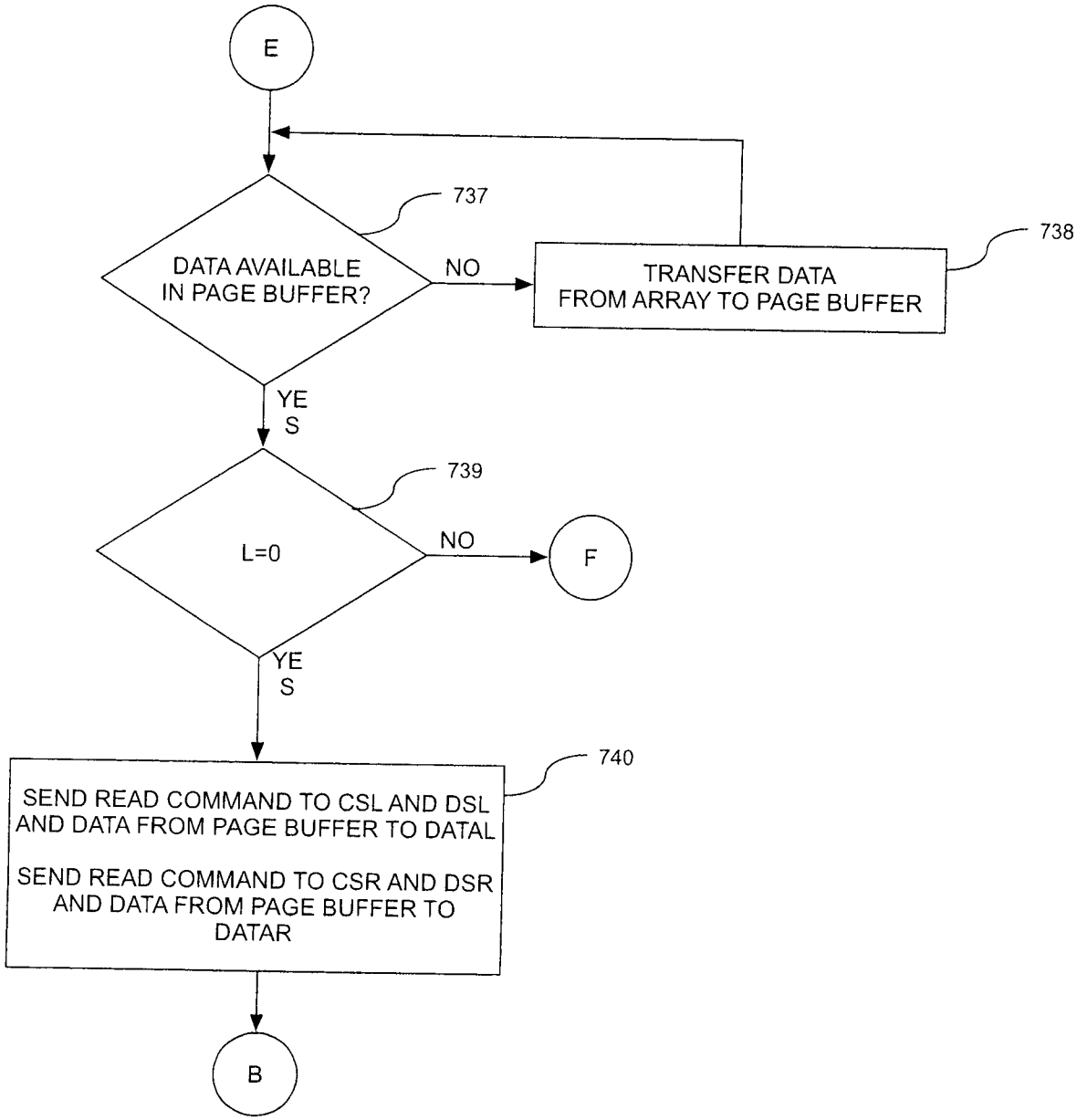

E
737
DATA AVAILABLE IN PAGE BUFFER?
NO
738
TRANSFER DATA FROM ARRAY TO PAGE BUFFER
YES
739
L=0
NO
F
YES
740
SEND READ COMMAND TO CSL AND DSL AND DATA FROM PAGE BUFFER TO DATAL
SEND READ COMMAND TO CSR AND DSR AND DATA FROM PAGE BUFFER TO DATAR
B

FIG. 7F

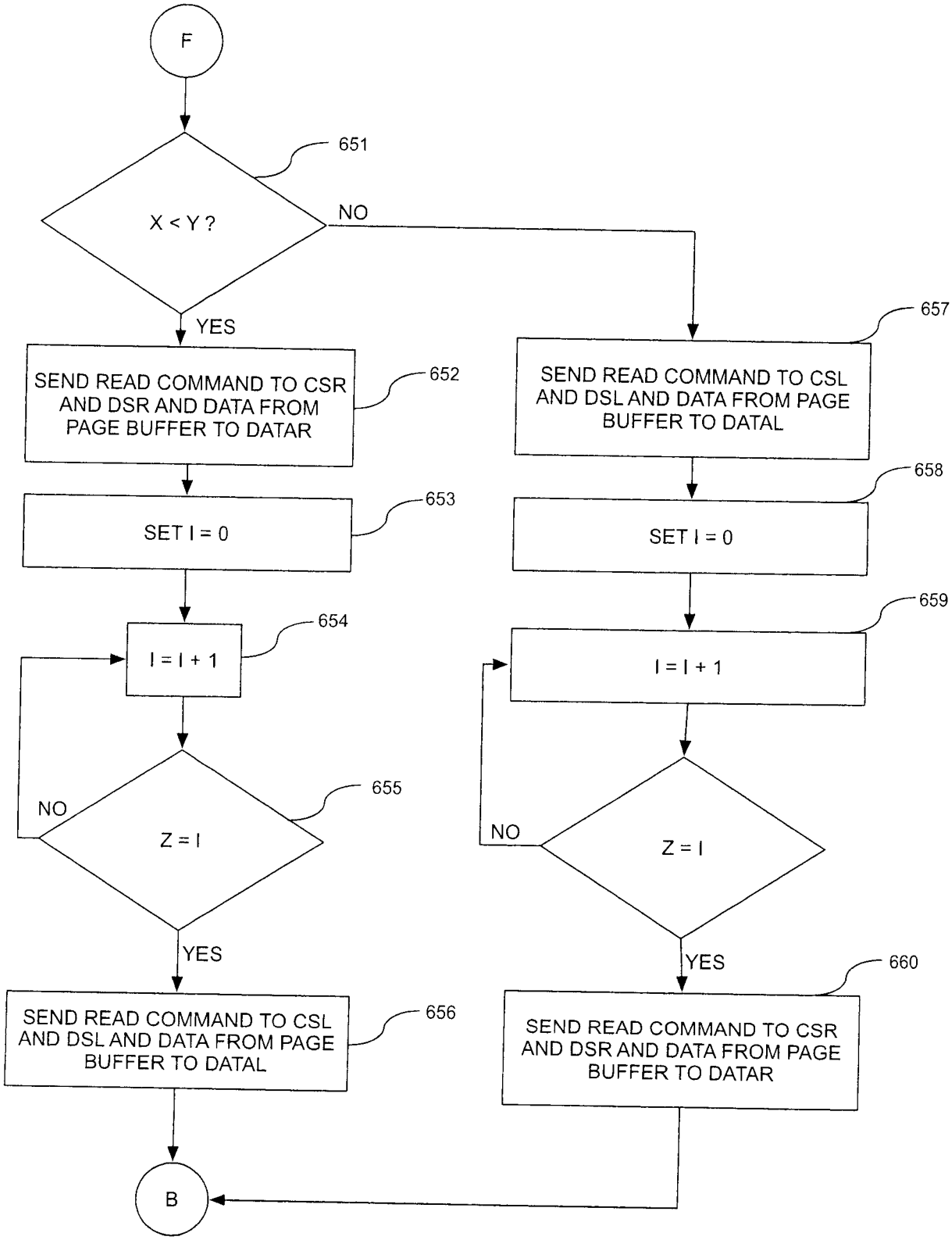

F
651
X < Y ?
NO
YES
SEND READ COMMAND TO CSR AND DSR AND DATA FROM PAGE BUFFER TO DATAR
652
SET I = 0
653
I = I + 1
654
Z = I
655
NO
YES
SEND READ COMMAND TO CSL AND DSL AND DATA FROM PAGE BUFFER TO DATAL
656
B
657
SEND READ COMMAND TO CSL AND DSL AND DATA FROM PAGE BUFFER TO DATAL
658
SET I = 0
659
I = I + 1
Z = I
NO
YES
660
SEND READ COMMAND TO CSR AND DSR AND DATA FROM PAGE BUFFER TO DATAR

FIG.7G

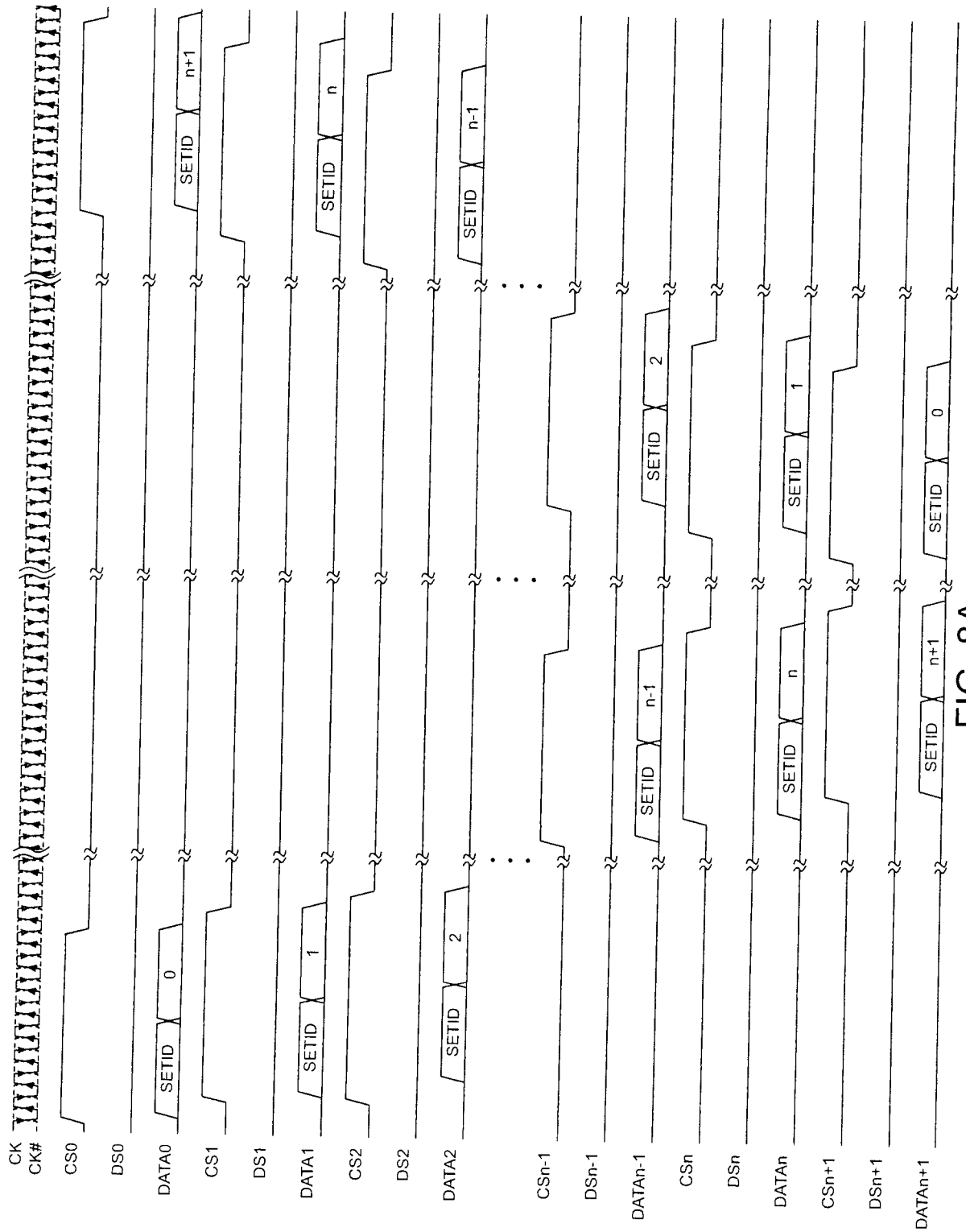

CK
CK#
CS0
DS0
DATA0
SETID
0
CS1
DS1
DATA1
SETID
1
CS2
DS2
DATA2
SETID
2
CSn-1
DSn-1
DATAn-1
SETID
n-1
CSn
DSn
DATAn
SETID
n
CSn+1
DSn+1
DATAn+1
SETID
n+1
SETID
n
SETID
n-1
SETID
2
SETID
1
SETID
0

FIG. 8A

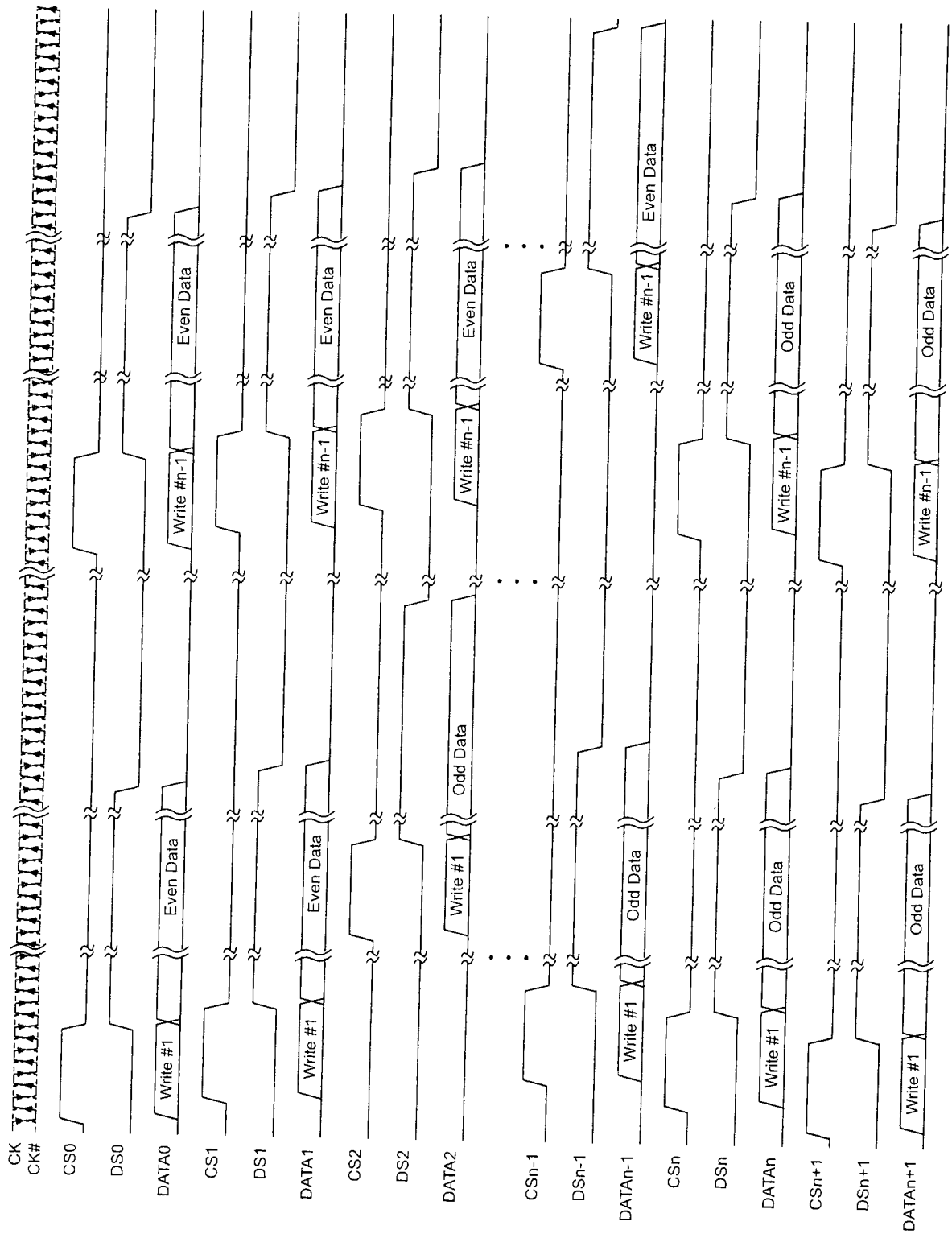

CK
CK#
CS0
DS0
DATA0
Write #1
Even Data
Write #n-1
Even Data
CS1
DS1
DATA1
Write #1
Even Data
Write #n-1
Even Data
CS2
DS2
DATA2
Write #1
Odd Data
Write #n-1
Even Data
CSn-1
DSn-1
DATAn-1
Write #1
Odd Data
Write #n-1
Even Data
CSn
DSn
DATAn
Write #1
Odd Data
Write #n-1
Odd Data
CSn+1
DSn+1
DATAn+1
Write #1
Odd Data
Write #n-1
Odd Data

FIG. 8B

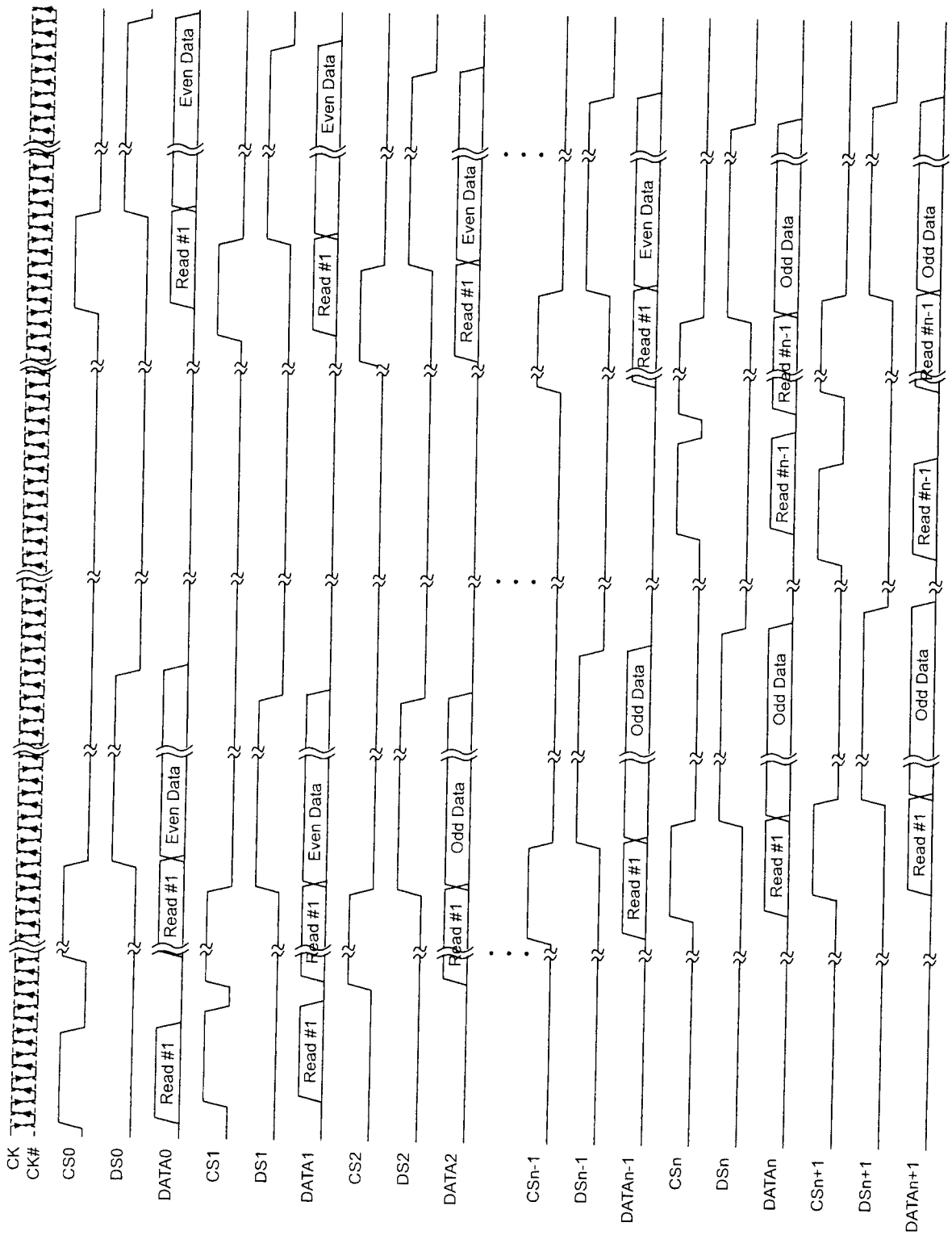

CK
CK#
CS0
DS0
DATA0
Read #1
Even Data
CS1
DS1
DATA1
Read #1
Even Data
CS2
DS2
DATA2
Read #1
Odd Data
Read #1
Even Data
CSn-1
DSn-1
DATAn-1
Read #1
Odd Data
Read #1
Even Data
CSn
DSn
DATAn
Read #1
Odd Data
Read #n-1
Odd Data
CSn+1
DSn+1
DATAn+1
Read #1
Odd Data
Read #n-1
Odd Data

FIG. 8C

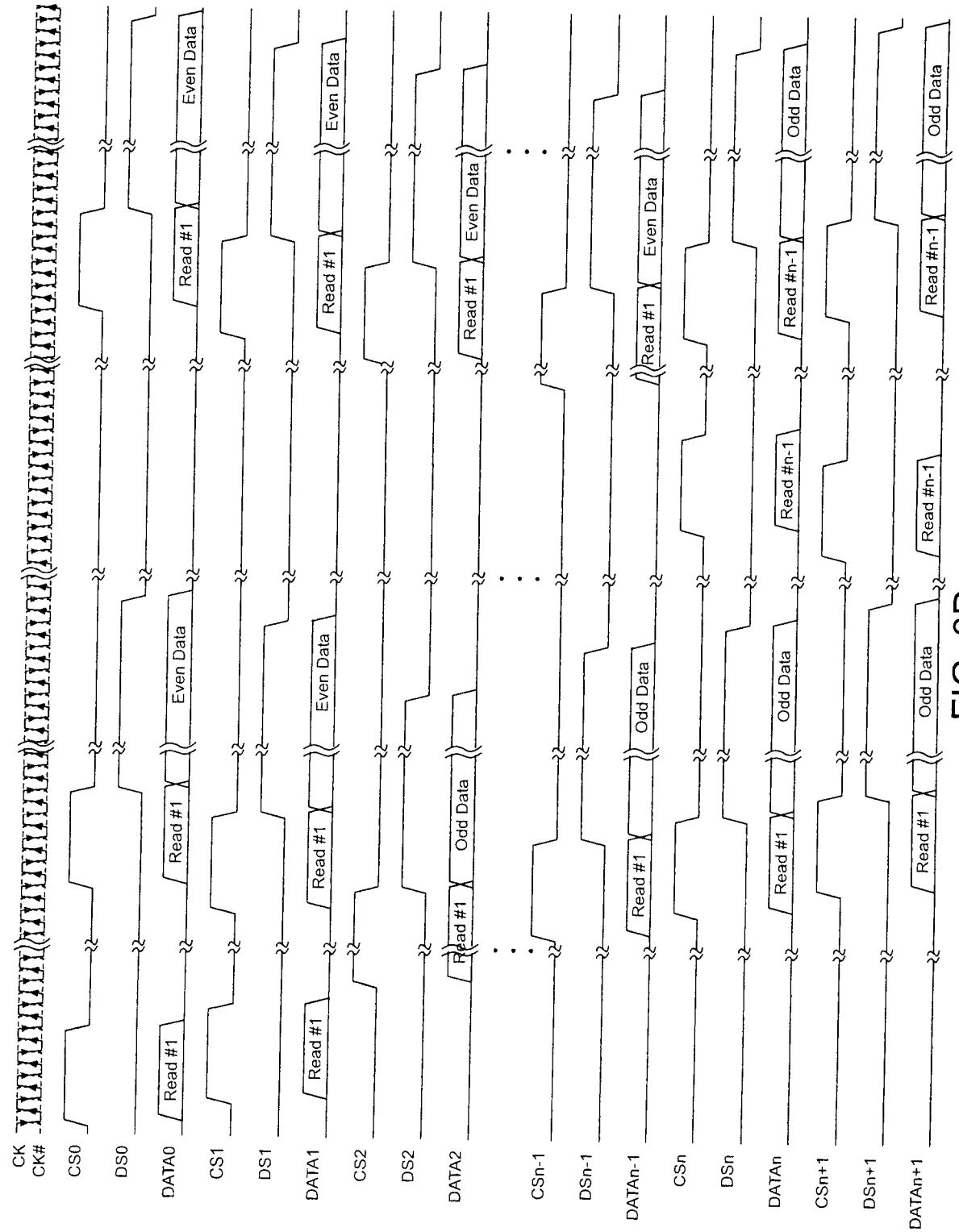

CK
CK#
CS0
DS0
DATA0
CS1
DS1
DATA1
CS2
DS2
DATA2
CSn-1
DSn-1
DATAn-1
CSn
DSn
DATAn
CSn+1
DSn+1
DATAn+1
Read #1
Even Data
Odd Data
Read #n-1

FIG. 8D

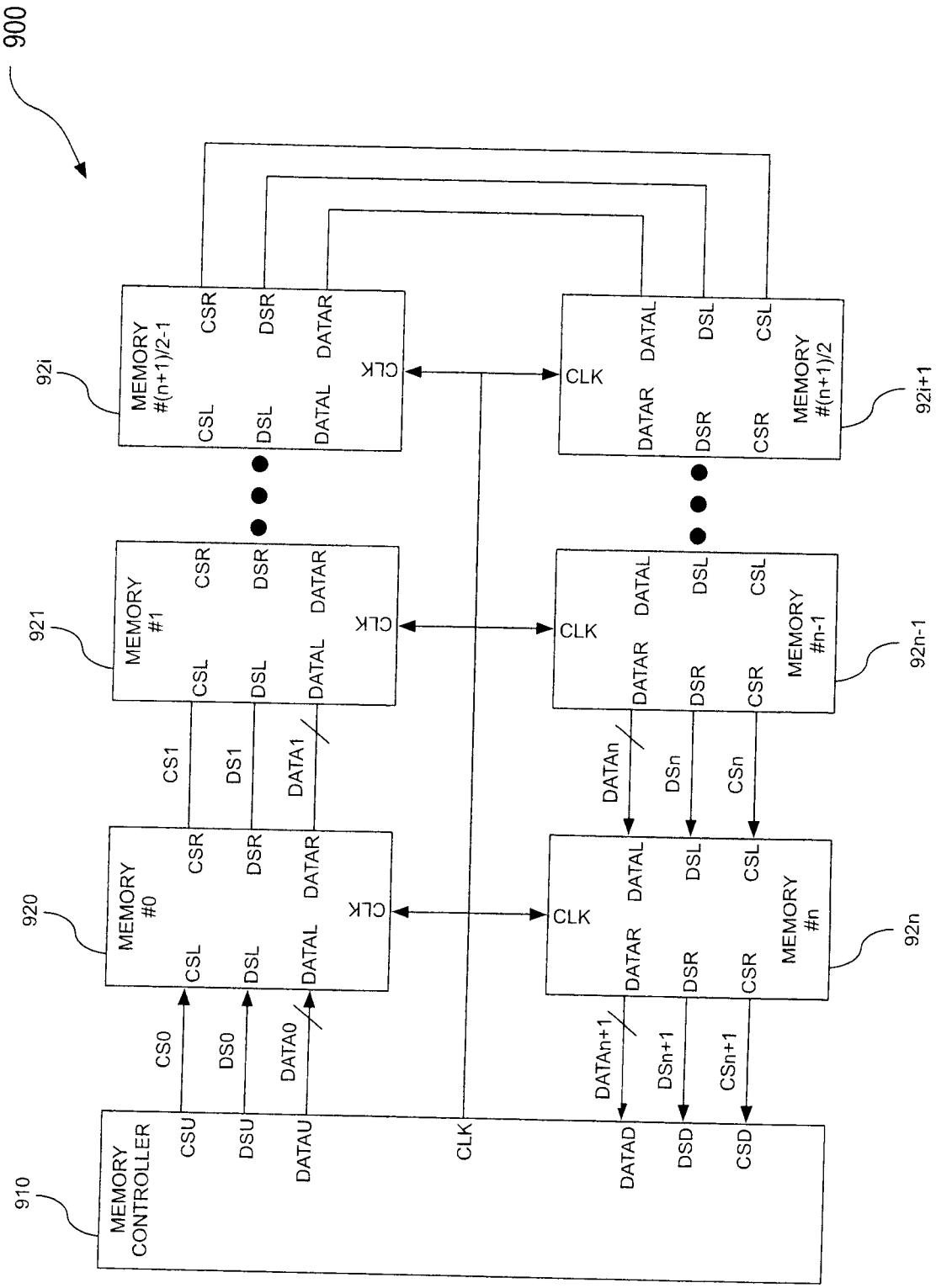

900
MEMORY CONTROLLER
910
CSU
DSU
DATAU
CLK
CS0
DS0
DATA0
MEMORY #0
920
CSL
DSL
DATAL
CSR
DSR
DATAR
CLK
CS1
DS1
DATA1
MEMORY #1
921
MEMORY #(n+1)/2-1
92i
MEMORY #(n+1)/2
92i+1
MEMORY #n-1
92n-1
MEMORY #n
92n
DATAn
DSn
CSn
DATAn+1
DSn+1
CSn+1
DATAD
DSD
CSD

FIG. 9A

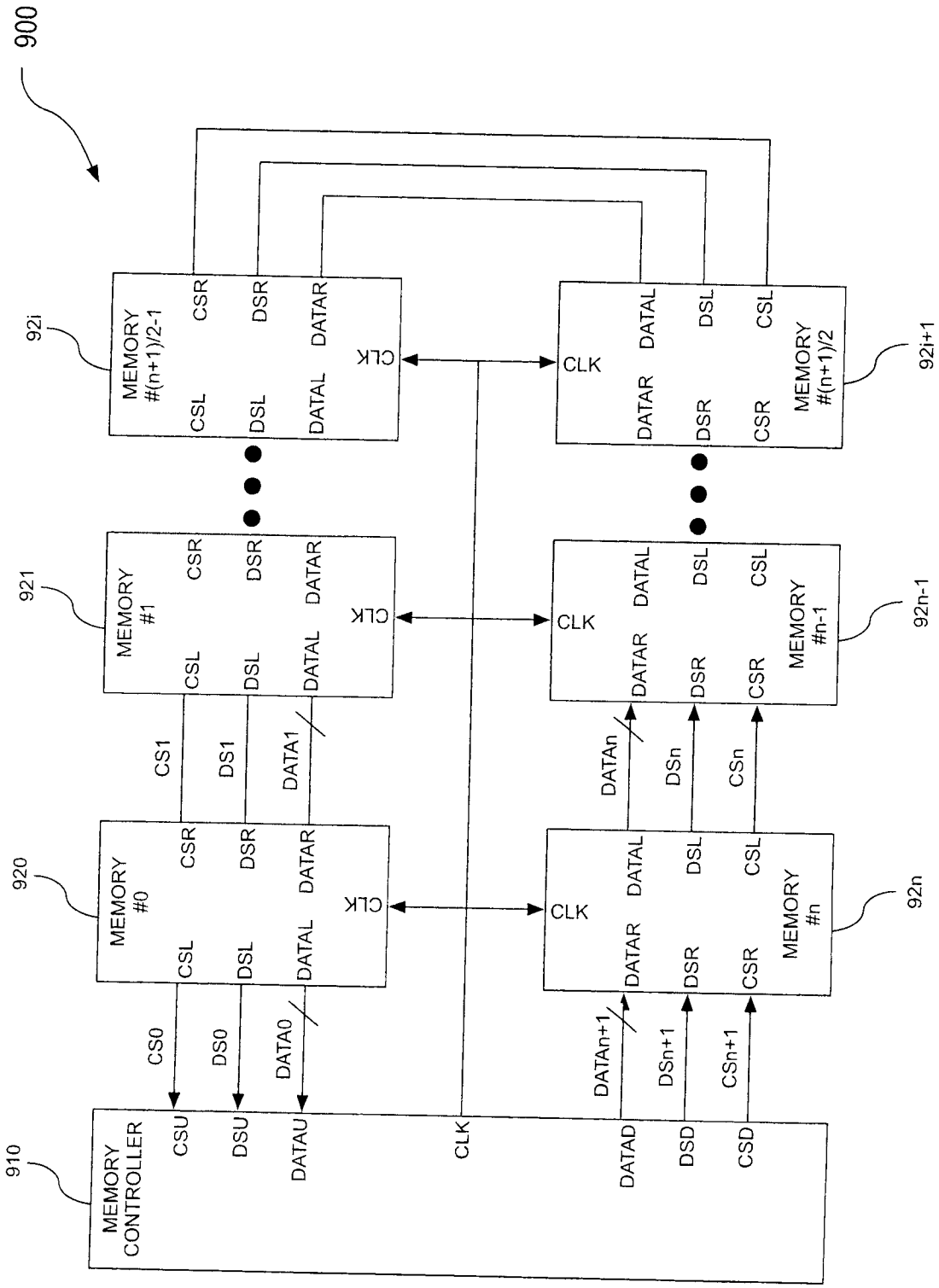

900
92i
MEMORY #(n+1)/2-1
CSR
DSR
DATAR
CLK
CSL
DSL
DATAL
CLK
DATAL
DSL
CSL
DATAR
DSR
CSR
MEMORY #(n+1)/2
92i+1
921
MEMORY #1
CS1
DS1
DATA1
DATAn
DSn
CSn
MEMORY #n-1
92n-1
920
MEMORY #0
CS0
DS0
DATA0
DATAn+1
DSn+1
CSn+1
MEMORY #n
92n
910
MEMORY CONTROLLER
CSU
DSU
DATAU
CLK
DATAD
DSD
CSD

FIG. 9B

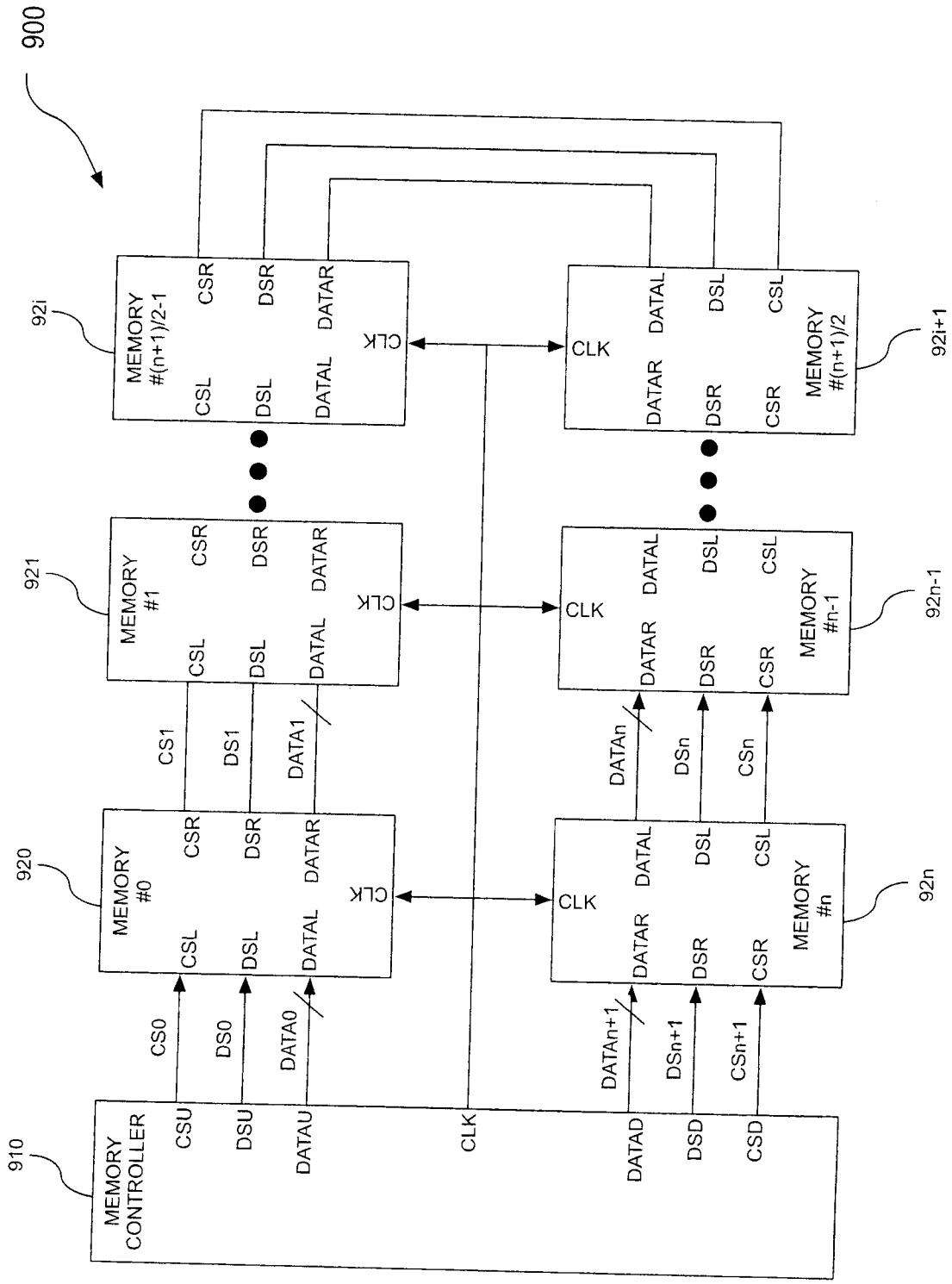

900
MEMORY CONTROLLER
910
CSU
DSU
DATAU
CLK
CS0
DS0
DATA0
CS1
DS1
DATA1
DATAn
DSn
CSn
DATAn+1
DSn+1
CSn+1
DATAD
DSD
CSD
MEMORY #0
920
MEMORY #1
921
MEMORY #n
92n
MEMORY #n-1
92n-1
MEMORY #(n+1)/2
92i+1
MEMORY #(n+1)/2-1
92i
CSL
DSL
DATAL
CSR
DSR
DATAR
CLK

FIG. 9C

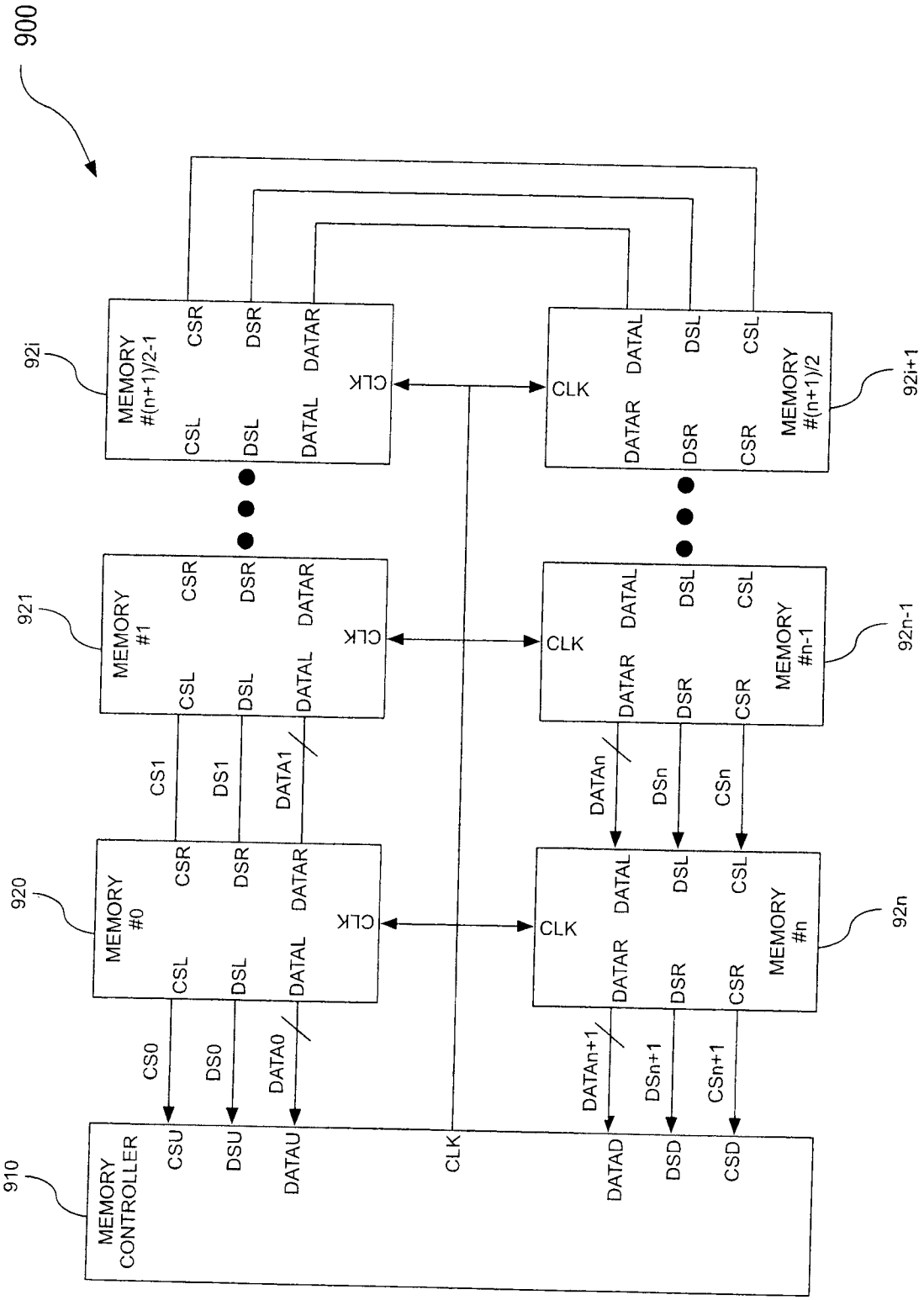

900
92i
MEMORY #(n+1)/2-1
CSR
DSR
DATAR
CLK
CSL
DSL
DATAL
92i+1
MEMORY #(n+1)/2
921
MEMORY #1
92n-1
MEMORY #n-1
920
MEMORY #0
92n
MEMORY #n
CS1
DS1
DATA1
DATAn
DSn
CSn
CS0
DS0
DATA0
DATAn+1
DSn+1
CSn+1
910
MEMORY CONTROLLER
CSU
DSU
DATAU
CLK
DATAD
DSD
CSD

FIG. 9D

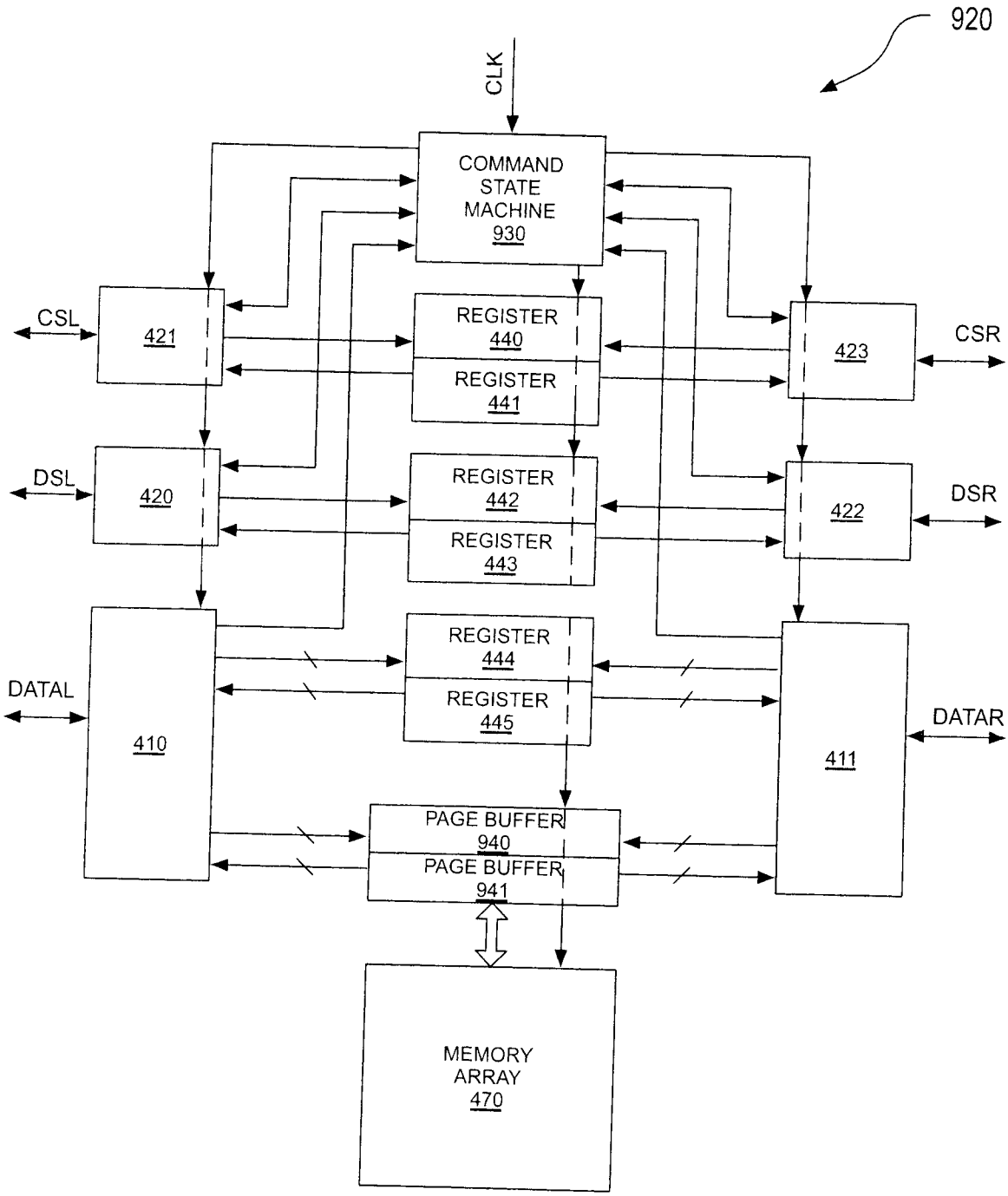

920
CLK
COMMAND STATE MACHINE 930
CSL
421
REGISTER 440
REGISTER 441
423
CSR
DSL
420
REGISTER 442
REGISTER 443
422
DSR
DATAL
410
REGISTER 444
REGISTER 445
411
DATAR
PAGE BUFFER 940
PAGE BUFFER 941
MEMORY ARRAY 470

FIG. 9E

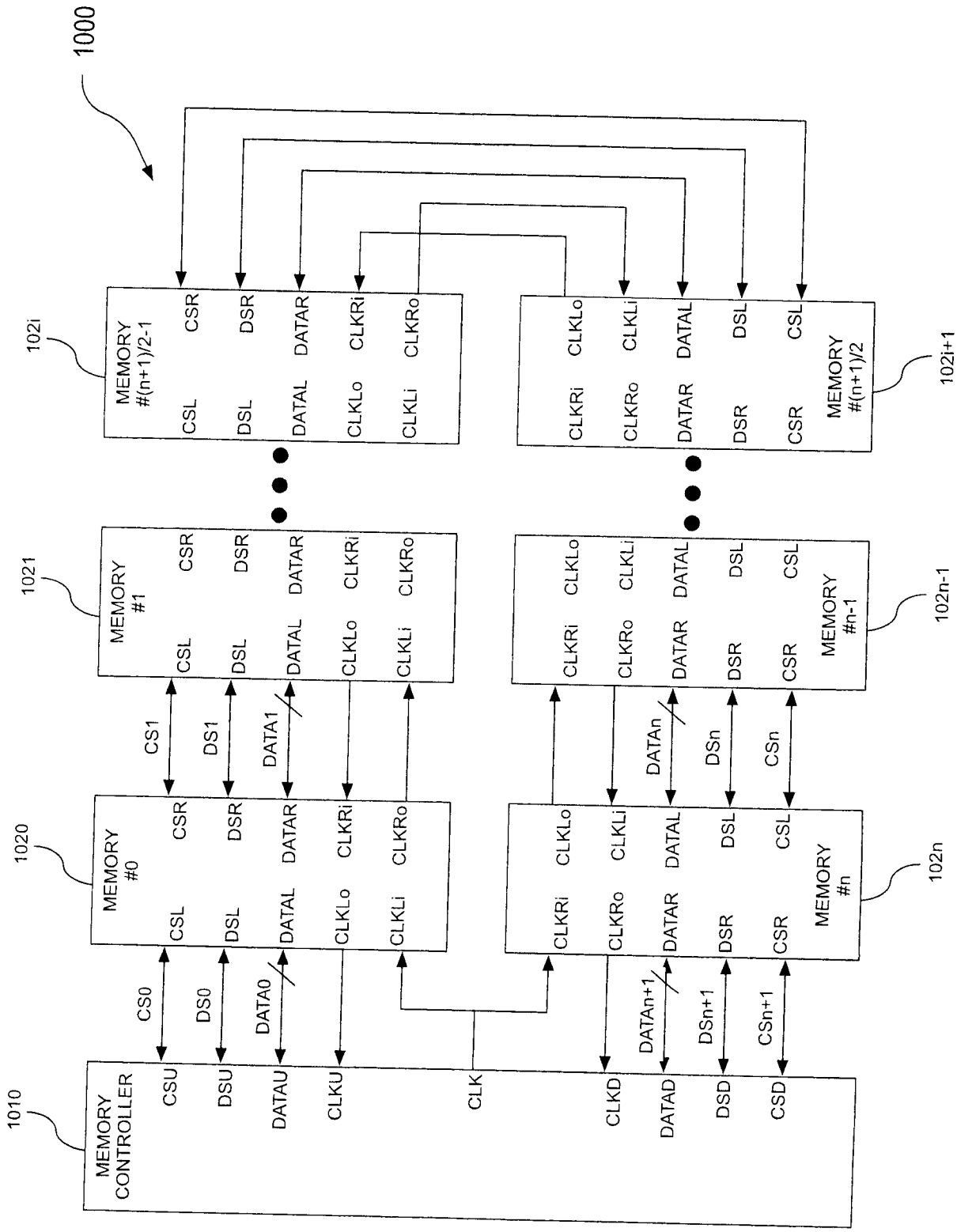

1000
1010
MEMORY CONTROLLER
CSU
DSU
DATAU
CLKU
CLK
CLKD
DATAD
DSD
CSD
CS0
DS0
DATA0
CS1
DS1
DATA1
DATAn
DSn
CSn
DATAn+1
DSn+1
CSn+1
1020
MEMORY #0
1021
MEMORY #1
102i
MEMORY #(n+1)/2-1
102i+1
MEMORY #(n+1)/2
102n-1
MEMORY #n-1
102n
MEMORY #n
CSL
DSL
DATAL
CLKLo
CLKLi
CSR
DSR
DATAR
CLKRi
CLKRo

FIG. 10A

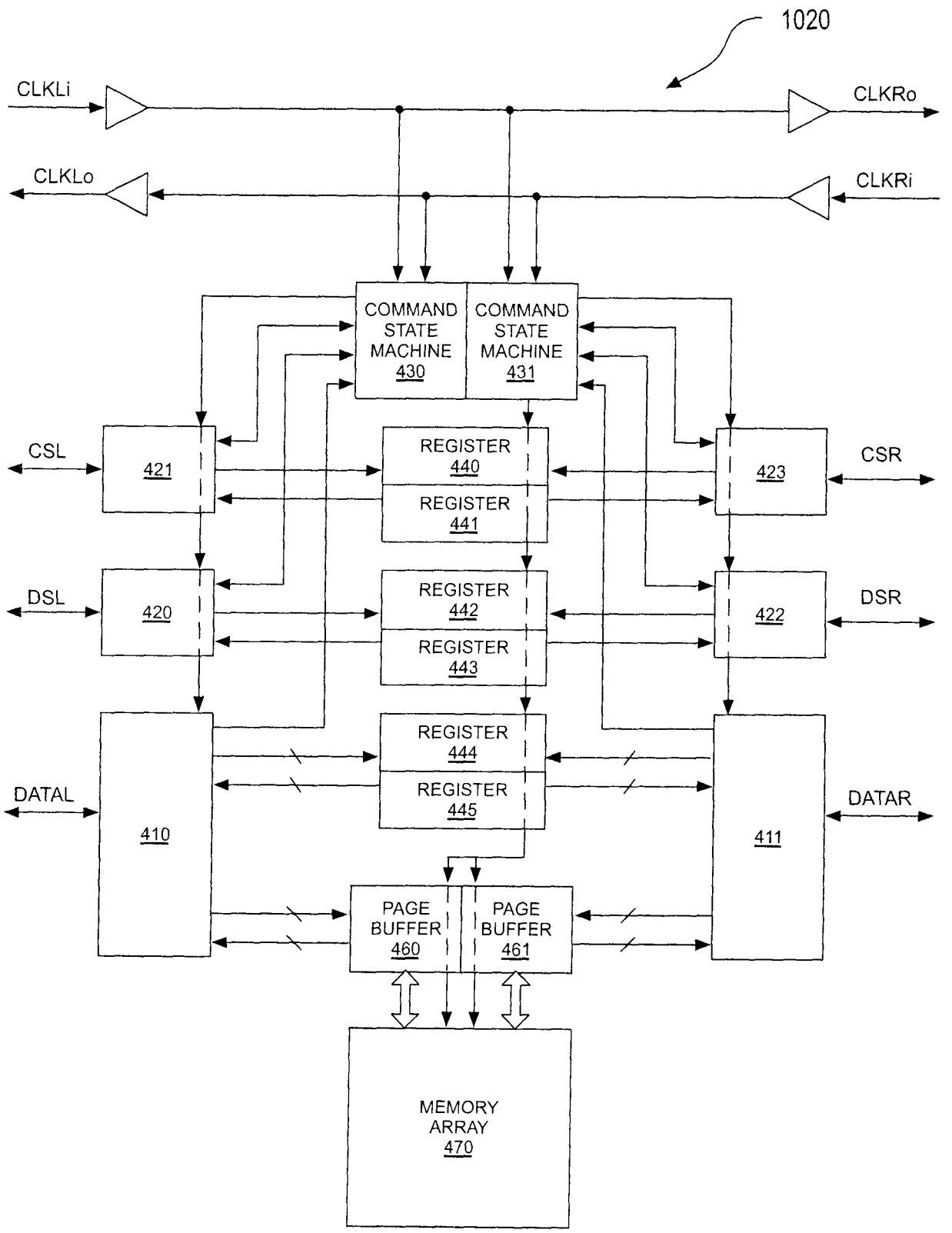

1020
CLKLi
CLKRo
CLKLo
CLKRi
COMMAND STATE MACHINE 430
COMMAND STATE MACHINE 431
CSL
421
REGISTER 440
REGISTER 441
423
CSR
DSL
420
REGISTER 442
REGISTER 443
422
DSR
REGISTER 444
REGISTER 445
DATAL
410
411
DATAR
PAGE BUFFER 460
PAGE BUFFER 461
MEMORY ARRAY 470

FIG. 10B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2011/000614

A. CLASSIFICATION OF SUBJECT MATTER
IPC: ***G06F 12/02*** (2006.01) , ***G06F 9/44*** (2006.01)
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC: ALL (2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)
Databases: Canadian Patent Database, TotalPatent, Google, IEEEXplore; Keywords: read, access, half, split, portion, partial, memory, chain, daisy, circular, loop, dual, port, simultaneously, concurrent, duplex, bidirection

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2006/0095592 A1 (Borkenhagen), 04 May 2006 (04-05-2006) ([0029], [0037], [0050], [0055]-[0064]; claims 31 and 35; Fig. 7)	1-3, 5, 8-19 20
Y	WO 2007/036050 A1 (OH et al.), 05 April 2007 (05-04-2007) ([0087]; Fig. 13B)	20

[ ] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 September 2011 (06-09-2011)	8 September 2011 (08-09-2011)

Name and mailing address of the ISA/CA	Authorized officer
Canadian Intellectual Property Office Place du Portage I, C114 - 1st Floor, Box PCT 50 Victoria Street Gatineau, Quebec K1A 0C9 Facsimile No.: 001-819-953-2476	Simon Chau (819) 994-7514

Patent Document Cited in Search Report	Publication Date	Patent Family Member(s)	Publication Date
US2006095592A1	04 May 2006 (04-05-2006)	US2006095592A1	04 May 2006 (04-05-2006)
		US7334070B2	19 February 2008 (19-02-2008)
WO2007036050A1	05 April 2007 (05-04-2007)	AU2005322870A1	13 July 2006 (13-07-2006)
		AU2005325674A1	03 August 2006 (03-08-2006)
		CA2583178A1	12 January 2006 (12-01-2006)
		CA2584288A1	12 January 2006 (12-01-2006)
		CA2591905A1	13 July 2006 (13-07-2006)
		CA2594983A1	03 August 2006 (03-08-2006)
		CA2623747A1	05 April 2007 (05-04-2007)
		CA2627663A1	05 April 2007 (05-04-2007)
		CA2644593A1	04 October 2007 (04-10-2007)
		CA2651434A1	29 November 2007 (29-11-2007)
		CN101133623A	27 February 2008 (27-02-2008)
		CN101147379A	19 March 2008 (19-03-2008)
		CN101147379B	25 May 2011 (25-05-2011)
		CN101164057A	16 April 2008 (16-04-2008)
		CN101278352A	01 October 2008 (01-10-2008)
		CN101278354A	01 October 2008 (01-10-2008)
		CN101410814A	15 April 2009 (15-04-2009)
		CN101416171A	22 April 2009 (22-04-2009)
		CN101449251A	03 June 2009 (03-06-2009)
		CN101449251B	11 May 2011 (11-05-2011)
		CN101611453A	23 December 2009 (23-12-2009)
		CN102104632A	22 June 2011 (22-06-2011)
		CN102123178A	13 July 2011 (13-07-2011)
		EP1774438A2	18 April 2007 (18-04-2007)
		EP1774439A2	18 April 2007 (18-04-2007)
		EP1832088A2	12 September 2007 (12-09-2007)
		EP1842354A2	10 October 2007 (10-10-2007)
		EP1929480A1	11 June 2008 (11-06-2008)
		EP1929480A4	15 October 2008 (15-10-2008)
		EP1932157A1	18 June 2008 (18-06-2008)
		EP1932157A4	15 October 2008 (15-10-2008)
		EP1932158A1	18 June 2008 (18-06-2008)
		EP1932158A4	15 October 2008 (15-10-2008)
		EP1981030A1	15 October 2008 (15-10-2008)
		EP1981031A1	15 October 2008 (15-10-2008)
		EP1981032A1	15 October 2008 (15-10-2008)
		EP1999601A1	10 December 2008 (10-12-2008)
		EP1999601A4	08 April 2009 (08-04-2009)
		EP2021930A1	11 February 2009 (11-02-2009)
		EP2021930A4	20 April 2011 (20-04-2011)
		EP2031516A2	04 March 2009 (04-03-2009)
		EP2031516A3	15 July 2009 (15-07-2009)
		EP2126918A1	02 December 2009 (02-12-2009)
		EP2126918A4	27 January 2010 (27-01-2010)
		EP2306460A2	06 April 2011 (06-04-2011)
		EP2306460A3	27 July 2011 (27-07-2011)
		EP2306461A2	06 April 2011 (06-04-2011)
		EP2306461A3	27 July 2011 (27-07-2011)
		EP2348510A1	27 July 2011 (27-07-2011)
		IL184308D0	31 October 2007 (31-10-2007)
		IL184750D0	03 December 2007 (03-12-2007)
		JP2008505545A	21 February 2008 (21-02-2008)
		JP2008505568A	21 February 2008 (21-02-2008)
		JP2008527507A	24 July 2008 (24-07-2008)
		JP2008529127A	31 July 2008 (31-07-2008)
		JP2009301586A	24 December 2009 (24-12-2009)
		JP2009510568A	12 March 2009 (12-03-2009)
		JP2009510656A	12 March 2009 (12-03-2009)
		JP2009510657A	12 March 2009 (12-03-2009)
		JP2009531746A	03 September 2009 (03-09-2009)
		JP2009538065A	29 October 2009 (29-10-2009)

JP2010514018A	30 April 2010 (30-04-2010)
KR20070074465A	12 July 2007 (12-07-2007)
KR20070083396A	24 August 2007 (24-08-2007)
KR20070092720A	13 September 2007 (13-09-2007)
KR20070104566A	26 October 2007 (26-10-2007)
KR20080056276A	20 June 2008 (20-06-2008)
KR20080057330A	24 June 2008 (24-06-2008)
KR20080068835A	24 July 2008 (24-07-2008)
KR20090007280A	16 January 2009 (16-01-2009)
KR20090031516A	26 March 2009 (26-03-2009)
KR20090097199A	15 September 2009 (15-09-2009)
US2007153576A1	05 July 2007 (05-07-2007)
US7515471B2	07 April 2009 (07-04-2009)
US2007076479A1	05 April 2007 (05-04-2007)
US7652922B2	26 January 2010 (26-01-2010)
US2008279003A1	13 November 2008 (13-11-2008)
US7719892B2	18 May 2010 (18-05-2010)
US2007143677A1	21 June 2007 (21-06-2007)
US7747833B2	29 June 2010 (29-06-2010)
US2006005240A1	05 January 2006 (05-01-2006)
US7757074B2	13 July 2010 (13-07-2010)
US2006195840A1	31 August 2006 (31-08-2006)
US7810089B2	05 October 2010 (05-10-2010)
US2009073768A1	19 March 2009 (19-03-2009)
US7826294B2	02 November 2010 (02-11-2010)
US2006195660A1	31 August 2006 (31-08-2006)
US7849269B2	07 December 2010 (07-12-2010)
US2010281217A1	04 November 2010 (04-11-2010)
US7849270B2	07 December 2010 (07-12-2010)
US2010199057A1	05 August 2010 (05-08-2010)
US7945755B2	17 May 2011 (17-05-2011)
US2010182838A1	22 July 2010 (22-07-2010)
US8000144B2	16 August 2011 (16-08-2011)
US2006015570A1	19 January 2006 (19-01-2006)
US2006195547A1	31 August 2006 (31-08-2006)
US2006195605A1	31 August 2006 (31-08-2006)
US2006200849A1	07 September 2006 (07-09-2006)
US2006248581A1	02 November 2006 (02-11-2006)
US2006253605A1	09 November 2006 (09-11-2006)
US2007076502A1	05 April 2007 (05-04-2007)
US2007109833A1	17 May 2007 (17-05-2007)
US2007165457A1	19 July 2007 (19-07-2007)
US2007233903A1	04 October 2007 (04-10-2007)
US2007233917A1	04 October 2007 (04-10-2007)
US2007234071A1	04 October 2007 (04-10-2007)
US2008140938A1	12 June 2008 (12-06-2008)
US2008222363A1	11 September 2008 (11-09-2008)
US2010030951A1	04 February 2010 (04-02-2010)
US2010241846A1	23 September 2010 (23-09-2010)
US2010332594A1	30 December 2010 (30-12-2010)
US2011002171A1	06 January 2011 (06-01-2011)
US2011179245A1	21 July 2011 (21-07-2011)
WO2006004725A2	12 January 2006 (12-01-2006)
WO2006004725A3	04 June 2009 (04-06-2009)
WO2006005078A2	12 January 2006 (12-01-2006)
WO2006005078A3	21 June 2007 (21-06-2007)
WO2006074072A2	13 July 2006 (13-07-2006)
WO2006074072A3	07 December 2006 (07-12-2006)
WO2006081032A2	03 August 2006 (03-08-2006)
WO2006081032A3	12 October 2006 (12-10-2006)
WO2007036047A1	05 April 2007 (05-04-2007)
WO2007036047B1	24 May 2007 (24-05-2007)
WO2007036048A1	05 April 2007 (05-04-2007)
WO2007036048B1	07 June 2007 (07-06-2007)
WO2007036050B1	24 May 2007 (24-05-2007)
WO2007109886A1	04 October 2007 (04-10-2007)
WO2007109887A1	04 October 2007 (04-10-2007)
WO2007109888A1	04 October 2007 (04-10-2007)
WO2007134444A1	29 November 2007 (29-11-2007)
WO2008077244A1	03 July 2008 (03-07-2008)