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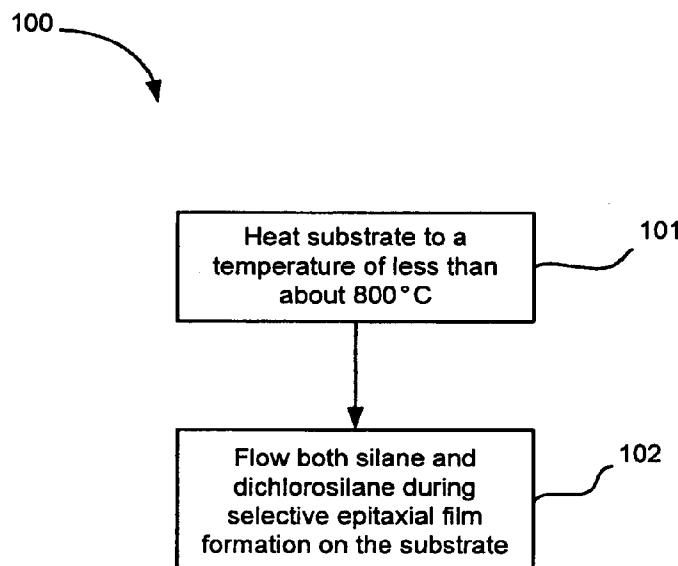
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(54) Title: METHODS OF CONTROLLING MORPHOLOGY DURING EPITAXIAL LAYER FORMATION



(57) Abstract: A first aspect of the invention provides a method of selectively forming an epitaxial layer on a substrate. The method includes heating the substrate to a temperature of less than about 800°C and employing both silane and dichlorosilane as silicon sources during epitaxial film formation. Numerous other aspects are provided.

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**METHODS OF CONTROLLING
MORPHOLOGY DURING EPITAXIAL LAYER FORMATION**

5 The present application claims priority from U.S. Provisional Patent Application Serial No. 60/820,956, filed July 31, 2006, which is hereby incorporated by reference herein in its entirety.

10 **CROSS REFERENCE TO RELATED APPLICATIONS**

 The present application is related to the following co-pending applications, each of which is hereby incorporated by reference herein in its entirety:

15 U.S. Patent Application Serial No. 11/001,774, filed December 1, 2004 (Docket No. 9618); and

 U.S. Patent Application Serial No. 11/227,974, filed September 14, 2005 (Docket No. 9618/P01).

20 **FIELD OF THE INVENTION**

 The present invention relates to semiconductor device manufacturing, and more particularly to methods of controlling morphology during epitaxial layer formation.

25 **BACKGROUND**

 As smaller transistors are manufactured, ultra shallow source/drain junctions are becoming more challenging to produce. Generally, sub-100 nm CMOS (complementary metal-oxide semiconductor) devices require a junction depth to be less than 30 nm. Selective epitaxial deposition is often utilized to form epitayers of silicon-containing materials (e.g., Si, SiGe and SiC) into the junctions. Generally, selective epitaxial deposition permits growth of epitayers on silicon moats with no growth on dielectric areas. Selective epitaxy can be used within semiconductor devices, such as elevated source/drains, source/drain

extensions, contact plugs or base layer deposition of bipolar devices.

Generally, a selective epitaxy process involves a deposition reaction and an etch reaction. The deposition and etch reactions occur simultaneously with relatively different reaction rates to an epitaxial layer and to a polycrystalline layer. During the deposition process, the epitaxial layer is formed on a monocrystalline surface while a polycrystalline layer is deposited on at least a second layer, such as an existing polycrystalline layer and/or an amorphous layer. However, the deposited polycrystalline layer is generally etched at a faster rate than the epitaxial layer. Therefore, by changing the concentration of an etchant gas, the net selective process results in deposition of epitaxy material and limited, or no, deposition of polycrystalline material. For example, a selective epitaxy process may result in the formation of an epilayer of silicon-containing material on a monocrystalline silicon surface while no deposition is left on a spacer region.

Selective epitaxy deposition of silicon-containing materials has become a useful technique during formation of elevated source/drain and source/drain extension features, for example, during the formation of silicon-containing MOSFET (metal oxide semiconductor field effect transistor) devices. Source/drain extension features are manufactured by etching a silicon surface to make a recessed source/drain feature and subsequently filling the etched surface with a selectively grown epilayer, such as a silicon germanium (SiGe) material. Selective epitaxy permits near complete dopant activation with *in-situ* doping, so that the post annealing process is omitted. Therefore, junction depth can be defined accurately by silicon etching and selective epitaxy. On the other hand, the ultra shallow source/drain

junction inevitably results in increased series resistance. Also, junction consumption during silicide formation increases the series resistance even further. In order to compensate for junction consumption, an elevated 5 source/drain is epitaxially and selectively grown on the junction. Typically, the elevated source/drain layer is undoped silicon.

However, current selective epitaxy processes have some drawbacks. In order to maintain selectivity during 10 present epitaxy processes, chemical concentrations of the precursors, as well as reaction temperatures must be regulated and adjusted throughout the deposition process. If not enough silicon precursor is administered, then the etching reaction may dominate and the overall process is 15 slowed down. Also, harmful over etching of substrate features may occur. If not enough etchant precursor is administered, then the deposition reaction may dominate reducing the selectivity to form monocrystalline and polycrystalline materials across the substrate surface. 20 Also, current selective epitaxy processes usually require a high reaction temperature, such as about 800°C, 1,000°C or higher. Such high temperatures are not desirable during a fabrication process due to thermal budget considerations and possible uncontrolled nitridation reactions to the substrate 25 surface.

Therefore, there is a need to have a process for selectively and epitaxially depositing silicon and silicon-containing compounds with optional dopants. Furthermore, the process should be versatile to form silicon-containing 30 compounds with varied elemental concentrations while having a fast deposition rate, smooth surface morphology and maintaining a process temperature, such as about 800°C or less, and preferably about 700°C or less.

SUMMARY OF INVENTION

A first aspect of the invention provides a method of selectively forming an epitaxial layer on a substrate.

5 The method includes heating the substrate to a temperature of less than about 800°C and employing both silane and dichlorosilane as silicon sources during selective epitaxial film formation.

In another aspect of the invention a method of 10 selectively forming an epitaxial layer on a substrate is provided. The method includes at least one deposition step and at least one etching step which are alternated. The method includes heating the substrate to a temperature of less than about 800°C. The deposition step employs both 15 silane and dichlorosilane as silicon sources. Each of the silicon source gases are flowed at a rate from about 10 to 100 sccm at a chamber pressure of about 5 to 50 Torr. The etching step includes flowing at least one of hydrogen chloride and chlorine.

20 In another aspect of the invention, a method of forming an epitaxial layer on a substrate is provided. The method includes (1) heating the substrate to a temperature of less than about 800°C; and (2) performing a selective epitaxial film formation process on the substrate so as to 25 form the epitaxial layer by employing both silane and dichlorosilane as silicon sources during the selective epitaxial film formation process. A ratio of silane to dichlorosilane is greater than 1. Numerous other aspects are provided.

30 Other features and aspects of the present invention will become more fully apparent from the following detailed description, the appended claims and the accompanying drawings.

DESCRIPTION OF DRAWINGS

FIG. 1 is a flowchart of a first exemplary method for forming an epitaxial film in accordance with the present invention.

5 FIG. 2 is a flowchart of a second exemplary method for forming an epitaxial film in accordance with the present invention.

DETAILED DESCRIPTION

10 During a selective epitaxial growth process on a silicon substrate patterned with dielectric films, formation of single-crystal semiconductor occurs only on the exposed silicon surfaces (e.g., not on the dielectric surfaces). Selective thickness is defined as the maximum film thickness 15 obtained on the silicon surfaces prior to the onset of film growth or nucleation on the dielectric surfaces.

20 Selective epitaxial growth processes may include simultaneous etch-deposition processes as well as alternating gas supply processes. In a simultaneous etch-deposition process, both etchant species and deposition species are flowed simultaneously. As such, an epitaxial layer is simultaneously deposited and etched during its formation.

25 U.S. Patent Application Serial No. 11/001,774, filed December 1, 2004 (Docket No. 9618), describes an alternating gas supply (AGS) process for forming epitaxial layers on a substrate. During an AGS process, an epitaxial deposition process is conducted on a substrate, and then an etching process is conducted on the substrate. The cycle of 30 an epitaxial deposition process followed by an etching process is repeated until a desired thickness of an epitaxial layer is formed.

35 An alternative precursor for selective silicon epitaxy at deposition temperatures less than 800°C is silane (SiH_4). At such lower temperatures, SiH_4 has a higher growth

rate than dichlorosilane (DCS). However, the present inventors have observed that an SiH₄-based process may introduce morphology issues (e.g., surface roughness or pitting).

5 In at least one embodiment of the invention, observed morphology issues associated with the use of SiH₄ may be reduced and/or eliminated by employing both SiH₄ and DCS (e.g., by mixing SiH₄ and DCS during film growth). This approach is believed to alter the diffusion mechanism on the
10 film's surface, allowing greater morphology control.

In some embodiments, the present invention may be employed with the AGS process described in U.S. Patent Application Serial No. 11/001,774, filed December 1, 2004 (Docket No. 9618), although the present invention may be
15 used with other selective epitaxial processes.

Silicon epitaxial films formed using a selective process with only SiH₄ as a silicon source (e.g., during an AGS process) were found to have surfaces that are rough and pitted. Silicon epitaxial films formed using a selective
20 process with both SiH₄ and DCS as silicon sources (e.g., during an AGS process) were found to have improved film morphology, such as improved surface smoothness (e.g., without pitting). Unlike other approaches such as a post-deposition smoothing step, the use of SiH₄ and DCS allows for
25 in-situ control of film morphology (e.g., during epitaxial film formation) without additional process steps.

In some embodiments, an example of a process which may use a silicon source as described above may include about 10 sccm to about 100 sccm of silane. In addition, the
30 silicon source may include about 10 sccm to about 100 sccm of dichlorosilane. In this example, during a deposition cycle in an AGS process, a chamber pressure in a range of about 5 Torr to about 50 Torr with a deposition time of about 2 to 250 seconds, and more preferably about 5 to 10
35 seconds and a temperature in a range between about 700°C and

about 750°C may be employed. In some embodiments, an SiH₄ to DCS ratio of greater than 1 may be employed, such as 2:1, 3:1, 4:1, 5:1, 7:1, 10:1, etc., (SiH₄:DCS). After the deposition cycle, an etchant process may be employed, for example, with about 50 sccm to about 500 sccm of hydrogen chloride (HCl) as the etchant, a chamber pressure of about 5 Torr to about 100 Torr with a deposition time of about 2 to 250 seconds, and more preferably about 5 to 10 seconds, and a temperature in a range between about 700°C and about 750°C.

10 After the etch cycle, a purge cycle may be conducted for about 10 seconds at a pressure of about 5 to about 50 Torr at a temperature in a range between about 700°C and about 750°C. Other process times, temperatures and/or flow rates may be used during deposition, etching and/or purging. For

15 example, chlorine (Cl₂) or a combination of Cl₂ and HCl may be employed during each etch step as described in U.S. Patent Application Serial No. 11/227,974, filed September 14, 2005 (Docket No. 9618/P01).

FIG. 1 is a flowchart of a first exemplary method 20 100 for forming an epitaxial film in accordance with the present invention. With reference to FIG. 1, in step 101, a substrate is loaded into a process chamber and is heated to a temperature of about 800 °C or less. In some embodiments, a lower temperature range may be used during epitaxial film 25 formation, such as less than 750°C, less than 700°C or less than 650°C.

In step 102, silane and dichlorosilane are flowed 30 into the process chamber, along with a suitable carrier gas and/or dopant(s) so as to form an epitaxial film on the substrate. In some embodiments, one or more etchant gases such as HCl, Cl₂, a combination of HCl and Cl₂, etc., may be flowed at the same time as the silicon source gasses (e.g., during a simultaneous deposition-etch process). In other 35 embodiments, a separate etchant step may be employed following deposition (e.g., during an AGS process).

Deposition and etching are continued until the desired epitaxial film thickness is achieved. In some embodiments, an SiH₄ to DCS ratio of greater than 1 may be employed, such as 2:1, 3:1, 4:1, 5:1, 7:1, 10:1, etc., (SiH₄:DCS). Other silicon source ratios may be used.

FIG. 2 is a flowchart of a second exemplary method 200 for forming an epitaxial film in accordance with the present invention. With reference to FIG. 2, in step 201, a substrate is loaded into a process chamber and is heated to a temperature of about 800 °C or less. In some embodiments, a lower temperature range may be used during epitaxial film formation, such as less than 750°C, less than 700°C or less than 650°C.

In step 202, silane and dichlorosilane are flowed into the process chamber, along with a suitable carrier gas and/or dopant(s) so as to form an epitaxial film on the substrate. In some embodiments, about 10 sccm to about 100 sccm of silane may be employed, as may be about 10 sccm to about 100 sccm of dichlorosilane. A pressure in a range of about 5 Torr to about 50 Torr may be employed. Deposition may be performed for about 2 to 250 seconds, and more preferably about 5 to 10 seconds. In some embodiments, an SiH₄ to DCS ratio of greater than 1 may be employed, such as 2:1, 3:1, 4:1, 5:1, 7:1, 10:1, etc., (SiH₄:DCS). Other flow rates, pressures, temperatures, times and/or SiH₄:DCS ratios may be used.

In step 203, an etchant gas such as HCl and/or Cl₂ is flowed into the process chamber, along with a suitable carrier gas so as to etch material deposited during step 202. For example, the substrate may be etched with about 50 sccm to about 500 sccm of hydrogen chloride (HCl) as the etchant at a chamber pressure of about 5 Torr to about 100 Torr for about 2 to 250 seconds, and more preferably about 5 to 10 seconds. Other etchants, flow rates, pressures and/or times may be used.

In step 204, after the etch cycle, a purge cycle may be conducted for about 2 to 250 seconds, and more preferably about 5 to 10 seconds. Other purge times may be used.

5 In step 205, a determination is made whether the desired epitaxial film thickness has been reached. If so, the process ends in step 206; otherwise, the process returns to step 202 to deposit additional epitaxial material on the substrate.

10 The foregoing description discloses only exemplary embodiments of the invention. Modifications of the above disclosed apparatus and methods which fall within the scope of the invention will be readily apparent to those of ordinary skill in the art. For instance, a lower
15 temperature range may be used during epitaxial film formation, such as less than 750°C, less than 700°C or less than 650°C.

20 Accordingly, while the present invention has been disclosed in connection with exemplary embodiments thereof, it should be understood that other embodiments may fall within the spirit and scope of the invention, as defined by the following claims.

THE INVENTION CLAIMED IS:

1. A method of forming an epitaxial layer comprising:
 - providing a substrate;
 - heating the substrate to a temperature of

5 less than about 800°C; and

 - performing a selective epitaxial film formation process on the substrate so as to form the epitaxial layer by employing both silane and dichlorosilane as silicon sources during the selective epitaxial film

10 formation process.
2. The method of claim 1 wherein heating the substrate comprises heating the substrate to a temperature of less than about 750°C.
- 15 3. The method of claim 1 wherein heating the substrate comprises heating the substrate to a temperature of less than about 700°C.
- 20 4. The method of claim 1 wherein heating the substrate comprises heating the substrate to a temperature of less than about 650°C.
- 25 5. The method of claim 1 wherein performing the selective epitaxial film formation process comprises:
 - flowing silane and dichlorosilane; and
 - flowing an etching gas that includes at least one of hydrogen chloride (HCl) and chlorine (Cl₂).
- 30 6. The method of claim 1 wherein performing the selective epitaxial film formation process comprises performing a deposition step followed by an etching step.

7. The method of claim 6 wherein performing the deposition step includes providing a flow of silane and a flow of dichlorosilane.

5 8. The method of claim 7 wherein the flow of silane is about 10 to 100 sccm.

9. The method of claim 7 wherein the flow of dichlorosilane is about 10 to 100 sccm.

10 10. The method of claim 7 wherein performing the deposition step includes employing a process pressure of about 5 to 50 Torr.

15 11. The method of claim 7 wherein performing the deposition step includes flowing silane and dichlorosilane for up to about 10 seconds.

20 12. The method of claim 6 wherein performing the etching step includes flowing an etching gas that includes at least one of hydrogen chloride (HCl) and chlorine (Cl₂).

25 13. The method of claim 12 wherein the flow of etching gas is about 50 to 500 sccm.

14. The method of claim 12 wherein performing the etching step includes employing a process pressure of about 5 to 100 Torr.

30 15. The method of claim 12 wherein the etching step includes flowing etching gas for up to about 10 seconds.

16. The method of claim 6 further comprising at least one purging step.

35

17. A method of forming an epitaxial layer comprising:

providing a substrate;

heating the substrate to a temperature of less than about 800°C;

5 performing a selective epitaxial film formation process comprising at least one deposition step and at least one etching step:

wherein the deposition step and etching step are alternated;

10 wherein the deposition step includes flowing silane and dichlorosilane each at a flow rate from about 10 to 100 sccm at a deposition pressure from about 5 to 50 Torr; and

15 wherein the etching step includes flowing at least one of hydrogen chloride and chlorine.

18. The method of claim 17 wherein the selective epitaxial film formation processes further comprises at least one purging step.

20 19. The method of claim 17 wherein heating the substrate comprises heating the substrate to a temperature of less than about 750°C.

25 20. The method of claim 17 wherein heating the substrate comprises heating the substrate to a temperature of less than about 700°C.

30 21. The method of claim 17 wherein heating the substrate comprises heating the substrate to a temperature of less than about 650°C.

22. A method of forming an epitaxial layer comprising:

providing a substrate;

35 heating the substrate to a temperature of

less than about 800°C; and

5 performing a selective epitaxial film formation process on the substrate so as to form the epitaxial layer by employing both silane and dichlorosilane as silicon sources during the selective epitaxial film formation process;

wherein a ratio of silane to dichlorosilane is greater than 1.

10 23. The method of claim 22 wherein the ratio of silane to dichlorosilane is greater than 2.

24. The method of claim 23 wherein the ratio of silane to dichlorosilane is greater than 5.

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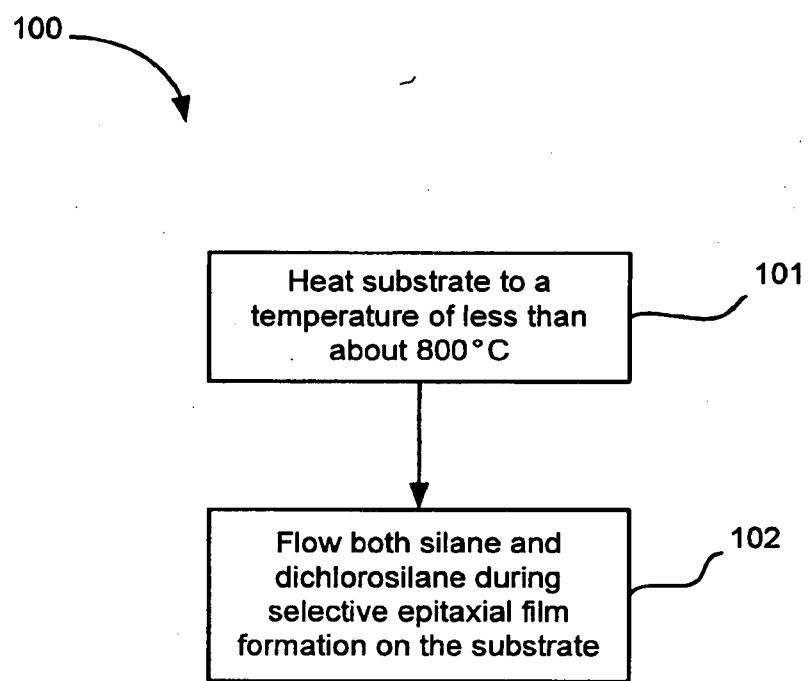


FIG. 1

2/2

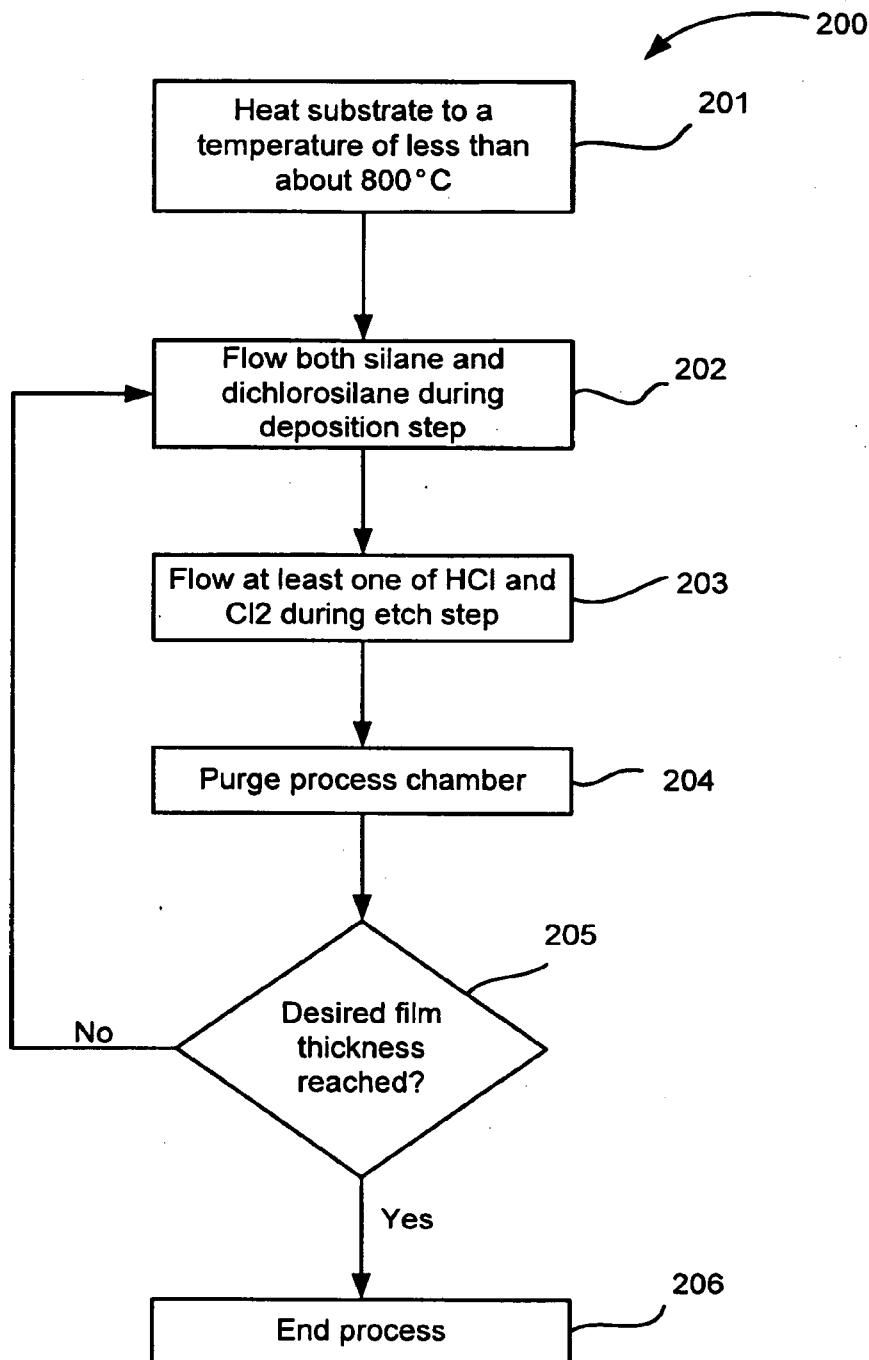


FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 07/17053

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 21/36 (2007.10)

USPC - 438/478, 257/E21.461

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

USPC -- 438/478, 27/E21.461

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
 WEST -- PGPB,USPT,USOC,EPAB,JPAB; Dialog Classic Files 654, 652, 351, 2, 6, 35, 65; Google Scholar, USPTO Web Page
 Search terms -- epitaxial layer, substrate, silane, dichlorosilane, ratio, deposition, etching, HCl, purging, heating, pressure, flow

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/0277272 A1 (SINGH et al.) 15 December 2005 (15.12.2005), para [0002], [0007], [0009]-[0011], [0013], [0016], [0018], [0019], [0048], [0049], [0056]	1-4, 6, 12, 16 ----- 5, 7-11, 13-15, 17-24
Y	US 2006/0166414 A1 (CARLSON et al.) 27 July 2006 (27.07.2006), para [0028], [0039], [0065]	5, 7-11, 13-15, 17-21
Y	US 2005/0191866 A1 (POWELL et al.) 01 September 2005 (01.09.2005), para [0004], [0041]	22-24

Further documents are listed in the continuation of Box C.

* Special categories of cited documents:	
"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E" earlier application or patent but published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed	

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13 November 2007 (13.11.2007)

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