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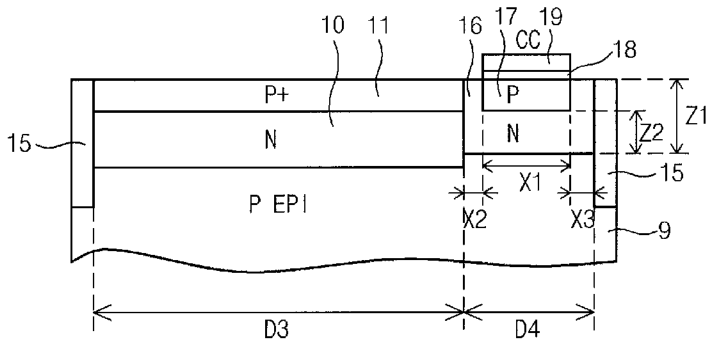
(54) Title: IMAGE SENSOR PIXEL HAVING PINNED PHOTODIODE WITH COUPLING CAPACITOR AND METHOD FOR SENSING A SIGNAL THEREOF



(57) Abstract: A pinned photodiode with a coupling capacitor and an image sensor using it. The pinned photodiode with the coupling capacitor comprises a first diffusion region having a second conductive type formed in an epitaxial layer having a first conductive type; a second diffusion region having a first conductive type formed over the first diffusion region; a third diffusion region having a second conductive type formed in the epitaxial layer and connected to the first diffusion region; a fourth diffusion region having a first conductive type formed in the third diffusion region; and a coupling capacitor connected to the fourth diffusion region to couple the voltage change of the third diffusion region to the outside. The image sensor comprises the pinned photodiode described above, a reset switch, a multi-functional switch between a variable voltage source and an output terminal of the coupling capacitor, and a signal amplifier.

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IMAGE SENSOR PIXEL HAVING PINNED PHOTODIODE WITH COUPLING CAPACITOR AND METHOD FOR SENSING A SIGNAL THEREOF

Technical Field

The present invention generally relates to a CMOS image sensor, and more specifically, to an image sensor pixel having a pinned photodiode (PPD) using a coupling capacitor without an ohmic-contacted output node.

Background of the Invention

Generally, an image sensor active pixel is a device configured to convert an external optical image signal into an electric image signal. Specifically, a CMOS image sensor is fabricated with a CMOS manufacturing technology. Each pixel of the CMOS image sensor changes light signals radiated from the corresponding unit of an object for photography into electrons with a photodiode, and converts the accumulated charge into voltage signals.

Fig. 1 is a circuit diagram illustrating a unit pixel of a general 3-transistor CMOS image sensor.

The unit pixel of the CMOS image sensor comprises a photodiode (PD) 1, a reset switch (RSW) 2, a capacitor CFD 4 of a floating diffusion sensing node 3, and a signal amplifier 5.

Hereinafter, the operation of the unit pixel of the CMOS image sensor is described.

The reset switch 2 resets the floating diffusion sensing node (FDSN) 3 into a reset voltage VR which is an initial value.

Signal electrons generated corresponding to incident light in the photodiode 1 are accumulated in the capacitor CFD 4 of the floating diffusion sensing node FDSN 3. The capacitor CFD 4 includes a junction capacitor of the photodiode 1, a capacitor located at an input terminal of the signal amplifier 5, and peripheral parasitic capacitors which are connected in parallel.

As the signal electrons are accumulated in the capacitor CFD 4, a changing signal voltage is transmitted to the input terminal of the signal amplifier 5.

An output signal of the signal amplifier 5 is connected to a signal line of a pixel array.

In the general CMOS image sensor pixel of Fig. 1, the ohmic-contacted floating diffusion sensing node FDSN 3 transmits a signal of the photodiode 1 to the input terminal of the signal amplifier 5.

While the ohmic contact is formed, many physical defects are generated so that a large dark current is generated from the floating diffusion sensing node FDSN 3.

Electrons of the dark current from the ohmic contact are added in the signal electrons while the photodiode 1 receives light and accumulates the signal electrons in the 3-transistor pixel structure and operation.

As a result, a noise generated around the FDSN 3 by the dark current severely degrades the image quality in the 3-transistor pixel structure.

When the photodiode 1 is reset at the reset voltage VR with the reset switch 2, a kTC reset noise is generated. And a correlated double sampling method used in a 4-transistor pixel cannot be applied to remove the reset noise in the 3-transistor pixel structure.

Since the photodiode 1 is directly connected to the floating diffusion sensing node FDSN 3 in the 3-transistor pixel, it is impossible to embody a shared structure where components other than the photodiode 1 are shared by two or more pixels to reduce the number of devices per pixel. The share structure cannot be adopted because electrons generated from all photodiodes of the shared pixels are mixed with each other.

Fig. 2 is a cross-sectional and circuit diagram illustrating a general 3-transistor image sensor pixel. A partially pinned photodiode part D1 and a reset switch part D2 are shown in the cross-sectional diagram, and a source follower 6 and an address switch 7 are shown in the circuit diagram.

The CMOS image sensor pixel comprises a partially pinned photodiode (PPPD), a reset switch (RSW), a source follower (SF) 6, an address switch (ASW) 7 and a constant current source 8.

A signal amplifier 5 includes the source follower SF 6, the address switch ASW 7 and the constant current source 8.

The reset switch RSW and the address switch ASW 7 are formed of a field effect transistor (FET) respectively. The reset switch RSW having a common drain with the SF 6 is connected to a driving voltage VDD. As a result, an additional reset voltage VR is not used but the driving voltage VDD is used as a reset voltage.

The partially pinned photodiode PPPD is formed of a pinned photodiode PPD including an ohmic-contacted diffusion sensing node. The partially pinned photodiode part D1 includes a n-type diffusion region 10 and a p+ diffusion region 11 which are formed in a p-type epitaxial layer (or p-type substrate) 9, and a n+ type diffusion region 12 for forming the ohmic-contacted sensing node in the n-type diffusion region 10.

The reset switch part D2 has a structure including a p-type well 13 formed in the p-type epitaxial layer (or p-type substrate) 9, a n+ type diffusion region 14 used as a reset-voltage-applying terminal formed in the p-type well 13, and an insulating layer and a gate electrode over a region where a channel is formed between the n+ type diffusion region 12 and the n+ type diffusion region 14.

A p-type well 15 is formed around the partially pinned photodiode part D1.

The partially pinned photodiode PPPD has a smaller dark current generated from the silicon surface than that of the general photodiode.

However, there is large dark current generated from the n+ type diffusion region 12 for forming the ohmic-contacted diffusion sensing node and a reset noise generated by the reset switch RSW.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Technical Subject

In order to overcome the above-described shortcomings, the present invention has the following objects.

Various embodiments of the present invention are directed at providing a photodiode and an image sensor pixel configured to reduce the dark current generated from the ohmic-contacted diffusion sensing node.

Various embodiments of the present invention are directed at providing a photodiode and an image sensor pixel configured to reduce reset noise.

Various embodiments of the present invention are directed at providing a photodiode and an image sensor pixel configured to inhibit generation of electrons in the interface between silicon and oxide layer on the floating diffusion sensing node, thereby reducing dark current and noise of the sensing node.

Various embodiments of the present invention are directed at providing a photodiode and an image sensor pixel configured to have a shared structure without any transfer gates between the photodiode and the sensing node.

Technical Solution

According to an embodiment of the present invention, a pinned photodiode comprises: an epitaxial layer having a first conductive type; a first diffusion region having a second conductive type formed in the epitaxial layer; a second diffusion region having a first conductive type formed over the first diffusion region; a third diffusion region having a second conductive type formed in the epitaxial layer and electrically connected to the first diffusion region; a fourth diffusion region having a first conductive type formed and floating in the third diffusion region; and a coupling capacitor connected to the fourth diffusion region and configured to transmit outside a voltage change of the third diffusion region .

According to an embodiment of the present invention, an image sensor pixel comprises: a photodiode which comprises an epitaxial layer having a first conductive type, a first diffusion region having a second conductive type formed in the epitaxial layer, a second diffusion region having a first conductive type formed over the first diffusion region, a third diffusion region having a second conductive type formed in the epitaxial layer and electrically connected to the first diffusion region, a fourth diffusion region having a first conductive type formed and floating in the third diffusion region, and a coupling capacitor connected to the fourth diffusion region and configured to transmit outside a voltage change of the third diffusion region ; a reset switch configured to reset the first diffusion region and the third diffusion region of the photodiode with a reset voltage source; a multi-functional switch which is connected between a variable voltage source and an output terminal of the coupling capacitor, and configured to apply a voltage of the variable voltage source to the output terminal; and a signal amplifier configured to transmit a signal corresponding to the voltage change transmitted by the coupling capacitor to a signal line of a pixel array.

According to an embodiment of the present invention, a method for sensing a signal of an image sensor pixel which comprises a photodiode that comprises an epitaxial layer having a first conductive type, a first diffusion region having a second conductive type formed in the epitaxial layer, a second diffusion region having a first conductive type formed over the first diffusion region, a third diffusion region having a second conductive type formed in the epitaxial layer and electrically connected to the first diffusion region, a fourth diffusion region having a first conductive type formed and floating in the third diffusion region, and a coupling capacitor connected to the fourth diffusion region and configured to transmit outside a voltage change of the third diffusion region ; a reset switch configured to reset the first diffusion region and the third diffusion region of the photodiode with a reset voltage source; a multi-functional switch which is connected between a variable voltage source and an output terminal of the coupling capacitor , and configured to apply a voltage of the variable voltage source to the output terminal; and a signal amplifier configured to transmit a signal corresponding to the voltage change transmitted by the coupling capacitor to a signal line of a pixel array, comprises the steps of: fixing the output terminal of the coupling capacitor at a first voltage level with the variable voltage source when the multi-functional switch is turned on; resetting the first diffusion region and the third diffusion region by turning on the reset switch; setting a voltage of the input terminal of the signal amplifier at a second voltage higher than the first voltage with the variable voltage source to read a value of the output voltage of the signal amplifier; storing electrons generated by absorbing light in the first diffusion region and the third diffusion region after the reset switch and the multi-functional switch are turned off; and sensing a change of the output voltage of the signal amplifier.

According to an embodiment of the present invention, a method for sensing a signal of an image sensor pixel which comprises a photodiode that comprises an epitaxial layer having a first conductive type, a first diffusion region having a second conductive type formed in the epitaxial layer, a second diffusion region having a first conductive type formed over the first diffusion region, a third diffusion region having a second conductive type formed in the epitaxial layer and electrically connected to the first diffusion region, a fourth diffusion region having a first conductive type formed and floating in the third diffusion region, and a coupling capacitor connected to the fourth diffusion region and configured to transmit outside a voltage change of the third diffusion region ; a reset switch configured to reset the first diffusion region and the third diffusion region of the photodiode with a reset voltage source; a multi-functional switch which is connected between a variable voltage source and an output terminal of the coupling capacitor, and configured to apply a voltage of the variable voltage source to the output terminal; and a signal amplifier configured to transmit a signal corresponding to the voltage change transmitted by the coupling capacitor to a signal line of a pixel array, comprises the steps of: fixing the output terminal of the coupling capacitor at a first voltage level with the variable voltage when the multi-functional switch is turned on; resetting the first diffusion region and the third diffusion region by turning on the reset switch; storing electrons generated by absorbing light in the first diffusion region and the third diffusion region after the reset switch and the multi-functional switch are turned off; setting a voltage of the input terminal of the signal amplifier at a second voltage higher than an input threshold voltage of the signal amplifier with the variable voltage source by turning on the multi-functional switch, and reading an output signal of the signal amplifier after the multi-functional switch is turned off; removing the electrons stored in the first diffusion region and the third diffusion region by turning on the reset switch; and sensing a change of the output voltage of the signal amplifier.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram illustrating a general 3-transistor image sensor pixel.

Fig. 2 is a cross-sectional and circuit diagram illustrating a general 3-transistor image sensor pixel.

Fig. 3 is a diagram illustrating a pinned photodiode part D3 and an output node part D4 in a capacitor combined pinned photodiode (CCPPD) according to an embodiment of the present invention.

Fig. 4 is a cross-sectional diagram taken along A-A' of Fig. 3.

Fig. 5 is a cross-sectional diagram taken along B-B' of Fig. 3.

Fig. 6 is a cross-sectional diagram taken along C-C' of Fig. 3.

Fig. 7 is a diagram illustrating the capacitor combined pinned photodiode CCPPD and a reset switch part D5 in an embodiment where the output node part D4 of the CCPPD is connected to the reset switch part D5.

Fig. 8 is a cross-sectional diagram taken along D-D' of Fig. 7.

Fig. 9 is a diagram illustrating the capacitor combined pinned photodiode CCPPD and the reset switch part D5 in an embodiment where the pinned photodiode part D3 of the CCPPD is connected to the reset switch part D5.

Fig. 10 is a cross-sectional diagram taken along E-E' of Fig. 9.

Fig. 11 is a cross-sectional diagram taken along F-F' of Fig. 9.

Fig. 12 is a cross-sectional diagram taken along G-G' of Fig. 9.

Fig. 13 is a cross-sectional and circuit diagram illustrating an image sensor pixel including the CCPPD and the reset switch RSW of Figs. 7 and 8, a multi-functional switch 24, and a signal amplifier 25.

Fig. 14 is a cross-sectional and circuit diagram illustrating an image sensor pixel including the CCPPD and the reset switch RSW of Figs. 9 through 12, a multi-functional switch 24, and a signal amplifier 25.

Fig. 15 is a diagram illustrating an example of Fig. 13 with the signal amplifier 25 comprising a source follower (SF) 26 and a constant current source 27.

Fig. 16 is a diagram illustrating an example of Fig. 15 wherein a driving voltage VDD of the source follower 26 is used in common as a reset voltage source.

Fig. 17 is a diagram illustrating an example of Fig. 14 with the signal amplifier 25 comprising a source follower (SF) 26 and a constant current source 27.

Fig. 18 is a diagram illustrating an example of Fig. 17 wherein a driving voltage VDD of the source follower 26 is used in common as a reset voltage source.

Preferred Embodiments

The present invention will be described in detail with reference to the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

Fig. 3 is a diagram illustrating a pinned photodiode part D3 and an output node part D4 in a capacitor combined pinned photodiode (CCPPD) according to an embodiment of the present invention.

The capacitor combined pinned photodiode CCPPD includes a pinned photodiode PPD part D3 and an output node part D4. The geometrical shape of the pinned photodiode part D3 and the output node part D4 can be changed.

Fig. 4 is a cross-sectional diagram taken along A-A' of Fig. 3, and Fig. 5 is a cross-sectional diagram taken along B-B' of Fig. 3.

The capacitor combined pinned photodiode CCPPD includes a n-type diffusion region 10 and a p+ type diffusion region 11 which are successively formed in a p-type epitaxial layer (or p-type substrate) 9. A p type well 15 is formed around the periphery of the pinned photodiode part D3.

Fig. 6 is a cross-sectional diagram taken along C-C' of Fig. 3.

The pinned photodiode part D3 includes the n-type diffusion region 10 and the p+ type diffusion region 11 which are successively formed in the p-type epitaxial layer (or p-type substrate) 9, The output node part D4 comprises a n-type diffusion region 16 formed in the p-type epitaxial layer (or p-type substrate) 9, a floating p-type diffusion region 17 used as a first electrode of a coupling capacitor CC in the n-type diffusion region 16, and an oxide layer 18 used as a dielectric layer and a second electrode 19 which are successively formed over the floating p-type diffusion region 17. The second electrode serves as an output terminal of the coupling capacitor. The floating p-type diffusion region 17 is formed not to contact with the p+ type diffusion region 11 and the p-type well 15 but to be floating in the n-type diffusion region 16.

The n-type diffusion region 16 of the output node part D4 touches the n-type diffusion region 10 of the pinned photodiode part D3. As a result, electrons are allowed to move between the n-type diffusion region 10 and the n-type diffusion region 16.

The p-type well 15 is formed around the pinned photodiode part D3 and the output node part D4.

The doping concentration of the n-type diffusion region 16 of the output node part D4 can be the same as or different from that of the n-type diffusion region 10 of the pinned photodiode D3.

A junction capacitor CFP is formed by junction of the floating p-type diffusion region 17 and the n-type diffusion region 16. The coupling capacitor CC consists of the oxide layer 18 as the dielectric layer, the floating p-type diffusion region 17 as the first electrode, and the electrode 19 formed over the oxide layer 18 as the second electrode. The junction capacitor CFP and the coupling capacitor CC are serially connected in the circuit. As a result, a voltage change of the n-type diffusion region 16 is transmitted through the junction capacitor CFP and the coupling capacitor CC to another parts.

When signal electrons generated by absorbing light in the pinned photodiode part D3 are accumulated in the n-type diffusion region 10, a part of the signal electrons moves into the n-type diffusion region 16 of the output node part D4, so that a voltage level of the n-type diffusion region 16 is changed.

The voltage change of the n-type diffusion region 16 is transmitted to the coupling capacitor CC through the junction capacitor CFP and in turn to the outside of the output node part D4 through the second electrode 19 which is the output terminal of the coupling capacitor CC. That is, when the second electrode 19 of the coupling capacitor CC is connected to the input terminal of the signal amplifier, a voltage proportional to the signal voltage change of the n-type diffusion region 16 is transmitted into the input terminal of the signal amplifier.

The impurity doping concentration of the n-type diffusion region 16 and the p-type diffusion region 17 serving as the first electrode of the coupling capacitor CC can be lower than that for ohmic contact. As a result, the dark current of the output node part D4 can be reduced in comparison with the ohmic-contacted diffusion sensing nodes 3 and 12 because physical defects generated in the sensing nodes 3 and 12 for forming the ohmic contact can be removed. The physical defects of the sensing nodes are main cause of the dark current of the sensing nodes.

The floating p-type diffusion region 17 serves as the first electrode of the coupling capacitor CC, and inhibits generation of electrons generated from the interface between the silicon and the oxide film 18, thereby reducing the dark current and noise of the output node. In the capacitor combined pinned photodiode CCPPD, the n-type diffusion region 10 of the pinned photodiode part D3 can be fully depleted by reset.

Also, the n-type diffusion region 16 of the output node part D4 can be also fully depleted by reset, with the control of the doping concentration of the n-type diffusion region 16 and geometrical sizes x1, x2, x3, z1 and z2. As a result, a reset noise and an image lag can be removed in the photodiode. Although the n-type diffusion region 16 of the output node D4 is not fully depleted by reset, the doping concentration of the n-type diffusion region 16 can be lower than that to form ohmic contact, thereby reducing the image lag and the reset noise in comparison with a general 3-transistor pixel having the ohmic-contacted diffusion sensing nodes 3 and 12.

Fig. 7 is a diagram illustrating the capacitor combined pinned photodiode CCPPD and a reset switch part D5 in an embodiment where the output node part D4 of the capacitor combined pinned photodiode CCPPD is connected to the reset switch part D5.

The capacitor combined pinned photodiode CCPPD includes a pinned photodiode PPD part D3 and an output node part D4. A reset switch part D5 is formed to adjoin the output node part D4. The geometrical shape of the pinned photodiode part 3, the output node part D4 and the reset switch part D5 can be changed.

Fig. 8 is a cross-sectional diagram taken along D-D' of Fig. 7.

The pinned photodiode part D3 includes the n-type diffusion region 10 and the p+ type diffusion region 11 which are successively formed in the p-type epitaxial layer (or p-type substrate) 9. The output node part D4 includes a n-type diffusion region 16 formed in the p-type epitaxial layer (or p-type substrate) 9, a floating p-type diffusion region 17 formed in the n-type diffusion region 16 which serves as the first electrode of a coupling capacitor CC, and an oxide layer 18 and a second electrode 19 which are used as the dielectric layer and the second electrode of a coupling capacitor CC respectively and successively formed over the floating p-type diffusion region 17. The second electrode

19 serves as an output terminal of the coupling capacitor CC. The floating p-type diffusion region 17 is formed not to contact with the p+ type diffusion region 11 and the p-type well 15 but to be floating in the n-type diffusion region 16.

The n-type diffusion region 16 of the output node part D4 touches the n-type diffusion region 10 of the pinned photodiode part D3. As a result, electrons are allowed to move between the n-type diffusion region 10 and the n-type diffusion region 16.

The p-type well 15 is formed around the capacitor combined pinned photodiode CCPPD except a part contacting with the reset switch part D5.

The reset switch part D5 comprise a p-type well 20 formed in the p-type epitaxial layer (or p-type substrate) 9, a n+ type diffusion region 21 used as a reset-voltage-applying terminal formed in the p-type well 20, and an oxide insulating layer 22 and a gate electrode 23 over a region where a channel is formed between the n-type diffusion region 16 of the output node part D4 and the n+ type diffusion region 21.

Fig. 9 is a diagram illustrating the capacitor combined pinned photodiode CCPPD and the reset switch part D5 in an embodiment where the pinned photodiode part D3 is connected to the reset switch part D5.

The capacitor combined pinned photodiode CCPPD includes a pinned photodiode PPD part D3 and an output node part D4. A reset switch part D5 is formed to contact with the pinned photodiode part D3. The geometrical shape of the pinned photodiode part 3, the output node part D4 and the reset switch part D5 can be changed.

Fig. 10 is a cross-sectional diagram taken along E-E' of Fig. 9.

The pinned photodiode part D3 includes the n-type diffusion region 10 and the p+ type diffusion region 11 which are formed in the p-type epitaxial layer (or p-type substrate) 9. The output node part D4 includes a n-type diffusion region 16 formed in the p-type epitaxial layer (or p-type substrate) 9, a floating p-type diffusion region 17 used as a first electrode of a coupling capacitor CC in the n-type diffusion region 16, and an oxide layer 18 used as a dielectric layer and a second electrode 19 which are successively formed over the floating p-type diffusion region 17. The second electrode serves as an output terminal of the coupling capacitor. The floating p-type diffusion region 17 is formed not to contact with the p+ type diffusion region 11 and the p-type well 15 but to be floating in the n-type diffusion region 16.

The n-type diffusion region 16 of the output node part D4 touches the n-type diffusion region 10 of the pinned photodiode part D3. As a result, electrons are allowed to move between the n-type diffusion region 10 and the n-type diffusion region 16.

The p-type well 15 is formed around the pinned photodiode part D3 and the output node part D4.

Fig. 11 is a cross-sectional diagram taken along F-F' of Fig. 9.

The pinned photodiode part D3 includes the n-type diffusion region 10 and the p+ type diffusion region 11 which are formed in the p-type epitaxial layer (or p-type substrate) 9.

The reset switch part D5 comprises a p-type well 20 formed in the p-type epitaxial layer (or p-type substrate) 9, a n+ type diffusion region 21 used as a reset-voltage-applying terminal formed in the p-type well 20, and an oxide layer 22 and a gate electrode 23 over a region where a channel is formed between the n-type diffusion region 10 of the output node part D3 and the n+ type diffusion region 21.

The p-type well 15 is formed around the pinned photodiode part D3 except a part contacting with the reset switch part D5.

Fig. 12 is a cross-sectional diagram taken along G-G' of Fig. 9. Here, the reset switch part D5, the pinned photodiode D3 and the output node part D4 are sequentially connected.

The reset switch part D5 comprises a p-type well 20 formed in the p-type epitaxial layer (or p-type substrate) 9, a n+ type diffusion region 21 used as a reset-voltage-applying terminal formed in the p-type well 20, and an oxide layer 22 and a gate electrode 23 over a region where a channel is formed between the n-type diffusion region 10 of the pinned photodiode part D3 and the n+ type diffusion region 21.

The pinned photodiode part D3 includes the n-type diffusion region 10 and the p+ type diffusion region 11 which are formed in the p-type epitaxial layer (or p-type substrate) 9, and the output node part D4 includes a n-type diffusion region 16 formed in the p-type epitaxial layer (or p-type substrate) 9, a floating p-type diffusion region 17 used as a first electrode of a coupling capacitor CC in the n-type diffusion region 16, and an oxide insulating layer 18 used as a dielectric layer and a second electrode 19 which are successively formed over the floating p-type diffusion region 17. The second electrode serves as an output terminal of the coupling capacitor. The floating p-type diffusion region 17 is formed not to contact with the p+ type diffusion region 11 and the p-type well 15 but to be floating in the n-type diffusion region 16.

The n-type diffusion region 16 of the output node part D4 touches the n-type diffusion region 10 of the pinned photodiode part D3. As a result, electrons are allowed to move between the n-type diffusion region 10 and the n-type diffusion region 16.

The p-type well 15 is formed around the pinned photodiode part D3 and the output node part D4 except a part contacting with the reset switch part D5.

Fig. 13 is a cross-sectional and circuit diagram illustrating an image sensor pixel including the capacitor combined pinned photodiode CCPPD and the reset switch RSW of Figs. 7 and 8, a multi-functional switch 24, and a signal amplifier 25. The capacitor combined pinned photodiode CCPPD and the reset switch part D5 are shown in the cross-sectional diagram, and the multi-functional switch 24 and the signal amplifier 25 are shown in the circuit diagram.

In the image sensor pixel of Fig. 13, the reset switch RSW is connected to the output node part D4 of the capacitor combined pinned photodiode CCPPD.

The capacitor combined pinned photodiode CCPPD absorbs light radiated from an object to generate signal electrons. The signal electrons are distributed in the n-type diffusion region 10 of the pinned photodiode part D3 and the n-type diffusion region 16 of the output node part D4.

The junction capacitor CFP and the coupling capacitor CC transmit the voltage change of the n-type diffusion region 16 to the input terminal of the signal amplifier 25. The voltage change occurs when the signal electrons flow into or out from the n-type diffusion region 16 of the output node part D4.

The reset switch RSW discharges the electrons stored in the n-type diffusion regions 10 and 16 of the capacitor combined pinned photodiode CCPPD through the n+ diffusion region 21 connected to the reset voltage source VR, to reset a voltage of the n-type diffusion regions 10 and 16 of the capacitor combined pinned photodiode CCPPD into an initial value.

The multi-functional switch 24 has the following functions in the operation of the above-described pixel.

The multi-functional switch 24 provides a discharging path to a floating structure when the input terminal of the signal amplifier 25 is floating. So, the multi-functional switch 24 prevents the related devices such as the signal amplifier 25 and coupling capacitor CC from malfunctioning and being damaged. The multi-functional switch 24 sets the initial voltage of the input terminal of the signal amplifier 25 and the second electrode 19 of the coupling capacitor CC to a predetermined value with a variable voltage source VC.

The output terminal of the signal amplifier 25 is directly connected to a signal line of a pixel array, or is connected to the signal line through an addressing switch for connecting/disconnecting an output signal of the signal amplifier 25. When the output terminal of the signal amplifier 25 is directly connected to the signal line of the pixel array without the addressing switch, the signal amplifier 25 is required to be controlled its on/off states.

There are two methods for the operation of the unit pixel of Fig. 13.

In the first method, the voltage of the variable voltage source VC is set at a first voltage VL (e.g., 0V) and the multi-functional switch 24 is turned on so that a voltage of the second electrode 19 of the coupling capacitor CC is fixed at the first voltage VL. The reset switch RSW is turned on to reset the n-type diffusion regions 10 and 16 of the capacitor combined pinned photodiode CCPPD. The voltage of the variable voltage source VC is set to be a second voltage VH higher than the first voltage VL. The second voltage VH is set to be a sufficiently higher value (e.g., driving voltage VDD of the signal amplifier 25) in consideration of the dropping range of the signal voltage due to light.

The reset switch RSW and the multi-functional switch 24 are turned off to finish the reset operation of the capacitor combined pinned photodiode CCPPD.

As the signal electrons corresponding to incident light are accumulated in the n-type diffusion regions 10 and 16 of the capacitor combined pinned photodiode CCPPD after resetting of the capacitor combined pinned photodiode CCPPD, the voltage of the n-type diffusion region 16 falls down and the voltage change is transmitted to the signal amplifier 25 through the junction capacitor CFP and the coupling capacitor CC. That is, the voltage of the second electrode 19 of the coupling capacitor CC and the input terminal of the signal amplifier 25 falls down from the initial value VH. The change of the signal voltage of the input terminal of the signal amplifier 25 gives information on the amount of the signal electrons, that is, on the amount of the incident light into the pixel.

In the second method, the voltage of the variable voltage source VC is set to be the first voltage VL (e.g., 0V), and the multi-functional switch 24 is turned on to fix the voltage of the second electrode 19 of the coupling capacitor CC at the first voltage VL. The reset switch RSW is turned on to reset the n-type diffusion regions 10 and 16 of the capacitor combined pinned photodiode CCPPD. The reset switch RSW is turned off to finish the reset operation of the capacitor combined pinned photodiode CCPPD. Here, the multi-functional switch 24 is kept on or turned off. Both of the ways are possible.

The signal electrons are accumulated in the n-type diffusion regions 10 and 16 of the capacitor combined pinned photodiode CCPPD by the incident light, and the amount of the accumulated signal electrons is read by the following operation.

The value of the variable voltage source VC is set to be a voltage VL1 larger than an input threshold voltage VT of the signal amplifier 25. The multi-functional switch 24 is turned on, if it was turn off before, to set the initial value of the second electrode of the coupling capacitor CC and the input terminal of the signal amplifier 25 at the voltage VL1. The multi-functional switch 24 is turned off and the reset switch RSW is turned on to discharge the signal electrons from the n-type diffusion regions 10 and 16 of the capacitor combined pinned photodiode CCPPD. As a result, the voltage of the n-type diffusion region 16 of the capacitor combined pinned photodiode CCPPD rises.

The voltage rise is transmitted to the coupling capacitor CC through the junction capacitor CFP, and in turn to the input terminal of the signal amplifier 25 through the second electrode 19 of the coupling capacitor CC. That is, when the signal electrons accumulated in the capacitor combined pinned photodiode CCPPD are reset, the voltage of the input terminal of the signal amplifier 25 rises from the initial value VL1. The amount of the signal electrons, that is, the amount of incident lights can be evaluated from the voltage rising value.

The second operation method is roughly opposite in concept to that of a general 4-transistor pixel.

Fig. 14 is a cross-sectional and circuit diagram illustrating an image sensor pixel including the capacitor combined pinned photodiode CCPPD and the reset switch RSW of Figs. 9 through 12, a multi-functional switch 24, and a signal amplifier 25.

The capacitor combined pinned photodiode CCPPD and the reset switch part D5 are shown in the cross-sectional diagram, and the multi-functional switch 24 and the signal amplifier 25 are shown in the circuit diagram.

The operation of Fig. 14 is the same as the operation of Fig. 13.

Fig. 15 is a diagram illustrating an example of Fig. 13 wherein the signal amplifier 25 comprises a source follower (SF) 26 and a constant current source 27.

Fig. 16 is a diagram illustrating an example of Fig. 15 wherein a driving voltage VDD of the source follower 26 is used in common as a reset voltage source VR.

The operation of Figs. 15 and 16 is as follows.

The voltage of the variable voltage source VC is set to be the first voltage VL (e.g., 0V), and the multi-functional switch 24 is turned on to fix the voltage of the second electrode 19 of the coupling capacitor CC at the first voltage VL. The first voltage VL is set so that the source follower active transistor 26 is automatically turned off. The reset switch RSW is turned on to reset the n-type diffusion regions 10 and 16 of the capacitor combined pinned photodiode CCPPD. The reset switch RSW is turned off to finish the reset operation of the capacitor combined pinned photodiode CCPPD. Here, the multi-functional switch 24 is kept on or turned off. Both of the ways are possible

The signal electrons are accumulated in the n-type diffusion regions 10 and 16 of the capacitor combined pinned photodiode CCPPD by the incident light signal. The amount of the accumulated signal electrons is read by the following operation.

The value of the variable voltage source VC is set to be a voltage VL1 larger than an input threshold voltage VT of the source follower active transistor 26. The multi-functional switch 24 is turned on, if it was turned off before, to set the initial value of the second electrode 19 of the coupling capacitor CC and a gate of the source follower active transistor 26 at the voltage VL1. The multi-functional switch 24 is turned off and the reset switch RSW is turned on to discharge the signal electrons from the n-type diffusion regions 10 and 16 of the capacitor combined pinned photodiode CCPPD. As a result, the voltage of the n-type diffusion region 16 of the output node part D4 of the capacitor combined pinned photodiode CCPPD rises. The voltage rise is transmitted to the gate of the source follower active transistor 26 through the second electrode 19 which is an output terminal of the coupling capacitor CC.

That is, when the signal electrons accumulated in the capacitor combined pinned photodiode CCPPD are reset, the voltage of the gate of the source follower active transistor 26 rises from the initial value VL1. The amount of the signal electrons, that is, the amount of the incident light can be evaluated from the voltage rising value.

In the above-described operation method of the pixel, the on/off states of the source follower active transistor 26 are controlled by the voltage setting value of the gate terminal. So, an addressing switch for selectively transmitting an output voltage to the signal line of the pixel array is not required.

The multi-functional switch 24 has the following functions in the pixel.

The multi-functional switch 24 provides a path for discharging net charge flowed into the electrically floating structure at the connecting node of the gate of the source follower active transistor 26 and second electrode 19 of the coupling capacitor CC. As a result, the multi-functional switch 24 prevents the malfunction or damage of the coupling capacitor CC and the source follower active transistor 26. The multi-functional switch 24 sets the initial voltage of the gate of the source follower active transistor 26 and the second electrode 19 of the coupling capacitor CC at a give value with the variable voltage source VC.

Fig. 17 is a diagram illustrating an example of Fig. 14 wherein the signal amplifier 25 comprises a source follower (SF) 26 and a constant current source 27.

Fig. 18 is a diagram illustrating an example of Fig. 17 wherein a driving voltage VDD of the source follower 26 is used in common as a reset voltage source VR.

The operation of Figs. 17 and 18 is substantially the same as that of Figs. 15 and 16.

Industrial Applicability

As described above, the CMOS image sensor according to an embodiment of the present invention has the following effects.

The signal voltage is transmitted to the signal amplifier with the coupling capacitor instead of the ohmic-contacted diffusion sensing node -in order to reduce a dark current generated from the ohmic contact.

The n-type diffusion regions 10 of the pinned photodiode part D3 and 16 of the output node part D4 are fully depleted by the reset operation to remove a reset noise and an image lag.

The floating p-type diffusion region 17 serves as the first electrode of the coupling capacitor CC as well as inhibits generation of electrons from the interface between the silicon and the oxide film to reduce a dark current and a noise of the sensing node.

The shared structure can be embodied by using the coupling capacitor instead of the ohmic-contacted diffusion sensing node.

While the invention is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and described in detail herein. However, it should be understood that the invention is not limited to the particular forms disclosed. Rather, the invention covers all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined in the appended claims.

What is Claimed is:

1. A pinned photodiode comprising:

an epitaxial layer having a first conductive type;

a first diffusion region having a second conductive type formed in the epitaxial layer;

a second diffusion region having a first conductive type formed over the first diffusion region;

a third diffusion region having a second conductive type formed in the epitaxial layer and electrically connected to the first diffusion region;

a fourth diffusion region having a first conductive type formed and floating in the third diffusion region; and

a coupling capacitor connected to the fourth diffusion region and configured to transmit outside a voltage change of the third diffusion region .

2. The pinned photodiode according to claim 1, wherein the second conductive type has an opposite polarity to that of the first conductive type.

3. The pinned photodiode according to claim 1, wherein the first diffusion region contacts physically with the third diffusion region.

4. The pinned photodiode according to claim 1, wherein the third diffusion region has the same impurity doping concentration as that of the first diffusion region.

5. The pinned photodiode according to claim 1, wherein a fifth diffusion

region having a second conductive type contacts physically between the first diffusion region and the third diffusion region.

6. The pinned photodiode according to claim 1, wherein the coupling capacitor comprises:

a first electrode formed with the fourth diffusion region;

an insulating layer formed over the fourth diffusion region; and

a second electrode formed over the insulating layer.

7. The pinned photodiode according to claim 6, wherein the second electrode of the coupling capacitor is formed of an opaque material and serves as an optical blocking mask for blocking an incident light into the third diffusion region.

8. The pinned photodiode according to claim 1, wherein the second diffusion region is connected electrically to a ground level or a negative voltage source.

9. An image sensor pixel comprising:

a photodiode which comprises an epitaxial layer having a first conductive type, a first diffusion region having a second conductive type formed in the epitaxial layer, a second diffusion region having a first conductive type formed over the first diffusion region, a third diffusion region having a second conductive type formed in the epitaxial layer and electrically connected to the first diffusion region, a fourth diffusion region having a first conductive type formed and floating in the third diffusion region, and a coupling capacitor connected to the fourth diffusion region and configured to transmit outside a voltage change of the third diffusion region ;

a reset switch configured to reset the first diffusion region and the third diffusion region of the photodiode with a reset voltage source;

a multi-functional switch, connected between a variable voltage source and an output terminal of the coupling capacitor, and configured to apply a voltage of the variable voltage source to the output terminal; and

a signal amplifier configured to transmit a signal corresponding to the voltage change transmitted by the coupling capacitor to a signal line of a pixel array.

10. The image sensor pixel according to claim 9, wherein the second conductive type has an opposite polarity to that of the first conductive type.

11. The image sensor pixel according to claim 9, wherein the coupling capacitor comprises:

a first electrode formed with the fourth diffusion region;

an insulating layer formed over the fourth diffusion region; and

a second electrode formed over the insulating layer.

12. The image sensor pixel according to claim 9, wherein the first diffusion region is fully depleted in the reset operation.

13. The image sensor pixel according to claim 9, wherein the third diffusion region is fully depleted in the reset operation.

14. The image sensor pixel according to claim 9, wherein the reset switch is connected between the first diffusion region and the reset voltage source.

15. The image sensor pixel according to claim 9, wherein the reset switch is connected between the third diffusion region and the reset voltage source.

16. The image sensor pixel according to claim 9, wherein the reset switch includes a Field Effect Transistor (FET) or a transfer gate structure.

17. The image sensor pixel according to claim 9, wherein the multi-functional switch forms a discharging path in order to prevent the output terminal of the coupling capacitor and the input terminal of the signal amplifier from being electrically a floating structure.

18. The image sensor pixel according to claim 9, wherein the multi-functional switch sets voltages of the output terminal of the coupling capacitor and the input terminal of the signal amplifier to be at predetermined values respectively.

19. The image sensor pixel according to claim 9, further comprising a switch configured to connect the output terminal of the signal amplifier to the signal line of the pixel array.

20. The image sensor pixel according to claim 9, wherein the signal amplifier is a source follower amplifier.

21. The image sensor pixel according to claim 9, wherein the reset voltage source is a driving voltage of the signal amplifier.

22. The image sensor pixel according to claim 9, wherein two or more pixels share the multi-functional switch and the signal amplifier.

23. A method for sensing a signal of an image sensor pixel which comprises a photodiode that comprises an epitaxial layer having a first conductive type, a first diffusion region having a second conductive type formed in the epitaxial layer, a second diffusion region having a first conductive type formed over the first diffusion region, a third diffusion region having a second conductive type formed in the epitaxial layer and electrically connected to the first diffusion region, a fourth diffusion region having a first conductive type formed and floating in the third diffusion region, and a coupling capacitor connected to the fourth diffusion region and configured to transmit outside a voltage change of the third diffusion region ; a reset switch configured to reset the first diffusion region and the third diffusion region of the photodiode with a reset voltage source; a multi-functional switch which is connected between a variable voltage source and an output terminal of the coupling capacitor, and configured to apply a voltage of the variable voltage source to the output terminal; and a signal amplifier configured to transmit a signal corresponding to the voltage change transmitted by the coupling capacitor to a signal line of a pixel array, the method comprising the steps of:

fixing the output terminal of the coupling capacitor at a first voltage level with the variable voltage source when the multi-functional switch is turned on;

resetting the first diffusion region and the third diffusion region by turning on the reset switch;

setting a voltage of the input terminal of the signal amplifier at a second voltage higher than the first voltage with the variable voltage source to read a value of the output voltage of the signal amplifier;

storing electrons generated by absorbing light in the first diffusion region and the third diffusion region after the reset switch and the multi-functional switch are turned off; and

sensing a change of the output voltage of the signal amplifier.

24. A method for sensing a signal of an image sensor pixel which comprises a photodiode that comprises an epitaxial layer having a first conductive type, a first diffusion region having a second conductive type formed in the epitaxial layer, a second diffusion region having a first conductive type formed over the first diffusion region, a third diffusion region having a second conductive type formed in the epitaxial layer and electrically connected to the first diffusion region, a fourth diffusion region having a first conductive type formed and floating in the third diffusion region, and a coupling capacitor connected to the fourth diffusion region and configured to transmit outside a voltage change of the third diffusion region ; a reset switch configured to reset the first diffusion region and the third diffusion region of the photodiode with a reset voltage source; a multi-functional switch which is connected between a variable voltage source and an output terminal of the coupling capacitor, and configured to apply a voltage of the variable voltage source to the output terminal; and a signal amplifier configured to transmit a signal corresponding to the voltage change transmitted by the coupling capacitor to a signal line of a pixel array, the method comprising the steps of:

fixing the output terminal of the coupling capacitor at a first voltage level with the variable voltage when the multi-functional switch is turned on;

resetting the first diffusion region and the third diffusion region by turning on the reset switch;

storing electrons generated by absorbing light in the first diffusion region and the third diffusion region after the reset switch and the multi-functional switch are turned off;

setting a voltage of the input terminal of the signal amplifier at a second voltage higher than an input threshold voltage of the signal amplifier with the variable voltage source by turning on the multi-functional switch, and reading an output signal of the signal amplifier after the multi-functional switch is turned off;

removing the electrons stored in the first diffusion region and the third diffusion region by turning on the reset switch; and

sensing a change of the output voltage of the signal amplifier.

25. The method according to claim 24, wherein the storing-the-electrons step is performed without turning off the multi-functional switch.

FIG. 1

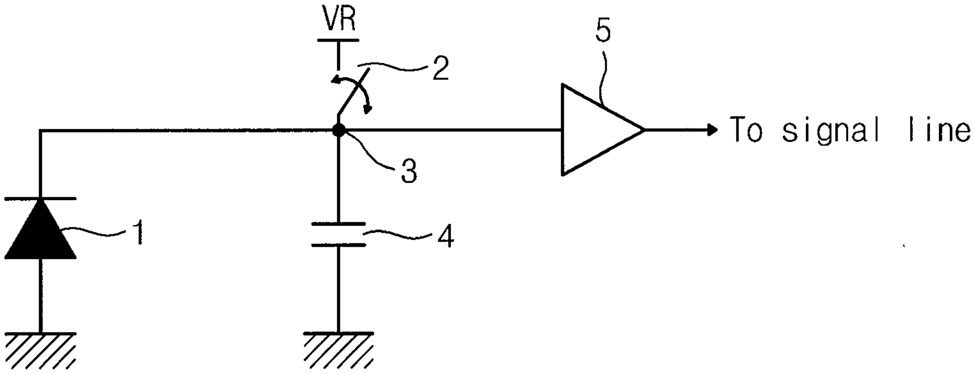
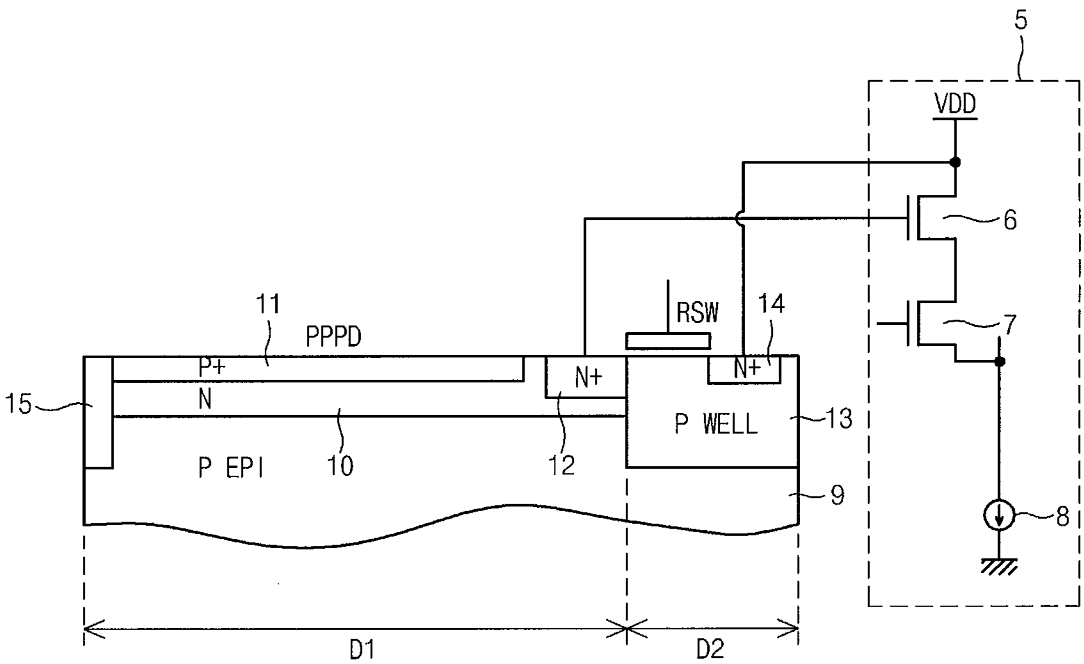

VR
2
5
To signal line
3
1
4

FIG. 2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7
8
11
PPPD
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12
9
D1
D2

FIG. 3

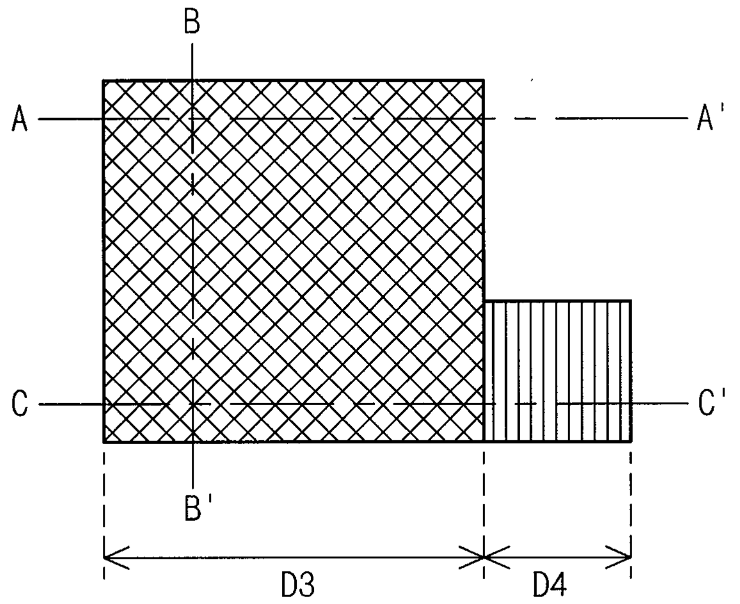


FIG. 4

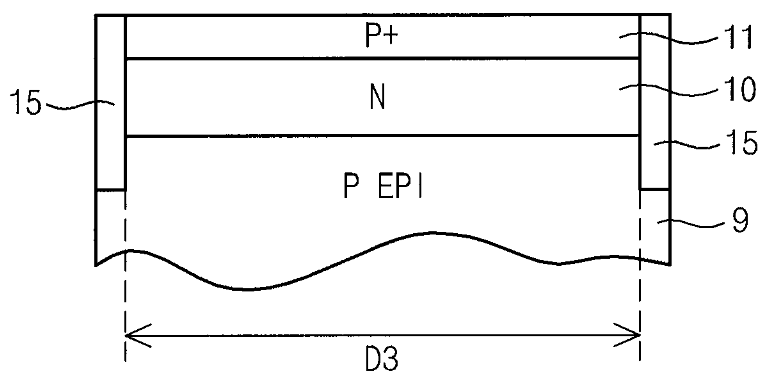


FIG. 5

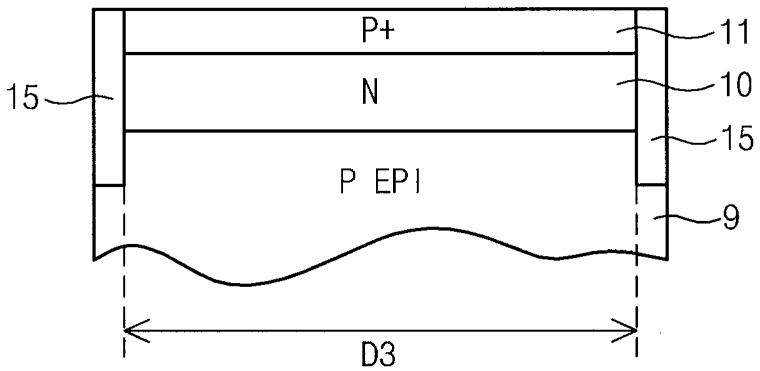
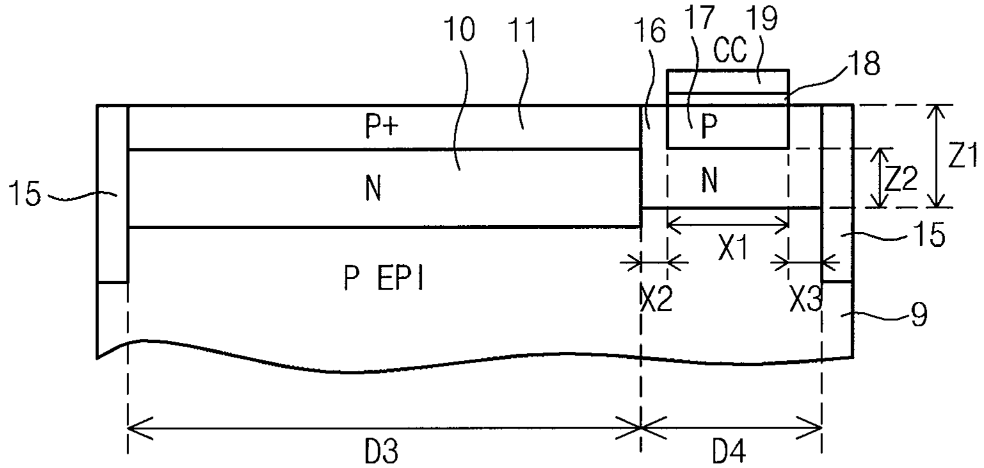

P+
N
P EPI
11
10
15
15
9
D3

FIG. 6


10
11
16
17
19
CC
18
P+
P
N
N
P EPI
15
15
9
Z1
Z2
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X2
X3
D3
D4

FIG. 7

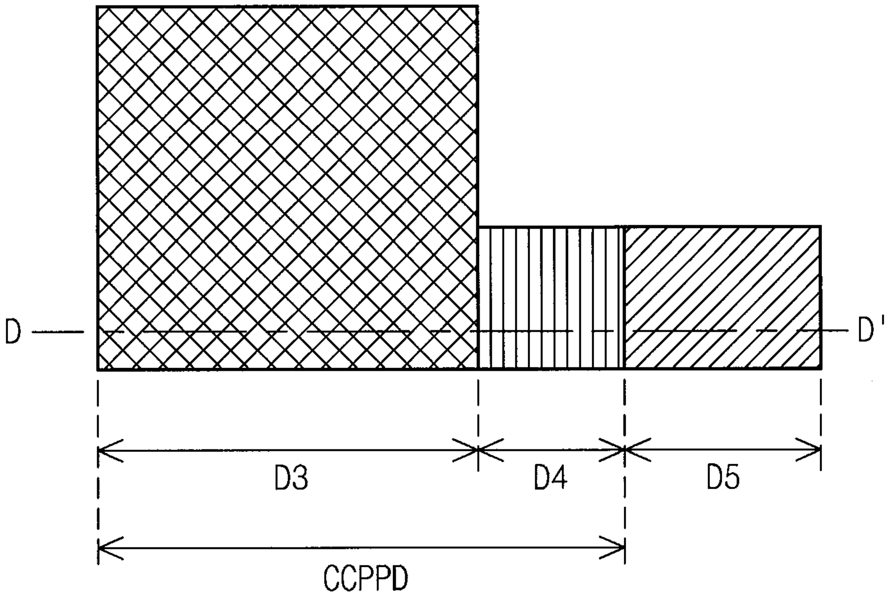
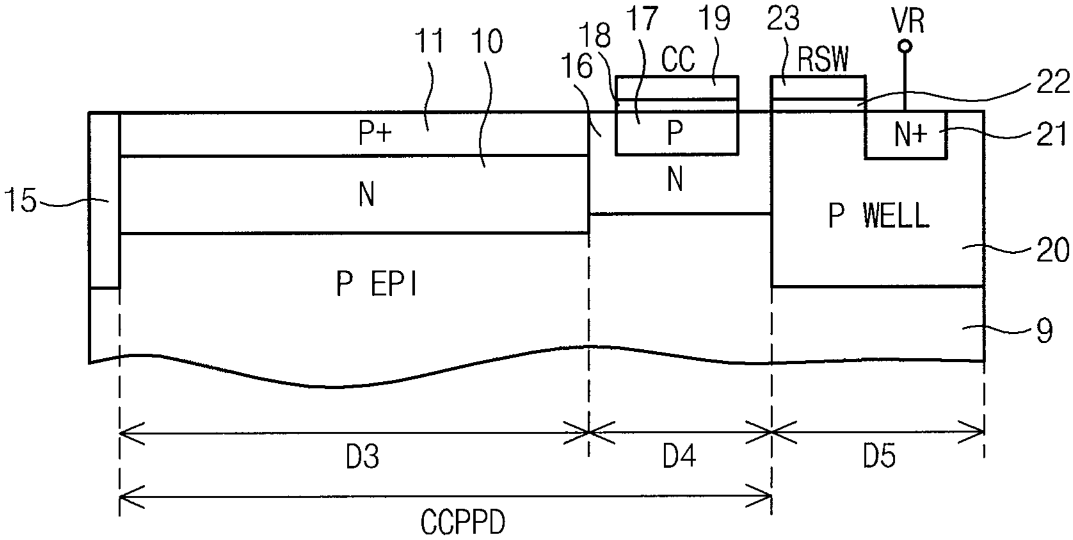

D
D'
D3
D4
D5
CCPPD

FIG. 8


11
10
18
17
CC
19
23
RSW
VR
16
22
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P
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21
15
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N
P WELL
20
P EPI
9
D3
D4
D5
CCPPD

FIG. 9

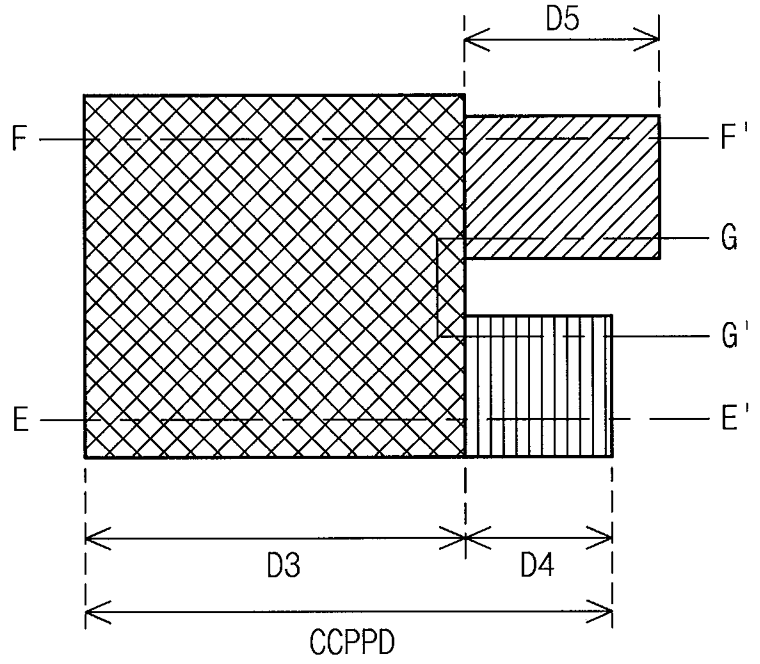

D5
F
F'
G
G'
E
E'
D3
D4
CCPPD

FIG. 10

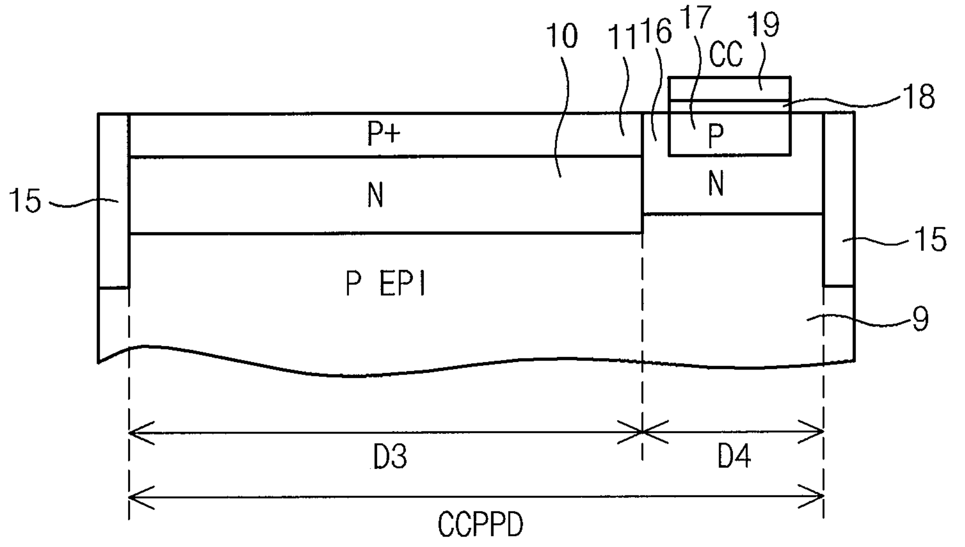
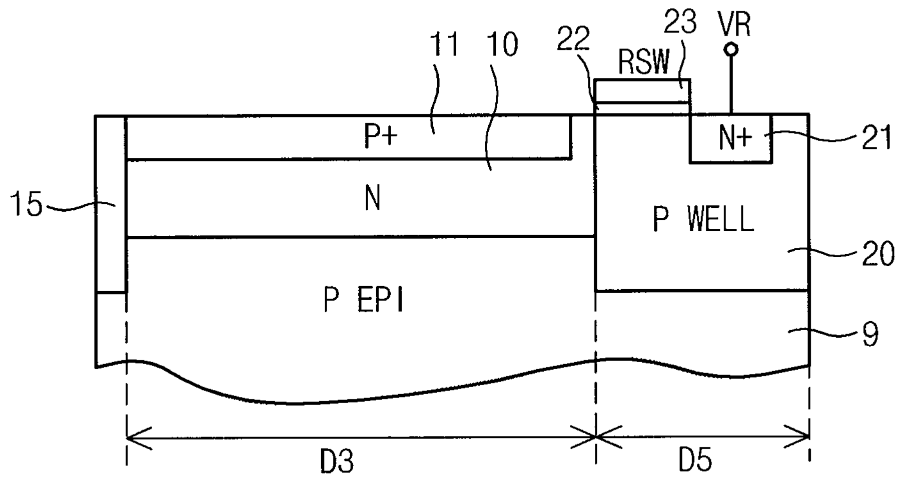

10
11
16
17
CC
19
18
P+
P
N
N
15
15
P EPI
9
D3
D4
CCPPD

FIG. 11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21
15
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P WELL
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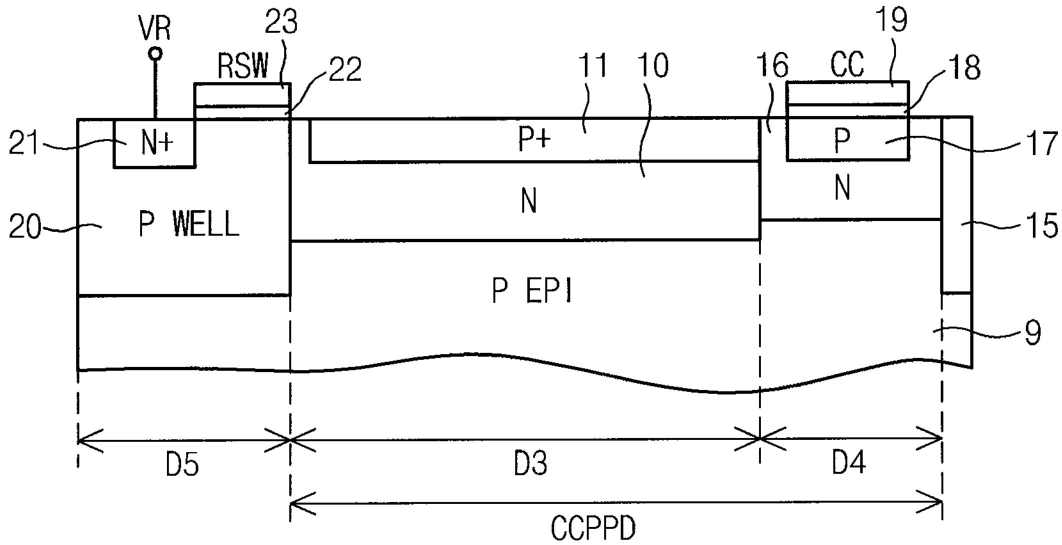
P EPI
9
D3
D5

FIG. 12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10
16
CC
19
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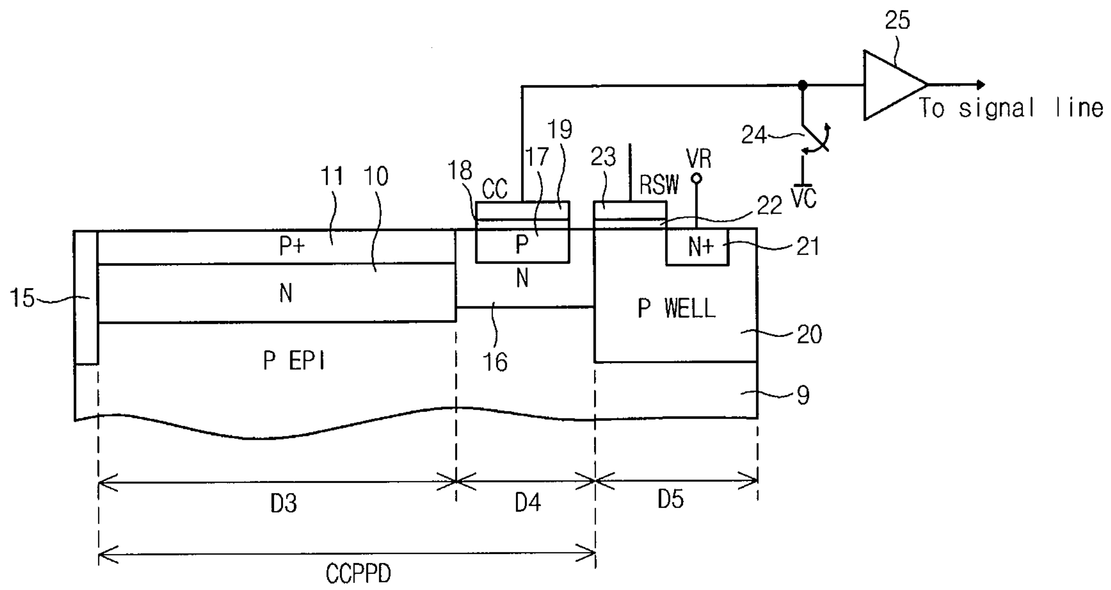
15
P EPI
9
D5
D3
D4
CCPPD

FIG. 13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To signal line
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VC
19
17
18
CC
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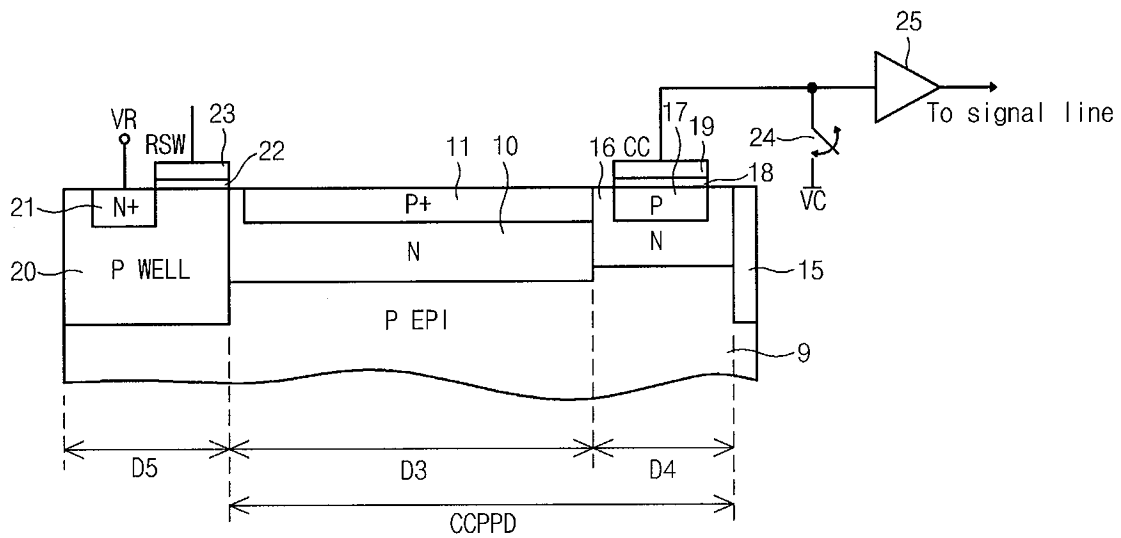
RSW
VR
22
11
10
P+
P
N+
21
15
N
N
P WELL
20
P EPI
16
9
D3
D4
D5
CCPPD

FIG. 14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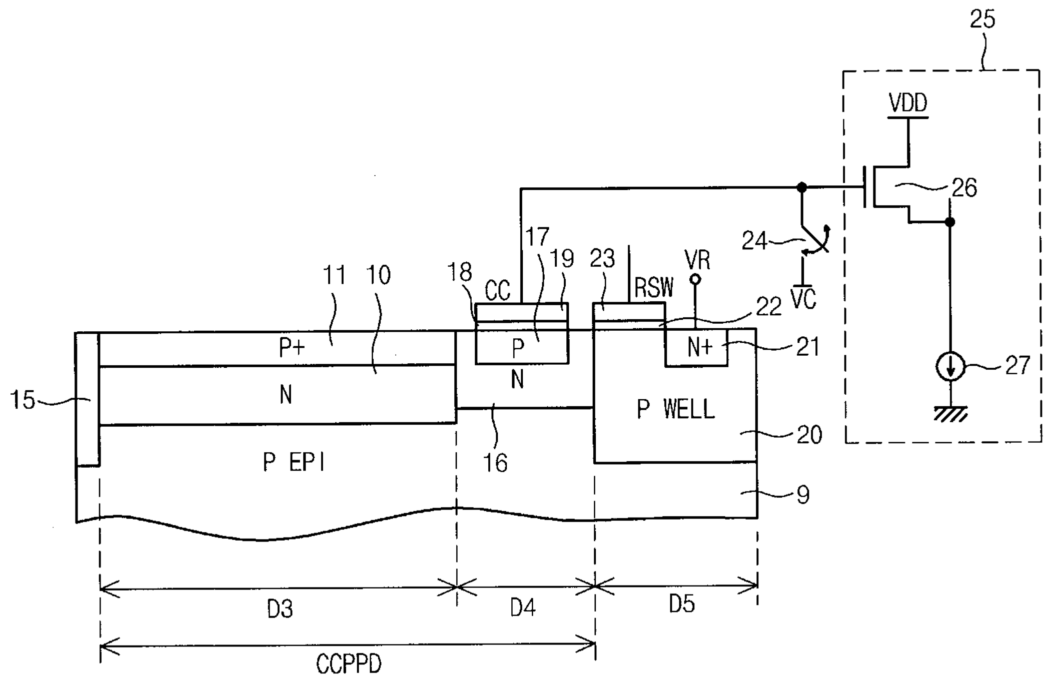
To signal line
VR
RSW
23
22
11
10
16
CC
17
19
24
18
VC
21
N+
P+
P
20
P WELL
N
N
15
P EPI
9
D5
D3
D4
CCPPD

FIG. 15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VC
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CC
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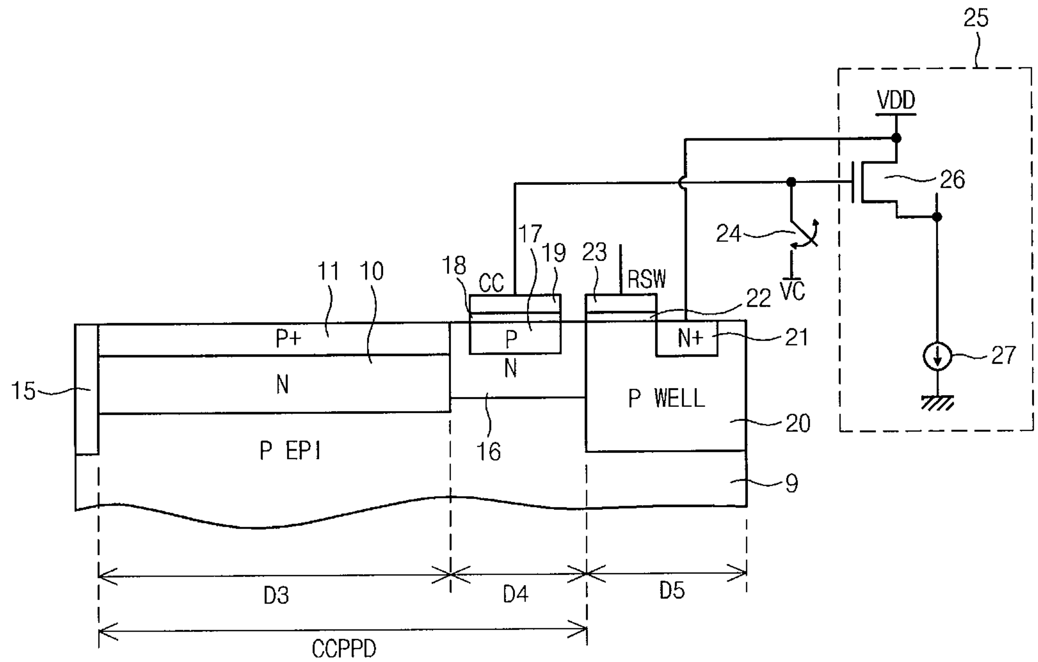
N
N
P WELL
20
16
P EPI
9
D3
D4
D5
CCPPD

FIG. 16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VC
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P+
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P EPI
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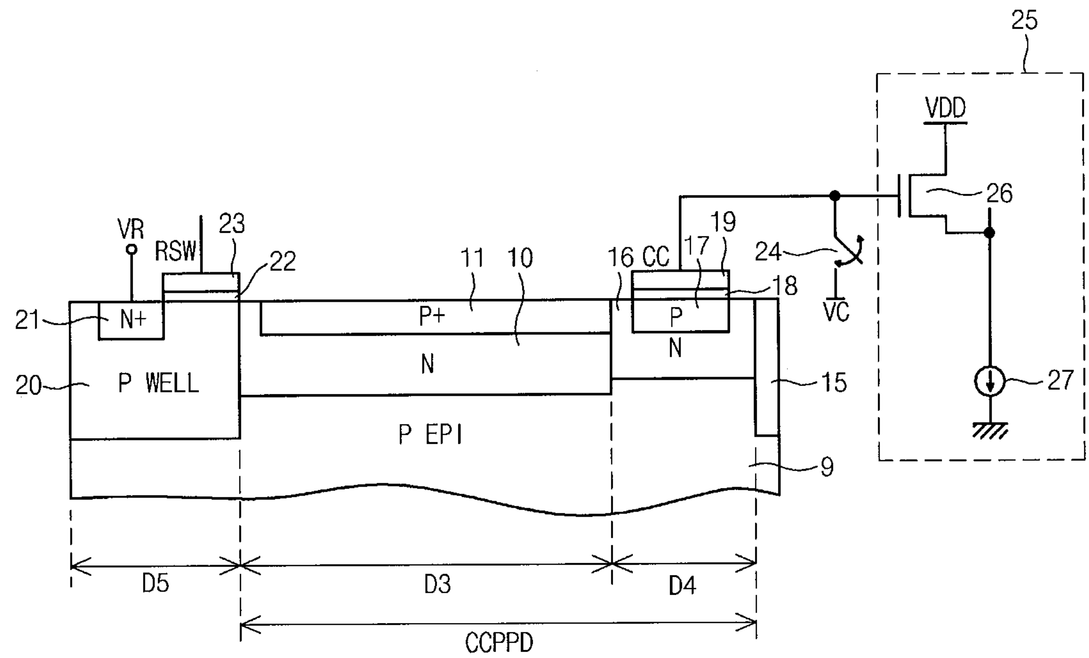
D3
D4
D5
CCPPD

FIG. 17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RSW
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P EPI
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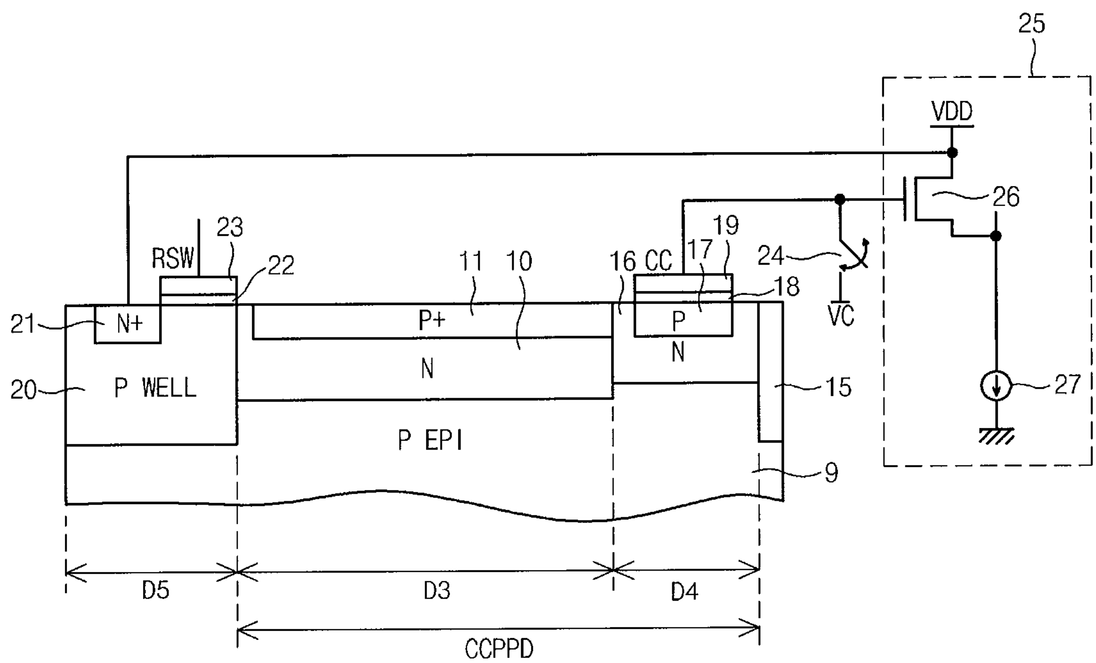
D5
D3
D4
CCPPD

FIG. 18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P+
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N
20
P WELL
N
15
P EPI
9
D5
D3
D4
CCPPD

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2006/004176

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/146(2006.01)i, H01L 31/10(2006.01)i, H04N 5/335(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC8 H01L27/146

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean Patents and applications for inventions since 1975
Korean Utility models and applictions for Utility models since 1975
Japanese Utility models and application for Utility models since 1975

Electronic data base consulted during the intertnational search (name of data base and, where practicable, search terms used)
e-KIPASS : "CMOS", "photodiode", "floating layer", "coupling capacitor", "dark current" , "switch", "amplifier"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 1020060090540 A (SAMSUNG ELECTRONICS CO., LTD.) 11 AUGUST 2006 See the abstract, figure 4b, claim 1-8	1-25
A	KR 1020030037871 A (HYNIX SEMICONDUCTOR INC.) 16 MAY 2003 See the abstract, figure 5, claim 1-15	1-25
A	JP 13-346104 A (NIKON CORP.) 14 DECEMBER 2001 See the abstract, figure 1, claim 1-7	1-25
A	US 6,051,447 A (Teh-Hsuang Lee, et al.) 18 APRIL 2000 See the abstract, column 4, line 36 - column 5, line 27, column 7, line 52- column 8, line 28, figures 3, 9	1-25

☐ Further documents are listed in the continuation of Box C.   ☒ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 FEBRUARY 2007 (22.02.2007)	**22 FEBRUARY 2007 (22.02.2007)**

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Korean Intellectual Property Office
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Republic of Korea
Facsimile No. 82-42-472-7140

Authorized officer
PARK, Keun Yong
Telephone No. 82-42-481-8508

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2006/004176

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR1020060090540	11.08.2006	KR20050086921A KR20050092782A KR20060090540A	30.08.2005 22.09.2005 11.08.2006
KR1020030037871	16.05.2003	NONE	
JP13346104 A	14.12.2001	NONE	
US06051447	18.04.2000	NONE	