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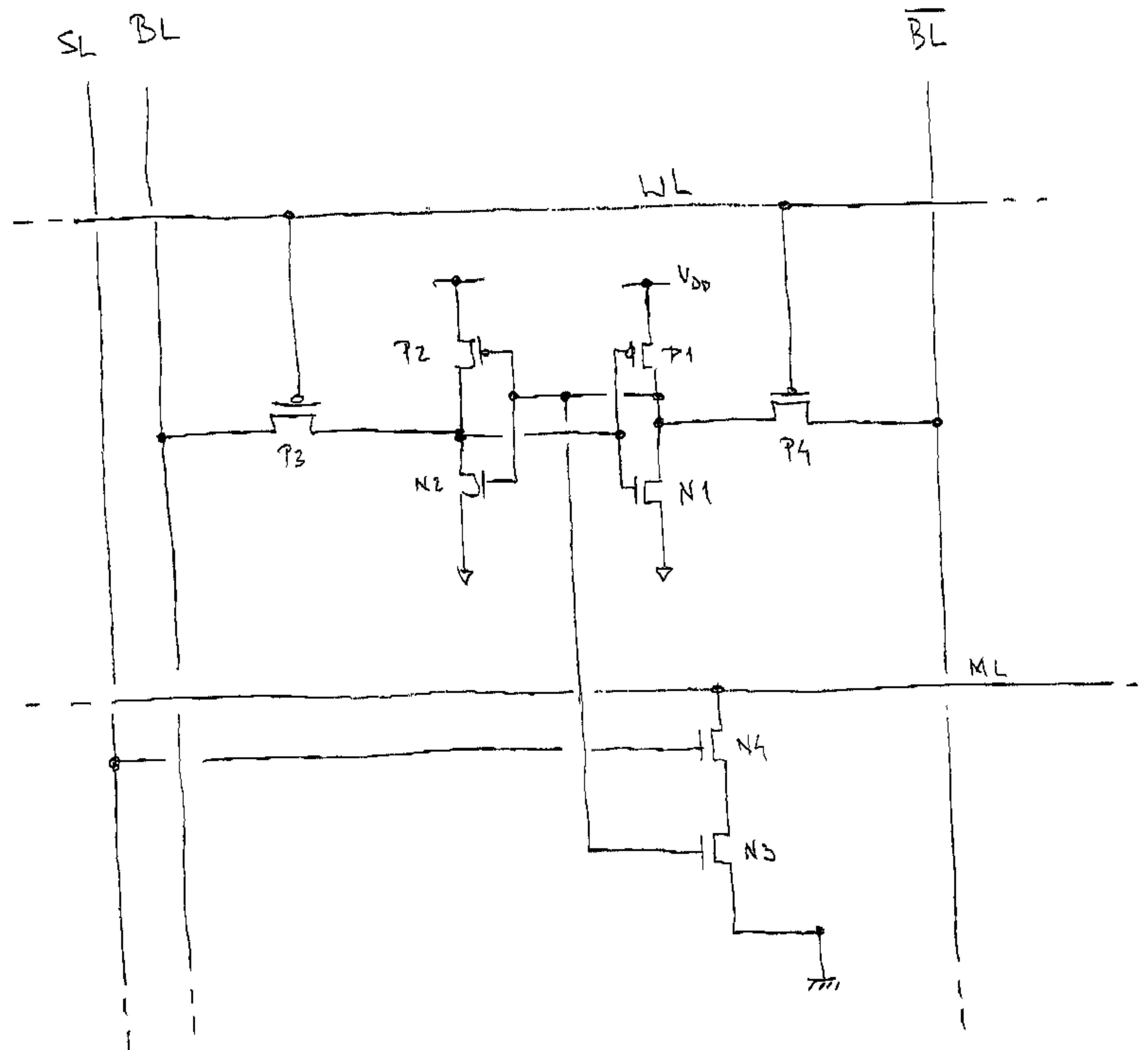
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(54) Titre : CELLULE DE MEMOIRE ADRESSABLE PAR CONTENU

(54) Title: CONTENT ADDRESSABLE MEMORY CELL



Content Addressable Memory Cell

BACKGROUND OF THE INVENTION

Conventional content addressable memory (CAM) has been implemented primarily using static
5 random access memory (SRAM) cells. SRAM-based CAMs have received widespread use due
to the high access speed of SRAM memory cells and the static nature of the cells. Furthermore,
SRAM cells can be manufactured using a pure-logic type fabrication process, that is, a process
commonly used for non-memory circuit blocks. DRAM-based CAMs have also been proposed
10 in the art. DRAM-based CAMs have the advantage of being able to store much more data than
SRAM-based CAMs for a given area due to the much smaller CAM cell size. However, because
of the dynamic nature of the DRAM cell, which is used to implement a DRAM-based CAM cell,
such cells require regular refresh operations in order to maintain the data.

SRAM-based CAM cells have been extensively discussed in the art. Current applications require
15 ternary CAMs which are capable of storing three logic states, for example, logic '0', logic '1'
and "don't care" states. Therefore, such CAM cells require two memory cells to store the logic
states, as well as a comparison-type circuit to compare stored data with search data provided to
the CAM. Some previous approaches in the art store data in a main memory cell and mask data
in a mask memory cell. The comparison circuit is then either enabled or disabled by the mask
20 memory cell contents. Examples of memory cells implementing such an approach is illustrated
by U.S. Patent No. 6,154,384, issued to Nataraj et al. and U.S. Patent No. 6,108,227 issued to
Voelkel. In ternary form using regular six transistor (6T) SRAM cells as storage elements,
SRAM-based CAM cells typically use 12 transistors to implement two 6T SRAM cells plus 4
transistors to implement an exclusive-NOR function for comparing search and stored data.

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The typical approach for implementing the memory cells is to use standard 6T SRAM cells.
That is, 2 p-channel transistors and 2 n-channel transistors in a cross-coupled inverter
relationship and a further 2 n-channel transistors as access devices from the bit lines.
Furthermore, for ternary CAM cells, n-channel devices are typically used in the comparison
30 circuit.

Although this approach is functional from a circuit point of view, difficulty arises when attempting to layout the elements of the CAM cells. The main problem is an imbalance between transistor types, leading to a non-optimized layout of the CAM cell. Out of the total of 16 transistors, only four are p-channel devices. Moreover, all n-channel devices in a cell need to be positioned in a common n+ diffusion. This includes the n-channel access devices, the n-channels of the cross-coupled inverters and the n-channels of the comparison circuit. The inevitable result is an unbalanced layout with regions containing the n-channels highly congested and wasted space around the two remaining p-channels used for the pull-up devices in the cross-coupled inverters.

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It is well known that because the n+ to p+ spacing rule is usually large relative to other rules in a typical CMOS fabrication process, and the n+ to p+ spacing cannot contain transistors therein, the aspect ration of the cell ends up being be narrow. That is, the smaller dimension of a typical cell will be in the direction of the line of the p-well separating n-channels and p-channels in the cell array. This minimises the area wasted in the p+ to n+ spacing. However, this too is made much more difficult given the imbalance between n-type and p-type devices in the conventional approach.

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Therefore, there is a need for an SRAM-based CAM cell that achieves a more efficient spatial layout than the prior art.

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BRIEF DESCRIPTION OF DRAWINGS:

Figure 1 is a circuit diagram of a ternary CAM half-cell according to an embodiment of the invention;

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Figure 2 is a circuit diagram of full ternary SRAM-based CAM cell according to one embodiment of the invention;

Figure 3 is a circuit diagram of full ternary SRAM-based CAM cell according to a second embodiment of the invention;

Figure 4 is a layout diagram of half-cell corresponding to circuit in figure 1.

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SUMMARY OF THE INVENTION

A new ternary SRAM-based CAM cell is disclosed which uses p-channel transistors as access transistors to the SRAM cells in order to improve the efficiency of the layout of the cell array.

The new implementation ensures a balanced number of p-channel and n-channel devices per cell
5 while still providing excellent functional characteristics.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A reduction in the ternary CAM cell area and optimization of the CAM cell layout is achieved by replacing the n-channel access devices used for the SRAM cells with p-channel access devices
10 and providing an active logic '0' activated word line instead of an active logic '1' activated word line. An SRAM cell with p-channel access devices is not normally used in regular SRAM due to the speed advantage of n-channel devices over p-channel devices. In a regular SRAM memory, the speed and other characteristics would suffer as a result. However, in a CAM cell, performance of the read/write is less critical since the main task which a CAM memory performs
15 on a regular basis is a search and compare function.

Using p-channel access devices instead of n-channel access devices results in a full ternary CAM cell with a more balanced number of p-channel transistors and n-channel transistors. It is preferable that the devices are balanced such that 8 n-channel devices and 8 p-channel devices
20 are used.

Referring to figure 1, a CAM half-cell in accordance with the invention is illustrated. The half-cell includes cross-coupled inverters P1, N1, P2, and N2 and p-channel access devices P3 and P4. The p-channel access devices P3 and P4 have their gates connected to a word line for
25 selectively connecting the cross-coupled inverters to complementary bit lines BL and \overline{BL} which carry read/write data. The output from the cross-coupled inverters P1, N1, P2, N2 is provided to an n-channel pull-down transistor N3 coupled to ground and to another n-channel transistor N4. Transistors N3 and N4 are coupled in series between a match line ML and ground. The gate of transistor N4 receives the search data via a search line SL. As can be seen from the devices in
30 figure 1, there are four p-channel transistors and four n-channel transistors making up the half-

cell as opposed to two p-channel transistors and six n-channel transistors as discussed regarding the prior art approach.

Referring to figure 2 a full ternary CAM cell in accordance with the invention is illustrated. The full ternary CAM cell comprises 8 p-channel transistors and 8 n-channel transistors. The transistors of the second SRAM cell component of the full ternary CAM cell have been numbered similarly to the corresponding transistors in figure 1 for ease of reference. It will be noted that there are two complementary bit line pairs, $BL1$, $\overline{BL1}$ and $BL2$, $\overline{BL2}$ and two search lines $SL1$ and $SL2$ accessing each full CAM cell.

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The general operation of the ternary CAM cell in figure 2 is now described. To perform a write operation, data to be stored in the CAM cell is loaded onto bit line pairs $BL1$, $\overline{BL1}$, and $BL2$, $\overline{BL2}$. The word line WL is asserted active logic '0' turning on p-channel access transistors P3, P4, P13 and P14. The data carried on the complementary bit line pairs is thereby written into the two SRAM cells and the word line is de-asserted.

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For a read operation, the complementary bit line pairs are precharged to $VDD/2$. The word line is asserted active logic '0' and the data from the SRAM cells is read onto the bit line pairs. The data then is transferred to data buses (not shown).

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For a search and compare operation search the match line is precharged to logic '1' and data is then placed on the search lines $SL1$ and $SL2$. Typically, search data and stored data are provided in such a manner that in the case of a mismatch, a more infrequent occurrence, a change occurs in the match line state. For example, if the match line is precharged to a logic '1', then a mismatch will discharge the match line to ground, whereas in the case of a match, a more frequent occurrence, no change occurs in the state of the match line.

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Therefore, if for example the CAM cell stores a logic '1' in the left SRAM cell and a logic '0' in the right SRAM cell illustrated in figure 2, and $SL1$ has logic '1' and $SL2$ has logic '0', this combination will result in a mismatch as follows. The output of the left SRAM cell will provide

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a logic '1' to transistor N4 and the search line SL1 will provide a logic '1' to transistor N3, thereby providing a path to discharge the match line ML to ground and thus indicate a mismatch.

If on the other hand, the CAM cell stores a logic '0' in the left SRAM cell and a logic '1' in the right SRAM cell, a match condition will result as follows. The output of the left SRAM cell will provide a logic '0' to the gate of transistor N4 while the search line SL1 will provide a logic '1' to the gate of transistor N3. As a result, no path to ground will exist between the match line ML and ground via transistors N3, N4. Similarly, the right SRAM cell will provide a logic '1' which will turn on transistor N14, and the search line SL2 will provide a logic '0' to transistor N13, which will be turned off. Therefore, once again, the path of transistors N13 and N14 will not provide a path to discharge the match line to ground. As a result, the match line will remain precharged to logic '1' indicating a match condition.

If a "don't care" state is stored in the CAM, that is a logic '0' in both the right and left SRAM cells in figure 2, then the output from each SRAM cell will produce a logic '0'. The logic '0' is provided to the gate of transistors N4 and N14 and therefore will ensure that no matter what data is provided on the search lines SL1, SL2, a match condition will be detected and the match line will remain unchanged.

This description of the basic operation only covers one possible match line detection scheme, however other approaches may be used as described in other co-pending MOSAID patent applications covering match line sensing circuits and methods.

Figure 3 illustrates an alternate embodiment of the invention with the access devices of the SRAM cells N23, N24, N33, N34 being n-channel devices and the transistors of the comparison circuit being p-channel devices P43, P44, P53, P54. The operation is similar to the operation of the embodiment of figure 2 with the appropriate voltages reversed for the devices that are different, as will be apparent to one skilled in the art.

Referring to Figure 4, there is shown a layout of a ternary CAM half-cell in accordance with the present embodiment, corresponding to the circuit shown in Figure 1. For convenience, the

transistor numbers of figure 1 are labelled on the corresponding areas in Figure 4. In the layout, the diagonally hashed lines enclose regions 100 representing active semiconductor areas (for example, diffusion or ion implanted areas), the squares with an X symbol therein represent metal contacts and the continuous lines enclose polysilicon layers 110 and the continuous lines
5 enclosing region 120 represent metal 1 layer. Other higher metal layers (there are 5 metal layers) are not included for simplification but will be included in a subsequent application.

As can be seen in figure 4 the p-channel devices are grouped at the top of the figure while the n-channel devices are grouped at the bottom, resulting in a well-balanced usage of cell area. The
10 compare circuitry is separated spatially from the access devices, which yields a well-packed efficient layout with a desirably narrow aspect ratio. As such according to the invention, only one p+ to n+ separation is necessary for the entire cell unlike prior art approaches which required at least two p+ to n+ separations. Competitive analysis reports demonstrate that prior art approaches using a 0.13um pure logic process end up with a cell size which is approximately
15 40% larger than the cell implemented using the present invention.

Advantages of the new layout described above include the connections to the search transistors being at the opposite end of the connections to the access transistors. This eases congestion in the upper layers of metal. Furthermore, the cell is close to the minimum width set by transistor
20 geometries, local interconnect (metal 1) and upper metals, all simultaneously. Minimum width and better aspect ratio again mean smaller area and reduce match line length, which is critical to speed and power.

Although the invention has been described with reference to specific embodiments, various
25 modifications will become apparent to a person skilled in the art with departing from the spirit of the invention.

SL BL

\overline{BL}

WL

V_{DD}

P2

P1

P3

P4

N2

N1

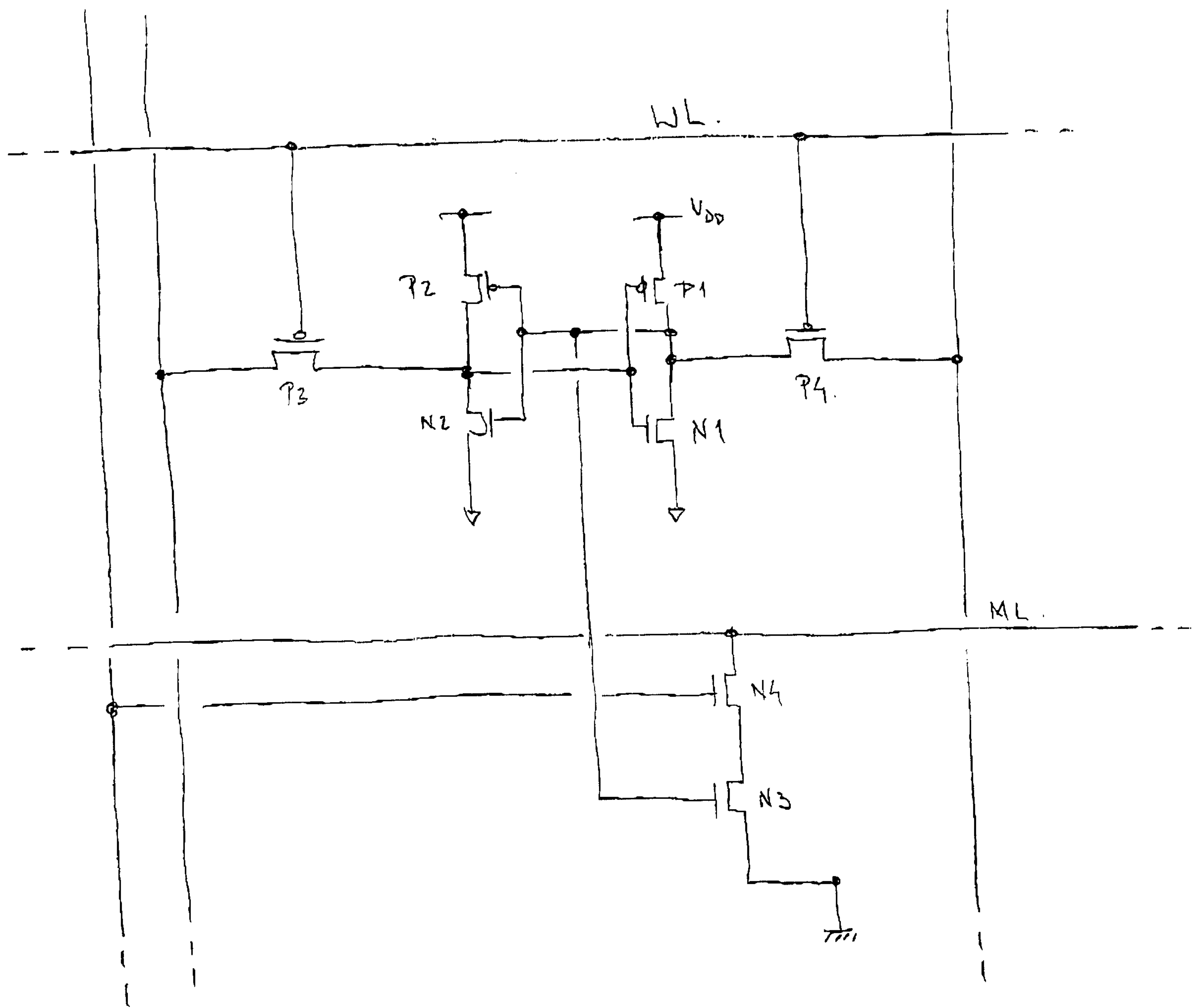
ML

N4

N3

GND

FIGURE 1



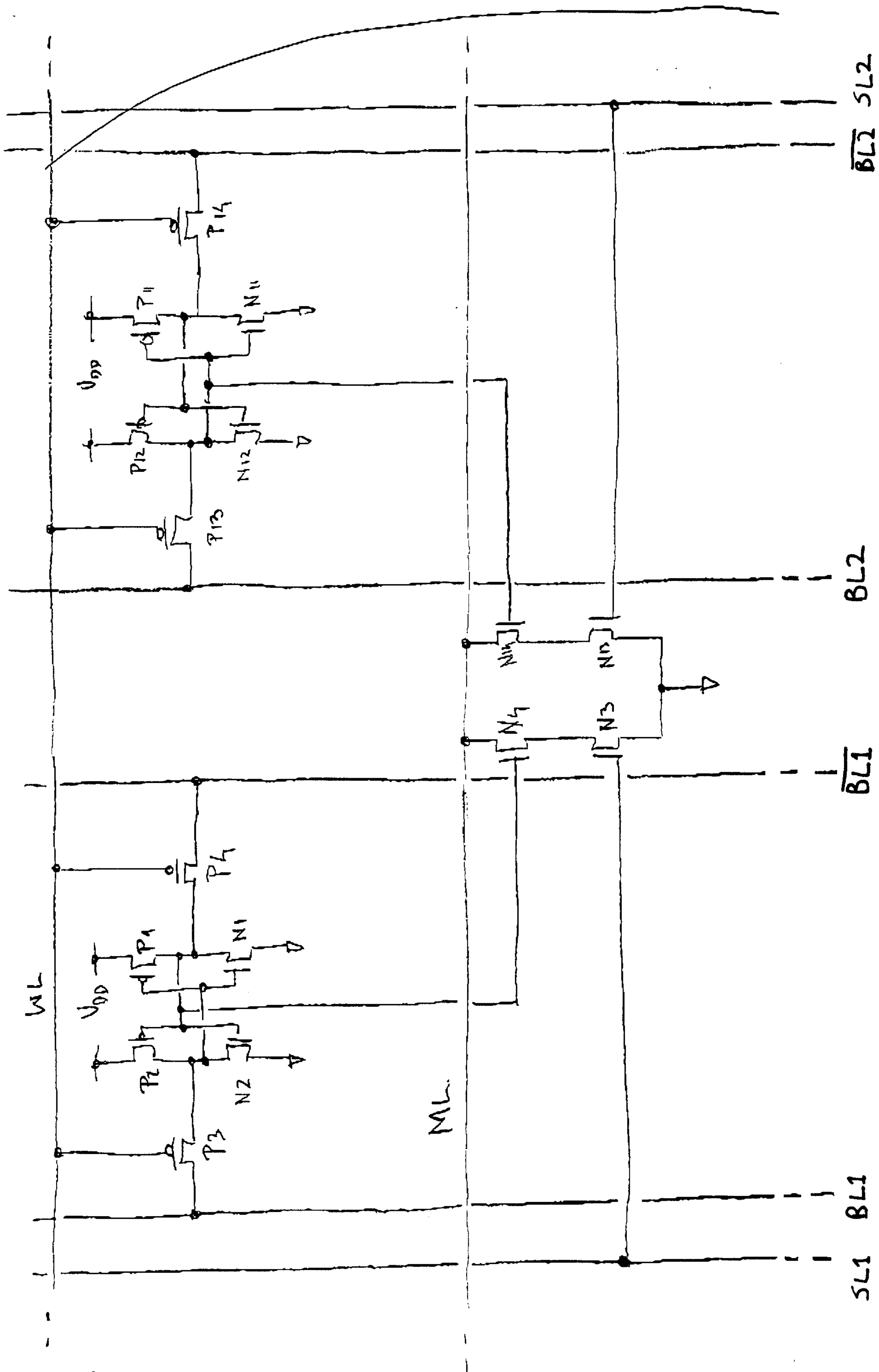


FIGURE 2

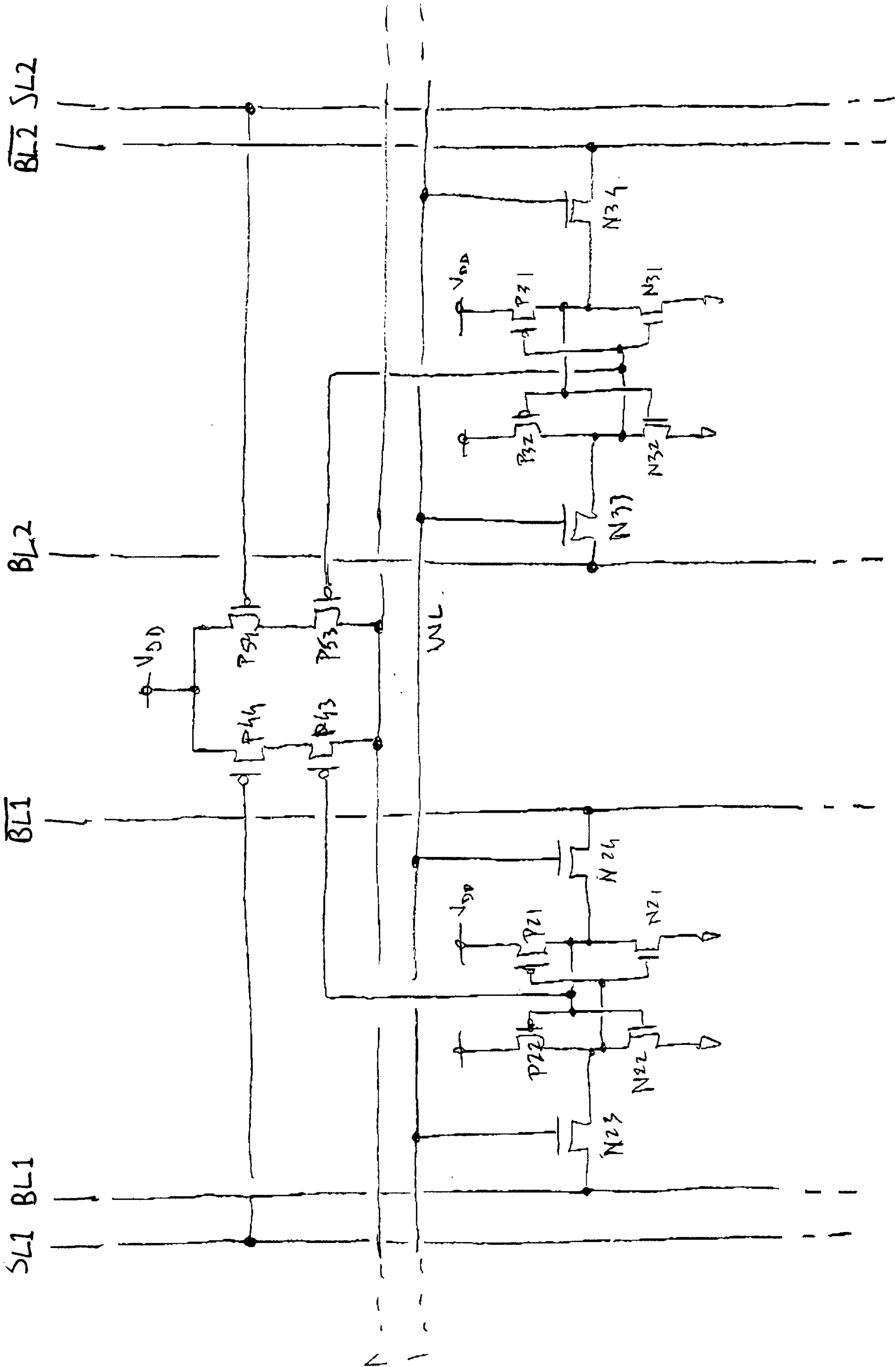


FIGURE 3

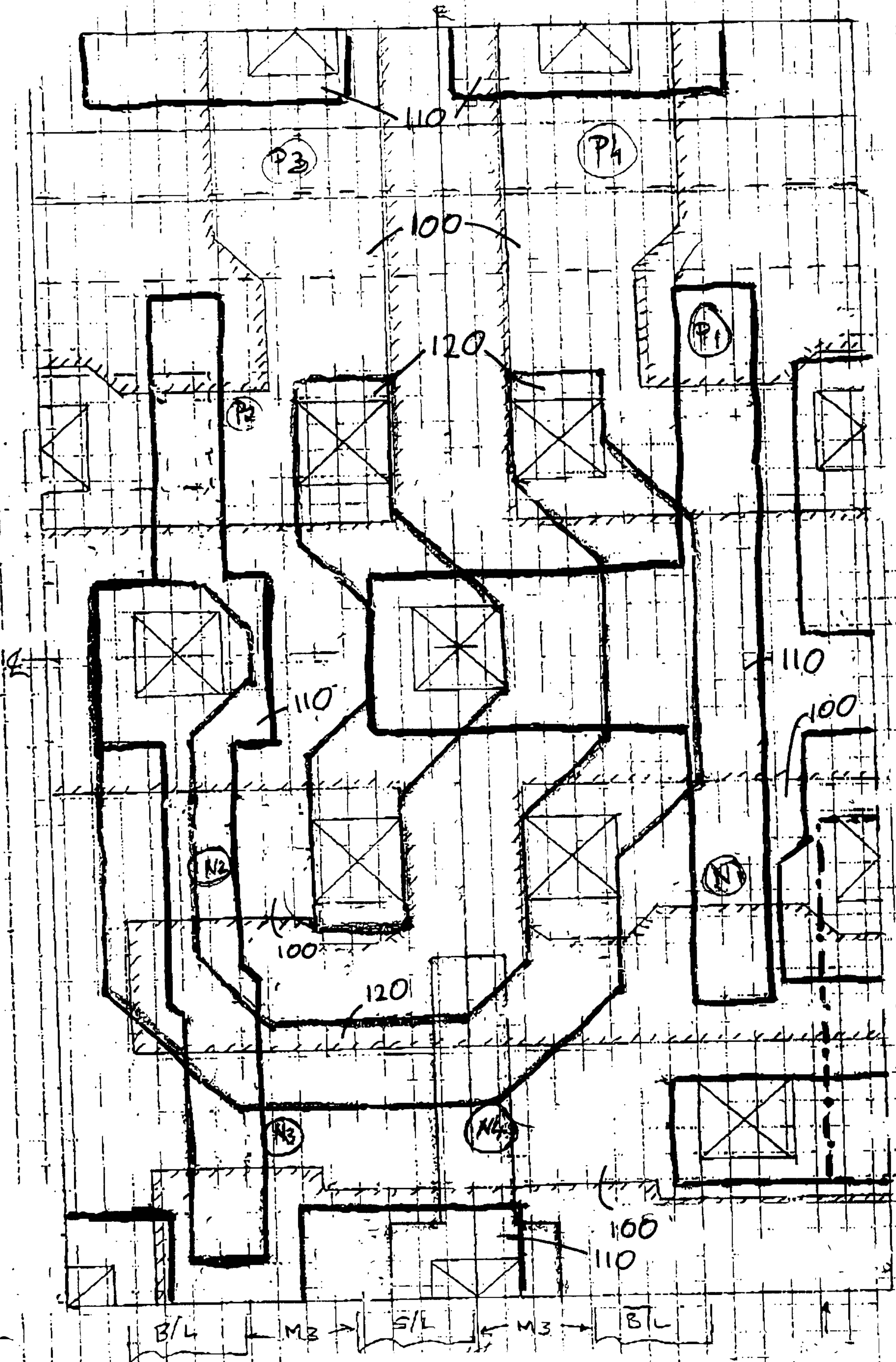


FIGURE 4

VOA
 -1-2001

SL BL

\overline{BL}

WL

V_{DD}

P2

P1

P3

P4

N2

N1

ML

N4

N3

GND

