A high speed pattern mass memory device for selecting and reading out any of character pattern information for printing or display from a mass information source including a number of different character patterns, in which all the handled character patterns are provided in a sequential-access mass-memory of low price while a rewritable random-access memory having an appropriate small memory capacity is provided as a second pattern memory connected to output so that the number of handled pattern information blocks different from one another is effectively increased in comparison with the small memory capacity of said random-access memory by transferring only different character patterns from the sequential-access mass-memory to the random-access mass memory in response to reference code units of an input data signal. The character patterns in the random-access memory are read out at a time by regenerating a train of the input data signal. Character patterns each having a high frequency in use may be fixedly stored in the random-access memory while only remainder character patterns other than the fixed character pattern are provided in the sequential-access mass memory and read out after temporarily storing to rewritable memory zones of the random-access memory.

2 Claims, 11 Drawing Figures
Fig. 1

Fig. 2
Fig. 3

Fig. 4
HIGH SPEED PATTERN MASS MEMORY DEVICE

This invention relates to a pattern memory for successively selecting and reading out pattern information in response to reference code units from a great number of pattern information and, particularly, to a pattern memory for selecting and reading out any of character pattern information for printing or display from a mass information source including a number of different characters, such as Japanese or Chinese.

In a case of printing or displaying in conventional arts a number of different characters including Chinese characters, such as Japanese, a great number of character patterns corresponding to all the handled characters are provided in a form of fixed memory in connection with display or printing circuitry. The fixed memory of this case is a mechanical type drum, a mechanical type belt, a photo-film, or a read only memory. In these fixed memories, a desired character pattern is simply selected in response to an input reference code unit and readout from the fixed memory for display or printing. Accordingly, a capacity of the character pattern memory is limited so that the number of handled different characters is also limited. In another system, a set of types (i.e. a font) can be changed or increased. However, increase of cost or adjustment time and troublesome handling cannot be avoided.

The number of handled characters can be increased on a large scale by use of a mass memory, such as a magnetic tape, magnetic drum or a magnetic disc. However, these mass memories are each a sequential access memory, so that readout times necessary for reading out desired information are not equal to one another and necessary reading out times are relatively longer than those of a random-access memory. Accordingly, the sequential-access mass memory cannot be applied to requirements for read out in a high speed an amount of pattern information blocks necessary for printing or displaying a line of pattern information blocks by way of example. On the other hand, while the random-access memory can be applied for requirements for readout in a high speed a small amount of pattern information blocks, it cannot handle a great number of pattern information, such as Japanese characters. In other words, about ten thousands character patterns which include Chinese characters of Mincho-style of about three to five thousands and remainders of Gothic-style are necessary for actual handling of Japanese. If a character pattern is representative of 1024 bits formed by 32 lines of 32 bits, all necessary bits are ten thousands times a total bits of the above 1024 bits and each necessary reference code unit. These great amount of necessary bits cannot be provided only in the form of a random-access memory.

An object of this invention is to provide a pattern memory capable of eliminating the above mentioned defects of conventional arts.

Another object of this invention is to provide a high-speed pattern mass-memory capable of readily changing the number of handled character patterns.

Further object of this invention is to provide a high-speed pattern mass-memory capable of reducing readout times by auxiliary and fixedly employing a random access memory for character patterns each having a high frequency in use.

In accordance with the principle of this invention, all the handled pattern information blocks are provided in a sequential-access mass-memory of low price, such as a magnetic disc pack or a magnetic tape, while a rewritable random-access memory having an appropriate small capacity is provided so that the number of simultaneously handled pattern information blocks different from one another is effectively increased in comparison with the small capacity of the random-access memory.

The principle, construction and operations of this invention will be understood from the following detailed discussion taken in conjunction with the accompanying drawings, in which the same or equivalent parts are designated by the same reference numerals, and in which:

FIG. 1 is a block diagram illustrating a fundamental construction of this invention;

FIGS. 2 and 7 are block diagrams each illustrating an example of a reference code comparator employed in this invention;

FIG. 3 is a block diagram illustrating an example of a pattern write-in control employed in this invention;

FIGS. 4 and 8 are block diagrams each illustrating an example of a pattern read-out control employed in this invention;

FIG. 5A shows a diagram illustrating the stored order of reference code units in a reference code memory employed in this invention;

FIG. 5B shows a diagram illustrating the stored order of reference code units in a data memory employed in this invention;

FIG. 5C shows diagram illustrating the order of addresses converted from reference code units of input data signals which are stored in a buffer register;

FIG. 5D shows a diagram illustrating an example of an input data signal; and

FIG. 6 is a diagram illustrating configuration of a pattern information block stored in a first pattern memory in this invention.

With reference to FIG. 1, the principle of this invention will first be described. Input data 11 are applied for printing or display from an information source, such as an electronic computer, a magnetic tape recorder or an communication channel, to a reference code comparator 20. The input data 11 is a train of reference code units and employed for selecting pattern information corresponding to the respective reference code units. The reference code comparator 20 examines whether or not each of the reference code units or the input data 11 is applied for the first time. If one of the reference code units is applied for the first time, it is stored in a reference code memory 30. In other words, only reference code units different from one another are stored in the reference code memory 30. In this case, the reference code units are stored in order of increasing number or decreasing number. The following explanation mainly relate to the increasing number.

When all empty memory zones of the reference code memory 30 are occupied by the different code units, an input data control signal 210 is sent out to an input data generator not shown, so that the input data 11 is stopped for a time. The input data 11 applied until this time have been stored in the data memory 40.
When a control signal 220 indicative of completion of the above mentioned examination of the reference code units is applied to a pattern write-in control 50 of a next stage, necessary pattern information are read out from a first pattern information memory 100, which is a circulating mass-memory employed for storing a number of necessary different pattern information, and written-in to a second pattern memory 70, which is a random-access memory having a sufficiently small capacity in comparison with the first pattern information memory 100. In other words, the reference code units stored in the reference code memory 30 are read out while the different pattern information each with a reference code unit are read out from the first pattern memory 100; and the pattern information blocks each having a reference code unit identified with one of the readout reference code units of the reference code memory 30 are successively stored in the second pattern memory 70.

In this case, addresses of the stored pattern information blocks in the pattern memory 70 are determined so as to correspond to the stored order of the reference code units in the reference code memory 30. In other words, the pattern information blocks from the pattern memory 100 are stored in the second memory 70 in the same stored order of the reference code units in the reference code memory 30.

When the above mentioned write-in operation of the pattern information blocks into the second pattern memory 70 are performed so as to correspond to all the reference code units of the reference code memory 30, a control signal 550 indicative of completion of selection of necessary pattern information blocks is applied from the pattern write-in control 50 to a pattern read-out control 60, so that the stored input data 410 are read-out from the data memory 40 and converted to addresses which are determined in accordance with the stored order of corresponding reference code units in the reference code memory 30 and employed for reading out corresponding pattern information blocks 710 from the second pattern memory 70.

As mentioned above, the input data 410 read out from the data memory 40 are successively processed and corresponding pattern information blocks 710 are sent out for displaying or printing. If the above operations are completed for all the readout input data 410 from the data memory 40, a control signal 620 indicative of termination of data is applied from the pattern read-out control 60 to the reference code comparator 20 so that the input data control signal 210 starts again the input data generator not shown. Accordingly, the input data 11 are again applied after the above mentioned stopped code unit to the reference code comparator 20 and the data memory 40 to perform the above mentioned operations.

By repeating the above mentioned operations, the pattern information blocks stored in the first pattern mass-memory 100 can be read out as a train of pattern information blocks in response to a section of the input data 11 from a stop point to an immediately stop point in accordance with the principle of this invention.

With reference to FIG. 2, construction and operations of an example of the reference code comparator 20 will be described below. In this case, while the maximum number of pattern information blocks to be stored in the second pattern memory 70 is usually equal to 1024 by way of example, it is assumed for simple explanation that the second pattern memory 70 has eight memory zones for eight pattern information blocks and the reference code memory 30 has eight memory zones for eight reference code units. Moreover, it is assumed that the input data signal 11 is a phrase of Japanese shown in FIG. 5D and having a meaning of "beautiful spring sunlight." Each of input data 11 is a number of four figures. FIG. 6 is an example of the pattern information block 130 which is stored in the first pattern memory 100 and formed by a reference code unit 131 and a pattern information part 132. The pattern information blocks 130 are stored in the first pattern memory 100 in order of increasing numbers of the reference code units 131.

In operation of the example shown in FIG. 2, a reference code "3013" indicative of a character pattern "L" (a main part of a meaning of "beautiful") is transferred to a register 21. A register 26, which comprises a counter, is at first reset to a state "0." The counting state of the register 26 indicates the number of reference code units stored in the reference code memory 30. Since the reference code unit "3013" of the input data signal 11 is decided as a first reference code unit in consideration of the state "0" of the register 26, the reference code unit "3013" is stored to a first zone 301 of the reference code memory 30 by the use of an address register 25 under control of a control 24. At the same time, the state of the register 26 is counted up to a state "1," which indicates that one reference code is stored to the reference code memory 30.

Next, a reference code unit "5021" representative of a character "L" (a first suffix of the meaning "beautiful") is transferred to the register 21. Since the state of the register 26 assumes the state "1," whether the reference code unit "5021" is an unstored reference code unit. Accordingly, the stored reference code unit "3013" is temporarily readout to a register 22, and contents A (i.e., 5021) of the register 21 is compared with contents B (i.e., 3013) of the register 22 at the comparator 23 so that a control signal indicative of a condition where the contents A are larger than the contents B is applied to the control 24. In response to the control signal from the comparator 23, the state of the address register 25 is set to a state "2" by the control 24 so that the contents A (5021) larger than the contents B (3013) are stored to the second memory zone of the reference code memory 30. Thereafter, the address register 25 is set to the state "1" so that the contents B (3013) of the register 22 is restored to the first memory zone of the reference code memory 30. At the same time, the state of the register 26 is counted up to the state "2."

As mentioned above, reference code units of the input data signal 11 are successively stored after the above comparison to the reference code memory 30. Accordingly, when an eleventh reference code unit "5021" representative of a character "L" is stored, eight reference code unit (1234), (1592), . . . and (5120) are arranged in order of increasing numbers as shown in FIG. 5A in the reference code memory 30.
The register 26 assumes a state "8," from which full occupation of the eight memory zones of the reference code memory can be detected by the control 24. At this time, a control signal 220 indicative of completion of the reference code comparison operation is applied to a control 56 described with reference to FIG. 3. In this case, the eleven reference codes (3013), (5021), \ldots and (5021) are arranged in the data memory 40 as shown in FIG. 5B.

With reference to FIG. 3, an example of the pattern write-in control 50 is provided for storing corresponding pattern information blocks from the first pattern memory 100 to the second pattern memory 70 in accordance with the eight reference code units, which are arranged in the reference code memory 30. The operation of the control 56 starts in response to the above mentioned control signal 220 from the control 24 of the reference code comparator 20 shown in FIG. 2. The state of an address register 55 is set to a state "1" for selecting the memory zone 301 of the reference code memory 30, so that the contents of the first memory zone 301 are read out and set to a register 52. Since the reference code units stored in the reference code memory 30 are as shown in FIG. 5A, a reference code (1234) representative of a character "\(\boxed{\text{sun}}\)" (a meaning of "sun") is readout to the register 52 from the memory zone 301. Next, a reference code 131 and a pattern information block 132 associated therewith are readout from the first pattern memory 100 in response to an access-signal 520 supplied from control 56. In this case, the reference code unit 131 is temporarily stored to a register 51, while the pattern information block 132 is temporarily stored in a pattern register 53. Respective contents C and D of the registers 51 and 52 are compared with each other. These comparison operations are repeatedly performed for reference code units, which are successively readout from the first pattern memory 100, until the contents C and D of the registers 51 and 52 coincide with each other. If the contents C and D of the registers 51 and 52 coincide with each other, a gate signal is applied from the control 56 to AND gates 57 and 58. The state "1" of the address register 55 passes through the opened AND gate 58 and is applied to the pattern memory 70 as a write-in address signal 540. On the other hand, the contents of the pattern register 53 pass through the opened AND gate 57 and are applied to the pattern memory 70 as a pattern information block 530. Accordingly, the pattern information block indicative of the character "\(\boxed{\text{sun}}\)" is stored to a memory zone of the address "1" in the second pattern information 70. Next, the state of the address register 55 is counted by "1," so that contents (1592) (i.e. representative of a character "\(\boxed{\text{spring}}\)" having a meaning of "spring") of the second memory zone 302 of the reference code memory 30 are read out and set to the register 52. Thereafter, contents of the memory zones of the first pattern memory 100 are successively scanned in the manner similar to the above mentioned operation for the first pattern information block "\(\boxed{\text{sun}}\)," so that the pattern information block "\(\boxed{\text{spring}}\)" is readout from the first pattern memory 100 and stored to the second memory zone of the second pattern memory 70.

As mentioned above, eight pattern information blocks corresponding to the above assumed eight reference code units are all selected from the first pattern memory 100 and stored to the second pattern memory 70. In other words, pattern information blocks corresponding to the reference code units shown in FIG. 5A are stored in the second pattern memory 70 in order of the arrangement shown in FIG. 5A. When write-in of the above pattern information to the pattern memory 70 is completed, a control signal 550 indicative of completion of the above pattern selection operation is sent to a control 66 shown in FIG. 4 mentioned below.

With reference to FIG. 4, an example of a pattern read-out control 60 is provided for reading out the pattern information blocks stored in the pattern memory 70 in accordance with the arrangement order of the reference code units stored in the data memory 40. The operations of the control 66 is started in response to the control signal 550 from the control 56 of the pattern write-in control 50 shown in FIG. 3. The contents of the data memory 40 are read out under control of an address register 64, so that the reference code unit 410 is set to a register 61. For the example shown in FIG. 5B, the reference code unit (3013) representative of a character "\(\boxed{\text{sun}}\)" having a meaning of "beautiful" is set to the register 61. The control 60 is access to the reference code memory 30 by the use of an address register 65, so that the reference code unit 302 is read out and set to a register 62. Respective contents E and F of the registers 61 and 62 are compared with each other at a comparator 63. These comparison operations are repeated until a coincidence between the contents E and F is obtained. If the contents E and F of the registers 61 and 62 coincide with each other, the contents of an address register 65 (i.e. a state "3" as understood from FIG. 5A since the reference code unit "3013" is stored in the third memory zone) is applied to a buffer register 68 through an AND gate 67. Next, a second reference code unit 410 representative of a character "\(\boxed{\text{sun}}\)" is readout to the register 61 as understood from FIG. 5B. In this case, an address number, to which the reference code unit 5021 is stored, is determined in a manner similar to the above mentioned operation so that a determined address "6" is applied to the buffer register 68. As mentioned above, all the reference code units stored in the data memory 40 are converted to corresponding address numbers, which are stored to the address register 68.

In FIG. 5C, contents of the buffer register 68 are shown as address numbers, which are converted from the contents of the data memory 40 shown in FIG. 5B in accordance with the contents of the reference code memory 30. Corresponding pattern information blocks 710 are successively readout from the pattern memory 70 in accordance with the contents of the buffer register 68 under control of the control 66.

When the pattern information blocks 710 are read out for all of the contents of the data memory 40, a control signal 620 indicative of completion of reading out is applied to the control 24 of the reference code comparator 20 shown in FIG. 2 from the control 66, so that a sequence of the above mentioned operations is again started.
In other words, a great number of different pattern information blocks exceeding over the capacity of the second pattern memory 70 (e.g. 1024 exceeding over the eight memory zones in the above example) can be handled by automatically performing repetition of three operations; the reference code comparison operation, the write-in operation of pattern information blocks, and the reading-out operation of pattern information blocks.

In the above example, the input data signal 11 is temporarily stored in the data memory 40. However, the data memory 40 may be eliminated, so that each of the reference code units of the input data signal 11 is twice generated at the reference code comparison operation and at the reading-out operation of pattern information blocks from an input information source not shown. In the above example, all pattern information blocks corresponding to the reference code units of the input data signal 11 are read out from the first pattern memory 100. However, pattern information blocks each having a high frequency in use may be stored in the second pattern memory 70 in advance except rewritable memory zones, so that the above mentioned operations are performed only for the rewritable memory zones of the second pattern memory 70 in accordance with this invention. In this case, the reference code units corresponding to the pattern information blocks fixedly stored in the second pattern memory 70 must be excluded from the above mentioned comparison operation in the reference code comparator 20, while the second pattern memory 70 is directly accessible by the pattern read-out control 60 without conversion to the address numbers. An example of this invention formed in accordance with this principle will be described with reference to FIGS. 7 and 8.

FIG. 7 is another example of input circuitry including the reference code comparator 20 to be contrasted with the example shown in FIG. 2. In FIG. 7, a decision circuit 27 is further provided before the reference code comparator 20 for comparing each of the reference code units of the input data signal 11 with reference code units corresponding to the fixed pattern and for generating a decision output only when the reference code unit of the input data signal 11 does not coincide with the reference code unit corresponding to one of the fixed pattern; and an AND gate 28 is further provided between the decision circuit 27 and the reference code comparator 20 for applying the input data signal to the reference code comparator 20 only when the decision output is generated from the decision circuit 27.

FIG. 8 is another example of pattern read-out circuitry including the pattern read-out control 60 to be contrasted with the example shown in FIG. 4. In FIG. 8, a distributor 601 is provided between the data memory 40 and the pattern read-out control 60 for distributing the output of the data memory 40 to fixed data 601B and variable data 601A respectively corresponding to the fixed pattern information blocks and other variable pattern information blocks. The variable data 601A is applied to the register 61, while the fixed data 601B is applied to the buffer register 68 through an OR gate 69. The output of the address register 65 is applied to one input of an AND gate which has the other input connected to a E=F output of the comparator 63, and the output of the AND gate 47 is applied to the OR circuit 69.

In another modification, the second pattern memory 70 is divided into a plurality of memory parts or comprises a plurality of memory parts, so that writing-in operations to the memory parts are alternately or successively performed while reading-out operations from the memory parts are alternately or successively performed for the memory parts different from the memory parts, to which the writing-in operation is now performed. As a result of this construction, a losttime between adjacent reading out times. However, the respective durations of reading out times must be equal to one another. Moreover, the data memory 40 must be divided into a plurality of memory parts, which are switched in synchronism with the switching of the memory parts of the pattern memory 70.

What we claim is:

1. A high speed pattern mass-memory device, comprising:
   a sequential-access pattern mass-memory for storing a plurality of different pattern information blocks each having a corresponding reference code unit,
   at least one random-access pattern memory for storing a plurality of different pattern information blocks the number of which is sufficiently smaller than the number of the different pattern information blocks of said sequential-access pattern mass-memory,
   input means for receiving an input data signal formed by a train of reference code units,
   comparison means coupled to the input means for detecting only different reference code units from said reference code units of the input data signal, said receiving of the input data signal being stopped when the number of said different reference code units reaches a predetermined number less than the number of memory zones in said random-access pattern memory,
   regeneration means coupled to said input means for regenerating said stopped input data signal,
   a reference code memory coupled to said comparison means for storing said different reference code units,
   pattern write-in control means coupled to said sequential-access pattern mass-memory, said comparison means and said reference code memory for reading out pattern information blocks corresponding to said different reference code units of said reference code memory from said sequential-access mass-memory and for writing-in said read-out pattern information blocks to said random-access pattern memory, and
   pattern read-out control means, coupled to said sequential-access pattern mass-memory, said random-access pattern memory, said comparison means, said regeneration means, said reference code memory and said pattern write-in control means, for temporarily storing address numbers corresponding to said reference code units of said stopped input data signal in accordance with established mutual relationship between said different reference code units of said reference code memory and address numbers of said pattern information blocks of said random access memory,
and for reading out at a time pattern information blocks corresponding to said reference code units of said input data signal from said random access pattern memory in the order of arrangement of said stored address numbers.

2. A high speed pattern mass-memory device according to claim 1, in which said random-access pattern memory comprises re-writable memory zones and fixed memory zones employed for fixedly storing fixed pattern information blocks each having a high frequency in use, and further comprising means coupled to said input means and said comparison means for deriving only reference code units corresponding to said pattern information blocks other than said fixed pattern information blocks and for applying said derived reference code units to said comparison means, and means coupled to said regeneration means and said pattern read-out means for directly employing reference code units of said input data signal corresponding to said fixed pattern information blocks as said address numbers used for reading-out said fixed pattern information blocks.

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