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(54) **A BUS ARRANGEMENT FOR A DRIVER OF A MATRIX DISPLAY**

BUSANORDNUNG FÜR ANSTEUERSCHALTUNG EINER MATRIXANZEIGEEINRICHTUNG

SYSTEME DE BUS POUR PILOTE D'AFFICHEUR

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Description

[0001] This invention relates generally to a bus arrangement for display devices and particularly to a system for applying brightness signals to pixels of a display device, such as a liquid crystal display (LCD) or a plasma display.

[0002] An arrangement according the state of the art is disclosed in US 5,170,158 A.

[0003] Display devices, such as liquid crystal displays or plasma displays, are composed of a matrix or an array of pixels arranged horizontally in rows and vertically in columns. The video information to be displayed is applied as brightness (gray scale) signals to data lines which are individually associated with each column of pixels. The rows of pixels are sequentially scanned and the capacitances of the pixels within the activated row are charged to the various brightness levels in accordance with the levels of the brightness signals applied to the individual columns.

[0004] Brightness information to be applied to the array of pixels may be formatted into M brightness information signals developed in M parallel brightness information carrying conductors, for example, M = 100. The M brightness information signals are applied to an input port of an input demultiplexer of the array. During each horizontal line interval of the video signal, the demultiplexer converts the M brightness information signals to MXN signals developed in MXN parallel conductors that are coupled via MXN data line drives to MXN column conductors of the array. The input demultiplexer may be formed by MXN thin film transistor (TFT's). Groups of M parallel conductors are successively selected, during each horizontal line interval of the video signal. The selection of each group of M parallel conductors is obtained by selection pulse signals developed in a bus of N parallel conductors.

[0005] The capacitance of the input busing structure associated with the N selection parallel conductors and the input busing structure associated with the M brightness information carrying parallel conductors can be a major source of both power dissipation and yield loss, especially for higher resolution self-scanned Active Matrix Liquid Crystal Displays (AMLCDs). Long metal runs across the display and multiple crossovers (Source/Drain metal-to-Gate metal) cause significant capacitive loads, resulting in both capacitance shorting failures, unwanted crosstalk among the brightness information carrying conductors and excessive dynamic power dissipation. It is desirable to reduce the number of crossovers of the input busing structure associated with the N selection parallel conductors and of the input busing structure associated with the M brightness information carrying parallel conductors.

[0006] The object is achieved by an arrangement according to claim 1.

[0007] Dependant claim relates to an advantageous embodiment.

FIGURE 1 illustrates an AMLCD with integrated driver circuits, according to an aspect of the invention, when incorporating the busing arrangement of FIGURE 2 and

FIGURE 2 illustrates a busing structure, in accordance with an aspect of the invention, that may be incorporated in the arrangement of FIGURE 1.

[0008] FIGURE 1 illustrates an integrated driver arrangement for storing information in an SVGA liquid crystal array. It should be understood that the invention may be utilized for storing information in pixels of a plasma display. Analog circuitry 11 receives a video signal representative of picture information to be displayed from, for example, an antenna 12. The analog circuitry 11 provides a video signal on a line 13 as an input signal to an analog-to-digital converter (A/D) 14.

[0009] The television signal from the analog circuitry 11 is to be displayed on a liquid crystal array 16 which is composed of a large number of pixel elements, such as a liquid crystal cell 16a, arranged horizontally in m = 600 rows and vertically in n = 2400 columns. Liquid crystal array 16 includes n = 2400 columns of data lines 17, one for each of the vertical columns of liquid crystal cells 16a, and m = 600 select lines 18, one for each of the horizontal rows of liquid crystal cells 16a.

[0010] A/D converter 14 includes an output bus 19-to provide brightness levels, or gray scale codes, to a memory 21 having 100 groups of output lines 22. Each group of output lines 22 of memory 21 applies the stored digital information to a corresponding digital-to-analog (D/A) converter 23. There are 100 D/A converters 23 that correspond to the 100 groups of lines 22, respectively. An output analog signal DBS(j) from a given D/A converter 23 is coupled via a corresponding brightness information carrying conductor DB(j) to a demultiplexer transistor MN1 associated with a corresponding column. Transistors MN1 may be thin film transistors (TFTs). The symbol (j) assumes values from 1 to 100 associated with the 100 D/A converter 23. Demultiplexer transistor MN1 applies the information of signal DBS(j) carried on corresponding brightness information carrying conductor DB(j) to a corresponding sampling capacitor C43 for storing an analog signal VC43 in capacitor C43. Signal VC43 is coupled to a corresponding data line driver 100 that drives corresponding data line 17 associated with a corresponding column.

[0011] A select line scanner 60 produces row select signals in lines 18 for selecting, in a conventional manner, a given row of array 16. The voltages carried in 100 data lines 17 are applied during a 32 microsecond line time to pixels 16a of the selected row.

[0012] The sampling in a given group of 100 signals DBS(j) of FIGURE 1 carried in brightness information carrying conductors DB(j) occurs simultaneously under the control of a corresponding data-word pulse signal DWS(i) forming a selection word. There are 24 pulse signals DWS(i), carried on 24 separate data-word conductors

DW(i), that occur successively during a 32 microsecond horizontal line time. The symbol (i) assumes values from 1 to 24 associated with the 24 separate conductors DW(i). Each pulse signal DWS(i) controls the sampling of a corresponding group of 100 signals DBS(j) in capacitors C43.

[0013] To provide an efficient time utilization, a two-stage pipeline cycle may be used. Signals DBS(j) are demultiplexed and stored in 2400 capacitors C43 by the operation of pulse signals DWS(i). Then, the information in capacitors C43 is transferred simultaneously to data line driver 100. Thus, capacitors C43 become available for the demultiplexing of the next row information, while the previous row information is applied to the pixels.

[0014] Except for the busing arrangement, as described later on, the circuitry of FIGURE 1 may operate, for example, similarly to that described in, for example, U. S. Patent No. 5,673,063 in the name of Sherman Weisbrod, entitled "A DATA LINE DRIVER FOR APPLYING BRIGHTNESS SIGNALS TO A DISPLAY". The busing arrangement of conductors DW(i) and DB(j), embodying an inventive feature, is explained in connection with FIGURE 2. Similar symbols and numerals in FIGURES 1 and 2 indicate similar items or functions.

[0015] As explained before, the crossover capacitance of the input busing structure associated with conductors DW(i) and DB(j) can be a major source of both power dissipation and yield loss, especially for higher resolution self-scanned Active Matrix Liquid Crystal Displays (AM-LCDs). Long metal runs across the display and multiple crossovers (Source/Drain metal-to-Gate metal) cause significant capacitive loads, resulting in both capacitance shorting failures, unwanted crosstalk among the brightness information carrying conductors, and excessive dynamic power dissipation. The busing arrangement of FIGURE 2 reduces the number of capacitive crossovers associated with the input bus structure thus reducing the power dissipation and improving yield.

[0016] Disadvantageously, the number of capacitive crossovers increases geometrically with the number of data-word conductors DW(i) according to the equation: number of crossovers = number of brightness information carrying conductors DB(j) x 1/2 x (number of data-word conductors DW(i)). It may be desirable to reduce the number of times conductors DWC(i) cross the bus of conductors DW(i) so as to reduce dynamic power dissipation and improve yield.

[0017] As shown in FIGURE 2, in a "cluster busing" bus structure, embodying an inventive feature, the brightness information carrying conductors DB(j), instead of being arranged individually and uniformly across the display, are grouped together into local "clusters" such as, for example, brightness information carrying conductors DB(1) - DB(4). The cluster of brightness information carrying conductors DB(1) - DB(4) are coupled to four transistors MN1 having gate electrodes that share, in common, conductor DW(24). In this example, the number of crossovers of brightness information carrying conductors DB(j)-to-data-word conductors DW(i) have been reduced by a factor of about 4 : 1. This, advantageously, reduces dynamic power dissipation, improves yield and reduces the crosstalk among the brightness information carrying-conductors.

[0018] The cluster busing arrangement adds a multiplicity of new local sub-arrays DBSA to the bus structure. Although these new local sub-arrays do add some additional crossovers of their own (2.5 per brightness information carrying conductor), this is a small price to pay for reducing the average number of crossovers in the main brightness information carrying conductor to data-word conductor matrix from 20/data-line to only 5/data-line. The total capacitive coupling in the input bus structure is thereby cut by a factor of approximately 4 using the cluster bus technique.

[0019] The primary advantages of cluster busing, therefore, include higher yield, lower power dissipation, and reduced crosstalk. However, another advantage to cluster busing is that we now break up the pattern of consecutive columns connected to a single signal DBS(j). Small errors in signal DBS(j)-to-signal DBS(j) will normally result in noticeable "block" errors because the human eye is very sensitive to large block patterns. Using the cluster bus technique, the blocks are broken-up into a finer pitch that is, advantageously, less obvious to the viewer.

[0020] Thus, whenever demultiplexing is done with a matrix of 2 signal types involving typically 20 or more lines, the structure may be improved through the addition of clusters of sub-arrays to reduce the complexity and capacitance of the main array.

Claims

1. An arrangement for transferring pixel information with respect to pixels arranged in columns and rows of an array (16) of a display device, comprising:

   a control bus (DW(1) ... DW(24)) for transmitting data-word pulse signals (DWS(i)), the control bus consisting of a plurality of data-word conductors (DW(i));

   a digital memory (21) to store brightness levels, and a plurality of groups of output lines (22), each group of output lines (22) arranged for applying the stored digital information to a corresponding digital-to-analog converter (23), where an output of each digital-to-analog converter (23) is connected to a conductor (DB(j)) for transferring the analog output signal of the connected digital-to-analog converter (23);

   where the conductors for transferring the analog output signal (DB(j)) are grouped to local cluster busses, said local clusters busses being separated from one another, each of said local cluster busses (DB(j)) having a first section extending

in a manner to cross said control bus (DW(1)...DW(24)) and a second section extending therefrom,
a plurality of semiconductor switches (MN1), each having a first terminal, a second terminal and a third terminal, where said first terminals are gates of the semiconductor switches (MN1) arranged to be controlled by one of said data-word pulse signals (DWS(i)),and said second terminals are sources being connected to one of the conductors for transferring the analog output signal (DB(j)),
and where said third terminal of each of said semiconductor switches (MN1) is coupled to an input terminal of a corresponding data line driver (100),
where a capacitor (C43) is connected with one terminal with ground and with the other terminal with the coupling of the third terminal and the data line driver (100) for storing the analog signal (VC43) transmitted on said coupling;
where said plurality of semiconductor switches (MN1) is separated into groups of semiconductor switches (MN1) and each of said groups is separated into subgroups of semiconductor switches (MN1), the semiconductor switches (MN1) of a given subgroup having the first terminals thereof coupled in common to a corresponding data-word conductor (DW(i)) and the third terminals thereof being coupled to consecutively disposed column conductors via said data line drivers (100), respectively, of said array (16), and where, for each local cluster bus, one of the second terminals of the semiconductor switches (MN1) per each subgroup of one of said groups of the semiconductor switches (MN1) is connected with a correspondent one of the conductors for transferring the analog output signal (DB(j)) of said local cluster bus;
and where each of the data-word conductors (DW(i)) is coupled to said first terminals of one respective subgroup per each of said groups of semiconductor switches (MN1) via a common extension conductor (DWC(i)), each of the common extension conductors (DWC(i)) crossing only once said local cluster bus (DB(j)) and once the connections of the second terminals of the semiconductor switches (MN1) of a subgroup with the second section of the corresponding local cluster bus (DB(j)).

2. The arrangement according to claim 1, **characterized in that** the data-word conductors (DW(i)) of said control bus extend along each of said plurality of semiconductor switches (MN1) to form a global bus arrangement.

Patentansprüche

1. Anordnung zum Übertragen von Pixelinformationen in Bezug auf Pixel, die in Spalten und Zeilen einer Anordnung (16) einer Anzeigevorrichtung angeordnet sind, wobei die Anordnung umfasst:

einen Steuerbus (DW(1) ... DW(24)) zum Senden von Datenwortimpulssignalen (DWS(i)), wobei der Steuerbus aus mehreren Datenwortleitern (DW(i)) besteht;
einen digitalen Speicher (21) zum Speichern von Helligkeitspegeln und mehrere Gruppen von Ausgangsleitungen (22), wobei jede Gruppe von Ausgangsleitungen (22) dafür ausgelegt ist, die gespeicherten digitalen Informationen an einen entsprechenden Digital/Analog-Umsetzer (23) anzulegen, wobei ein Ausgang jedes Digital/Analog-Umsetzers (23) mit einem Leiter (DB(j)) zum Übertragen des analogen Ausgangssignals des verbundenen Digital/Analog-Umsetzers (23) verbunden ist;
wobei die Leiter zum Übertragen des analogen Ausgangssignals (DB(j)) zu lokalen Cluster-Bussen gruppiert sind, wobei die lokalen Cluster-Busse voneinander getrennt sind, wobei jeder der lokalen Cluster-Busse (DB(j)) einen ersten Abschnitt, der in einer Weise, dass er den Steuerbus (DW(1) ... DW(24)) schneidet, und einen zweiten Abschnitt, der davon ausgeht, aufweist,
mehrere Halbleiterschalter (MN1), die jeweils einen ersten Anschluss, einen zweiten Anschluss und einen dritten Anschluss aufweisen, wobei die ersten Anschlüsse Gates der Halbleiterschalter (MN1) sind, die dafür ausgelegt sind, durch eines der Datenwortimpulssignale (DWS(i)) gesteuert zu werden, und die zweiten Anschlüsse Sources sind, die mit einem der Leiter zum Übertragen des analogen Ausgangssignals (DB(j)) verbunden sind, und wobei der dritte Anschluss jedes der Halbleiterschalter (MN1) mit einem Eingangsanschluss eines entsprechenden Datenleitungstreibers (100) gekoppelt ist,
wobei ein Kondensator (C43) mit einem Anschluss mit Masse und mit dem anderen Anschluss mit der Kopplung des dritten Anschlusses und des Datenleitungstreibers (100) zum Speichern des an der Kopplung gesendeten analogen Signals (VC43) verbunden ist;
wobei die mehreren Halbleiterschalter (MN1) in Gruppen von Halbleiterschaltern (MN1) getrennt sind und wobei jede der Gruppen in Untergruppen von Halbleiterschaltern (MN1) getrennt ist, wobei die ersten Anschlüsse der Halbleiterschalter (MN1) einer gegebenen Untergruppe gemeinsam mit einem entsprechenden

Datenwortleiter (DW(i)) gekoppelt sind und ihre dritten Anschlüsse jeweils über die Datenleitungstreiber (100) nachfolgend angeordneten Spaltenleitern der Anordnung (16) gekoppelt sind, und wobei für jeden lokalen Cluster-Bus einer der zweiten Anschlüsse der Halbleiterschalter (MN1) pro jeder Untergruppe einer der Gruppen der Halbleiterschalter (MN1) mit einem entsprechenden der Leiter zum Übertragen des analogen Ausgangssignals (DB(j)) des lokalen Cluster-Busses verbunden ist;
und wobei jeder der Datenwortleiter (DW(i)) über einen gemeinsamen Verlängerungsleiter (DWC(i)) mit den ersten Anschlüssen einer jeweiligen Untergruppe pro jeder der Gruppen von Halbleiterschaltern (MN1) gekoppelt ist, wobei jeder der gemeinsamen Verlängerungsleiter (DWC(i)) nur einmal den lokalen Cluster-Bus (DB(j)) und einmal die Verbindungen der zweiten Anschlüsse der Halbleiterschalter (MN1) einer Untergruppe mit dem zweiten Abschnitt des entsprechenden lokalen Cluster-Busses (DB(j)) schneidet.

2. Anordnung nach Anspruch 1, **dadurch gekennzeichnet, dass** die Datenwortleiter (DW(i)) des Steuerbusses entlang jedes der mehreren Halbleiterschalter (MN1) verlaufen, um eine globale Busanordnung zu bilden.

Revendications

1. Un système permettant de transférer des informations de pixel relatives aux pixels disposés en colonnes et en lignes d'un ensemble (16) d'un dispositif d'affichage, comprenant :

un bus de commande (DW(1)... DW(24)) permettant de transmettre des signaux de pulsation de mot de données (DWS(i)), le bus de commande comprenant une pluralité de conducteurs de mots de données (DW(i)) ;
une mémoire numérique (21) pour enregistrer des niveaux de luminosité, et une pluralité de groupes de lignes de sortie (22), chaque groupe de lignes de sortie (22) disposé pour appliquer les informations numériques enregistrées à un convertisseur numérique-analogique correspondant (23), où une sortie de chaque convertisseur numérique-analogique (23) est connectée à un conducteur (DB(j)) pour transférer le signal de sortie analogique du convertisseur numérique-analogique connecté (23) ;
où les conducteurs permettant de transférer le signal de sortie analogique (DB(j)) sont groupés sur les bus de grappe locaux, lesdits bus de grappe locaux étant séparés les uns des autres, chacun desdits bus de grappe locaux (DB(j)) présentant une première section qui s'étend de manière à traverser ledit bus de commande (DW(1)...DW(24)) et une seconde section qui s'étend à partir de celui-ci,
une pluralité de commutateurs semi-conducteurs (MN1), chacun présentant un premier terminal, un deuxième terminal et un troisième terminal, où lesdits premiers terminaux sont des portails des commutateurs semi-conducteurs (MN1) disposés pour être contrôlés par un desdits signaux de pulsation de mot de données (DWS(i)), et lesdits seconds terminaux sont des sources connectées à un des conducteurs pour transférer le signal de sortie analogique (DB(j)), et où ledit troisième terminal de chacun desdits commutateurs semi-conducteurs (MN1) est couplé à un terminal d'entrée d'un pilote de ligne de données (100),
où un condenseur (C43) est connecté à un terminal au sol et à l'autre terminal, au couplage du troisième terminal et du pilote de ligne de données (100) pour enregistrer le signal analogique (VC43) transmis sur ledit couplage ;
où ladite pluralité de commutateurs semi-conducteurs (MN1) est séparée en groupes de commutateurs semi-conducteurs (MN1) et chacun desdits groupes est séparé en sous-groupes de commutateurs semi-conducteurs (MN1), les commutateurs semi-conducteurs (MN1) d'un sous-groupe donné ayant les premiers terminaux de celui-ci couplés en commun à un conducteur de mot de données correspondant (DW(i)) et les troisièmes terminaux de celui-ci étant couplés aux conducteurs de colonne disposés de manière consécutive via lesdits pilotes de ligne de données (100), respectivement, dudit ensemble (16) et où, pour chaque bus de grappe local, un des seconds terminaux des commutateurs semi-conducteurs (MN1) par chaque sous-groupe de l'un desdits groupes des commutateurs semi-conducteurs (MN1) est connecté à un des conducteurs correspondants pour transférer le signal de sortie analogique (DB(j)) dudit bus de grappe local ;
et où chacun des conducteurs de mot de données (DW(i)) est couplé auxdits premiers terminaux d'un sous-groupe respectif par chacun des dits groupes de commutateurs semi-conducteurs (MN1) via un conducteur d'extension commun (DWC(i)), chacun des conducteurs d'extension communs (DWC(i)) traversant une seule fois lesdits bus de grappe local (DB(j)) et une seule fois les connexions des seconds terminaux des commutateurs semi-conducteurs (MN1) d'un sous-groupe avec la seconde section du bus de grappe local correspondant (DB(j)).

2. Le système selon la revendication 1, **caractérisé en ce que** les conducteurs de mot de données (DW(i)) dudit bus de commande s'étendent le long de chacune desdites pluralités de commutateurs semi-conducteurs (MN1) pour former un système de bus global.

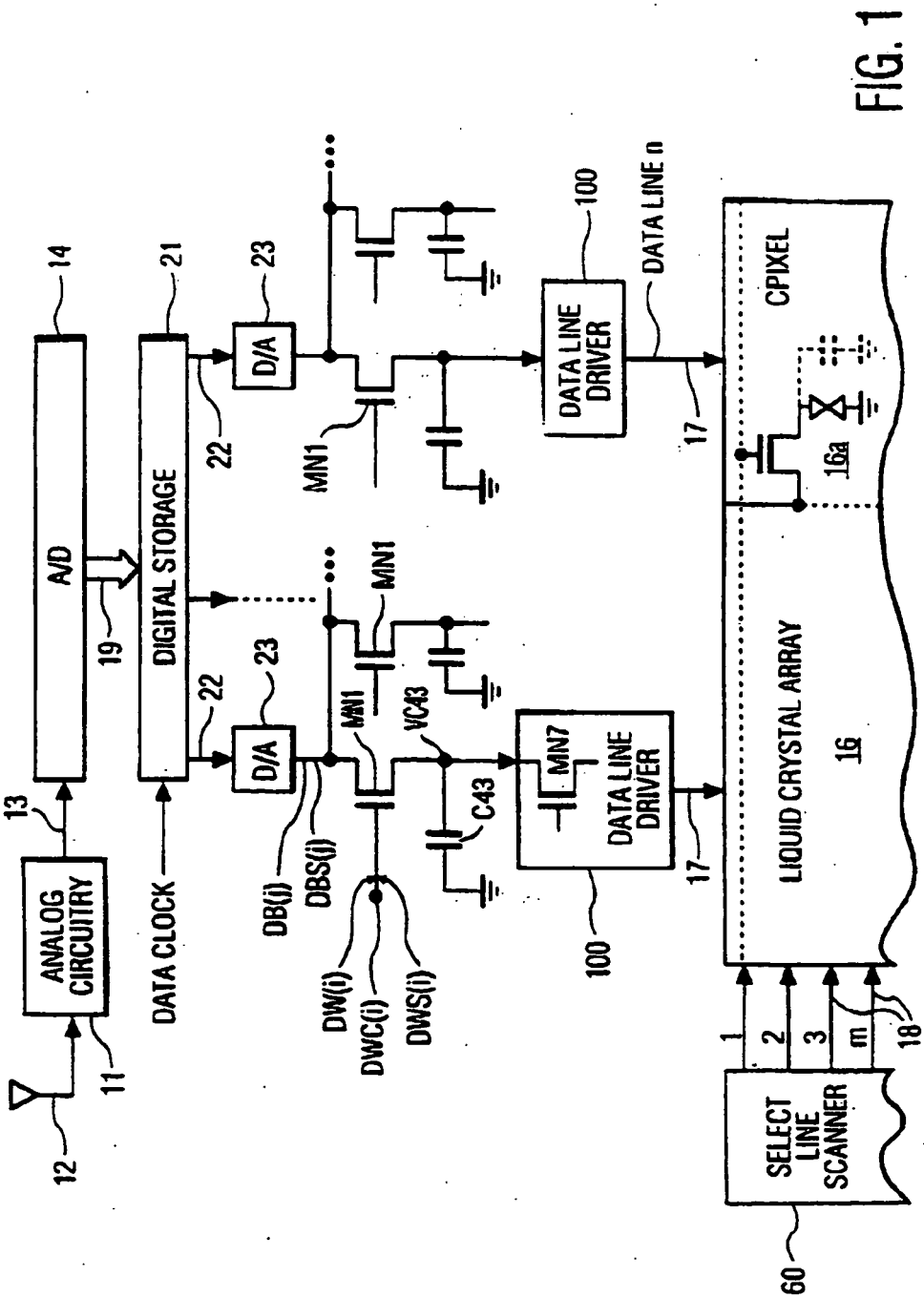
A/D
14
DIGITAL STORAGE
21
D/A
23
22
MN1
DATA LINE DRIVER
100
DATA LINE n
17
CPIXEL
16a
LIQUID CRYSTAL ARRAY
16
ANALOG CIRCUITRY
13
11
12
19
DATA CLOCK
DB(j)
DBS(j)
DW(i)
DWC(i)
DWS(i)
VC43
C43
MN7
1
2
3
m
18
SELECT LINE SCANNER
60

FIG. 1

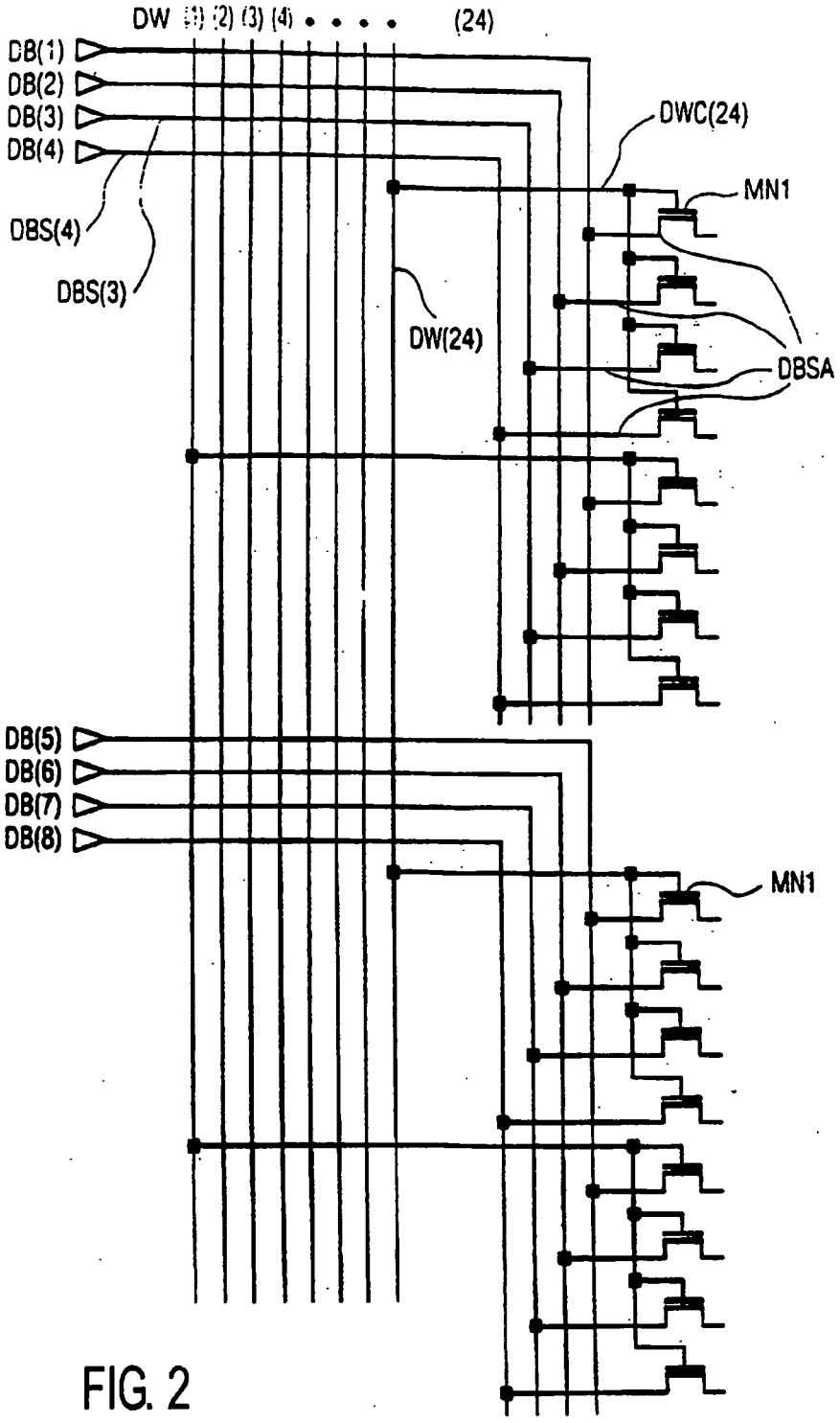
DW (1) (2) (3) (4) • • • • (24)
DB(1)
DB(2)
DB(3)
DB(4)
DBS(4)
DBS(3)
DWC(24)
MN1
DW(24)
DBSA
DB(5)
DB(6)
DB(7)
DB(8)
MN1

FIG. 2

REFERENCES CITED IN THE DESCRIPTION

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