(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 632 590 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
24.03.1999 Bulletin 1999/12

(51) Int Cl.[6]: **H03K 5/01**

(21) Application number: **94304699.5**

(22) Date of filing: **28.06.1994**

(54) **Glitch suppressor circuit and method**

Schaltung und Verfahren zur Unterdrückung von Störsignalen

Circuit et méthode de suppression des impulsions de bruit

(84) Designated Contracting States:
DE FR GB IT SE

(30) Priority: **30.06.1993 US 83517**

(43) Date of publication of application:
04.01.1995 Bulletin 1995/01

(73) Proprietor: **HARRIS CORPORATION**
Melbourne, FL 32919 (US)

(72) Inventor: **Dupre, Jean L.**
Braisbriand, Quebec J7H 1K1 (CA)

(74) Representative: **van Berlyn, Ronald Gilbert**
23, Centre Heights
London NW3 6JG (GB)

(56) References cited:
EP-A- 0 394 861
EP-A- 0 458 766
US-A- 4 775 840

EP 0 632 590 B1

Description

[0001] The present invention relates to the suppression of "glitches" ,i.e., those unwanted variations in control signals which result from contact bounce, interference of various types and/or noise.

[0002] Low voltage control signals are applied to semiconductor devices for myriad reasons, and an unwanted variation in such control signals often has serious adverse effects on the operation of the circuit. It is known to suppress these temporary variations by requiring that any change in the control signal appear for a predetermined finite period of time before it is recognized as a desired control signal and not as an undesired transient. By way of example, the specification of U.S. Patent No. 4,525,635 discloses the use of two bistable devices as a transient suppression circuit, with the two bistable devices used to sample the control signal at two different times and concurrence of the bistable devices required for propagation of the control signal into the circuit. In this way, the binary state of the control signal must remain constant over the two samples for the signal to be recognized as a control signal, and the glitch suppression circuit acts as a filter for transients having less duration than the two samples.

[0003] However, there are times when it is desired to bypass the glitch suppression circuit and to propagate the control signal directly into the circuit. Accordingly, an object of the present invention is to provide a novel circuit and method for selectively bypassing a glitch suppression circuit.

[0004] Another object is to provide a novel selectively bypassable glitch suppression circuit which can be integrated into the control lines for an operating circuit.

[0005] A further object is to provide a novel selectively operable transient filter circuit and method.

[0006] Yet another object is to provide a novel circuit and method which may be integrated into the design of a semiconductor device without regard to the desirability of the glitch suppression circuit in the application of the integrated circuit

[0007] Still another object is to provide a novel integrated circuit and method which contains a glitch suppression circuit in every input line and thus avoids any additional constraint from either temperature or process parameters on the operating circuit.

[0008] The invention is defined in Claim 1. The preamble portion of this Claim corresponds to the prior art disclosed in EP-A-0 394 861.

[0009] The invention will now be described, by way of example, with reference to the accompanying drawings in which:

[0010] Figure 1 is a schematic circuit diagram of a prior art glitch suppression circuit.

[0011] Figure 2 is a schematic circuit diagram of the selectively bypassable glitch suppression circuit.

[0012] Figure 3 is a functional block diagram of the bypassable glitch suppression circuit of the present invention integrated into a semiconductor chip.

[0013] Figure 1 shows the prior art glitch suppression circuits which typically contain two bistable devices or flip-flops which sample and store the state of a control signal at two different clock intervals. When the state of the control signal remains unchanged for the requisite time interval, a logic circuit provides an output signal to the operating circuit.

[0014] Figure 2 shows a glitch suppression circuit of the present invention which includes an input terminal 10 which receives a control signal and is connected to an input terminal of a first bistable device 12 which is sampled a time T1 by the application of a clock signal from an input terminal 14.

[0015] When toggled by the clock signal at time T2, the bistable device 12 provides an output signal which reflects the state of the control signal at time T1. This signal is applied to an input terminal of a second bistable device 16. At time T3, the clock signal causes the output state of the control signal at time T2 to be reflected as the output signal of the bistable device 12 and the output signal from the bistable device 16 to reflect the state of the control signal at time T1.

[0016] In the prior art circuits, a logic circuit responsive to the output signals from the two flip-flops provides the output signal of the glitch suppressor circuit. In this way, the glitch suppressor circuit provides an output signal only when the state of the control signal has remained unchanged for two successive clock cycles.

[0017] Figure 2 shows the output signals from the bistable devices 12 and 16 are applied to the two input terminals of an Exclusive OR ("XOR") gate 18 which provides a signal to the "Clear" input terminal CL of a third flip-flop 20.

[0018] The third flip-flop 20 is connected to function as a multiplexer for (a) the negative output signal from the bistable device 16 and (b) the output signal from the negative Q terminal of the flip-flop (through an inverter 26), and to treat the multiplexed signal as the input signal to terminal D of the flipflop 20.

[0019] The output signal from the OR gate 22 is applied to the CL input terminal and the output signal from the OR gate 24 is applied to the "Preset" input terminal PR of the flip-flop 20. Note in Figure 2 that the terminals CL and PR have been reversed for convenience in drafting. The output signal from the positive Q output terminal is applied through an inverter 28 as the output signal of the glitch suppressor circuit.

[0020] In this way, the glitch suppressor circuit of the present invention provides an output signal only when the state of the control signal has remained unchanged for two successive clock cycles.

[0021] Because there are control lines as to which no glitch suppressor is desired, and because there are times when a glitch suppressor is not desired for a control line, the circuit of the present invention provides for a selective bypass.

[0022] Figure 2 shows a reset signal may selectively

be applied by way of an input terminal 19 to one input terminal of two, two input terminal, OR gates 22 and 24. The control signal is applied to the other input terminal of the two OR gates 22 and 24, through an inverter 26 in the case of the OR gate 22. In this way, OR gate 22 provides an output signal in response to either a binary low control signal or a binary high reset signal, and OR gate 24 provides an output signal in response to either a binary high control signal or a binary high reset signal. As a result, an output signal from one of the two OR gates 22 and 24 will be provided for each transition of the control signal as well as a result of the application of a reset signal to the input terminal 19.

[0023] The output signals from the OR gates 22 and 24 are applied to complementary reset terminals (i.e., CL and PR) of both of the bistable devices 12 and 16 and the flip-flop 20 so that all three will be reset.

[0024] The glitch suppressor circuit thus becomes transparent to the control signal when a reset signal is present on the input terminal 19, and that the control signal as sampled during successive clock cycles will be propagated therethrough without the requirement that the state of the control signal remain the same for two clock cycles.

[0025] The number of bistable devices may be increased for any given clock signal to enlarge the time period over which the state of the control signal must remain constant to be recognized as such.

[0026] The bistable devices and gates referenced herein may be any suitable conventional circuits capable of performing the functions indicated. In addition, other functionally equivalent circuits may be employed. Even where the same circuit elements are used, the connections may be varied, with the addition or deletion of inverters, to balance the use of positive and negative gong output signals, etc.

[0027] In the design and manufacture of integrated circuits, it has heretofore not been practical to incorporate glitch suppressor circuits in the control lines because of the flexibility needed for such ICs, both as to the decision as to whether such a suppressor was needed on a control line at all, and if so, as to when such suppressor was desired. As shown in Figure 3, the present invention permits the integration of the glitch suppressor circuit 30 of the present invention into each control line 32 of an integrated circuit 34 without regard for such considerations, with knowledge that the decision as to whether and when to include may be later resolved by the selective application of a simple reset signal. By designing the glitch suppressor circuits into each control line 32 of the IC 34, the cost of the glitch suppressor circuit is significantly reduced.

[0028] As shown in Figure 3, three input lines are provided to each of the glitch suppressor circuits, i.e., one each for the control signal, clock and reset signal. Of course, the clock signal may be provided from one or more sources internal of the IC 34 and the necessity for the third external connection thus obviated.

[0029] When designed into an IC, the glitch suppressor circuit of the present invention may be used as a filter, to reduce the noise sensitivity of a circuit, to debounce switch contacts thus permitting direct connection to the IC, and to suppress the effects of sampling during transition of the control signal due to a lock of synchronism between the clock and control signals.

[0030] Further, the integration of the glitch suppression circuit into the IC subjects it to the same process parameters during manufacturing and subjects it to the same temperature conditions during operation. Thus the glitch suppression circuit imposes no constraints on the IC.

[0031] A resettable glitch suppression circuit integrated into each input control line of a semiconductor chip to provide flexibility for each control line as to whether or not, and if so when, the glitch suppression circuit is operable.

Claims

1. A glitch suppression circuit comprising a first bistable device for receiving a control signal to provide a first output signal related to the state thereof at a time T2, a second bistable device for receiving said first output signal and to provide a second output signal related to the state of said first output signal at a time T1, a third bistable device, means for applying successive clock cycles to said first, second and third bistable devices, means to provide a third output signal for application to said third bistable device when the state of said first and second output signals changes between the times T1 and T2, reset means, operable independently of the state of said control signal for setting said first, second and third bistable devices to a predetermined state so that the state of the control signal when sampled during each clock cycle may be propagated therethrough, characterized in that one or more operating circuits each have one or more control signal lines, the glitch suppression circuit being located in each of said control lines, each of said glitch suppression circuits including bypass means and a bypass control line for selectively bypassing the glitch suppression function in response to the application of a signal to the control line thereof.

2. A circuit as claimed in claim 1, characterised by a control signal applied to the first of a plurality of series connected bistable devices logically connected together to provide an output signal only when the state of the control signal remains unchanged for a number of clock cycles equal to the number of series connected bistable devices, the method of selectively bypassing the function of the circuit comprising the steps of selectively resetting each of the bistable devices during each of the clock cycles

whereby the output signal from the last of the binary devices during successive clock cycles represents the state of the control signal during successive clock cycles.

3. A circuit as claimed in claim 2, characterized in that said glitch suppression circuit includes three or more resettable bistable devices.

Patentansprüche

1. Schaltung zur Unterdrückung von Störsignalen, bestehend aus einem ersten bi-stabilen Bauteil zum Empfang eines Steuersignals, um ein erstes Ausgangssignal zu liefern, das sich auf seinen Zustand zu einem Zeitpunkt T2 bezieht, einem zweiten bistabilen Bauteil zum Empfang des ersten Ausgangssignals, um ein zweites Ausgangssignal zu liefern, das sich auf den Zustand des ersten Ausgangssignals zu einem Zeitpunkt T1 bezieht, einem dritten bi-stabilen Bauteil, Mitteln zum Anlegen aufeinanderfolgender Taktzyklen an das erste, das zweite und das dritte bi-stabile Bauteil, Mitteln zum Erzeugen eines dritten Ausgangssignals zum Anlegen an das dritte bi-stabile Bauteil, wenn der Zustand des ersten und zweiten Ausgangssignales sich zwischen den Zeitpunkten T1 und T2 ändert, unabhängig von dem Zustand des Steuersignals arbeitende Rückstellmittel zum Einstellen des ersten, des zweiten und des dritten bi-stabilen Bauteils auf einen vorbestimmten Zustand, so daß der Zustand des Steuersignals, wenn es während jedes Taktzyklus abgetastet wird, durch diese hindurch übertragen werden kann, **dadurch gekennzeichnet,** daß eine oder mehrere im Betrieb befindliche Schaltungen jeweils einen oder mehrere Steuersignalleitungen besitzen, wobei die Schaltung zur Unterdrükkung von Störsignalen sich in jeder dieser Steuersignalleitungen befindet und jede der Schaltungen zur Unterdrückung von Störsignalen Bypassmittel und eine Bypass-Steuersignalleitung zum selektiven Umleiten der Störsignal-Unterdrückungsfunktion in Abhängigkeit vom Anliegen eines Signals an der Steuersignalleitung besitzt.

2. Schaltung nach Anspruch 1, **gekennzeichnet durch** ein an das erste von mehreren in Reihe geschalteten bi-stabilen Bauteilen angelegtes Steuersignal, die logisch miteinander verbunden sind, um ein Ausgangssignal zu liefern, nur wenn der Zustand des Steuersignals während einer Anzahl von Taktzyklen unverändert bleibt, die gleich der Zahl der in Reihe geschalteten bi-stabilen Bauteile ist, wobei das Verfahren zum selektiven Umleiten der Funktion der Schaltung darin besteht, daß jedes der bi-stabilen Bauteile während jedes Taktzyklus selektiv zurückgestellt wird, wodurch das Ausgangssignal des letzten der bi-stabilen Bauteile während aufeinanderfolgender Taktzyklen den Zustand des Steuersignals während aufeinanderfolgender Taktzyklen repräsentiert.

3. Schaltung nach Anspruch 2, **dadurch gekennzeichnet,** daß die Schaltung zur Unterdrückung von Störsignalen drei oder mehr zurück- bzw. neu einzustellende bi-stabile Bauteile aufweist.

Revendications

1. Circuit de suppression d'impulsions de bruit comprenant un premier dispositif bistable pour recevoir un signal de commande afin de fournir un premier signal de sortie concernant son état à l'instant T2, un second dispositif bistable pour recevoir ledit premier signal de sortie et pour fournir un second signal de sortie concernant l'état dudit premier signal de sortie à l'instant T1, un troisième dispositif bistable, des moyens pour appliquer des cycles d'horloge successifs auxdits premier, second et troisième dispositifs bistables, des moyens pour fournir un troisième signal de sortie à appliquer audit troisième dispositif bistable lorsque l'état desdits premier et second signaux de sortie change entre les instants T1 et T2, des moyens de réinitialisation, pouvant agir indépendamment de l'état dudit signal de commande pour réinitialiser lesdits premier, second et troisième dispositifs bistables à un état prédéterminé de façon que l'état du signal de commande, lorsqu'il est échantillonné pendant chaque cycle d'horloge, puisse se propager à travers eux, caractérisé en ce que un ou plusieurs circuit(s) de fonctionnement comporte(nt, chacun une ou plusieurs ligne(s) acheminant les signaux de commande, le circuit de suppression d'impulsions de bruit étant placé dans chacune desdites lignes de commande, chacun desdits circuits de suppression d'impulsions de bruit incluant des moyens de dérivation et une ligne de commande de dérivation pour contourner sélectivement la fonction de suppression d'impulsions de bruit en réponse à l'application d'un signal à sa ligne de commande.

2. Circuit selon la revendication 1, caractérisé par un signal de commande appliqué à la première d'une pluralité de dispositifs bistables connectés en série, connectés ensemble de façon logique afin de fournir un signal de sortie seulement lorsque l'état du signal de commande reste inchangé pendant un certain nombre de cycles d'horloge égal au nombre de dispositifs bistables connectés en série, le procédé consistant à contourner sélectivement la fonction du circuit comprenant les étapes consistant à réinitialiser sélectivement chacun des dispositifs bistables pendant chacun des cycles d'horloge de

façon que le signal de sortie du dernier des dispositifs binaires pendant les cycles d'horloge successifs représente l'état du signal de commande pendant des cycles d'horloge successifs;

3. Circuit selon la revendication 2, caractérisé en ce que ledit circuit de suppression d'impulsions de bruit comprend trois, ou davantage, dispositifs bistables réinitialisables.

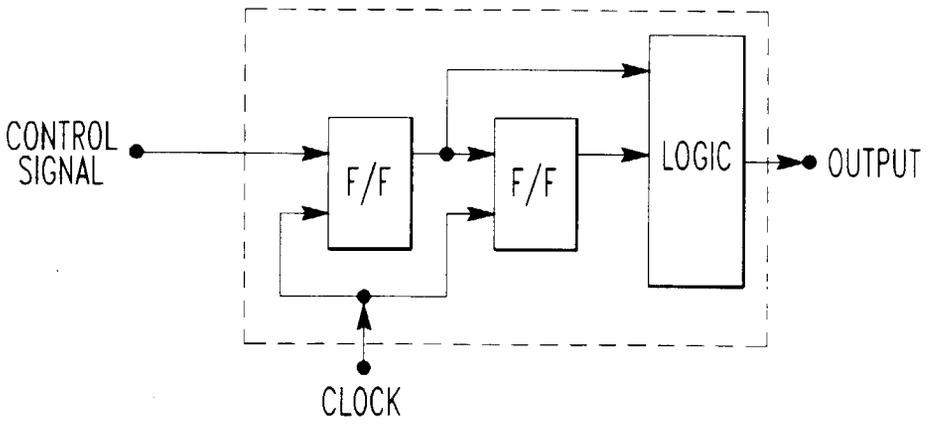

Figure 1

PRIOR ART

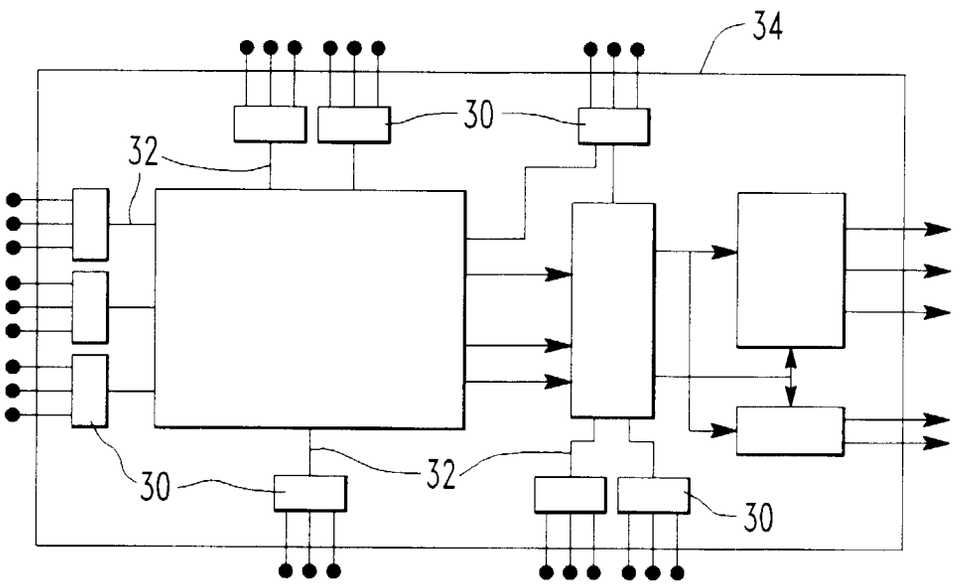

Figure 3

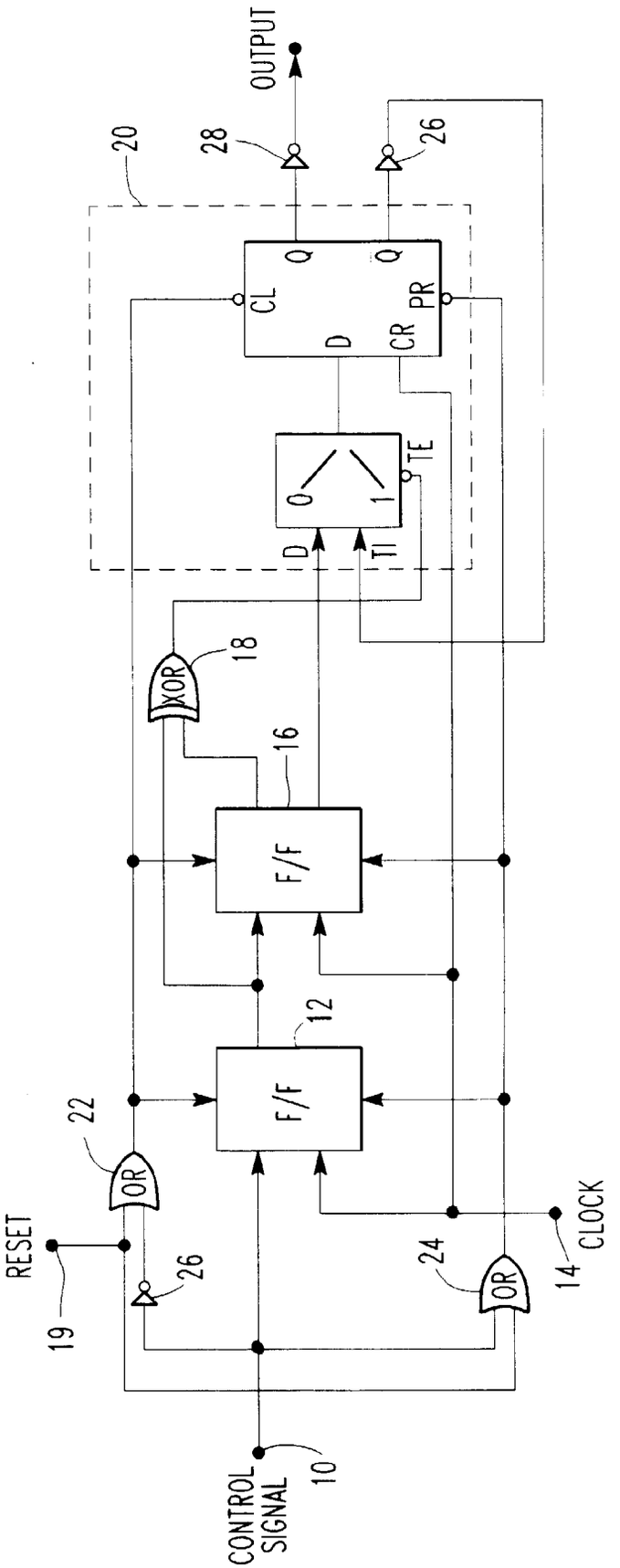
OUTPUT
28
26
20
Q
Q
CL
PR
D
CR
TE
0
1
TI
D
18
XOR
16
F/F
12
F/F
22
OR
RESET
19
26
24
OR
14
CLOCK
CONTROL
SIGNAL
10

Figure 2