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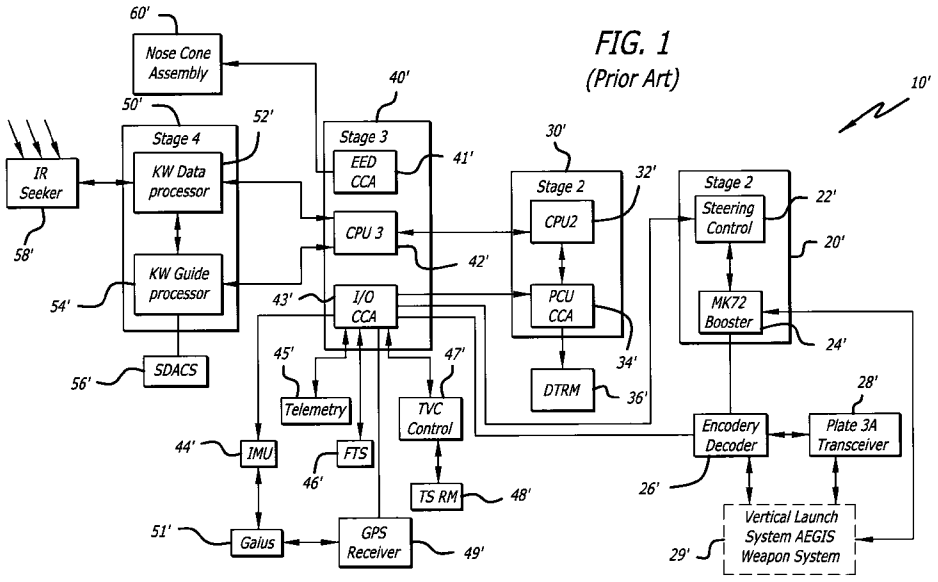
(54) Title: SCALABLE ELECTRONICS ARCHITECTURE



(57) Abstract: A multi-stage missile with plural stages adapted to be physically coupled to and decoupled from adjacent stages and a processor disposed on a single stage for controlling each stage thereof. In the illustrative embodiment, the processor includes a field programmable gate array. In the illustrative embodiment, the processor is disposed on stage 4 of a four-stage missile and performs guidance and navigation functions for each stage and control functions for stages 2, 3 and 4. In a specific embodiment, a serial bus interface is included for coupling the processor to electronic circuitry on each of the stages of the missile. In the best mode, the interface is an IEEE 1394b interface with a physical layer interface and a link layer interface.

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SCALABLE ELECTRONICS ARCHITECTURE

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to electrical and electronic circuits and systems. More specifically, the present invention relates to electrical and electronic circuits and systems used for missile guidance and control.

Description of the Related Art:

The threat posed by nuclear ballistic missiles has prompted an interest in an interceptor missile capable of destroying ballistic missiles in flight. To destroy a ballistic missile early in its flight, the interceptor missile must have a long-range capability. Currently, a long-range capability necessitates a multi-stage missile interceptor design.

Multi-stage missiles typically have booster vehicles and payload assemblies with separate avionics suites to provide independent auto pilot, guidance and navigation, tracking, mid-course communication, and target discrimination functions. The booster hands off mission responsibilities after payload ejection to the KV (kill vehicle).

Unfortunately, separate booster and payload avionic processing increases design and assembly complexity and costs with the incorporation of redundant

electronic hardware, oversized harness cabling, additional power resources, and associated required mechanical packaging hardware.

This architecture was previously necessitated by limited processing capabilities, which required large dedicated processors to be networked throughout the system. This was also due, at least in part, to the fact that typically, each stage is manufactured by a different manufacturer and each manufacturer includes a processor to control electronic circuitry in each stage to insure proper and timely operation.

In addition, typically, connections between stages of multi-stage interceptor missiles are generally point-to-point serial interfaces with the number of interfaces required being related to the number of stages (N) in a factorial relationship (N!). For example, a three-stage interceptor typically requires six interfaces (3x2x1), while a four stage vehicle typically requires twenty-four interfaces (4x3x2x1). These interfaces require cabling that adds to the weight of the missile, increases its cost and limits its performance. This approach also lead to complex interconnections and interface communication protocols between independent units, further complicating software integration, assembly and test requirements.

Hence, a need exists in the art for a lightweight, low cost, high-performance multi-stage missile interceptor. Specifically, a need remains in the art for a system or method for reducing the cost and weight associated with inter-stage connections in a multi-stage missile.

SUMMARY OF THE INVENTION

The need in the art is addressed by the multi-stage missile of the present invention. hi the most general embodiment, the inventive missile includes plural stages adapted to be physically coupled to and decoupled from adjacent stages and a processor disposed on a single stage for controlling each stage of the missile.

In the illustrative embodiment, the processor includes a field programmable gate array. In the illustrative embodiment, the processor is disposed on stage 4 of a four stage missile and performs guidance and navigation functions for each stage and control functions for stages 2, 3 and 4.

In a specific embodiment, a serial bus interface is included for coupling the processor to electronic circuitry on each of the stages of the missile. In the best mode, the interface is an IEEE 1394b interface with a physical layer interface and a link layer interface.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a simplified block diagram of the navigation, guidance and control system of a typical multi-stage interceptor missile implemented in accordance with conventional teachings.

Fig. 2 is a block diagram showing an illustrative implementation of a navigation, guidance and control system of a multi-stage interceptor missile implemented in accordance with the teachings of the present invention.

Fig. 3 is a block diagram of an illustrative implementation of the digital interface unit in accordance with the present teachings.

Fig. 4 is a simplified block diagram showing an illustrative arrangement by which a digital interface unit is scaled by the addition of a second processor in accordance with the present teachings.

Fig. 5 is a flow diagram of an illustrative implementation of software executed by the guidance processor of the digital interface unit of the present invention.

DESCRIPTION OF THE INVENTION

Illustrative embodiments and exemplary applications will now be described with reference to the accompanying drawings to disclose the advantageous teachings of the present invention.

While the present invention is described herein with reference to illustrative embodiments for particular applications, it should be understood that the invention is not limited thereto. Those having ordinary skill in the art and access to the teachings provided herein will recognize additional modifications, applications, and embodiments within the scope thereof and additional fields in which the present invention would be of significant utility.

Fig. 1 is a simplified block diagram of the navigation, guidance and control system of a typical multi-stage interceptor missile implemented in accordance with conventional teachings. The system 10' includes four stages 20', 30', 40' and 50'. Stage 1 20' has a first central processing unit (CPUl) 22' which controls a booster motor 24'. The booster 24' is initiated by a weapon system controller 29'.

In accordance with conventional teachings, the second stage 30' has a second CPU 32' which controls a Power Condition Unit (PCU CCA) 34'. The PCV CCA 34' communicates with a telemetry unit 35' and a Dual Thrust Rocket Motor (DTRM) 36'.

The third stage 40' has a third CPU 42' which communicates with an inertial measurement unit 44', a telemetry system 45', a Flight Termination System (FTS) 46', a Global Positioning Satellite (GPS) receiver 49' and a Thruster Vector Control (TVC) controller 47' via an input/output Circuit Card Assembly (CCA) unit 43'. The IMU is coupled to the GPS receiver 49' via a GPS Aided Navigation System (GAINS) 51'. The third CPU is also in communication with the nose cone assembly 60' via a Electrical Explosive Device (EED CCA) 41'. The I/O CCA communicates via a communication link 55'.

The fourth stage 50' is a fourth CPU which performs data processing (52') and guidance processing (54'). The data processor 52' is coupled to an infrared seeker 58'. The guidance processor 54' is coupled to a Solid Divert Altitude Control System (SDACS) 56'. Communication with the fourth stage is effected via a second communication link 57'.

In accordance with the present teachings, an interceptor is disclosed which is configured to concentrate micro-processing functions into a single computer located within the Kill Vehicle (KV) or payload, instead of each booster stage. The inventive system incorporates a single-node-centric, micro-processing system that performs auto pilot, guidance and navigation, tracking, and target discrimination functions for the vehicle flight from booster launch egress to target interception.

In the illustrative embodiment, the system is scalable allowing for the vehicle to be configured with any number of rocket motor stages. This enables a reconfiguration of the overall vehicle design without impacting the electronic architecture. In addition, the communication interfaces between the stages is simplified by the use of an IEEE 1394b bus interface.

Fig. 2 is a block diagram showing an illustrative implementation of a navigation, guidance and control system of a multi-stage interceptor missile implemented in accordance with the teachings of the present invention. As per the system 10' of Fig. 1, the inventive system 10 includes a first stage electronics module 20, a second stage module 30, a third stage module 40 and a fourth stage module 50. However, in accordance with the present teachings, a single CPU 52 is provided in the fourth stage 50 in lieu of a CPU in each preceding stage as shown in Fig. 1. As a result, each stage functions with simplified electronic circuitry. Fewer interfaces and less cabling are required between stages. This is illustrated in Fig. 2.

As shown in Fig. 2, the fourth stage 50 includes a digital interface unit (DIU) 52 that performs guidance, navigation and control functions along with payload maintenance and autopilot navigation. The DIU 52 is disposed on a forward assembly along with a conventional valve drive unit 54 and a power conditioning unit (PCU)

56. The DIU 52 communicates through a conventional communications link 58 and antenna 59 via a switch 61. Telemetry is provided to the DIU via a telemetry unit 60, an encryption circuit 62, switch 61 and antenna 59. The DIU controls the switch 61 and allows the telemetry unit 60 to use an antenna on stage 3 or an antenna on stage 4.

The valve drive 54 operates through a conventional liquid divert attitude and control system (LDACS) 64. A conventional seeker assembly 70 is included with a sensor 72 and an electronics package 74. The seeker electronics package 74 includes an image processor 76 and a data processor 78. A cryogenics unit 86 cools the focal plane array 71 of an infrared sensor 72 in the seeker assembly 70. Numerous batteries are deployed throughout the system as is common in the art.

The data processor 78 receives inputs from an IMU 80 and communicates with the DIU 52. The DIU 52 communicates with the electronics subsystems in the first, second and third stages via a serial bus interface 80. In the preferred embodiment, the serial bus interface 80 is an IEEE 1394b interface. In the illustrative embodiment, the IEEE 1394b bus is a six-wire cable interface that extends through stages 3, 2 and 1 and the interstage interfaces are identical.

The third stage electronics subsystem includes a thrust vector controller (TVC) and attitude control system (ACS) 42 and a controller 44 therefor. The controller 44 may be implemented with discrete logic, application specific integrated circuit or other suitable arrangement. The controller 44 receives guidance, navigation and autopilot commands from the DIU 52 through the bus 80 and provides thrust vector and attitude control signals in response thereto.

The controller 44 is coupled to electrically activated explosive devices 46, a power conditioning unit (PCU) 48 and input/output interface 41. The I/O interface 41 receives vehicle location data from an onboard GPS receiver 49 and communicates with the DIU 52 on stage 4 via the serial bus 80. The I/O interface 41 and bus 80 allow GPS, guidance, attitude control and other stage related data to be forwarded to the DIU 52 and allow the DIU to trigger the ejection of the stage by activating the electrical explosive devices 46. On activation of the explosive devices, a squib is sent

to a mechanical ejector 86 to effect separation of the stage. The squib is a high-energy pulse that serves to activate a battery 84 in the fourth stage. The squib pulse is also applied to the cryogenics unit 82. A conventional flight termination system (FTS) 88 is included in third stage as is common in the art.

The second stage electronics package 30 is coupled to the DIU 52 via the serial bus 80. The second stage is similar to the third stage 40 with the exception that an IMU 34 is included in the second stage along with a linear shaped charge (LSC) 36 for mechanical separation. There is no CPU in 30. An Input Output (I/O) Controller 31 collects telemetry and inertial measurement unit data.

The electronics package for the first stage 20 includes a thrust vector controller 22, TVC drivers 24, separation ordinance 26 and an LSC 28. As per the second and third stages, the first stage 20 is coupled to the DIU 52 via the bus 80.

Note that the only connections required between stages are for antenna, serial bus, power supply and squib.

The system 10 is 'centric' in that the software required for guidance and control of multiple stages is concentrated in one stage. In the illustrative embodiment, the software is executed by the DIU 52 in the fourth stage. However, the present teachings are not limited thereto. Specific purpose processors and processors implemented in hardware may be used in lieu of the general purpose CPU of the DIU without departing from the scope of the present teachings. In addition, the centric processor may be located on stages other than stage 4.

Fig. 3 is a block diagram of an illustrative implementation of the digital interface unit in accordance with the present teachings. In the illustrative implementation of Fig. 3, the DIU 52 includes a guidance processor 90, a field programmable gate array (FPGA) 110, and an IEEE 1394b bus controller 120. In the illustrative embodiment, the guidance processor 90 includes three PC 750FX or PC 750GX processors with L2 cache 92 and nonvolatile RAM and Flash memory 94. As discussed more fully below, the system is scalable to allow for the addition of processors and stages with minimal cost, weight and complexity.

The FPGA 110 may be implemented with a Xilinx Virtex II Pro or equivalent gate array. The FPGA 110 handles various interrupts and is provided with an RS 232 interface code module 112, a serial interface 114 and a custom interface 116. The RS 232 interface communicates with a debug port (not shown) or a spare port (not shown) via a first transceiver 122 and an RS 422 interface. The serial interface 114 communicates with the communications link 58, telemetry unit 60, and IMU 80 via a second transceiver 124 and a Low Level Differential Signal (LVDS) or RS 422 interface. The custom interface 116 communicates with seeker electronics 70, ordinance valve driver (not shown), Liquid Divert Altitude Control (LDAC) 64 and other analog devices via a third transceiver 126 and a custom I/O interface 116.

The FPGA 110 further includes a memory interface 118 and a Peripheral Computer Interface (PCI) core 119. The FPGA 110 communicates with the guidance processor 90 and the bus controller 120 via a local bus 96. The FPGA 110 includes plural ports, interfaces and interface logic circuits to enable multiple processors to be added to the DIU 52. This is illustrated in Fig. 4.

Fig. 4 is a simplified block diagram showing an illustrative arrangement by which a digital interface unit is scaled by the addition of a second processor in accordance with the present teachings. In Fig. 4, first and second processors 90 and 91 are coupled to the system 10 via the FPGA 110.

Returning to Fig. 3, the bus controller 120 provides IEEE 1394b connectivity between stages and a test port (not shown). This bus allows for "daisy chain" interconnection betweens stages for design simplicity and robustness. The bus controller 120 includes a physical layer 128 and a link layer 129 and is otherwise conventional in design and function.

Hence, the system architecture through each of the stages is scalable. The FPGA design and IEEE 1394b bus interconnection between stages allows for the addition and deletion of stages without adding complexity. Hence, processor, circuitry and cabling cost and weight requirements are reduced.

Fig. 5 is a flow diagram of an illustrative implementation of software executed by the guidance processor of the digital interface unit of the present invention. The software 100 includes stage 1 control software 140. When stage 1 separation is ordered by the DIU 52 (Fig. 2), stage 1 separates and a 'Stage 1 Gone' signal is sent to the DIU by a signal from stage 2. At step 142, the software 100 checks for the presence of this signal and activates Stage 2 control software (step 144) on receipt thereof.

Similarly, when stage 2 separation is ordered by the DIU, stage 2 separates and a 'Stage 2 Gone' signal is sent to the DIU by a signal from stage 3. At step 146, the software 100 checks for the presence of this signal and activates Stage 3 control software (step 144) on receipt thereof. Finally, when stage 3 separation is ordered by the DIU, stage 3 separates and a 'Stage 3 Gone' signal is sent to the DIU by a signal from stage 4 (the nose assembly). At step 150, the software 100 checks for the presence of this signal and activates Stage 4 (terminal) control software (not separately shown) on receipt thereof.

Thus, the present invention has been described herein with reference to a particular embodiment for a particular application. Those having ordinary skill in the art and access to the present teachings will recognize additional modifications applications and embodiments within the scope thereof.

It is therefore intended by the appended claims to cover any and all such applications, modifications and embodiments within the scope of the present invention.

Accordingly,

WHAT IS CLAIMED IS:

[EUROSTYLE] CLAIMS

1. A multi-stage missile system (10) characterized by:

plural stages (20, 30, 40, 50) adapted to be physically coupled to and decoupled from adjacent stages and

a processor (52) disposed on a single stage (50) for controlling each stage.

2. The invention of Claim 1 wherein said processor (52) further includes a serial bus interface (80) for coupling said processor (52) to electronic circuitry on each of said stages.

3. The invention of Claim 2 wherein said interface (80) is an IEEE 1394b interface.

4. The invention of Claim 3 wherein said interface (80) includes a physical layer interface.

5. The invention of Claim 4 wherein said interface (80) includes a link layer interface.

6. The invention of Claim 1 wherein said processor (52) is adapted to perform guidance functions for said stages.

7. The invention of Claim 1 wherein said processor (52) is adapted to perform navigation functions for said stages.

8. The invention of Claim 1 wherein said processor (52) is adapted to perform control functions for said stages.

9. The invention of Claim 1 wherein said processor (52) includes a field programmable gate array (110).

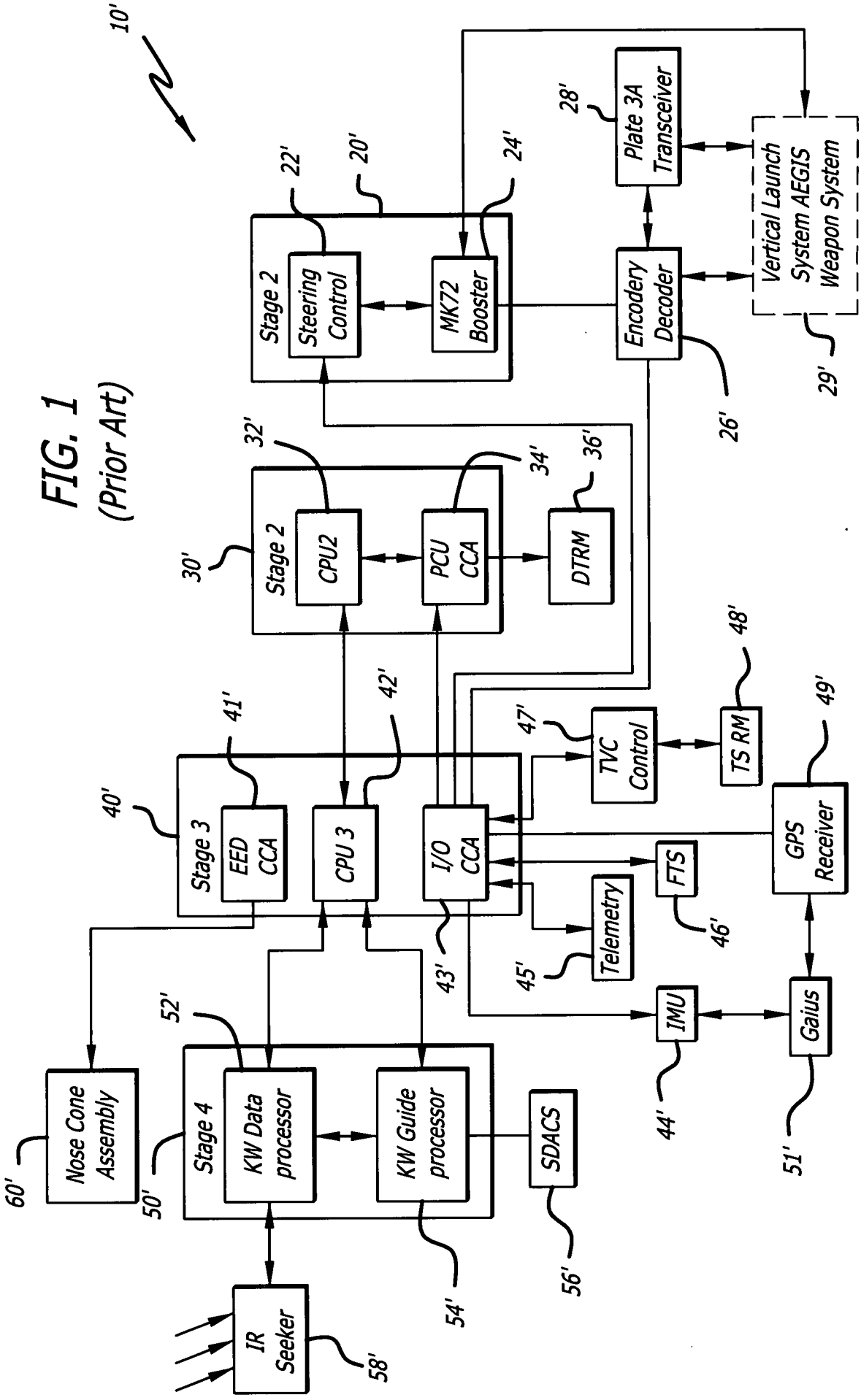

FIG. 1
(Prior Art)

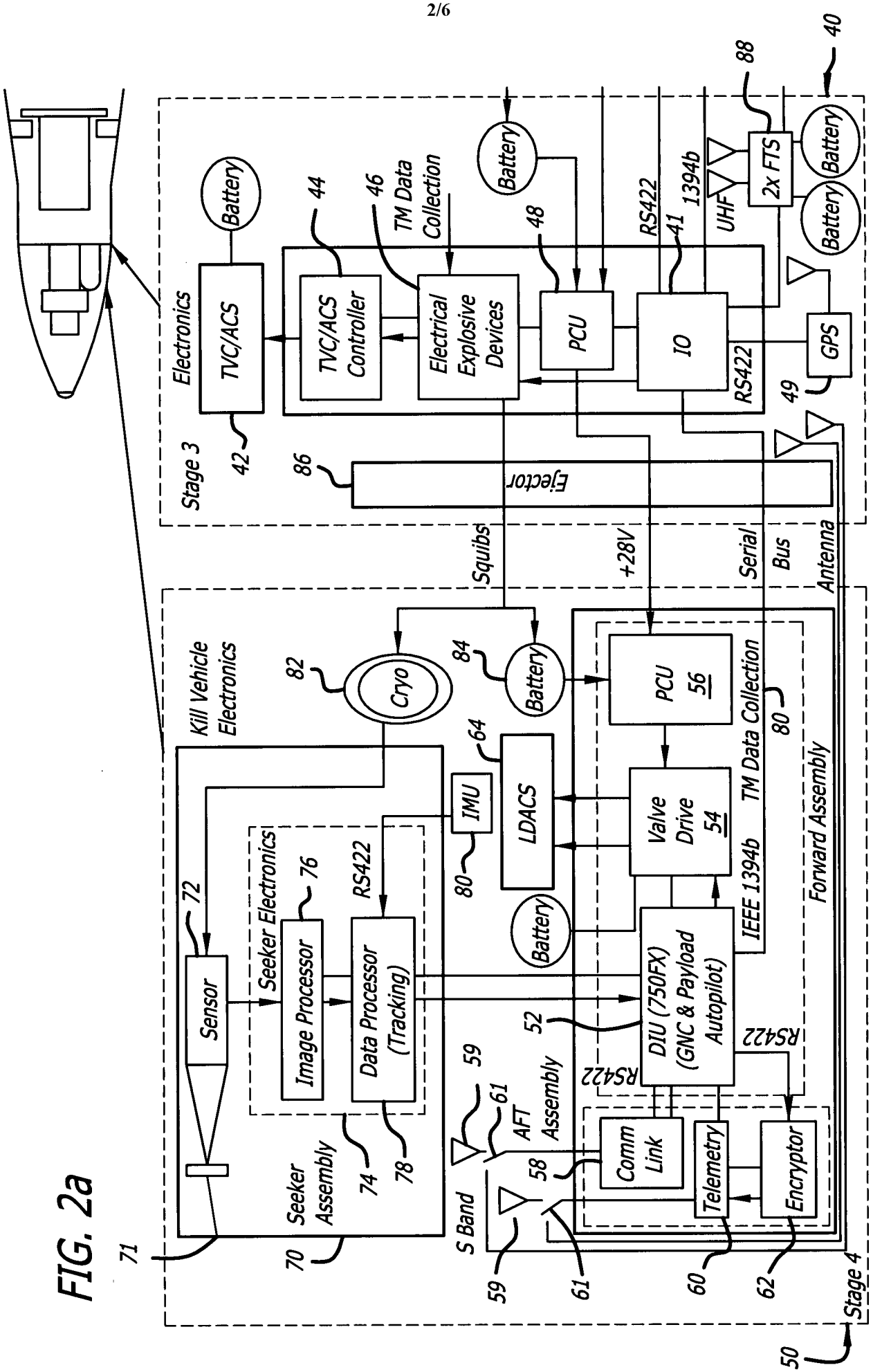
Stage 3
Electronics
TVC/ACS
Battery
42
TVC/ACS Controller
44
TM Data Collection
46
Electrical Explosive Devices
48
PCU
IO
RS422
41
1394b
UHF
2x FTS
88
40
GPS
49
Ejector
86
Squibs
+28V
Serial Bus
Antenna
Kill Vehicle Electronics
Cryo
82
84
Battery
PCU 56
80
TM Data Collection
Forward Assembly
IMU
64
LDACS
Valve Drive 54
IEEE 1394b
Seeker Electronics
Sensor
72
Image Processor
76
Data Processor (Tracking)
RS422
DIU (750FX) (GNC & Payload Autopilot)
52
RS422
Seeker Assembly
74
78
70
71
AFT Assembly
59
61
S Band
Comm Link
58
Telemetry
Encryptor
60
62
Stage 4
50

FIG. 2a

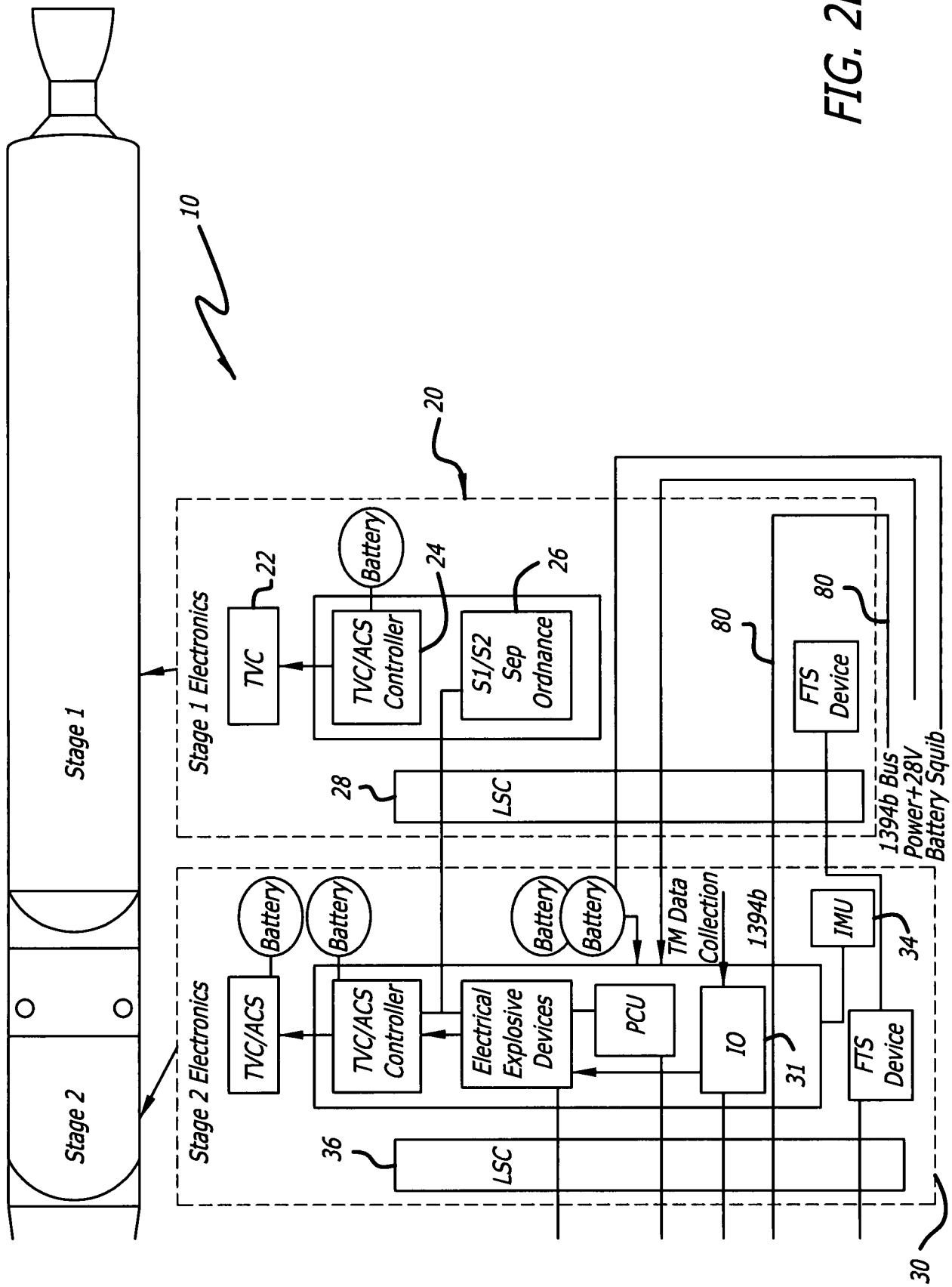
10
20
Stage 1
Stage 2
Stage 1 Electronics
Stage 2 Electronics
TVC
22
TVC/ACS
TVC/ACS Controller
24
S1/S2 Sep Ordnance
26
Battery
28
LSC
36
Electrical Explosive Devices
PCU
IO
31
TM Data Collection
1394b
80
FTS Device
IMU
34
1394b Bus
Power+28V
Battery Squib
30

FIG. 2b

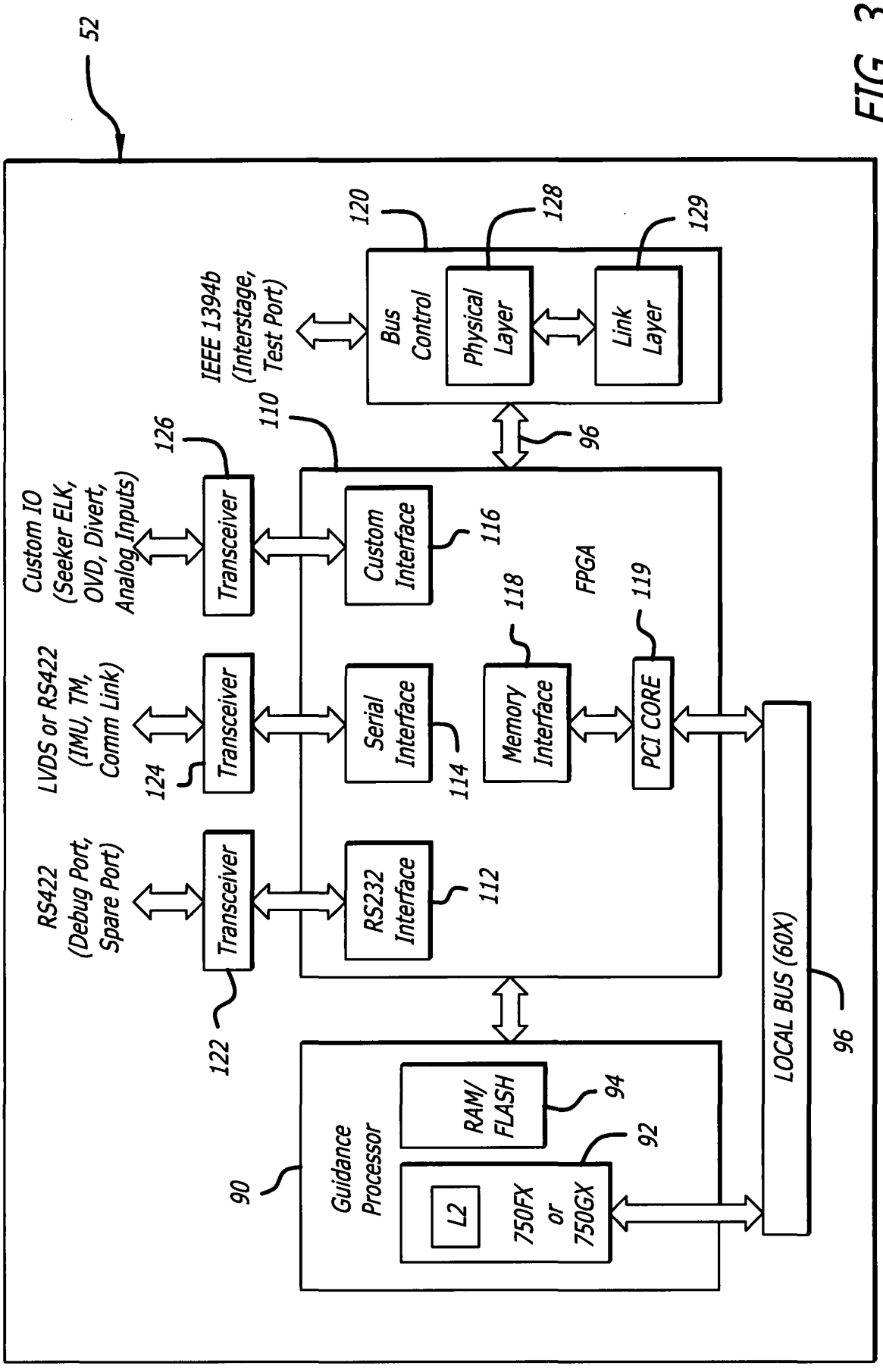
52
IEEE 1394b (Interstage, Test Port)
120
Bus Control
128
Physical Layer
129
Link Layer
96
110
126
Custom IO (Seeker ELK, OVD, Divert, Analog Inputs)
Transceiver
Custom Interface
116
LVDS or RS422 (IMU, TM, Comm Link)
124
Transceiver
Serial Interface
114
118
Memory Interface
FPGA
119
PCI CORE
RS422 (Debug Port, Spare Port)
Transceiver
RS232 Interface
112
122
LOCAL BUS (60X)
96
90
Guidance Processor
RAM/ FLASH
94
92
L2
750FX or 750GX

FIG. 3

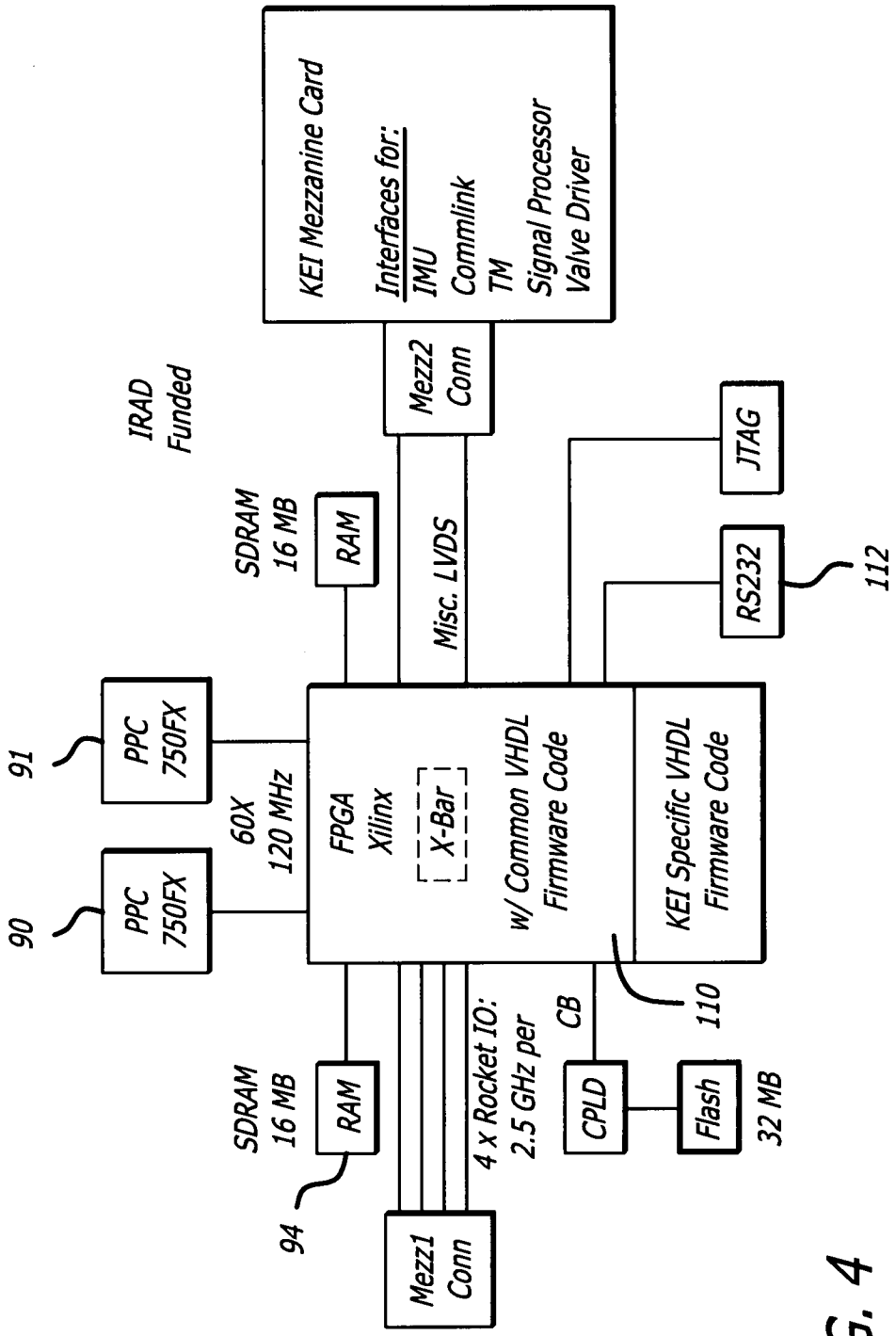
KEI Mezzanine Card
Interfaces for:
IMU
Commlink
TM
Signal Processor
Valve Driver
Mezz2 Conn
IRAD Funded
SDRAM 16 MB
RAM
Misc. LVDS
JTAG
RS232
112
91
PPC 750FX
90
PPC 750FX
60X 120 MHz
FPGA Xilinx
X-Bar
w/ Common VHDL Firmware Code
KEI Specific VHDL Firmware Code
110
SDRAM 16 MB
RAM
94
4 x Rocket IO: 2.5 GHz per
CB
CPLD
Flash
32 MB
Mezz1 Conn

FIG. 4

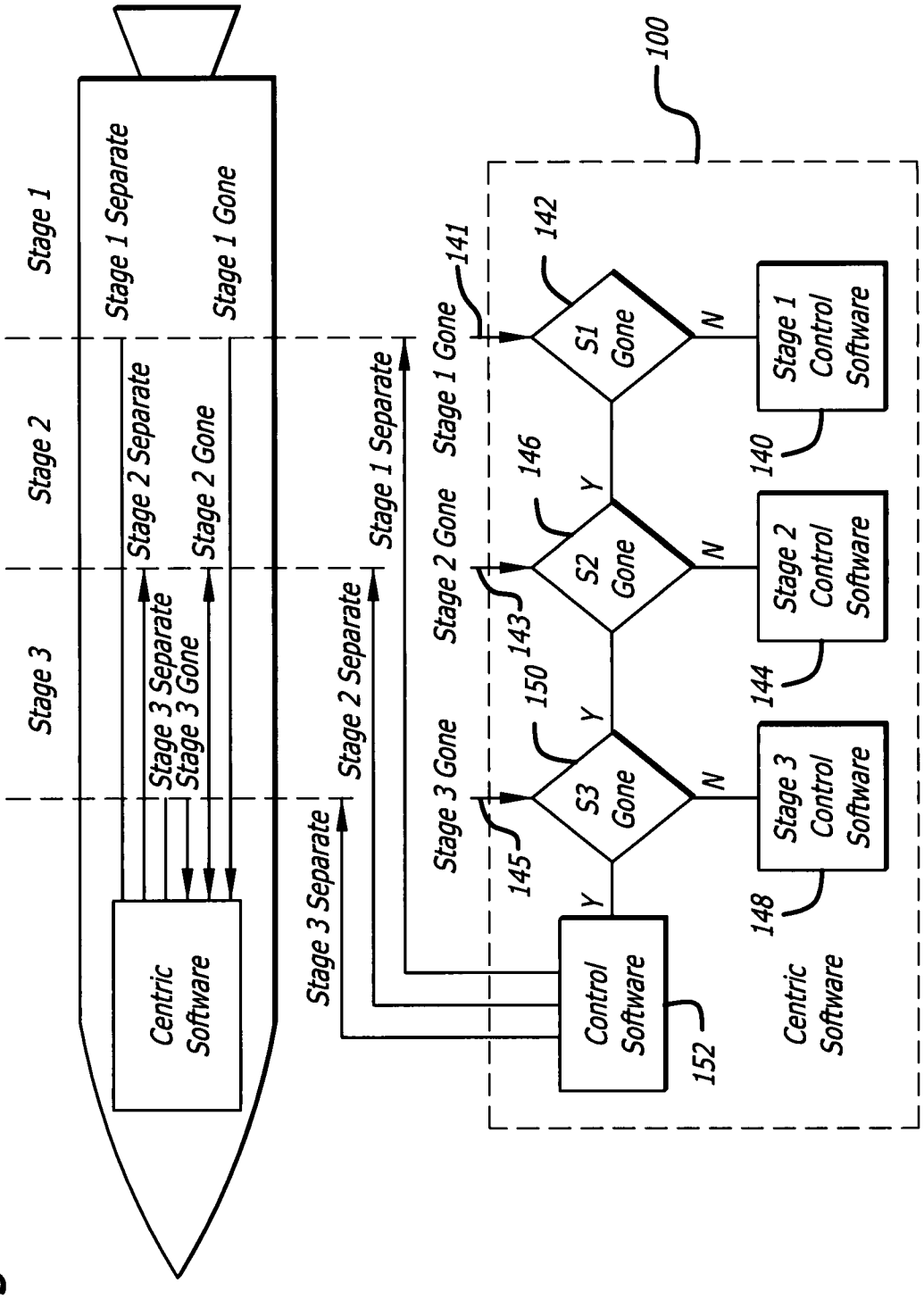
Stage 1
Stage 2
Stage 3
Stage 1 Separate
Stage 1 Gone
Stage 2 Separate
Stage 2 Gone
Stage 3 Separate
Stage 3 Gone
Centric Software
Stage 3 Separate
Stage 2 Separate
Stage 1 Separate
Stage 3 Gone
Stage 2 Gone
Stage 1 Gone
141
142
S1 Gone
N
Stage 1 Control Software
140
146
Y
S2 Gone
N
Stage 2 Control Software
144
143
150
Y
S3 Gone
N
Stage 3 Control Software
148
145
Y
Control Software
152
Centric Software
100

FIG. 5