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(54) Benævnelse: **DC-link-spændingsudligningssystem og fremgangsmåde til multilevel konverter**

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DESCRIPTION

[0001] This invention relates generally to multilevel converters and more specifically to a system and method for DC link voltage balancing in multilevel converters.

[0002] Multilevel converters are generally used in high power industrial applications such as variable speed drive (VSD) systems or in energy conversion applications such as a solar (or photovoltaic) power generation systems, wind turbine generators and marine and hydrokinetic power generation systems. One example of a multi-level converter is a neutral point clamped (NPC) converter. A three level converter, for example, typically includes two capacitor voltages in series with a center tap as the neutral and two phase legs each comprising two pairs of switching devices in series. In one example, each switching device comprises an anti-parallel connection of a unidirectional electronic switching device, such as an insulated gate bipolar transistor or an insulated gate commutated thyristor, and a diode, such as a free-wheeling diode.

[0003] Various conventional NPC's are discussed in the following references:

BUSQUETS-MONGE S ET AL: "Closed-Loop Control Design for a Three-Level Three-Phase Neutral-Point-Clamped Inverter Using the Optimized Nearest-Three Virtual-Space-Vector Modulation", POWER ELECTRONICS SPECIALISTS CONFERENCE, 2006. PESC '06. 37TH IEEE JEJU, KOREA 18-22 JUNE 2006, PISCATAWAY, NJ, USA, IEEE, 18 June 2006 (2006-06-18), pages 1-7, XP010945247, DOI: 10.1109/PESC.2006.1711953 ISBN: 978-0-7803-9716-3;

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[0004] DC link voltage balancing is a challenge when operating three level neutral clamped converters (NPC). DC link voltage unbalance may overstress the capacitors and switching devices and cause over voltage and under voltage trips during the operation of the converter. In severe DC link voltage unbalance conditions, one capacitor may become fully charged to the full DC-link voltage such that stress on the capacitor and the switching devices is doubled and the output waveforms become two level rather than three-level. DC link voltage unbalance also causes an increase in output voltage total harmonic distortion (THD) and may cause the control loop to become unstable.

[0005] One of the methods of compensating DC link voltage unbalance is utilizing measured DC-link voltages for pulse width modulation (PWM) control of the three level converter. This method, however, includes additional expense, does not compensate for steady-error in DC link voltage, and also results in high THD in the output voltage and injects active 2^{nd} harmonic current at AC side. Another method of compensating DC link voltage unbalance is to use zero sequence voltage or DC bias voltage injection. However, this method also has high THD in the output voltage at some operation points and becomes unstable at low power factors.

[0006] Therefore, it is desirable to provide a method and a system that will address the foregoing issues.

[0007] The present invention, as defined by the appended claims, is thus provided.

[0008] Various features, aspects, and advantages of the present invention will become better understood when the following detailed description is read with reference to the accompanying drawings in which like characters represent like parts throughout the drawings, wherein:

FIG. 1 is a circuit diagram of one leg of a conventional neutral point clamped multilevel converter and its output waveform;

FIG. 2 is a circuit diagram of a three phase three level converter for use in accordance with an embodiment of the present invention;

FIG. 3 is a schematic representation of different load connections at different switching states for the embodiment of FIG. 2;

FIG. 4 is a detailed block diagram of a converter controller in accordance with an embodiment of the present invention;

FIG. 5 is detailed block diagram of a neutral point (NP) controller in accordance with an embodiment of the present invention;

FIG. 6 is a graphical representation of an NPC current simulation plots;

FIG. 7 is a graphical representation of plots for determining common voltage signal; and

FIG. 8 is a graphical representation of output current total harmonic distortion simulation plots.

[0009] FIG. 1 illustrates a schematic 10 of one leg or one phase of a conventional neutral point clamped (NPC) or diode clamped three level converter and its output waveform 12. One leg 14 of the three-level converter includes four switching devices 16, 18, 20, and 22 and two clamping diodes 24 and 26. Input voltages V1 and V2 are controlled to each have a voltage equal to Vdc/2, where Vdc is the total DC link voltage. Voltage V3 is the phase A output voltage measured with respect to a center point or a neutral point 28 of DC link 30. Switching device 16 is complementary to switching device 20 so that, when switching device 16 is gated on, switching device 20 is gated off and vice versa. Similarly, switching devices 18 and 22 are complementary.

[0010] In operation, each leg of the NPC three level converter has three switching stages P, O, and N respectively. The three switching stages and the respective output voltages are given in following table:

Table 1

Switching Stage	Switching Device 16	Switching Device 18	Switching Device 20	Switching Device 22	Voltage V3
P	ON	ON	OFF	OFF	+Vdc/2
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-Vdc/2

[0011] In the first switching stage P, switching devices 16 and 18 are turned on and switching devices 20 and 22 are turned off. Assuming a stable operation, V1=V2=Vdc/2, and V3 becomes Vdc/2. In the second switching stage O, switching devices 18 and 20 are turned on while switching devices 16 and 22 are turned off. In this stage, V3 is equal to zero. In the third switching stage N, switching devices 16 and 18 are turned off whereas switching devices 20 and 22 are turned on. This results in V3 becoming - Vdc/2 as shown in a waveform 12. Thus, it can be seen that the phase voltage V3 has three levels Vdc/2, -Vdc/2, and 0. When all three legs of the NPC three-phase converter are combined, then the resulting line to line voltages have five levels namely Vdc, Vdc/2, 0, -Vdc/2 and -Vdc.

[0012] The converter leg 14 of FIG. 1 may be modified so as to increase the number of voltage levels to any level depending on the circuit topology and number of switching devices and diodes in the circuit. As the number of levels in the converter increases, the output waveform of the converter approaches a pure sine wave, resulting in lower harmonics in the output voltage. In general, the number of switching stages can be higher than three as switching devices may not be gated on if the corresponding free-wheeling diode is going to conduct current. This operation mode does not affect the number of levels of the output phase voltage.

[0013] FIG. 2 illustrates a schematic 40 of a three phase three level converter for use in accordance with an embodiment of the present invention. The converter 40 includes a split DC link 42 with a neutral point 41 and capacitors 43 and 45 and three switching legs 44, 46, and 48 with output terminals 47, 49, and 51 respectively (for phases a, b, and c). A three phase load 61 is connected across the three phase output terminals 47, 49, and 51. A converter controller 50 provides switching pulse commands to switching devices of the switching legs 44, 46, and 48 based on DC link voltage and power signals. As described earlier, the output line voltages at output terminals 47, 49, and 51 will have five levels, namely Vdc, Vdc/2, 0, -Vdc/2 and -Vdc.

[0014] FIG. 3 shows the effect of switching states on neutral point voltage deviation. When the converter is operated with a switching state [PPP], in other words, when all legs are in a P switching state, the upper two switching devices (FIG. 2) in each of the three converter legs are turned on, connecting the load terminals 47, 49, and 51 to the positive DC bus as shown in circuit 60. Since the neutral point 41is left unconnected, this switching state does not affect neutral point voltage Vn. Circuit 62 shows the converter operation with a switching state POO (one leg with P switching state and the other two legs with O switching state as described in Table 1). In this state the three-phase load is connected between the positive DC bus and neutral point, and the neutral current i_n flows in through the neutral point causing Vn to increase. In contrast, the switching state ONN causes Vn to decrease as shown in circuit 64. For switching state PON in circuit 66, terminals 47, 49 and 51 are connected to the positive DC bus, the neutral point, and the negative bus, respectively. In this state, depending on the load current, the neutral-point voltage Vn may rise or drop. In switching state PNN, as shown in circuit 68, the terminals are connected to the positive and negative DC buses. The neutral point is left unconnected and thus the neutral point voltage is not affected. Thus, depending on the switching states and the load current, the neutral point voltage varies and may not remain balanced at Vdc/2.

[0015] FIG. 4 shows a detailed block diagram of a converter controller 50 for use in the configuration of FIG. 2 in accordance with one embodiment of the present invention. Controller 50 includes a DC link voltage regulator 82, a differential mode current regulator 84, a neutral point (NP) controller 86 and a PWM controller 88. DC link voltage regulator 82, generates a d-domain reference current command signal i^*_d based on an error signal which is a difference between the reference or the desired total DC link voltage $u^*_{DC,tot}$, and the actual total DC link voltage $u_{DC,tot}$ as obtained by a comparator 90, for example. In one embodiment, DC link voltage regulator 82 comprises a proportional-integral (PI) regulator. In one embodiment, a q-domain reference current command signal i^*_q may be generated by a reactive power regulator 81 based on a difference between a desired amount of reactive power or a reference reactive power Q* and an actual reactive power Qa. Differential mode current regulator 84 receives d-q domain reference current command signals i^*_d, i^*_q and d-q domain actual current command signals i_d , i_q and uses those signals to generate d-q domain reference voltage command signals u^*_d and u^*_q based on the difference between the reference and the actual current command signals. In one embodiment, actual current command signals i_d, i_q are determined from measured three phase a-b-c domain load currents i_a, i_b, i_c by transforming them into d-q domain currents. Differential mode current regulator includes two PI regulators. One for d-domain currents i^*_d and i_d for generating d domain reference voltage command signal u^*_d and the other one for q-domain currents i^*_q and i_q for generating q domain reference voltage command signal u^*_q.

[0016] As further shown in FIG. 4, d-q to a-b-c domain transformation matrices 92 and 94 may be used to transform d-q domain reference current command signals i^*_d, i^*_q and d-q domain reference voltage command signals u^*_d, u^*_q into the a-b-c domain reference current command signals i^*_a, i^*_b, i^*_c and a-b-c domain reference voltage command signals u^*_a, u^*_b, u^*_c, respectively, based on a phase angle θ. The phase angle θ is generated by a phase locked loop (PLL) (not shown) based on three phase load voltages or grid voltages if the converter is connected to the power grid. NP controller 86 generates a common mode reference voltage signal u^*_{cm} for compensating the DC link voltage unbalance. The common mode reference voltage signal u^*_{cm} is then further added to the a-b-c domain reference voltage command signals u^*_a, u^*_b, u^*_c before providing the combined voltage signal to PWM controller 88. The resultant signal of addition of u^*_a, u^*_b, u^*_c and u^*_{cm} is thus used by the multilevel converter controller to balance the neutral point voltage.

[0017] NP controller 86 generates the common mode reference voltage signal u^*_{cm} based on d-domain reference current command signal i^*_d, a-b-c domain reference current command signals i^*_a, i^*_b, i^*_c, a-b-c domain reference voltage command signals u^*_a, u^*_b, u^*_c and differential DC link voltage signal Δu_{dc} as discussed below with respect to FIG. 5. In one embodiment, NP controller 86 may use measured load current signals i_a, i_b, i_c rather than reference current command signals i^*_a, i^*b, i^*_c for generating the common mode reference voltage signal. PWM controller 88 also receives measured half DC-link voltages i.e., the top capacitor voltage or the positive bus DC link voltage with respect to neutral point $u_{DC,p}$ and the bottom capacitor voltage or the negative bus DC link voltage with respect to neutral point $u_{DC,m}$ and generates three phase duty cycle signals $DC_{a...c}$ for the three level converter given by:

$$DC_{a...c} = \begin{cases} \dfrac{u^*_{a...c}}{u_{DC,p}} & \text{for } u^*_{a...c} \geq 0 \\ -\dfrac{u^*_{a...c}}{\;} & \text{for } u^*_{a...c} < 0 \end{cases} \quad (1)$$

$$u_{DC,m}$$

[0018] The above generated three phase duty cycles are then utilized to produce PWM pulses for individual switching devices of the multilevel converter. In one embodiment, a sine triangular PWM or a space vector PWM is used for generating the PWM pulses.

[0019] FIG. 5 shows a detailed block diagram of the NP controller 86 of FIG. 4. NP controller 86 includes a Min-Max classifier 100 to determine instantaneous minimum, maximum, and medium current and voltage values, $i_{u\min}$, $i_{u\max}$, i_{umid}, and $u_{\min}$, $u_{\max}$, u_{mid} of the a-b-c domain reference current i^*_a, i^*_b, i^*_c and reference voltage u^*_a, u^*_b, u^*_c signals respectively. For example, minimum, maximum, and medium values for a-b-c domain reference voltages may be -147V, 147V and 0V at a particular instant. The instantaneous minimum, maximum, and medium current and voltage values are then provided to a NP current pre-calculator 102 and a NP limit calculator 104.

[0020] NP current pre-calculator determines the current that flows into the neutral point if no additional common mode reference voltage is injected to the reference voltage command signals. In other words, it determines the present neutral point current without disturbing the common mode reference that is being added to the a-b-c domain reference voltage command signals. The neutral point current signal $i^*_{np,\,pre}$ is calculated by following equation:

$$i^*_{np,pre} = \begin{cases} \dfrac{u_{\max} . i_{u\max} + u_{mid} . i_{umid}}{u_{DC,p}} + \dfrac{u_{\min} . i_{u\min}}{u_{DC,m}} & for\ u_{mid} \geq 0 \\ \dfrac{u_{\max} . i_{u\max}}{u_{DC,p}} + \dfrac{u_{mid} . i_{umid} + u_{\min} . i_{u\min}}{u_{DC,m}} & for\ u_{mid} < 0 \end{cases} \quad (2)$$

[0021] The average value of neutral point current $i^*_{np,\,pre}$ over a time period becomes zero if it is not modified.

[0022] NP limit calculator 104 determines minimum and maximum limits for neutral point current signal $i^*_{np,\,pre}$, and common mode reference voltage signal u^*_{cm}. The limits are identified based on several constraints. For example, the amplitude of the common mode reference voltage is limited by the modulation index (MI) of the multilevel converter which indicates the peak line-to-line output voltage that can be generated by the multilevel converter and is generally lower than the total DC-link voltage at any instant. In one embodiment, the maximum and minimum limits $u^*_{cm,\max}$ and $u^*_{cm,}$ min for the common mode reference voltage are given by:

$$u^*_{cm,\min} = \max(u_{\max} - u_{DC,p} . DC_{\max},\ (1 - DC_{\max}) . u_{DC,p} + u_{\min} \quad (3)$$

$$u^*_{cm,\max} = \min(u_{\min} - u_{DC,m} . DC_{\max},\ (1 - DC_{\max}) . u_{DC,m} + u_{\max} \quad (4)$$

where DC_{max} is a constant which indicates maximum duty cycle that can be achieved in the circuit and depends on circuit design. Similarly, maximum, medium, and minimum limits $i^*_{np,max}$, $i^*_{np,mid}$, and $i^*_{np,min}$ for the neutral point current signal may be given by

$$i^*_{np,I...III} = \begin{cases} \dfrac{(u_{max} - u_{cm,I....III}).i_{u\,max} + (u_{mid} - u_{cm,I....III}).i_{umid}}{u_{DC,p}} + \dfrac{(u_{min} - u_{cm,I....III}).i_{u\,min}}{u_{DC,m}} & for\ (u_{mid} - u_{cm,I....III}) \geq 0 \quad (5) \\ \dfrac{(u_{max} - u_{cm,I....III}).i_{u\,max}}{u_{DC,p}} + \dfrac{(u_{mid} - u_{cm,I....III}).i_{umid} + (u_{min} - u_{cm,I....III}).i_{u\,min}}{u_{DC,m}} & for\ (u_{mid} - u_{cm,I....III}) < 0 \quad (6) \end{cases}$$

where I, II and III refers to *min*, *mid* and *max* respectively. The maximum and minimum current limit and voltage limit signals are then provided to a waveform corrector 106 and a dynamic common mode (CM) voltage regulator 108.

[0023] A proportional - integral (PI) regulator 110 generates a DC control signal g_{cm} based on a differential DC link voltage signal Δu_{dc} after subtracting it from zero to indicate whether the differential DC link voltage is above or below zero. The differential DC link voltage is a difference between top capacitor voltage and the bottom capacitor voltage of the DC link. In an optional embodiment, d domain reference current command signal i^*_d is used as a factor that could be used to modify the PI regulator 110 gain. The resulting DC control signal g_{cm} will have values between +1 and -1 and is utilized by waveform corrector 106 along with maximum and minimum current limit signals for modifying the neutral point current signal $i^*_{np,\ pre}$ determined in equation 2 from NP current pre-calculator 102. If no DC-link unbalance is detected, that is, if Δu_{dc}=0 or g_{cm}=0, then the neutral point current signal $i^*_{np,\ pre}$ is not changed. Otherwise, the neutral point current signal $i^*_{np,\ pre}$ will be modified and the modified neutral point current signal i^*_{np} will be given as:

$$i^*_{np} = \begin{cases} i^*_{np,pre} + g_{cm}.(i^*_{np.max} - i^*_{np,pre}) & for\ g_{cm} > 0 \\ i^*_{np,pre} & for\ g_{cm} = 0 \\ i^*_{np,pre} - g_{cm}.(i^*_{np,min} - i^*_{np,pre}) & for\ g_{cm} < 0 \end{cases} \quad (7)$$

[0024] It can be seen from the above equation that if DC control signal g_{cm} is zero (if there is no voltage unbalance) then the neutral point current signal need not be modified and hence it remains $i^*_{np,\ pre}$. However, if g_{cm} is not zero, then the current $i^*_{np,\ pre}$ is modified or regulated based on the DC control signal g_{cm}. Further, it is ensured that the modified current signal i^*_{np} is within the maximum and minimum limits $i^*_{np,\max}$ and $i^*_{np,\min}$ determined in equations 5 and 6 respectively.

[0025] Dynamic CM voltage regulator 108 generates the common mode reference voltage signal u^*_{cm} for compensating the DC link voltage unbalance based on the modified current signal i^*_{np}. In one embodiment, the dynamic CM voltage regulator 108 includes a look-up table that provides the required CM reference voltage magnitude according to the modified current signal. At a particular instant, for a given current signal i^*_{np}, the look up table will have voltage values within the maximum and minimum limit signals $u^*_{cm,\max}$ and $u^*_{cm,\min}$ determined in equations 3 and 4 respectively at that instant. The voltage values in the look up table vary depending on the load power factor. The curve between voltage values and the respective current values in the lookup table for a given power factor is partly linear and in most cases there is only one solution available. For example, at a load power factor of 0.9 the curve will be a flat line. In certain cases, there may be two solutions available. In these cases, the solution with lower amplitude is chosen as described in more detail in FIG. 7.

[0026] FIG. 6 shows neutral point current simulation plots 130 and 140 for two different power factors. Plot 130 is for a power factor of 0.9 and the DC control signal g_{cm} =0.5, whereas plot 140 is for same power factor but for g_{cm} =1. In both plots 130 and 140 horizontal axis 131 represents a reference vector angle in degree which is representative of time, and vertical axis 133 represents normalized current values in amperes. Curves 132 and 142 represent maximum neutral point current signals $i^*_{np,\max}$ and curves 134 and 144 represent minimum neutral point current signals $i^*_{np,\min}$. Similarly, curves 136 and 146 represent neutral point current signals $i^*_{np,pre}$ and curves 138 and 148 represent modified neutral point current signals i^*_{np} respectively. It can be seen from plot 140 that when g_{cm} =1, $i^*_{np,pre} = i^*_{np,\max}$ as given by equation 7 and thus, the curves 142 and 148 are overlapped.

[0027] FIG. 7 shows simulation plots 160, 162 and 164 for determining common mode voltage for three different power factors in accordance with an embodiment of the present invention. In all plots 160, 162 and 164, horizontal axis 161 represents common mode voltage in volts, and vertical axis 163 represents normalized modified neutral point current i^*_{np} / i_{peak}, where i_{peak} is the peak neutral point current. In one embodiment, the vertical axis may directly be represented with only modified neutral point current. Plot 160 is for phase angle 209.7^0, plot 162 is for phase angle 59.7^0 and plot 164 is for phase angle 149.7^0. It can be seen from plots 160 and 162 that for a desired amount of modified neutral point current i^*_{np} 165, there exists only one solution 166 and 167 respectively. Further, it can be seen from plot 164 that there are two solutions 168 and 169 for the desired amount of modified neutral point current 165. All the solutions 166, 167, 168 and 169 fall within the three limits: minimum $u^*_{cm,\ \min}$, medium $u^*_{cm,\ med}$, and maximum $u^*_{cm,\ \max}$ respectively. The exact value of the desired common mode voltage is then found from slope of the curve between minimum voltage and medium voltage and medium voltage and maximum voltage with respect to neutral point current. In one embodiments, all the common mode voltage values for a given power factor or the phase angle and the neutral point current are stored in a lookup table. As described earlier, if there are two solutions as in plot 164 then the one with lower magnitude is selected. Thus, in plot 164, solution 168 which has lower magnitude compared to solution 169 is selected.

[0028] FIG. 8 shows simulation plots 170 and 180 for total harmonic distortion (THD) in output currents. Fast Fourier transform (FFT) plot 170 is for a multilevel converter operation without any NP controller whereas FFT plot 180 is for a multilevel converter operation with a NP controller as described herein. Both plots are for zero power factor. FFT plot 170 shows that 2nd and 4th harmonics have significant amplitudes whereas FFT plot 180 shows that the harmonics are well suppressed.

[0029] One of the advantages of the NP controller described herein is improved stability of three level converters even when operating at zero power factor. The NP controller further reduces the THD of output current and may reduce the cost of the DC link capacitors.

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Patentkrav

1. Styresystem (50) til at styre en multilevel konverter (40), hvilket styresystem (50) omfatter:

en differentialmodus-strømregulator (84) til generering af referencespænding-kommandosignaler baseret på en forskel mellem referencestrøm-kommandosignaler og faktisk-strøm-kommandosignaler;

en nulpunkt (NP) -kontroller (86) til bestemmelse af et modificeret nulpunktsstrømsignal i respons på en DC-link-spændingsubalance og under anvendelse af det modificerede nulpunktsstrømsignal til at generere et fælles-modus-referencespændingssignal; og

en PWM-kontroller (88) til generering af omskifterimpulser til multilevel konverteren (40) baseret på referencespænding-kommandosignalerne og fælles-modus-referencespændingssignalet;

referencestrøm-kommandosignalerne omfatter d-q-domæne-referencestrøm-kommandosignaler og referencespænding-kommandosignalerne omfatter d-q-domæne-referencespænding-kommandosignaler, hvor nævnte styresystem (50) yderligere omfatter en DC-link-spændingsregulator (82) til generering af d-domæne-referencestrøm-kommandosignalet baseret på en forskel mellem et reference-DC-link-spændingssignal og et ønsket DC-link-spændingssignal; **kendetegnet ved, at:**

en reaktiv effekt-regulator (81) til generering af q-domæne-referencestrøm-kommandosignalet baseret på en forskel mellem et reference reaktiv-effekt-signal og et ønsket reaktiv-effekt-signal;

hvor NP-kontrolleren (86) omfatter en minimum-maksimum-klassifikator (100) til bestemmelse af momentane minimum-, mellem-, og maksimumspændings- og strømsignaler blandt referencestrøm-kommandosignaler og referencespænding-kommandosignaler eller blandt målte strømkommandosignaler og referencespænding-kommandosignaler, hvor NP-kontrolleren (86) omfatter en NP-strøm-forudberegner (102) til generering af et nulpunktsstrømsignal baseret på de momentane minimum-, mellem-, og maksimumspændings- og strømsignaler;

hvor nævnte styresystem (50) yderligere omfatter en NP-grænseværdiberegner (104) til bestemmelse af minimum- og maksimumgrænser for nulpunktsstrømsignalet og det fælles-modus-referencespændingssignal, en kurveforms-korrektor (106) til generering af det modificerede nulpunktsstrømsignal baseret på minimum- og maksimumgrænserne for nulpunktsstrømsignalet og et DC-styresignal, og en dynamisk fælles-modus-(CM)-spændingsberegner (108) til generering af fælles-modus-referencespændingssignalet baseret på den modificerede nulpunktsstrøm og minimums- og maksimumsgrænser for nulpunktsstrømsignalet og fælles-modus-referencespændingssignalet.

2. Fremgangsmåde til styring af en multilevel konverter (40) under anvendelse af styresystemet (50) ifølge krav 1, hvilken fremgangsmåde omfatter:

(a) at generere (84) referencespænding-kommandosignaler baseret på en forskel mellem referencestrøm-kommandosignaler og faktisk-strøm-kommando **kendetegnet ved, at:**

(b) i respons på en spændingsubalance på et DC-link af multilevel konverteren,

(i) at anvende referencespænding-kommandosignalerne og referencestrøm-kommandosignaler til generering af (86) et modificeret nulpunktsstrømsignal til at kompensere for DC-link-spændingsubalancen;

(ii) at anvende det modificerede nulpunktsstrømsignal til generering af (108) et fælles-modus-referencespændingssignal; og

(iii) at generere (88) omskifterimpulser til multilevel konverteren baseret på summering af referencespænding-kommandosignaler og fælles-modus-referencespændingssignalet.

3. Multilevel konverter (40) omfattende:

en flerhed af faseben (44, 46, 48), der hver har mindst to indvendige omskifterindretninger, mindst to udvendige omskifterindretninger, mindst to begrænserdioder og en delt DC-link; og

et styresystem (50) som defineret i krav 1.

DRAWINGS

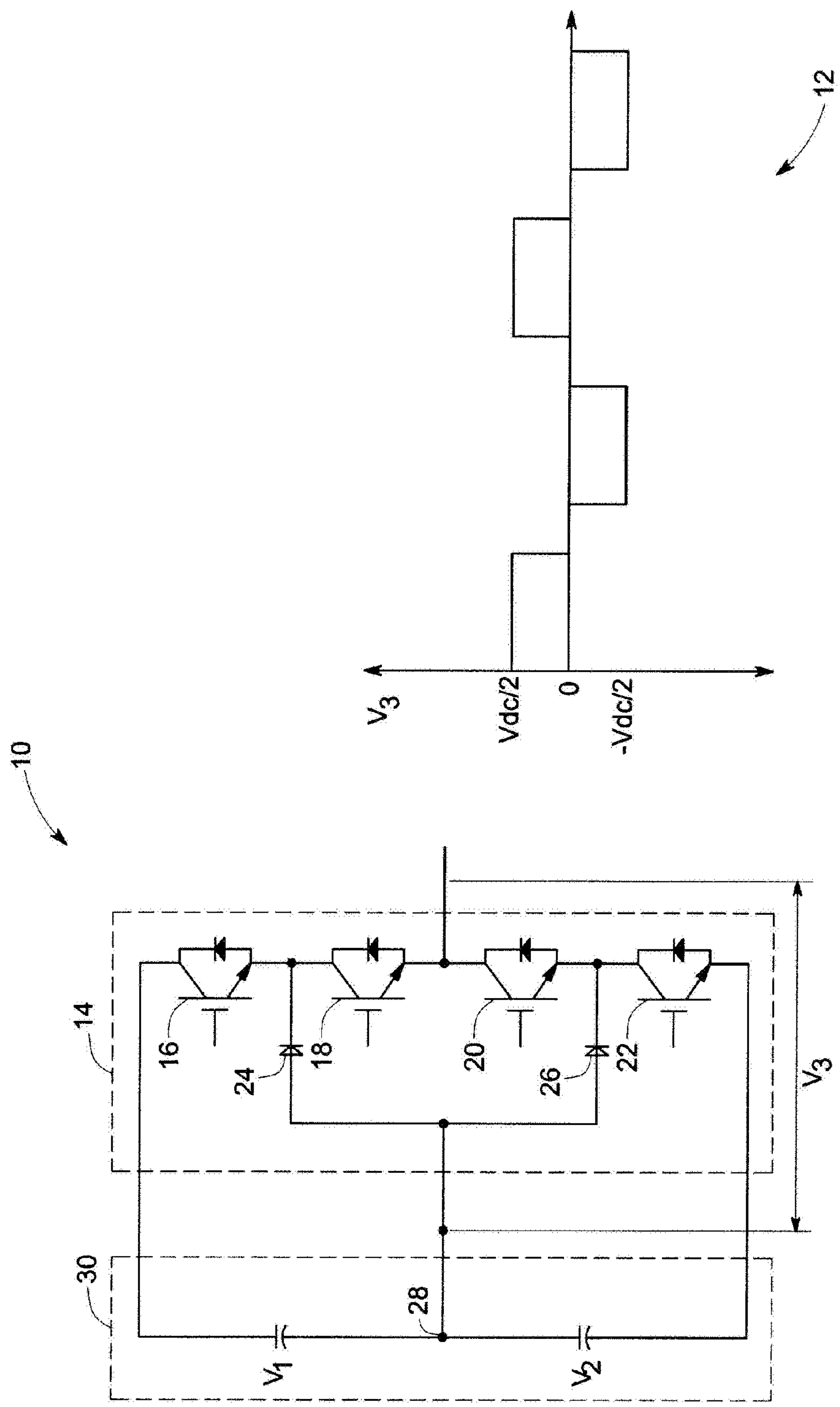


FIG. 1

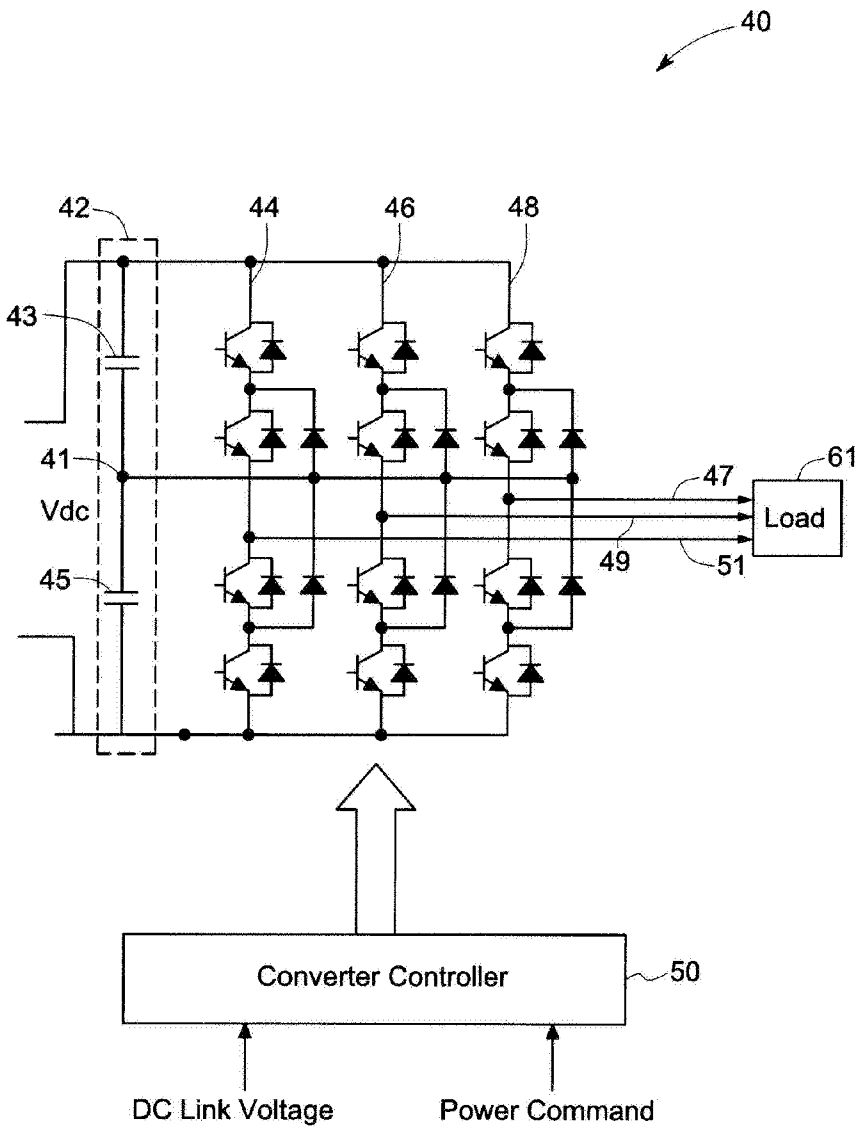

40
42
44
46
48
43
41
Vdc
45
47
61
Load
49
51
Converter Controller
50
DC Link Voltage
Power Command

FIG. 2

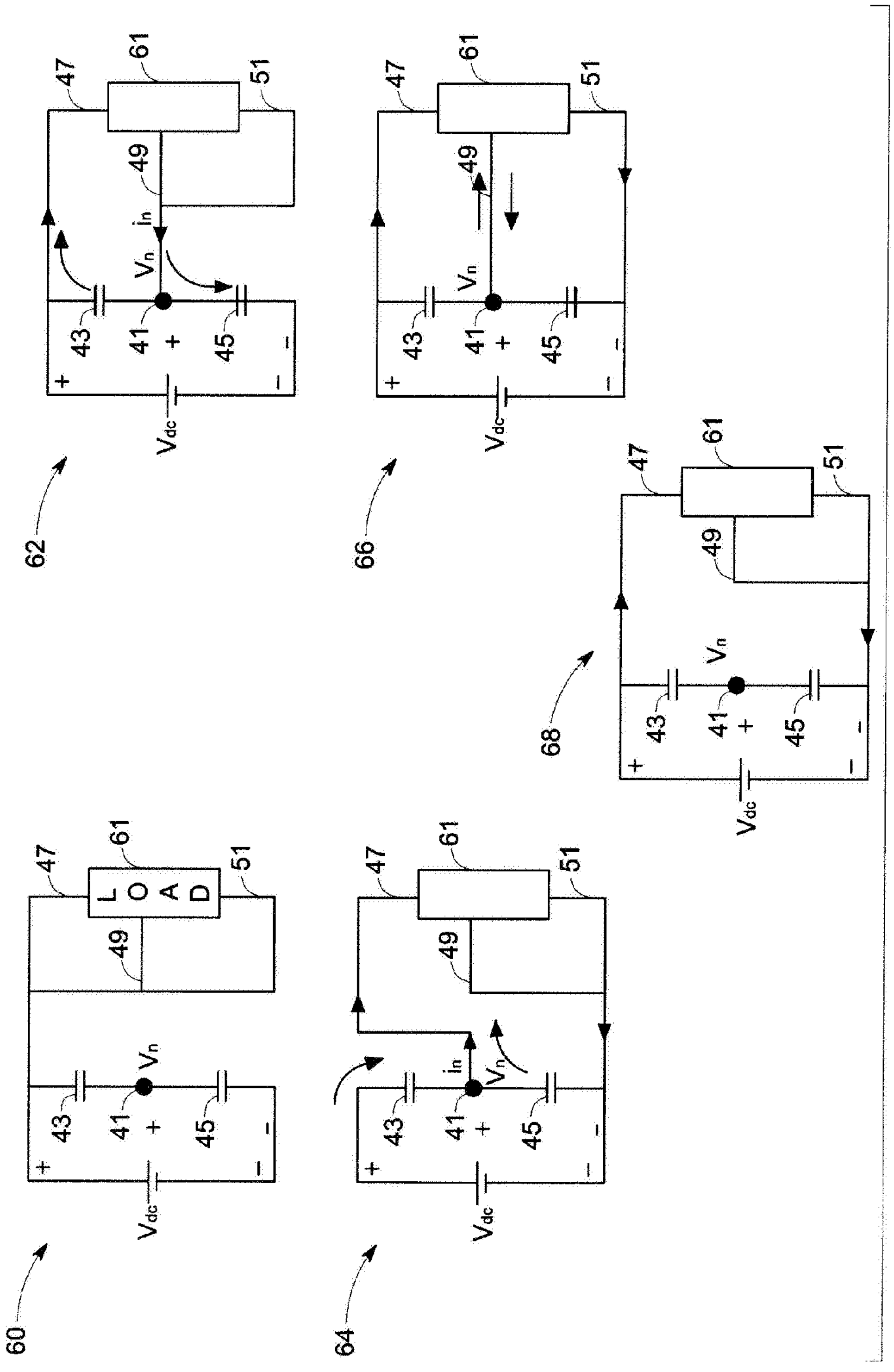
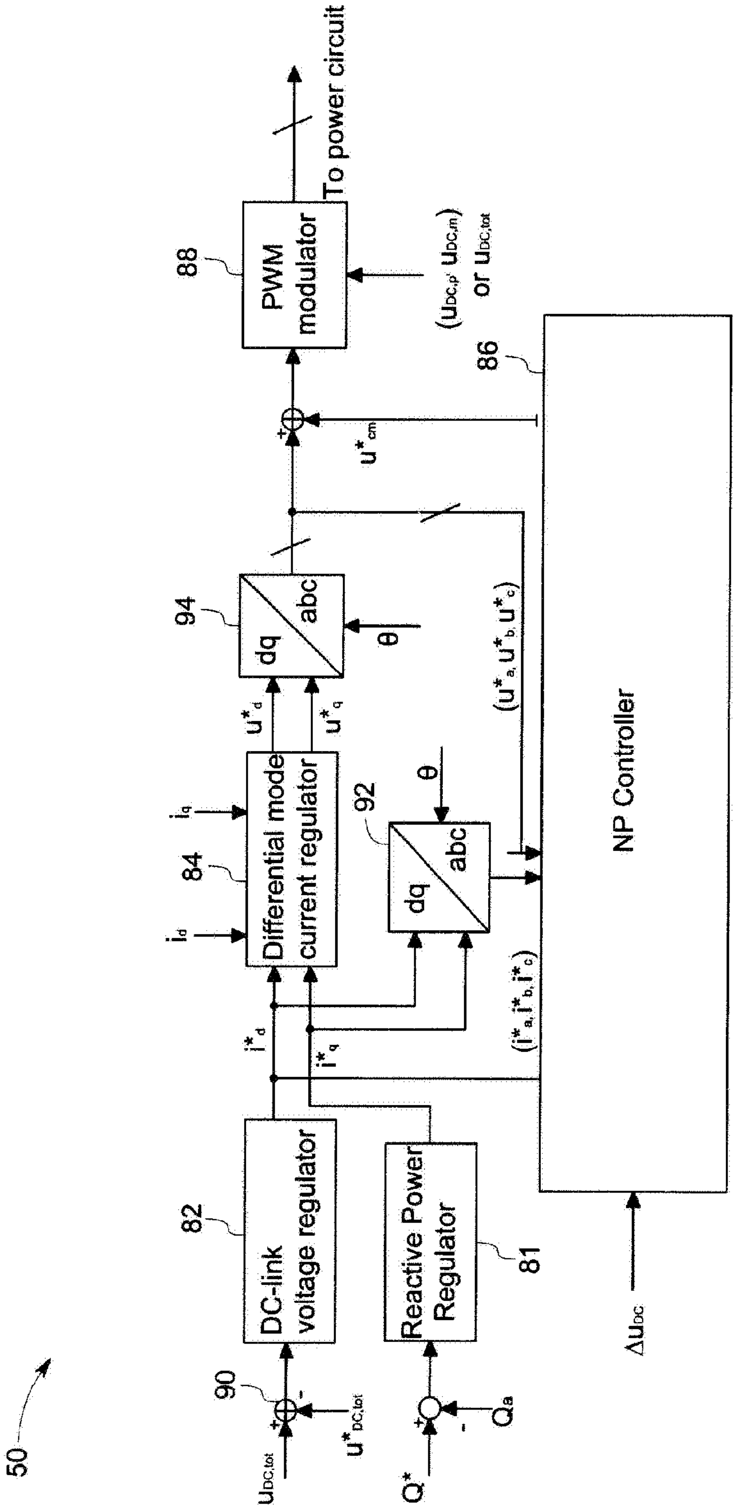


FIG. 3



50
To power circuit
88
PWM modulator
(uDC,p, uDC,m) or uDC,tot
86
u*cm
94
dq
abc
θ
u*d
u*q
(u*a, u*b, u*c)
84
Differential mode current regulator
iq
id
92
θ
NP Controller
(i*a, i*b, i*c)
i*d
i*q
82
DC-link voltage regulator
Reactive Power Regulator
81
ΔuDC
90
uDC,tot
u*DC,tot
Q*
Qa

FIG. 4

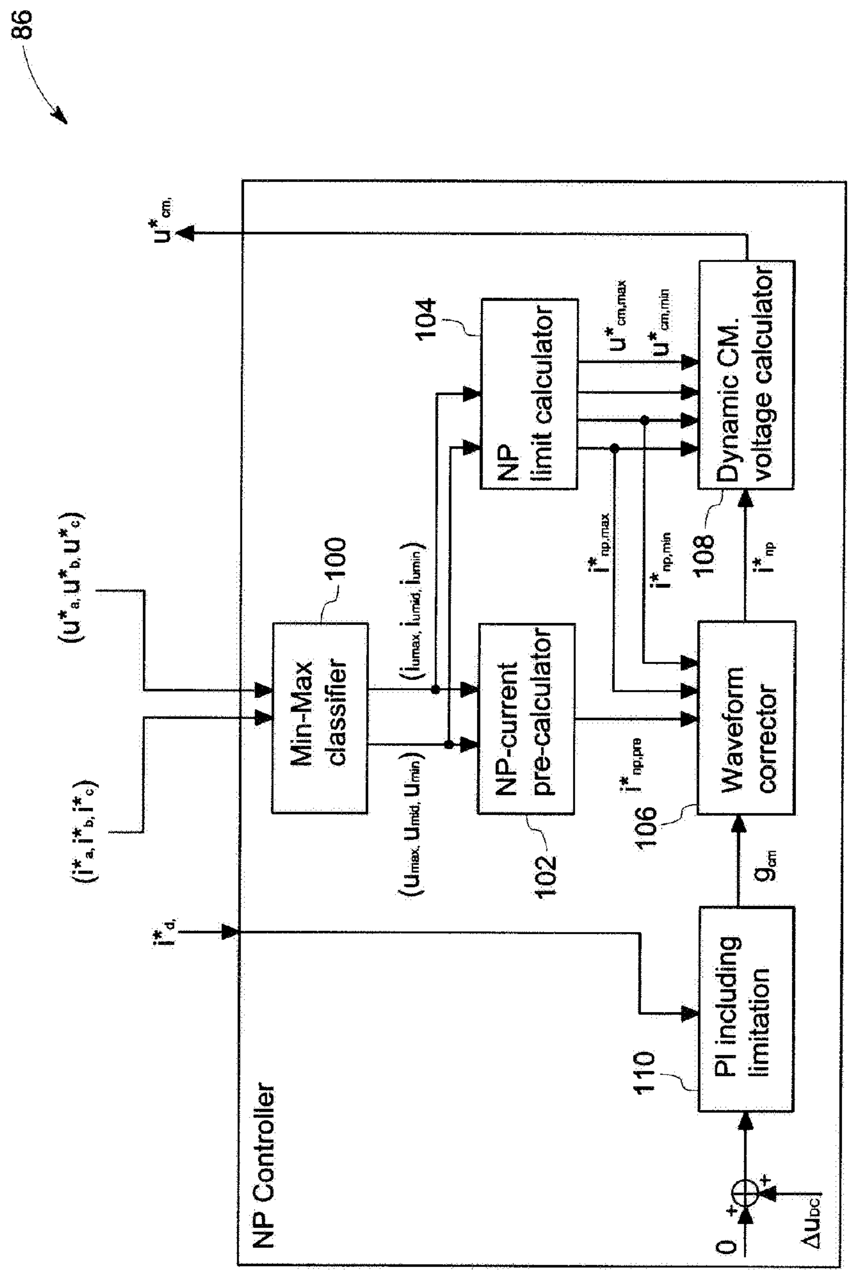

86
NP Controller
u^*_{cm}
(u^*_a, u^*_b, u^*_c)
(i^*_a, i^*_b, i^*_c)
i^*_d
Min-Max classifier
100
$(i_{umax}, i_{umid}, i_{umin})$
$(u_{max}, u_{mid}, u_{min})$
NP-current pre-calculator
102
NP limit calculator
104
$u^*_{cm,max}$
$u^*_{cm,min}$
$i^*_{np,max}$
$i^*_{np,min}$
$i^*_{np,pre}$
Waveform corrector
106
Dynamic CM. voltage calculator
108
i^*_{np}
g_{cm}
PI including limitation
110
0
+
+
Δu_{DC}

FIG. 5

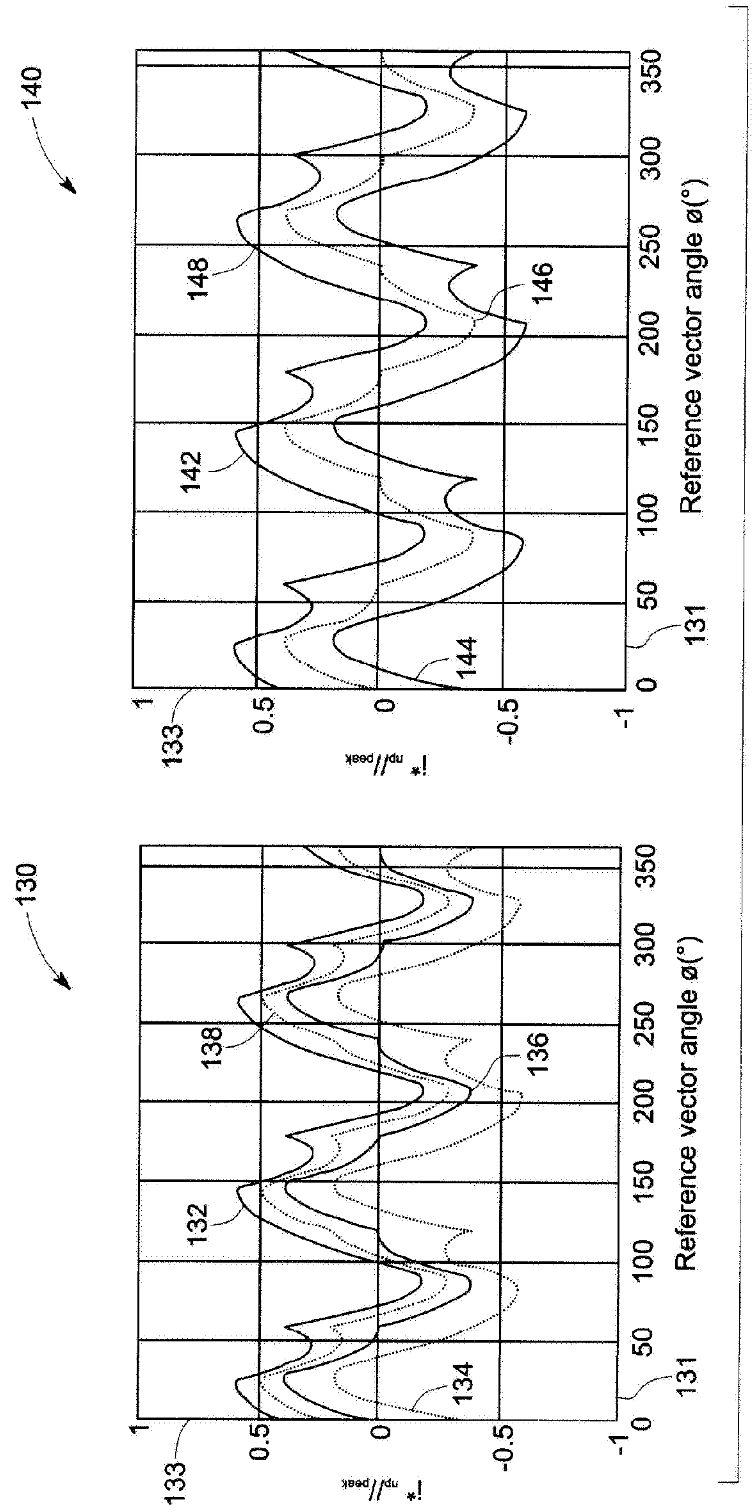

140
130
148
146
142
144
138
136
132
134
131
133
Reference vector angle ø(°)
0
50
100
150
200
250
300
350
1
0.5
0
-0.5
-1

FIG. 6

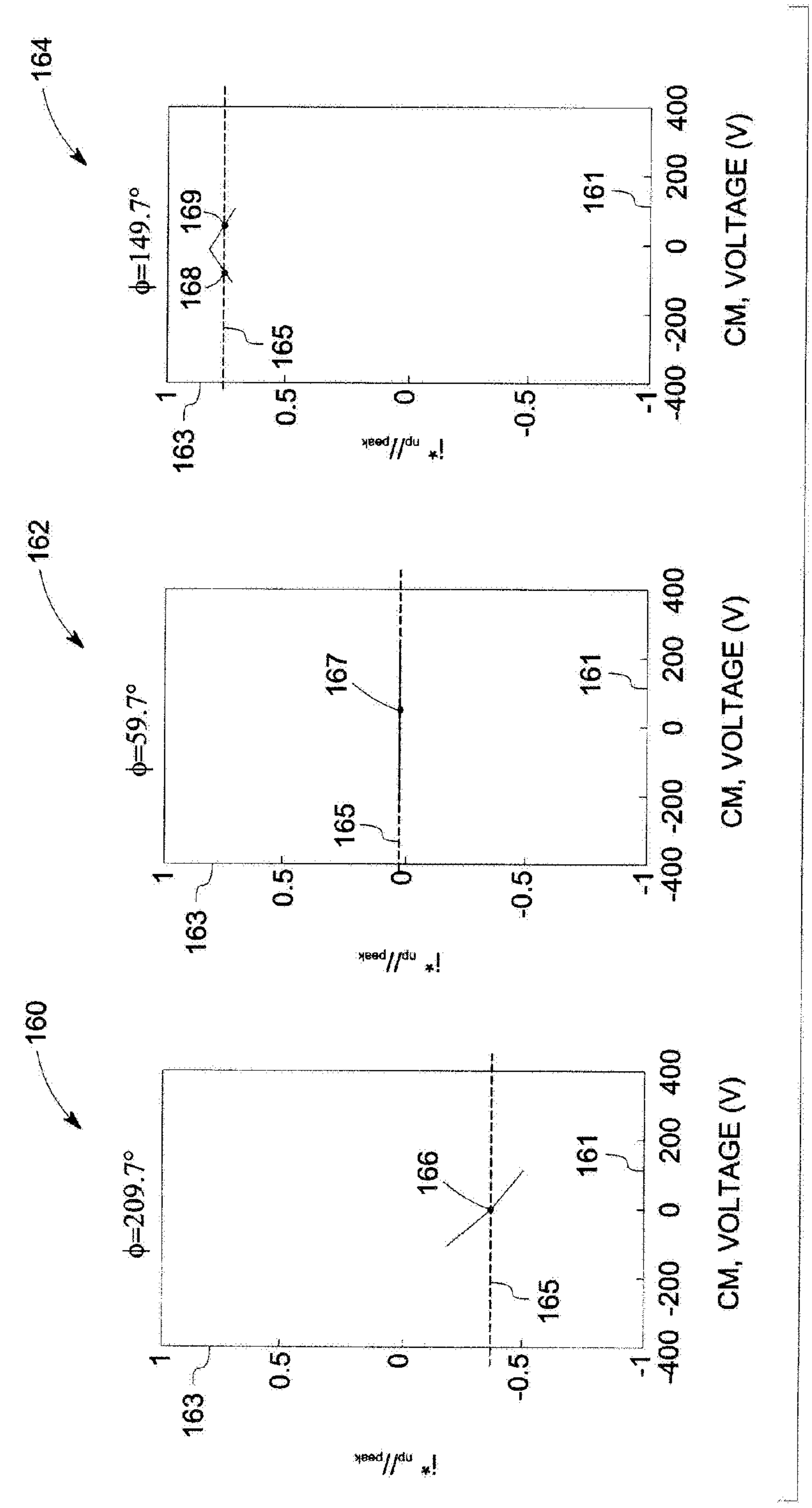

164
162
160
φ=149.7°
φ=59.7°
φ=209.7°
168
169
167
166
165
163
161
CM, VOLTAGE (V)

FIG. 7

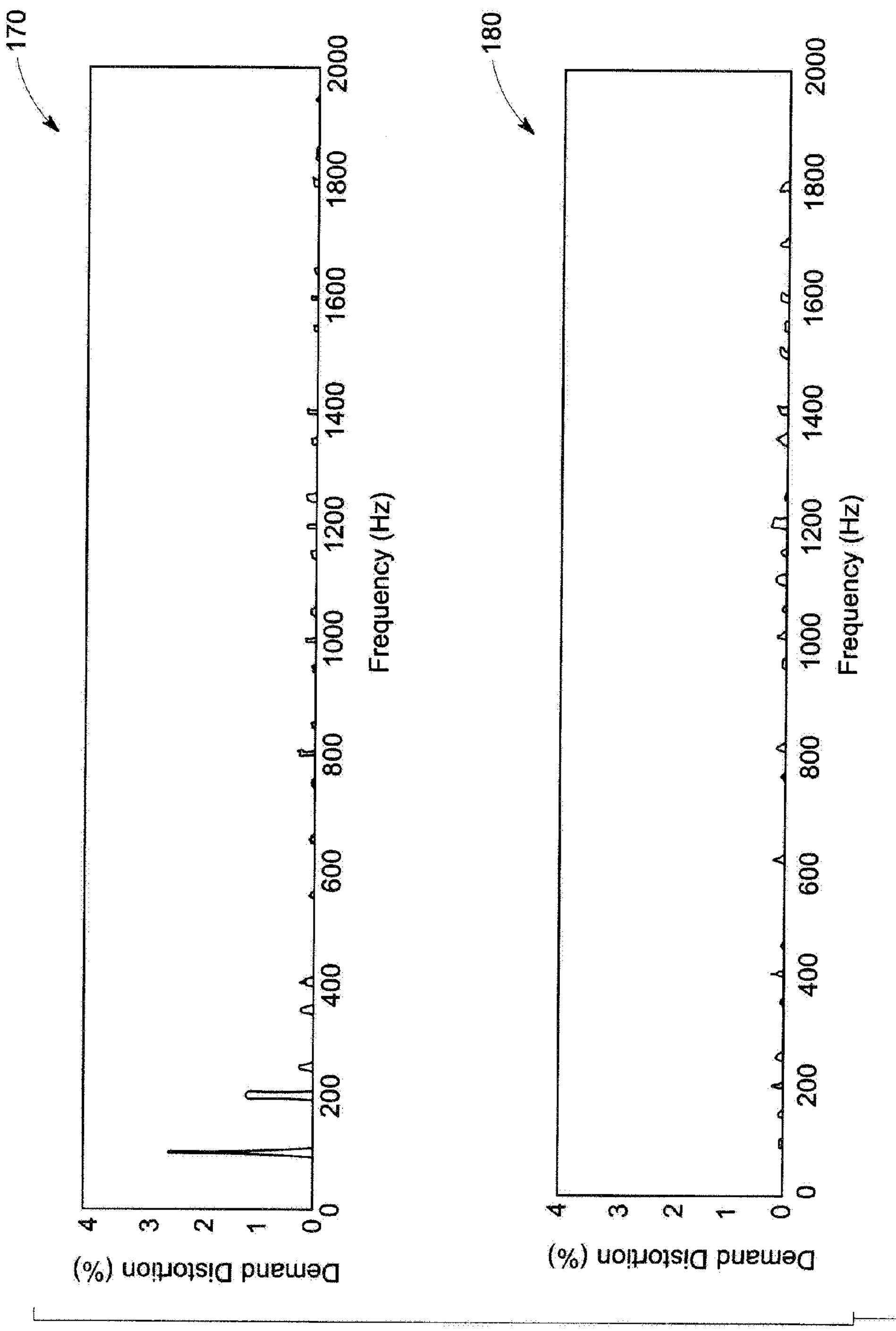

170
180
Demand Distortion (%)
Demand Distortion (%)
0
1
2
3
4
0
200
400
600
800
1000
1200
1400
1600
1800
2000
Frequency (Hz)
Frequency (Hz)

FIG. 8