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(71) Applicant: **Sun Microsystems, Inc.**
Santa Clara, California 95054 (US)

(72) Inventors:
 • **Smith, Brian L.**
Sunnyvale, California 94089 (US)

• **Wu, Jue**
Mountain View, California 94043 (US)
 • **Jong, Jyh-Ming**
Saratoga, California 95070 (US)
 • **Fong, Wai**
San Jose, California 95129 (US)
 • **Yuan, Leo**
Los Altos, California 94024 (US)
 • **Chakrabarti, Prabhansu**
Sunnyvale, California 94086 (US)

(74) Representative: **Davies, Simon Robert**
D Young & Co,
21 New Fetter Lane
London, EC4A 1DA (GB)

(54) **System and method for adjusting communications over signal lines**

(57) A method and apparatus are provided for the automated calibration of I/O over a multi-variable eye window. A transmitter conducts data transmissions to a receiver of an integrated circuit (IC) over a plurality of signal lines. The data transmissions are conducted according to certain parameters or sets of parameters, which may include voltage levels at which signals are transmitted or timing delays. The receiver determines

whether the correct data value was received over each signal line. The results are recorded in a storage mechanism in the same IC as the receiver. The storage mechanism may, for each signal line, store a pass/fail result corresponding to the particular parameters for the data transmission. The system selects the parameters with which subsequent transmissions are to be conducted over each of the plurality of signal lines from the storage mechanism.

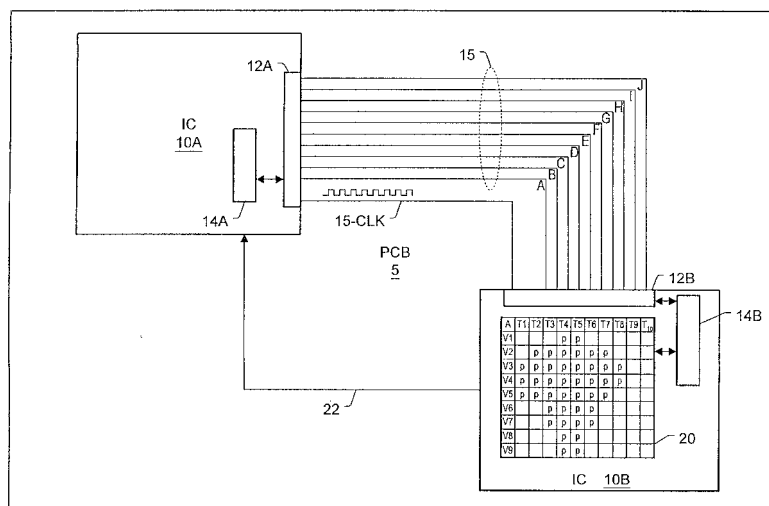


Fig. 3

Description

Field of the Invention

[0001] This invention relates to electronic systems, and generally to the optimization and margin characterization of signal lines.

Background of the Invention

[0002] In the design and operation of high-speed digital systems, such as computer systems, skew occurring on signal lines is one important consideration. Skew may be defined as timing differences between signals due to various propagation delays. In order for data to be received at the correct value, it must be latched into a receiver at a certain time, at a certain voltage level. One timing difference of critical importance in digital systems is the timing difference that may exist between clock signals and data signals. These timing differences may occur for a number of reasons, such as varying signal line lengths, electrical characteristics of individual signal lines, and so on.

[0003] Figure 1 is a drawing of an exemplary printed circuit board (PCB) having two integrated circuits (IC) coupled by a plurality of signal lines. PCB 5 includes IC's 10A and 10B. IC's 10A and 10B include data ports 12A and 12B, respectively. Data ports 12A and 12B are coupled to each other by a plurality of signal lines 15. Due to space limitations, signal lines 15 must be routed in the manner shown in the drawing. Due to this routing, some of signal lines 15 are significantly longer than others. Signals traveling along the longer signal lines may take longer to travel between the two data ports. In some cases, data transfers between the two ports may be required to be performed in parallel. Thus, the receiving data port must latch the data from all lines simultaneously. Thus, since the data must be latched simultaneously, the timing differences between the various signal lines becomes critical.

[0004] Calibrating I/O lines may include tuning voltage levels and timing delays so that a signal is sampled within an enclosed area of an eye pattern. An exemplary eye pattern is shown in Figure 2. The eye pattern may be plotted as an area on a graph of voltage vs. time (setup time, hold time), with voltage on the vertical axis and time on the horizontal axis. The contiguous enclosed regions within the lines may represent the area in which data may be accurately latched into a receiver. Ideally, signal sampling will occur in the middle of the eye pattern, at a point where both the voltage level and the setup/hold time allow for a large margin of operation for these parameters. Optimizing the reception of such signal transmissions may include tuning the voltage offset levels and tuning delay times as to ensure that the signal arrives at the receiver at a voltage level of sufficient magnitude. Optimizing the reception may also include adjusting a timing delay for sampling the signal in order

to ensure that the setup and hold times are sufficient to properly receive the data. This may be performed for clock synchronous or source synchronous systems, but may have a greater impact on source synchronous systems, which typically operate at higher clock frequencies and with smaller margins of operation.

[0005] Sampling at points other than the middle of the eye pattern may reduce the margin of operation for either the voltage or setup/hold time. For example, if the voltage at which the signal is sampled is at a level that is above the midpoint, the margin of operation of the delay time may be less. Similarly, if a signal is sampled at a setup/hold time that is at a point other than the midpoint, the margin of operation of the voltage may be less. Furthermore, changing the voltage levels may affect the setup/hold times, and changes to the setup/hold times may affect the voltage levels. Thus, tuning both the voltage levels and delay times may involve the balancing of potentially conflicting requirements.

[0006] The calibrating of I/O lines may often times be performed during the design verification phase for an electronic system. This may involve a manual process of setting the voltage and timing delays for signal transmissions that occur in the system. Typically, these parameters, once set, do not change throughout the operating life of the system. Thus, changes in the operating conditions of the system may result in lower margins of operation for the voltage levels and/or the timing delays.

Summary of the Invention

[0007] A method and apparatus are provided, as set out in the appended claims, which may be used in the automated calibration of I/O over a multi-variable eye window. In one embodiment, a transmitter conducts data transmissions to a receiver over a plurality of signal lines. The transmitter and the receiver may be part of a single integrated circuit (with the transmitter and receiver coupled by signal lines which loop back), or may be located on separate integrated circuits. In some embodiments, either the transmitter or the receiver may be part of a test system.

[0008] In one embodiment, the data transmissions are conducted according to a certain set or sets of parameters that include voltage levels at which signals are transmitted (i.e. a voltage level for a logic one and a second voltage level for a logic zero), voltage threshold levels for which received signals are recognized as a logic one or logic zero, and timing delays. The receiver receives the data transmissions, and latches in the transmitted data according to the set parameters. After receiving the data, the receiver determines whether the correct data value or sequence of patterns was received over each signal line. The results of this determination are recorded in a storage mechanism, such as a table of entries stored within the IC in which the receiver is located. The table stores, for each signal line, a pass/fail result corresponding to the particular parameters un-

der which the data transmission occurred. The table may comprise a plurality of entries of pass/fail results corresponding to data transmissions over individual signal lines. The system selects the parameters with which subsequent data transmissions are to be conducted over each of the plurality of signal lines from the table.

[0009] In one embodiment, the system is configured to select a particular set of parameters for each signal line over which data is to be transmitted. The set of parameters for a given signal line may then differ from the parameters selected for other signal lines. As previously noted, the set of parameters may include voltage levels for each data value (e.g. logic zero and logic one) and may also include a delay time. The voltage levels may be set by an adjustable voltage source in the transmitter, which includes separate voltage levels for each signal line in this embodiment. Alternatively, logic voltage offset (or threshold) levels (i.e. those levels for which the receiver recognizes a signal to be a logic 0 or logic 1) may be adjusted by the receiver. The delay time may also be adjusted by the receiver, or in some embodiments, the transmitter. Thus, it may be possible to adjust both the voltage level and the delay time for each individual signal line (at either the receiver or transmitter, depending upon the embodiment) in order to get the sampling point at or near the middle of the eye pattern.

[0010] In another embodiment, some parameters may be adjusted for a group of lines. For example, a transmitter may include only one adjustable voltage source for a group of signal lines. Thus, the voltage is adjusted for each of the signal lines associated with the transmitter simultaneously in order to provide the voltage setting that gives the best margin for these signal lines. Similarly, a receiver may be configured to adjust voltage threshold levels for each of its signal lines individually, or may adjust all of its associated signal lines simultaneously. In such embodiments, the system chooses a set or sets of parameters from the table (stored in the same IC as the receiver) that allows signals to be sampled for all lines such that all signals are sampled within the eye pattern. In some cases, if the group of signal lines are of equal lengths, or if the delay time is such that a receiver may sample signals from each signal line associated with it within the eye pattern, a parameter set common to all lines may be chosen. In such cases, the voltage levels and the delay time are common for all signal lines associated with the respective transmitter and receiver. Parameters may also be adjusted at a chip level for some embodiments. Optimization may be performed based on worst case scenarios to provide the best possible margin across a set of signals that share a common parameter.

[0011] As previously noted, the table of entries or other type of data structure may be stored in the IC in which the receiver is located, and may include transmission or reception parameters for each of the signal lines associated with the receiver. In other embodiments, the table of entries is stored in the IC in which the transmitter is

located. In one embodiment, the table includes a plurality of rows and columns, where each row and each column represents a parameter. Each table may correspond to a single signal line, although storage mechanisms having other types of data structures may also be used. At each row-column intersection, a pass indicator is present, indicating whether or not the receiver associated with the particular signal line (represented by the table) is able to correctly read the data value or sequence of patterns for the particular set of parameters (represented by the rows and columns of the table). In some embodiments, the table may be compressed down in size to include only those entries for which a passing result was obtained. The table may be further compressed to include only results for the beginning and end of the largest range of passing results.

[0012] In various embodiments, the data structure may be multi-dimensional. For example, a table may include columns corresponding to voltage levels, rows corresponding to delay times, and a third dimension that corresponds to a third parameter, such as termination. Thus, each element of the data structure may correspond to a voltage level and a delay time for a given signal line. It should be noted that additional parameters may also be included (as will be discussed below), and thus the data structure may include any number of dimensions. The data structure may take on any shape or organization (e.g. a cube, etc.) as necessary. As with the table, such a data structure may be compressed in size. The use of a multi-dimensional data structure may help optimization among a larger number of variables.

[0013] Parameters may be selected from the table using one of several different search algorithms available. Such search algorithms include, but are not limited to, linear or binary searches, searches based on first pass and first fail after pass (FP/FFAP), or largest margin of operation for one or more parameters.

[0014] Thus, in various embodiments, the system and method for automated calibration of I/O over a multi-variable eye window may allow signal lines for a receiver to be calibrated so that signal sampling occurs within the parameters defining an eye window. The calibration may be automatically performed at various times (such as system start-up), and may be re-performed if necessary. A table associated with the receiver may allow for the system to selectively calibrate each signal line individually, or calibrate groups of signal lines relative to one or more parameters.

Brief Description of the Drawings

[0015] Various preferred embodiments of the invention will now be described in detail by way of example only, with reference to the following drawings:

Figure 1 is a drawing of an exemplary printed circuit board having two integrated circuits (IC's) coupled by a plurality of signal lines;

Figure 2 is a drawing illustrating an exemplary eye pattern;

Figure 3 is a drawing of one embodiment of a printed circuit board having two IC's, wherein the second IC includes a table;

Figure 4 is a drawing of one embodiment of a table such as included in Figure 3, configured to store test results for signal transmissions; and

Figure 5 is a flowchart of a method in accordance with one embodiment of the present invention for the automated calibration of I/O lines.

Detailed Description

[0016] Turning now to Figure 3, a drawing of one embodiment of a printed circuit board having two IC's, wherein the second IC includes a table is shown. PCB 5 includes a first IC 10A and a second IC 10B, coupled by a plurality of signal lines 15. The embodiment shown includes 10 signal lines, 15A through 15J, which provide electrical coupling between IC 10A and IC 10B through transmit port 12A and receiver port 12B. The embodiment shown is a source synchronous I/O system, and thus clock line 15-CLK is used to provide a clock signal for synchronizing data transmissions. (It will be appreciated that a range of timing mechanisms may be used in other embodiments, which are not necessarily all source synchronous).

[0017] In the embodiment of Figure 3, transmitter 12A generates a clock signal which is received by receiver 12B, which latches data received over the signal lines on one of the clock edges. Other communications links, such as communications link 22 are present and allow second IC 10B to send information to first IC 10A. Communications link 22 may include one or more signal lines.

[0018] First IC 10A also includes a control unit 14A, and second IC 10B includes control unit 14B. Control units 14A and 14B provide control functions to transmitter 12A and receiver 12B, respectively, and may be utilized in determining and setting the parameters for communications between the two IC's. In an alternative embodiment, a third device known as a service processor is present. The service processor reads information from first IC 10A and/or second IC 10B, and may also adjust parameters for these devices.

[0019] First IC 10A is configured to transmit data to second IC 10B through transmitter 12A. In the embodiment of Figure 3, transmitter 12A is a source synchronous transmitter, and generates a clock signal, which is conveyed to second IC 10B via clock line 15-CLK. Transmitter 12A in the embodiment shown is coupled to signal lines 15A through 15J, and conducts data transmissions over these lines.

[0020] Transmitter 12A may include one or more adjustable voltage sources. In one particular embodiment, transmitter 12A includes a separate adjustable voltage source for each signal line. In another embodiment, a

single adjustable voltage source is common to all signal lines associated with the transmitter 12A. The adjustable voltage sources are configured to control the voltage levels at which data signals are transmitted from transmitter 12A, for example, by setting voltage levels for logic one signals and logic zero signals. If necessary, the voltage levels for the data signals may be adjusted in order to ensure that the data signals are sampled within the parameters defining an eye pattern. In one embodiment, control unit 14A is utilized to set the voltage levels for the data signals based on information received from second IC 10B through communications link 22. Control unit 14A may also be utilized to set the voltage levels of various parameter sets when conducting transmissions, in order to determine the optimal parameters or sets of parameters for conducting subsequent data transmissions. Furthermore, other parameters (e.g. delay shifting) may be set or adjusted at transmitter 12A.

[0021] Second IC 10B includes receiver 12B, which is configured to receive data transmissions from transmitter 12A of first IC 10A via signal lines 15A through 15J. In the embodiment shown, receiver 12B is a source synchronous receiver, and thus is configured to receive a clock signal transmitted over clock line 15-CLK. This clock signal is used to synchronize the latching of received data transmissions. Receiver 12B may also be configured to adjust timing delays for receiving signals. For example, if receiver 12B is receiving data in parallel over signal lines 15A - 15J, it may delay the latching of signals received on one or more of the shorter signal lines (15A, 15B, etc.) in order to ensure that the signals are all latched simultaneously. Thus receiver 12B may include at least one digital locked loop (DLL), which may be configured to adjust a phase shift for each signal line. Alternatively, receiver 12B may include an analog phase locked loop (PLL) instead of the DLL. In one embodiment, receiver 12B includes a separate DLL for each signal line, while other embodiments include a single DLL configured to adjust the timing delay for a plurality of signal lines. In embodiments utilizing a single DLL for multiple signal lines, the DLL may be configured to adjust the phase shift (and thus the time delay) on an individual basis for each associated signal line. By adjusting the delay time, the DLL of receiver 12B helps to ensure that the setup time and hold time are sufficient to enable data transmissions to be sampled within the parameters that define the eye pattern.

[0022] PCB 5 may be configured to perform automated calibration of signal lines 15. To perform the calibration, data transmissions are conducted between first IC 10A and second IC 10B according to a set of parameters, including voltage levels and time delays. First IC 10A transmits data through transmitter 12A according to parameters including voltage levels for logic 1's and 0's. Second IC 10B is configured to receive data according to parameters including a timing delay and a reference voltage.

[0023] During the calibration, first IC 10A transmits a

plurality of test vectors for each set of parameters, ensuring that receiver 12B is required to sample a plurality of logic 1's and logic 0's. Second IC 10B latches data in through receiver 12B for each test vector transmitted, and keeps track of the results, including determining whether receiver 12B reads the correct data values on each signal line. Control unit 14B can then be used to perform comparison functions for the received data. In one embodiment, the test vectors and order of transmission are stored or generated in second IC 10B. It should be noted that test vectors may also be calculated by invoking a built-in self-test or other method, which could then eliminate the need for test vector storage.

[0024] Control unit 14B compares the latched data from each data transmission received from first IC 10A with the expected results defined by the stored or generated test vectors. Control unit 14B then also writes pass/fail results and other information into table 20, and may be further utilized to adjust the delay time or other receiver parameters for subsequent transmissions of test vectors and normal data transmissions.

[0025] In order for data to be latched into receiver 12B at the correct logic value, it must be latched in with the scope of parameters that define the eye pattern. Upon completion of the data transmissions according to the set of parameters, second IC 10B records the results for each signal line in a table 20 (or other data structure), as noted above. At least a pass/fail status for each signal line and the parameter set is recorded in table 20. In the embodiment shown, table 20 corresponds to signal line 15A, and includes test results for various voltage threshold and delay time settings. Test results are stored for each of the remaining signal lines in additional ones of table 20, wherein each signal line has its own corresponding table. Various embodiments of table 20 will be discussed in further detail below.

[0026] After conducting transmissions according to a first set of parameters, the process may be repeated for a second set of parameters. The second set of parameters may include different voltage levels and/or different timing delays. Again, a plurality of test vectors are transmitted through transmitter 12A, and are then received by receiver 12B. After completing the data transmissions, the results may again be recorded in table 20 for each signal line, along with the corresponding set of parameters under which the transmissions occurred. The process may then be repeated for as many different parameters or parameter sets as necessary.

[0027] Based on the results obtained from conducting transmissions according to a number of parameter sets, second IC 10B (or a service processor in some embodiments) selects a parameter set or sets for which transmissions are to be conducted during normal operations. Selection of the parameter set or sets may be based in part on the configuration of both transmitter 12A and receiver 12B. For example, if transmitter 12A includes only one adjustable voltage source for the plurality of signal lines, then the same logic voltage levels will be selected

for each line. Conversely, if transmitter 12A includes separate adjustable voltage sources for each signal line, logic voltage levels which provide the most margin of operation within the eye pattern may be selected for each individual signal line. Similarly, if the DLL configuration of receiver 12B permits, time delays may be individually selected for each signal line 15 in order to provide sufficient margin of operation for setup time and hold time.

[0028] Second IC 10B may provide information to first IC 10A through communications link 22 for parameters controlled or set by first IC 10A (e.g. voltage levels). Alternatively, the parameters may be controlled or set by a service processor or external master chip that is separate from first IC 10A and second IC 10B. In general, parameters may be controlled and selected by a receiver, a transmitter, or a service processor, or various combinations of these elements may be used to control and select parameters.

[0029] In some cases, it may be necessary to re-calibrate signal lines 15. In such cases, PCB 5 is configured to allow the calibration procedure to be rerun. In various embodiments, the calibration procedure may be rerun during a system startup or initialization routine, or may be run in conjunction with a BIST (built-in self-test). In general, the automated calibration routine is run at any time necessary in order to ensure the integrity of data received over one or more signal lines. Furthermore, some embodiments may allow for the tracking of a change history for the margins of operation for each signal line. Tracking the changes in margin of operation over time for each signal line then allows for predictions of future performance or pending failure of a device associated with those signal lines for which tracking is performed.

[0030] It should be noted that PCB 5 may include integrated circuits other than those shown here, and thus both first IC 10A and second IC 10B may include further transmitters and receivers. Thus each IC on PCB 5 may include a number of transmitters and receivers, enabling communications between the various IC's mounted on PCB 5. Tables such as table 20, or other storage mechanisms, may then be implemented in any IC that is configured for automated calibration. Multiple tables (or other types of data structures which comprise the storage mechanism), each corresponding to a communications port, may be implemented for IC's having multiple communications ports, while in some other embodiments, a single table may be configured to store information for more than one communications port. Some IC's may include communications ports that are configured for both transmitting and receiving data. It should also be noted that, while the embodiments shown here are configured for source synchronous I/O, other embodiments that do not use source synchronous I/O are contemplated. For example, the voltage threshold setting may be adjusted for two or more devices synchronized to a single clock. Changing the voltage threshold setting in such a system

may then affect the margin of operation for each of the two or more devices synchronized to the single clock.

[0031] Moving now to Figure 4, a drawing of one embodiment of a table configured to store test results for signal transmissions is shown. In the embodiment shown, table 20 stores test results for a single signal line (signal line A), although in other embodiments, types of data structures other than a table are possible. Table 20 includes columns (T1 - T10) corresponding to a first parameter (e.g. delay time). Table 20 also includes a plurality of rows (rows V1-V11 in this example), wherein each of the rows corresponds to a second parameter (e.g. voltage threshold). Table 20 may also be a multi-dimensional data structure for three or more parameters. There is no theoretical limit to the number of dimensions in table 20, and the size of table 20 may be adjusted depending upon the particular implementation.

[0032] Each parameter set for which rows, columns, or additional dimensions are implemented may include voltage levels for signal transmissions, time delays, and other parameters, as discussed above. Other parameters in addition to the voltage threshold levels and time delays may include termination (i.e. resistance of terminating resistors), signal drive strength, and pre-emphasis (strength pre-emphasis or delay pre-emphasis) or other signal shaping approaches.

[0033] Table 20 includes a plurality of cells at each row-column intersection. Each cell includes information on the performance of signal transmissions over the corresponding signal line for the corresponding parameter set. In the embodiment shown, some cells include pass information, indicating the signal line passed the particular test for the parameter set represented by the row column intersection. A signal line may be considered to pass a test for a particular set of parameters if it successfully reads the correct data value for each data value transmitted over that line during the transmission of test vectors (or, in some embodiments, if the bit error rate is acceptable).

[0034] During the calibration procedure, signal lines may be tested by transmitting a number of test vectors from first IC 10A to second IC 10B, where each test vector includes a plurality of logic 1's and logic 0's to be transmitted over each signal line during each test. If a receiver 12B reads the correct logic value for each transmission over a given signal line (or reads data values within an acceptable bit error rate), the signal line may be considered to have passed the test for the parameter set, and thus a pass indication may be written into the corresponding cell.

[0035] In some embodiments, a fail indication may be written into the cell if the corresponding signal line does not pass a test for a particular parameter set. In other embodiments, such as that shown, the mere absence of a pass indication may be used to indicate that the corresponding signal line did not pass a test for the particular parameter set.

[0036] In other embodiments, only passing results are

kept. In such embodiments, the table or other storage mechanism may be compressed in size. For example, in one embodiment, a table may be compressed to include all passing results, but no failing results. In another embodiment, the table may be compressed to include only passing results that have a certain margin of operation for one or more of the parameters (e.g. the table may be compressed to include the largest contiguous range of passes for one or more of the parameters).

[0037] In embodiments where the table is compressed to store only a range of passes, it may be possible to compress the table further, storing only those parameters which represent the starting and ending points for the range of passes without storing any of the intermediate values. The starting and ending points may be represented respectively by a first passing result within a range and the first failing result subsequent to the first passing result. (The ending point may also be represented by the last passing result in the range).

[0038] After results have been recorded for each signal line and parameter set, selection of a particular parameter set is performed for each signal line. The selection of parameter sets for signal lines is based on factors such as the physical configuration of the signal lines, the transmitter, and the receiver. For example, on the transmitter side, if a plurality of signal lines is associated with a single adjustable voltage source, the voltage levels for the data signals to be transmitted will be set to the same level for each of the associated signal lines. Conversely, if each signal line is associated with a separate adjustable voltage source, the voltage levels for data signals transmitted over each of the signal lines may be adjusted separately, allowing a greater degree of control. In general, some embodiments may allow for the selection of parameters for each signal line individually, while some embodiments may allow for the selection of parameters for groups of signal lines.

[0039] On the receiver side, the time delays may be adjusted on an individual basis for each signal line in some embodiments, or may be adjusted for all signal lines on a group basis in others. In one embodiment, a separate DLL (or PLL) may be dedicated to each individual signal line, and thus the time delay for that signal line may be adjusted for its associated signal line without affecting the other signal lines. In other embodiments, a single DLL may be associated with a group of signal lines, and thus adjusts the timing delay for each signal line simultaneously. In some embodiments, it may also be possible to adjust the timing delays on the transmitter side.

[0040] Various selection algorithms may be used to determine the parameters used for transmissions across each signal line. In one embodiment, selection algorithms are executed by control unit 14B. One selection algorithm may include scanning rows or columns in a table associated with a particular signal line. The row or column is scanned to ascertain the first passing set of parameters for the associated signal line, and the first

failing set that occurs after encountering the first passing set. A point at or near the midway point between the first pass and first fail after pass may be selected for the parameter set for subsequent transmissions over that particular signal line. However, the algorithm should also ensure that any other transmission parameters meet at least minimum margin requirements.

[0041] Some selection algorithms may prioritize one parameter over another in making a selection for subsequent transmission. For example, voltage may be prioritized as a parameter over delay time (or clock-to-data skew) in order to ensure an optimal amount of operating margin for voltage, while ensuring that at least a minimum margin is met for delay time. In another example, delay time may be prioritized over voltage in order to ensure an optimal margin for delay time, while ensuring that at least a minimum margin is met for voltage.

[0042] Additional information may be considered when selecting parameter sets for signal lines. Some algorithms may consider information concerning margin of operation in choosing a parameter set. For example, if choosing between parameter set 5 or parameter set 6 for signal line G, the selection algorithm may select the parameter set having the larger margin of operation for a given parameter. In another example where a common parameter set is chosen for the group of signal lines of Figure 4, an average margin of operation may be computed for one or more parameters for the plurality of signal lines. The parameter set chosen may be that which has the greatest average margin of operation.

[0043] In some cases, a given signal line may not pass for any parameter set. This may be an indication of a broken signal line or a faulty transmitter or receiver. This information may be provided to a user for troubleshooting purposes.

[0044] Table 20 (or other data structures) may be stored in memory circuitry within an IC. Types of memory circuitry in which table 20 may be stored include DRAM, SRAM, registers, and flash memory.

[0045] Turning now to Figure 5, a flowchart for one embodiment of a method for the automated calibration of I/O lines is shown. Method 50 begins with the setting of voltage levels or voltage threshold levels (Operation 52). In some embodiments, voltage threshold levels may be set by a receiver, such as receiver 12B of Figure 3. The voltage threshold levels typically include the minimum voltage level for which the receiver will recognize a data bit to be a logic high (or logic 1) and the maximum voltage level for which the receiver will recognize a logic low (or logic 0). In some embodiments, the receiver may be able to adjust the voltage threshold levels individually for each line, while in other embodiments, the receiver may adjust the voltage threshold levels for a plurality of signal lines. Some embodiments may allow for the setting of voltage transmission levels at the transmitter (including settings for transmissions with pre-emphasis) by an adjustable voltage source.

[0046] In Operation 54, skew between the clock sig-

nals and data signals is adjusted by a receiver, such as receiver 12B of Figure 3, which is coupled to the transmitter by a plurality of signal lines. The receiver (or, in some embodiments, the transmitter) may be able to adjust the skew between the clock and data signals individually for each of its associated signal lines, or may adjust skew for a plurality of signal lines. The adjustment of the skew can be used to determine a point in time within a clock cycle when signals are sampled by the receiver. The skew may also determine the margins of operation for setup time and hold time for the sampled signals. In one embodiment, the skew may be adjusted by one or more DLL circuits (or PLL circuits) associated with the receiver, whereby the skew is adjusted by adjusting timing delays within the DLL. Timing delays may be adjusted by time-shifting the clock signals, the data signals, or both.

[0047] With the voltage levels and skew set, the transmitter begins transmitting data to the receiver (Operation 56). The transmitted data typically comprise test vectors. A plurality of test vectors may be transmitted by the transmitter, to allow the receiver to sample a number of logic 1's and logic 0's. For each test vector transmitted by the transmitter and received by the receiver, a control unit or other circuitry in the IC of the receiver keeps track of whether or not correct data values are latched into the receiver.

[0048] After completing the transmission of the test vectors for the particular voltage levels and delay times, pass/fail information is recorded in a table or other storage mechanism (Operation 58). The pass/fail information may then be used to select parameters for subsequent data transmissions. The selection may be made for individual circuit lines, or for a plurality of circuit lines.

[0049] In Operation 60, a determination is made as to whether more transmissions of test vectors are to be made. If it is desired to test and or calibrate the circuitry according to additional transmission and reception parameters, additional transmissions may be made, and thus the method may return to Operation 52.

[0050] If no additional transmissions are to be made, the method then performs a selection algorithm in order to select the various parameters for which data transmissions are to be conducted under normal operations (Operation 62). Various selection algorithms may be used to select parameters for transmissions, and may depend upon the configuration of the devices involved. Some embodiments may allow for the adjusting of parameters for each signal line individually. For example, the table of Figure 4 may include test results for a signal line which may be individually tuned. If the parameters to be adjusted are voltage and delay time, a selection algorithm may select either voltage V5 or V6, and either delay time T4 or T5 to provide the maximum amount of operating margin for both of these parameters. The selection of these parameters allows for signals to be sampled at or near the center of the eye pattern, and provides a large margin of operation.

[0051] In other embodiments, parameters are adjusted for a group of signal lines. In such embodiments, parameters may be prioritized to allow for larger margins of operation for the prioritized parameter, while meeting at least minimum requirements for the remaining parameters.

[0052] Parameters may be selected from the tables or other data structures using one of several different search algorithms available to the system. Such search algorithms include, but are not limited to, linear or binary searches, searches based on first pass and first fail after pass (FP/FFAP), or largest margin of operation for one or more parameters.

[0053] It should be noted that while the various embodiments of the system and the method described above include a first IC (having a transmitter) and a second IC (having a receiver), embodiments are also contemplated having only a single IC. Such a single IC embodiment may include both a transmitter and a receiver, and may further include a table such as shown in Figure 4. In this case, the method involves data transmissions from the transmitter of the IC to the receiver of the IC. It should also be noted that many IC's may include multiple transmitters and/or receivers. Furthermore, the method may also be performed by conducting data transmissions between a chip and automated test equipment.

[0054] Various other aspects of the invention are also disclosed in the following numbered clauses:

1. A system comprising:

a transmitter;
a receiver coupled to the transmitter by a plurality of signal lines;
wherein the transmitter is configured to conduct a plurality of data transmissions over the plurality of signal lines;
wherein the receiver is configured to:

receive the data transmissions and to sample data into the receiver according to different parameters; and
determine whether a correct data value is received by the receiver for each data transmission;

and wherein the system is further configured to:

store data transmission results in a storage mechanism, wherein the data transmission results are indicative of whether correct data values were received for the data transmissions; and
select parameters for each of the plurality of signal lines for subsequent data transmissions based on the data transmission results.

2. The system as recited in clause 1, wherein the different parameters include different delay times at which data is sampled by the receiver.

3. The system as recited in clause 1 wherein the different parameters include different sampling voltage threshold levels.

4. The system as recited in clause 1, wherein the transmitter and the receiver are both embodied in a single integrated circuit.

5. The system as recited in clause 1, wherein the transmitter is embodied in a first integrated circuit, and the receiver is embodied in a second integrated circuit.

6. The system as recited in clause 1, wherein selecting parameters for each of the plurality of signal lines includes selecting a unique set of parameters for each of the plurality of signal lines.

7. The system as recited in clause 1, wherein selecting a set of parameters for each of the plurality of signal lines includes selecting a common parameter for a plurality of signal lines.

8. The system as recited in clause 1, wherein the different parameters determine a point in an eye pattern at which a signal is sampled.

9. The system as recited in clause 1, wherein the delay time determines a margin of operation for set-up time.

10. The system as recited in clause 1, wherein the delay time determines a margin of operation for hold time.

11. The system as recited in clause 1, wherein a data value is considered correct if the data value is received in an area defined by the parameters of an eye pattern.

12. The system as recited in clause 1, wherein the receiver is configured to provide an indication to the transmitter of a voltage level for subsequent data transmissions.

13. The system as recited in clause 1, wherein the receiver is configured to adjust voltage threshold levels, wherein the voltage threshold levels determine a voltage level at which the receiver will recognize a logic high and a voltage level at which the receiver will recognize a logic low.

14. The system as recited in clause 1, wherein the storage mechanism is a table, and wherein the table

is configured to store transmission results for each of the plurality of signal lines according to each of the parameters for which transmissions are conducted.

15. The system as recited in clause 14, wherein the table is stored in a set of registers coupled to the receiver.

16. The system as recited in clause 14, wherein the table is stored in a dynamic random access memory (DRAM) coupled to the receiver.

17. The system as recited in clause 14, wherein the table is stored in a static random access memory (SRAM) coupled to the receiver.

18. The system as recited in clause 1 wherein the transmitter is a source synchronous transmitter and the receiver is a source synchronous receiver.

19. The system as recited in clause 18, wherein the source synchronous transmitter includes an adjustable voltage source, wherein the adjustable voltage source is configured to generate a voltage level at which signals are to be transmitted over one or more of the plurality of signal lines.

20. The system as recited in clause 18, wherein the source synchronous receiver is configured to adjust a timing delay for each of the plurality of signal lines, wherein adjusting the timing delay determines a point in time at which a signal received over one or more of the plurality of signal lines is sampled.

21. The system as recited in clause 1, wherein the transmitter and the storage mechanism are located within the same integrated circuit.

22. The system as recited in clause 1, wherein the receiver and the storage mechanism are located within the same integrated circuit.

23. The system as recited in clause 1, wherein the system includes a service processor, wherein the service processor is configured to select parameters for each of the plurality of signal lines for subsequent data transmissions based on the data transmission results.

24. The system as recited in clause 1, wherein the system includes a plurality of devices, wherein each of the devices is synchronized to a single clock.

25. The system as recited in clause 24, wherein the transmitter is located in a first device, and the receiver is located in a second device.

26. The system as recited in clause 24, wherein the transmitter and the receiver are both located in a single device.

27. The system as recited in clause 14, wherein the table is compressed to store only passing results.

28. The system as recited in clause 14, wherein the table is compressed to store only starting and ending points for a range of passes.

29. An integrated circuit comprising:

a receiver port, the receiver port coupled to a plurality of signal lines, wherein the receiver port is configured to receive data transmissions over the plurality of signal lines from a transmitter port, wherein the data transmissions include one or more test vectors;

a storage mechanism, the storage mechanism configured to store results obtained from the reception of test vectors transmitted by the transmitter port, wherein the results are indicative of whether a correct data value was received for test vector; and

a control unit coupled to the receiver and the storage mechanism, wherein the control unit is configured to select parameters from the storage mechanism for subsequent data transmissions from the transmitter.

30. The integrated circuit as recited in clause 29, wherein the parameters include different delay times at which data is sampled by the receiver port.

31. The integrated circuit as recited in clause 29, wherein the parameters include different sampling voltage threshold levels.

32. The integrated circuit as recited in clause 29, wherein the integrated circuit comprises the transmitter port.

33. The integrated circuit as recited in clause 29, wherein a remote integrated circuit comprises the transmitter port.

34. The integrated circuit as recited in clause 29, wherein the receiver is coupled to the transmitter by a plurality of signal lines.

35. The integrated circuit as recited in clause 29, wherein the control unit is configured to select parameters unique to each signal line for each of the plurality of signal lines.

36. The integrated circuit as recited in clause 29, wherein the control unit is configured to select com-

mon parameters for all of the plurality of signal lines.

37. The integrated circuit as recited in clause 29, wherein the parameters determine a point within an eye pattern at which a signal is sampled.

38. The integrated circuit as recited in clause 29, wherein the storage mechanism is a table, wherein the table is configured to store transmission results for each of the plurality of signal lines according to each of the parameters for which transmissions are conducted.

39. The integrated circuit as recited in claim 38, wherein the table is stored in a set of registers.

40. The integrated circuit as recited in claim 38, wherein the table is stored in a dynamic random access memory (DRAM).

41. The integrated circuit as recited in claim 38, wherein the table is stored in a static random access memory.

[0055] In conclusion, while the present invention has been described with reference to particular embodiments, it will be understood that these embodiments are illustrative only. Accordingly, the skilled person will be aware of many other potential modifications and adaptations that fall within the scope of the claimed invention and its equivalents.

Claims

1. A method comprising:

performing a plurality of communications between a transmitter and a receiver according to different parameters;
determining whether a correct data value is received by the receiver for each of the plurality of communications;
storing data transmission results in a storage mechanism, wherein the data transmission results are indicative of whether correct data values were received for the plurality of communications; and
selecting designated parameters for each of the plurality of signal lines for subsequent communications between the transmitter and the receiver based upon the data transmission results.

2. The method as recited in claim 1, wherein the different parameters include different delay times at which data is sampled by the receiver.

3. The method as recited in claim 2, wherein the delay time determines a margin of operation for setup time.

5 4. The method as recited in claim 2, wherein the delay time determines a margin of operation for hold time.

5. The method as recited in any preceding claim, wherein the different parameters include different sampling voltage threshold levels.

10 6. The method as recited in claim 5, further comprising the receiver indicating to the transmitter a voltage level for subsequent communications.

15 7. The method as recited in claim 5 further comprising the receiver setting voltage threshold levels, wherein setting the voltage threshold levels determines a voltage threshold level for which the receiver will recognize a logic high and a voltage threshold level for which the receiver will recognize a logic low.

20 8. The method as recited in any preceding claim, wherein the transmitter and receiver are both embodied in a single integrated circuit.

25 9. The method as recited in any of claims 1 to 7, wherein the transmitter is embodied in a first integrated circuit, and the receiver is embodied in a second integrated circuit.

30 10. The method as recited in any preceding claim, wherein said selecting includes selecting a unique set of parameters for each of the plurality of signal lines.

35 11. The method as recited in any of claims 1 to 9, wherein said selecting includes selecting a common set of parameters for the all of the plurality of signal lines.

40 12. The method as recited in any preceding claim, wherein the different parameters determine a point in an eye pattern at which a signal is sampled.

45 13. The method as recited in claim 12, wherein a data value is considered correct if the data value is received within an area defined by the parameters of the eye pattern.

50 14. The method as recited in any preceding claim, wherein the storage mechanism is a table, wherein the table is configured to store transmission results for each of the plurality of signal lines according to each of the parameters for which transmissions are conducted.

55 15. The method as recited in claim 14, wherein the table

is stored in a set of registers in the second IC.

16. The method as recited in claim 14, wherein the table is stored in a dynamic random access memory (DRAM) in the second IC.

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17. The method as recited in claim 14, wherein the table is stored in a static random access memory (SRAM) in the second IC.

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18. The method as recited in any of claims 1 to 14, wherein a service processor is configured to monitor data transmissions between the transmitter and the receiver, and wherein the service processor further comprises the storage mechanism.

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19. The method as recited in any preceding claim, wherein the transmitter is a source synchronous transmitter and the receiver is a source synchronous receiver.

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20. The method as recited in claim 19 wherein the source synchronous transmitter includes an adjustable voltage source, wherein the adjustable voltage source is configured to generate a voltage level at which signals are to be transmitted over one or more of the plurality of signal lines.

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21. The method as recited in claim 19, wherein the source synchronous receiver is configured to adjust a timing delay for each of the plurality of signal lines, wherein adjusting the timing delay determines a point in time in which a signal received over one or more of the plurality of signal lines is sampled.

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22. A system comprising:

a transmitter;
a receiver coupled to the transmitter by a plurality of signal lines;
wherein the transmitter is configured to conduct a plurality of data transmissions over the plurality of signal lines;
wherein the receiver is configured to:

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receive the data transmissions and to sample data into the receiver according to different parameters; and
determine whether a correct data value is received by the receiver for each data transmission;

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and wherein the system is further configured to:

store data transmission results in a storage mechanism, wherein the data transmission results are indicative of whether correct data values were received for the data trans-

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missions; and

select parameters for each of the plurality of signal lines for subsequent data transmissions based on the data transmission results.

23. The system as recited in claim 22, wherein the transmitter and the storage mechanism are located within the same integrated circuit.

24. The system as recited in claim 22, wherein the receiver and the storage mechanism are located within the same integrated circuit.

25. The system as recited in claim 22, wherein the system includes a service processor, wherein the service processor is configured to select parameters for each of the plurality of signal lines for subsequent data transmissions based on the data transmission results.

26. The system as recited in any of claims 22 to 25, wherein the system includes a plurality of devices, wherein each of the devices is synchronized to a single clock.

27. The system as recited in claim 26, wherein the transmitter is located in a first device, and the receiver is located in a second device.

28. The system as recited in claim 26, wherein the transmitter and the receiver are both located in a single device.

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29. The system as recited in any of claims 22 to 28, wherein the storage mechanism is a table, and wherein the table is configured to store transmission results for each of the plurality of signal lines according to each of the parameters for which transmissions are conducted.

30. The system as recited in claim 29, wherein the table is compressed to store only passing results.

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31. The system as recited in claim 29, wherein the table is compressed to store only starting and ending points for a range of passes.

32. An integrated circuit comprising:

a receiver port, the receiver port coupled to a plurality of signal lines, wherein the receiver port is configured to receive data transmissions over the plurality of signal lines from a transmitter port, wherein the data transmissions include one or more test vectors;
a storage mechanism, the storage mechanism configured to store results obtained from the re-

ception of test vectors transmitted by the transmitter port, wherein the results are indicative of whether a correct data value was received for test vector; and

a control unit coupled to the receiver and the storage mechanism, wherein the control unit is configured to select parameters from the storage mechanism for subsequent data transmissions from the transmitter.

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33. The integrated circuit as recited in claim 32, wherein the integrated circuit comprises the transmitter port.

34. The integrated circuit as recited in claim 32, wherein a remote integrated circuit comprises the transmitter port.

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35. The integrated circuit as recited in claim 32, wherein the receiver is coupled to the transmitter by a plurality of signal lines.

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36. A system for implementing the method of any of claims 1 to 21.

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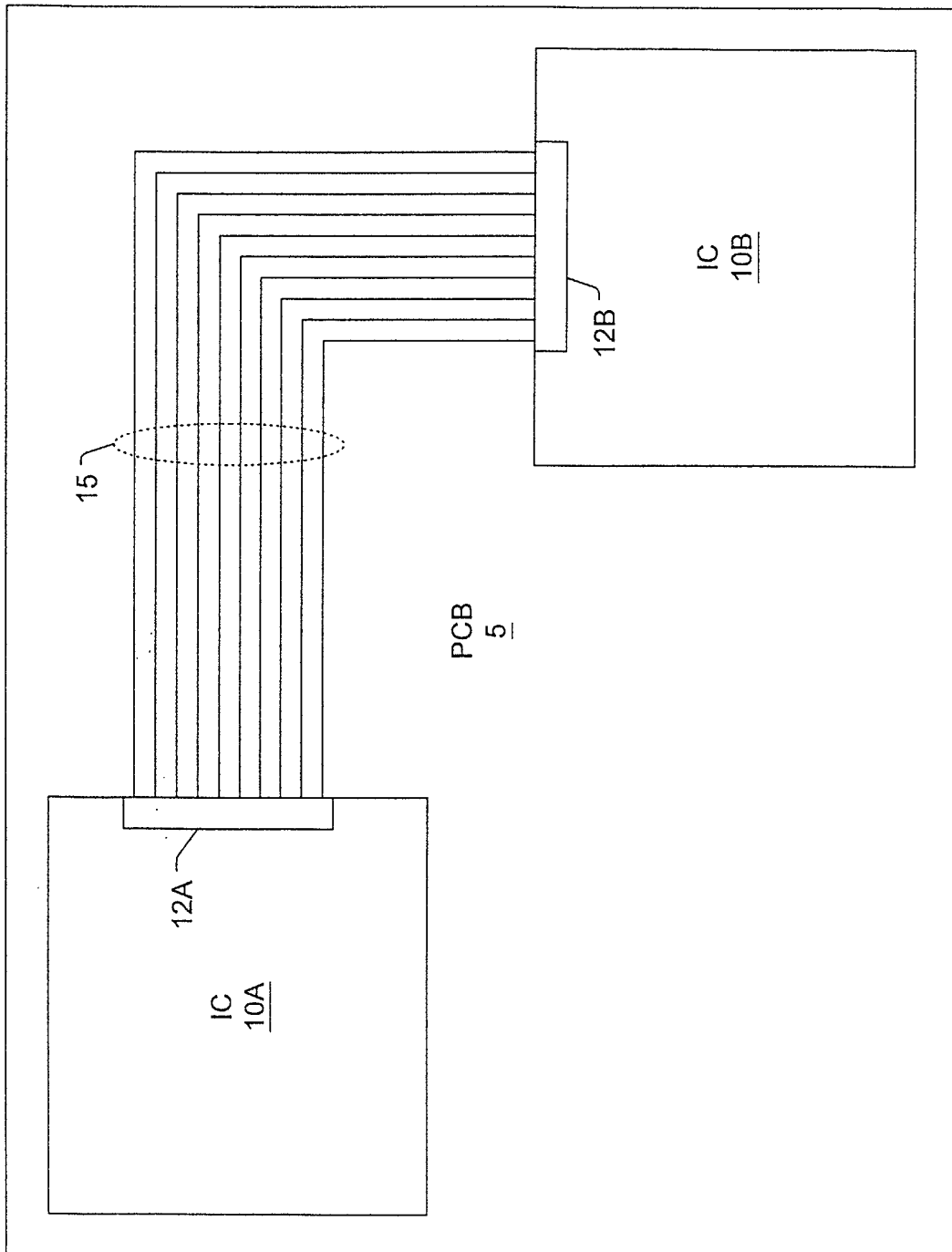


Fig. 1
(Prior Art)

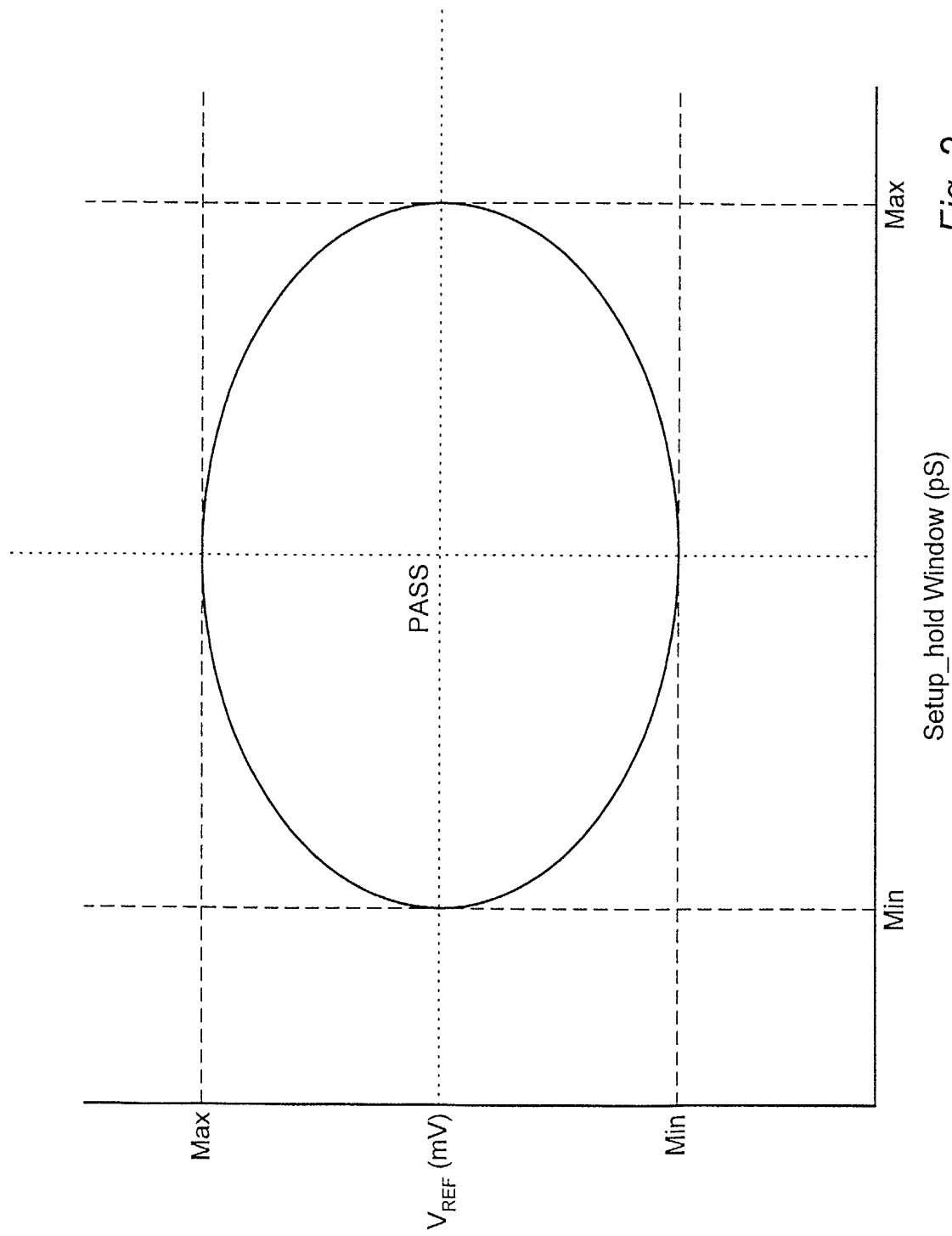


Fig. 2
(Prior Art)

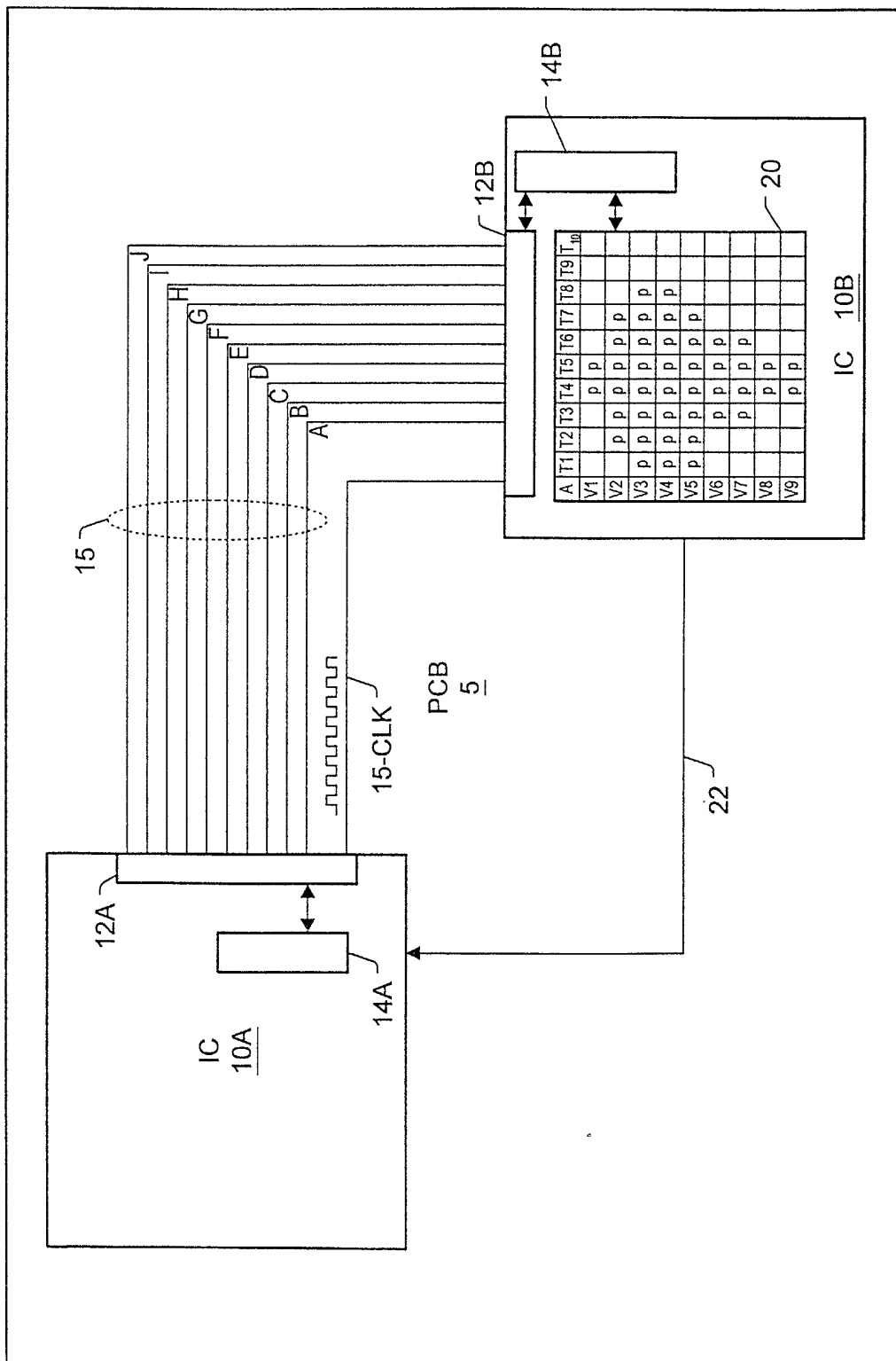


Fig. 3

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Signal Line A	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10
V1				p	p	p				
V2			p	p	p	p				
V3			p	p	p	p	p			
V4		p	p	p	p	p	p	p		
V5	p	p	p	p	p	p	p	p	p	
V6	p	p	p	p	p	p	p	p	p	p
V7		p	p	p	p	p	p	p	p	
V8		p	p	p	p	p	p			
V9			p	p	p	p	p			
V10			p	p	p	p	p			
V11			p	p	p	p				

Fig. 4

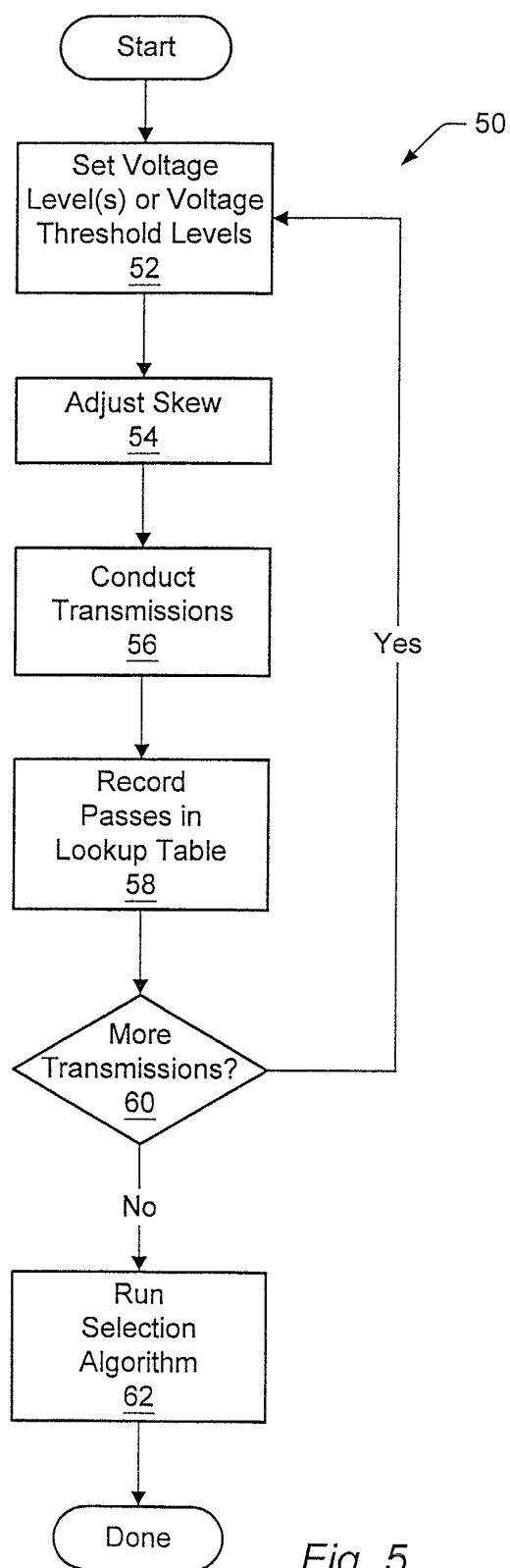


Fig. 5



European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 02 25 6425

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	US 6 041 419 A (LI KEN MING ET AL) 21 March 2000 (2000-03-21) * column 2, line 21 - line 62 * ----	1-4, 8-19, 21-36	G06F1/10
A	US 5 935 257 A (NISHIMURA KOICHI) 10 August 1999 (1999-08-10) * column 3, line 33 - column 4, line 41 * ----	1-36	
P,A	US 6 326 830 B1 (MOBERLY JERRY ET AL) 4 December 2001 (2001-12-04) * column 1, line 5 - line 58 * -----	1-36	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
			G06F
The present search report has been drawn up for all claims			
Place of search MUNICH		Date of completion of the search 5 February 2003	Examiner Juenger, B
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1503 03 82 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 02 25 6425

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
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05-02-2003

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 6041419	A	21-03-2000	WO	9961971 A1	02-12-1999
US 5935257	A	10-08-1999	JP	10320074 A	04-12-1998
			KR	248913 B1	15-03-2000
US 6326830	B1	04-12-2001	NONE		