We Claim:

1. A method for reducing access power in a memory array comprising: dynamically placing a group of memory cells in the memory array in a reduced power state; and dynamically enabling a selected group of the memory cells during an access operation on the selected memory cells.

2. The method of claim 1, wherein the access operation comprises a read.

3. The method of claim 1, wherein the access operation comprises a write.

4. The method of claim 1, wherein the memory cells include an 8 transistor Static Random Access Memory (8T SRAM) cell, such that forming the 8T SRAM cell comprises: forming a storage element; coupling a write word line and a pair of complementary write bitlines to the storage element through two write access transistors; and coupling the storage element to a read word line and a read bitline through two read access transistors.

5. The method of claim 4, further comprising, for a read operation, dynamically precharging selected read bitlines before and after the read operation on the 8T SRAM cell.

6. The method of claim 4, further comprising dynamically placing the read bitline in a floating state during an inactive mode of the 8T SRAM cell.

7. The method of claim 4, further comprising, for a write operation, dynamically precharging the pair of complementary bitlines before and after the write operation on the 8T SRAM cell.

8. The method of claim 4, further comprising configuring a tristate write driver to dynamically place the pair of complementary write bitlines in a floating state during an inactive mode of the 8T SRAM cell.

9. The method of claim 4, further comprising, during a light sleep mode, floating all read and write bitlines of the memory array.

10. The method of claim 1, wherein the group of memory cells belong to a set.

11. The method of claim 1, wherein the group of memory cells belong to a bank.

12. The method of claim 1, wherein an 8T SRAM cell comprises two or more read ports.

13. The method of claim 1, wherein the 8T SRAM cell comprises two or more write ports.

14. A method for reducing access power in a memory array comprising: dynamically placing write circuitry in a reduced power state; and dynamically enabling or disabling the write circuitry in response to a write request.

15. A memory array comprising: logic for dynamically placing a group of memory cells in the memory array in a reduced power state; and logic for dynamically enabling a selected group of the memory cells during an access operation on the selected memory cells.

16. The memory array of claim 15, wherein the access operation comprises a read.

17. The memory array of claim 15, wherein the access operation comprises a write.

18. The memory array of claim 15, wherein the memory cells include an 8 transistor Static Random Access Memory (8T SRAM) cell, such that the 8T SRAM cell comprises: a storage element; at least one write word line and at least one pair of complementary write bitlines coupled to the storage element through at least one pair of write access transistors; and at least one read word line and at least one read bitline coupled to the storage element through at least one pair of read access transistors.

19. The memory array of claim 18, further comprising a second write word line and a second pair of complementary write bitlines coupled to the storage element through a second pair of write access transistors; and a second read word line and a second read bitline coupled to the storage element through a second pair of read access transistors.

20. The memory array of claim 18, further comprising, logic for dynamically precharging selected read bitlines before and after a read operation on the 8T SRAM cell.

21. The memory array of claim 18, further comprising logic for dynamically placing selected read bitlines in a floating state during an inactive mode of the 8T SRAM cell.

22. The memory array of claim 18, further comprising, logic for dynamically precharging selected complementary bitlines before and after a write operation on the 8T SRAM cell.

23. The memory array of claim 18, further comprising a tristate write driver configured to dynamically place selected complementary write bitlines in a floating state during an inactive mode of the 8T SRAM cell.

24. The memory array of claim 18, further comprising, logic for floating all read and write bitlines of the memory array during a light sleep mode.

25. The memory array of claim 18, wherein the group of memory cells belong to a set.

26. The memory array of claim 18, wherein the group of memory cells belong to a bank.

27. The memory array of claim 15 integrated in at least one semiconductor die.

28. The memory array of claim 15 integrated into a device, selected from the group consisting of a set top box, music player, video player, entertainment unit, navigation

device, communications device, personal digital assistant (PDA), fixed location data unit, and a computer.

29. A memory array comprising: logic for dynamically placing write circuitry in a reduced power state; and logic for dynamically enabling or disabling the write circuitry in response to a write request.

30. The memory array of claim 29, wherein the logic for dynamically enabling or disabling the write circuitry comprises precharge transistors configured to drive complementary write bitlines.

31. The memory array of claim 30, wherein the precharge transistors are PMOS transistors coupled to positive power supply voltage VDD.

32. The memory array of claim 29, wherein the logic for dynamically placing the write circuitry in reduced power state comprises PMOS transistors configured to disable a path from positive power supply voltage VDD to complementary write bitlines in response to a sleep signal, and NMOS transistors configured to disable a path from the complementary write bitlines to ground voltage in response to a sleep signal.

33. The memory array of claim 29 comprising two or more read ports.

34. The memory array of claim 29 comprising two or more write ports.

35. The memory array of claim 29 integrated in at least one semiconductor die.

36. The memory array of claim 29 integrated into a device, selected from the group consisting of a set top box, music player, video player, entertainment unit, navigation device, communications device, personal digital assistant (PDA), fixed location data unit, and a computer.

37. A memory array comprising: means for dynamically placing a group of memory cells in the memory array in a reduced power state; and means for dynamically

enabling a selected group of the memory cells during an access operation on the selected memory cells.

38. The memory array of claim 37, wherein the means for dynamically enabling further comprises means for dynamically precharging selected read bitlines before and after a read access operation on the selected memory cells.

39. The memory array of claim 37, wherein the means for dynamically enabling further comprises means for dynamically precharging a pair of complementary write bitlines before and after a write access operation on the selected memory cells.

40. The memory array of claim 37, wherein the group of memory cells belong to a set.

41. The memory array of claim 37, wherein the group of memory cells belong to a bank.

42. The memory array of claim 37 integrated in at least one semiconductor die.

43. The memory array of claim 37 integrated into a device, selected from the group consisting of a set top box, music player, video player, entertainment unit, navigation device, communications device, personal digital assistant (PDA), fixed location data unit, and a computer.

44. A method for reducing access power in a memory array comprising: step for dynamically placing a group of memory cells in the memory array in a reduced power state; and step for dynamically enabling a selected group of the memory cells during an access operation on the selected memory cells.

45. The method of claim 44, wherein the access operation comprises a read.

46. The method of claim 44, wherein the access operation comprises a write.

47. The method of claim 44, wherein the memory cells include an 8 transistor Static Random Access Memory (8T SRAM) cell, such that forming the 8T SRAM cell comprises: step for forming a storage element; step for coupling a write word line and a pair of complementary write bitlines to the storage element through two write access transistors; and step for coupling the storage element to a read word line and a read bitline through two read access transistors.

48. The method of claim 47, further comprising, for a read operation, step for dynamically precharging selected read bitlines before and after the read operation on the 8T SRAM cell.

49. The method of claim 47, further comprising step for dynamically placing the read bitlines in a floating state during an inactive mode of the 8T SRAM cell.

50. The method of claim 47, further comprising, for a write operation, step for dynamically precharging the pair of complementary bitlines before and after a write operation on the 8T SRAM cell.

51. The method of claim 47, further comprising step for configuring a tristate write driver to dynamically place the pair of complementary write bitlines in a floating state during an inactive mode of the 8T SRAM cell.

52. The method of claim 47, further comprising, during a light sleep mode, step for floating all read and write bitlines of a memory array.

53. The method of claim 44, wherein the group of memory cells belong to a set.

54. The method of claim 44, wherein the group of memory cells belong to a bank.

55. The method of claim 44, wherein the 8T SRAM cell comprises two or more read ports.

56. The method of claim 44, wherein the 8T SRAM cell comprises two or more write ports.

57. A method for reducing access power in a memory array comprising: step for dynamically placing write circuitry in a reduced power state; and step for dynamically enabling or disabling the write circuitry in response to a write request.

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