(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 February 2012 (23.02.2012)

PCT

(10) International Publication Number
WO 2012/023902 A1

(51) International Patent Classification:
H05K 3/10 (2006.01) *H05K 3/46* (2006.01)
H01L 23/48 (2006.01)

(21) International Application Number:
PCT/SG2010/000303

(22) International Filing Date:
18 August 2010 (18.08.2010)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

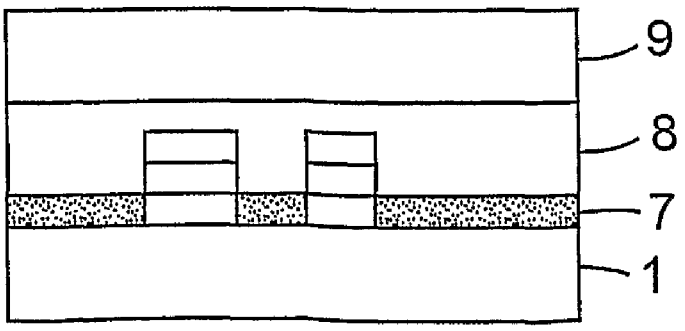
Published:

— *with international search report (Art. 21(3))*

WO 2012/023902 A1

(54) Title: A FLEXIBLE CIRCUIT AND A METHOD OF PRODUCING THE SAME

FIG. 1F



(57) Abstract: A structure comprising a flexible dielectric film supporting on at least one side a thermoplastic polyimide layer, and on it a conductive layer, is treated by an "semi- additive" process. The "semi-additive" process comprises forming a patterned photo¬ resist layer, filling gaps in the photo-resist layer with conductive material, removing the photo-resist and exposed portions of the laminated conductive layer, and covering the structure with a coverlay. The inventors have realized that the process of laminating the copper layer onto the thermoplastic polyimide layer roughens the surface of the thermoplastic polyimide layer, thus anchoring the copper layer to the polyimide, which means that when the conductive material is deposited into the gaps in the photo-resist, conductive bodies are formed which are strongly anchored to the thermoplastic polyimide layer, and which can be used as electrodes of a flexible circuit.

A flexible circuit and a method of producing the same

Field of the Invention

The present invention relates to methods for producing flexible members, and in particular flexible circuits, such as ones which are suitable for use in printer heads.

Background of the Invention

A common method of forming a flexible circuit is referred to here as a "subtractive process". The starting material is a flexible dielectric layer covered by a layer of adhesive. Various apertures (such as die windows, sprocket holes, tooling holes etc) are formed in the dielectric layer by a punching process. A layer of copper is laminated onto the adhesive. Patterned photo-resist is formed on the copper. Then, the copper is etched through gaps in the photo-resist. Then the photo-resist is removed, leaving a pattern of circuitry ("electrodes"). Then a coverlay is adhered over the electrodes. Each electrode has the same thickness as the laminated copper layer. The thickness of the electrodes is sufficient for low current applications, but not for high current applications, such as printer heads.

Furthermore, following the etching, the electrodes tend to be trapezoidal in cross-section, tapering in the direction away from the flexible dielectric layer. This means that to achieve a given cross-sectional area with a given thickness of copper, the base of the electrodes must be wider than it would be if the electrodes were rectangular in cross-section. This makes it harder to achieve miniaturization. In one investigation it was found that the subtractive process produced electrodes having a thickness of about 30 μm shaped such that, for their lowest 15 μm, the angle between the surface of the dielectric layer and the sides of the electrodes was less than 70 degrees.

It is known for the starting material of the subtractive process to be a material known by the trade designation "UPISEL N", which is available commercially from Ube-Nitto Kasei Co. Ltd., Japan. One form of UPISEL N consists of a flexible dielectric substrate

of the polyimide material known by the trade designation "UPILEX S", which is also available commercially from Ube-Nitto Kasei Co. Ltd., Japan, having a thickness of approximately 42 μm and made from biphenyldicarboxylicacid dianhydride (BBDA) and phenyl diamine (PDA). The UPILEX S sheet is covered, on one or both sides, with approximately 4 μm thermoplastic polyimide layer, onto which a layer of copper has been laminated.

The copper on commercially available UPISEL N comes in a variety of thicknesses, e.g., 35 μm, 18 μm, 12 μm, and 3 μm. Using a subtractive etching process with the thicker copper layers would require the removal of a substantial amount of copper, which is inefficient and costly. Using a subtractive process with the 3 μm layer would result in electrodes having no greater thickness than 3 μm. Such thin electrodes are only suitable for the production of products such as Liquid Crystal Displays (LCDs) and integrated circuit (IC) packaging for which electrodes of this thickness are acceptable. These problems make UPISEL N generally unsuitable for applications in which the electrodes must be thicker, so as to be capable of carrying a higher current. One example of such applications is in the head of a printer, for which electrodes of thickness at least 30 μm are typically required.

This is not the only difficulty of providing acceptable printer head circuits. They must additionally be highly resistant to degradation from their harsh environment, particularly exposure to solvent based alkaline ink. There is increasing demand for printer head circuits which are able to operate in such an environment for long periods of time, such as 5-7 years.

Summary of the invention

The present invention aims to produce a new and useful flexible member, such as a flexible circuit.

One aspect of the invention provides that a structure comprising a flexible dielectric film supporting a thermoplastic polyimide layer on at least one side, and on it a

laminated conductive layer, is treated by a "semi-additive" process. The semi-additive process comprises forming a patterned photo-resist layer, filling gaps in the photo-resist layer with conductive material, removing the photo-resist and exposed portions of the laminated conductive layer, and then adhering a coverlay onto the structure. The present inventors have realized that the process of laminating the conductive layer onto the thermoplastic polyimide layer roughens the surface of the thermoplastic polyimide layer as it conforms to the shape of the surface of the conductive layer during lamination, thus anchoring the conductive layer to the polyimide. This means that when the conductive material is deposited onto the conductive layer in the gaps in the photo-resist, conductive bodies are formed which are strongly anchored to the thermoplastic polyimide layer. These conductive bodies can be used as electrodes of the flexible circuit.

Experimentally, it was found that a semi-additive process permitted fabrication of electrodes with a thickness of over 35 μm and an angle with the surface of the substrate, even measured over the bottom 17 μm of the electrodes, of over 80 degrees. The higher angle means that miniaturization is more easily achieved.

Although the use of a semi-additive process for forming electrodes is not new, it has not previously been known to use this process when the starting material employs a thermoplastic layer. This meant that the electrodes formed were limited in thickness, since if they were too thick they tended to become separated from the flexible dielectric substrate in use. In other words, the possibility of forming electrode bodies of desired thickness by a semi-additive process, strongly anchored to the flexible dielectric via the rough thermoplastic polyimide layer, has not previously been realized.

An example of a structure on which the semi-additive process can be performed is the form of UPISEL N described above, which has a laminated layer of either rolled copper foil or electro-deposited copper foil. As noted, this material has not previously been used in a semi-additive process, and was designed for use in a subtractive process.

Some previous applications of the semi-additive method have employed as a starting material a layer of a polyimide film available under the trade designation "KAPTON E" from DuPont, which does not include a thermoplastic layer. The present inventors have found that certain embodiments of the present invention have lower surface degradation than products formed using KAPTON E because the thermoplastic polyimide provides high resistance to hydrolysis. Furthermore, the embodiments of the present invention provide improved resistance to trace delamination due to corrosion caused by ink ingression. In fact, they provide superior dry and wet peel properties over known constructions with KAPTON E film, as well as less waviness and warpage and much better reliability. While the KAPTON E products may be suitable for many applications, when more robust products are desired, embodiments of the present invention can provide an advantage.

The above summary of the present invention is not intended to describe each disclosed embodiment or every implementation of the present invention. The Figures and detailed description that follow below more particularly exemplify illustrative embodiments.

Brief description of the drawings

An embodiment of the invention will now be described for the sake of example only, with reference to the following figures, in which:

Figs. 1A-1F illustrate steps of a method which is an embodiment of the invention; and

Fig. 2 is a flow diagram of the method of Figs. 1A-1F.

Detailed description

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings that form a part hereof. The accompanying drawings show, by way of illustration, specific embodiments in which the invention may be practiced. It is to be understood that other embodiments may be utilized, and structural or logical changes may be made without departing from the scope of the present invention. The

following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the invention is defined by the appended claims.

An embodiment of the invention will now be described with reference to Figs. 1A-1F and 2.

As described below, the process involves a semi-additive process performed on a product illustrated in cross-sectional view in Fig. 1A. The structure comprises a flexible dielectric substrate 1, a thermoplastic polyimide (TPPI) layer 2 and a copper layer 3 laminated onto the TPPI layer 2. The lamination process is performed at a temperature of at least about 350 degrees C and produces surface roughness in the TPPI layer that is the negative image of the copper surface to which the TPPI layer is laminated. Before the lamination, the TPPI layer may have roughness on the nanometer level (for example, the upper surface of the layer may have a standard deviation from its mean level of less than 100nm), but afterwards the roughness is on the micrometer level, which may be defined as having a standard deviation from its mean level of at least 0.5 μm, and more preferably in the range 0.6 μm and 3 μm. The lower surface of the copper layer 3 may have a nodular structure with the same, or a different, degree of roughness.

Such a structure can be produced using the commercially available SR and SE series of the product UPISEL N available under the trade designation SE0320YSB or SE0320MSH which include a structure similar to that shown in Fig. 1A. That is, a flexible polyimide dielectric substrate is covered on one side with a TPPI layer, onto which a rolled or electro-deposited copper foil layer of thickness 3 μm has been laminated. However, in some forms the laminated copper layer is covered by a thick copper carrier layer.

If the UPISEL N has a carrier layer, this carrier layer is removed in a first processing step shown as step 11 of Fig. 2, to form the structure of Fig. 1A. In this case, the layer 3 typically has a thickness of 3 μm, and the roughness of the TPPI layer 2 is between 0.6 μm and 3 μm. This is the standard deviation of portions of the interface from the

average level of the interface. It can also be termed the "nominal thickness" of the nodules on the laminated rolled copper foil layer. In different versions of UPISEL N the nominal thickness of the nodules is different, depending upon the intended application.

Note that another form of UPISEL N exists in which the flexible polyimide dielectric substrate is covered on both sides by, in order, a TPPI layer, a laminated copper layer, and a thick copper carrier layer that form a multilayer structure. Again, the laminated copper layer has a nodular structure. The nominal thickness of the nodules need not be the same on both sides of the structure. This form of UPISEL N can also be employed in the present invention. Specifically, the processing steps described below can be performed as desired on either or both of the sides of the structure. Before performing the processing steps described below on either of the sides of the structure, the copper carrier layer is removed from that side of the structure.

Before or after the semi-additive process, apertures (die windows, sprocket holes, tooling holes etc) may be formed in the structure, but that process, which may be carried out using a conventional punching procedure, or otherwise, will not be described further here.

In a processing step 12 of Fig. 2, photo-resist 4 is deposited and patterned over the laminated copper layer 3, to give the structure of Fig. 1B.

In step 13 of Fig. 2, copper is deposited by electroplating to a desired thickness, e.g., 40 μm in the illustrated embodiment, into the gaps in the photo-resist 4, covering the thin copper layer 3 in the regions where it is exposed, as shown in Fig. 1C. The deposited copper 5 is joined to the laminated copper layer 3.

In step 14 of Fig. 2, the photo-resist 4 is then removed, exposing parts of the thin copper layer 3, as shown in Fig. 1D.

In step 15, the exposed portions of the thin copper layer 3 are etched away, thus exposing corresponding portions of the roughened TPPI layer. The upper portion of

deposited copper 5 is also inadvertently etched away. This produces the structure of Fig. 1E, in which the TPPI layer is indicated as layer 7 having an exposed rough upper surface in the portions marked by shading. The remaining portions of the copper layer 3 and the deposited copper 5 overlying them together form bodies 6 of copper which have a desired thickness and are well-fixed to the TPPI layer 7 due to the nodular teeth of the lower surface of the bodies 6.

In step 16, an adhesive 8 and cover film 9 are then laminated over the structure, together forming a coverlay. The structure is then cured. This gives the structure of Fig. 1F. The coverlay, like the remaining copper, is strongly retained on the rough TPPI layer 7. The coverlay may be a Elephane CL-XU4013 from Tomoegawa Industries Ltd in which the adhesive 8 is a polyamide/phenolic adhesive of thickness 40 μm and is coated on a cover film 9 of UPILEX SN which UPILEX SN films are available from Ube-Nitto Kasei Co. Ltd. and which have a thickness of 13 μm prior to the lamination.

Examples

This invention is illustrated by the following examples, but the particular materials and amounts thereof recited in these examples, as well as other conditions and details should not be construed to unduly limit this invention.

Examples 1-5 (Ex. 1-5)

Ex. 1-5 were made from a 20" (50.80cm) width x 50m length section of UPISEL N available under the trade designation SE0320YSB from Ube-Nitto Kasei Co. Ltd. The section of UPISEL N was first slit into 13.4" (34.04cm) width strips. Following removal of the 18 μm copper carrier layer, apertures were formed in the UPISEL N by a punching process. It was then subjected to a semi-additive process on one of its two sides in the same manner as described above. After the photo-resist was applied and patterned, about 45 μm of copper was electro-deposited onto the exposed portions of the laminated copper. After the photo-resist was removed, the exposed portions of the laminated copper layer were etched away, to give electrodes of thickness of about 35 μm between exposed portions of the TPPI layer. As determined with a scanning electron microscope the electrodes had a generally rectangular cross-section, and the

angles between their side-walls and the surface of the TPPI layer was about 81.4 degrees. The UPILEX S has a relatively small coefficient of thermal expansion compared to the copper, which means that it experiences little heat shrinkage, giving good dimensional stability.

Comparative Example A (C.E. A)

C. E. A was made using a 14" (35.56cm) width x 50m roll of KAPTON E having a thickness of 50 μm as the starting material. KAPTON E is a flexible polyimide material, but does not carry a surface layer of thermoplastic polyimide. The KAPTON E was processed by first seeding a 2-20nm thin chrome (Cr) tie layer onto one face of the KAPTON E by vacuum deposition, then depositing a thin copper layer of thickness about 100nm onto the tie layer by vacuum deposition to form a conductive surface. The substrate was then subjected to electroplating to build up the thin copper layer to a thickness of about 3 μm. This provided a structure similar to the UPISEL N starting material of Ex. 1-5. The structure was then subjected to a semi-additive process in the same manner as Ex. 1-5., in which about 45 μm of copper were electro-deposited using a patterned photo-resist. Then after the photo-resist was removed, the exposed portions of the 3 μm copper layer and the underlying nodular copper layer was etched away. This resulted electrodes of thickness 35 μm between exposed portions of the polyimide layer. The 14" (35.56cm) web was then slit down into 7cm width strips and it was then cut into individual patterned circuits.

It was found that when C.E. A was subjected to an ink vapor test in which the circuit samples were suspended in a sealed vessel in a space above alkaline liquid ink at an elevated temperature of 100 degrees C for 3days, the corroded copper ions readily form copper complexes with chelating compounds present in the ink and the resulting complex catalysis leads to opening of polyimide rings in the KAPTON E. This causes the degradation of the polyimide surface and copper trace delamination.

Examples 6-10 (Ex. 6-10) and Comparative Example B (C.E. B)

Ex. 6-10 and C.E. B were made, respectively, by applying a coverlay material made of a 13 μm thickness of UPISEL SN cover layer and 40 μm adhesive layer, available under

the trade designation Elephane CL-XU 4013 from Tomoegwawa Co. Ltd. Japan, to Ex. 1-5 and C.E. A.

The coverlay was cut into pieces with respective pattern by a die cut method and was pre-tacked by placing the individual pieces of coverlay manually onto the individual circuit in a 7cm width roll and pressed down using heated flat pins (about 160 degrees C) for about 4secs. Lamination of the pre-tacked coverlay onto the circuits were carried out by applying a pressure of about 200psi (pounds per square inch) ($1.38x10^6$ Nm^{-2}) at about 180 degrees C temperature for about 6secs.

The laminated circuits in a 7cm width reel form were then subjected to a curing process. The curing profile was employed with heating from 30 degrees C to 90 degrees C with increments of 10 degrees C per minute and allowed to stay at about 90 degrees C for about 60mins and then ramped up to 180 degrees C by increments of 10 degrees C per minute. After allowing the circuits to maintain at a temperature of about 180 degrees C for about 2hrs, the temperature was slowly reduced to 30 degrees C over a period of 2hrs.

The coverlay laminated resulting circuits were cut into individual circuits of 48mm x 27mm and subjected to an ink vapor test in which the circuit samples were suspended in a sealed vessel in a space above alkaline liquid ink at an elevated temperature of 100 degrees C for 3days.

In C.E. B, delamination occurred at the interfaces (i) between the adhesive of the coverlay and the KAPTON E polyimide layer thereby the copper traces lift off from the polyimide surface, and (ii) between the adhesive and the cover film in the coverlay. However, unlike in C.E. B, in Ex. 6-10 of the invention, delamination only occurred at the interface between the adhesive and the cover film in the coverlay. No delamination was observed at the interface between the adhesive of the coverlay and thermoplastic polyimide layer of the UPISEL N. It is believed this is due to higher peel strength imparted, at least in part, by the strong bond between the roughened TPPI layer and the adhesive of the coverlay. The ink vapor test is particularly significant, because it is

believed that the ink vapor ingress is responsible for the delamination of the coverlay in C.E. B.

Pieces of Ex. 6-10 and C.E. B, 0.125" (0.32cm) wide and 48mm long, were also subjected to a standardized "peel test", in which the coverlay was gradually peeled away from the underlying layer(s) using an applied load of 10N and at a speed of 2"/min (5.1cm/min). The portion of the coverlay which had been removed at each stage was held at an angle of 90 degrees from the plane of the circuit. The results are shown in Table 1.

The results in Table 1 labeled "dry peel test" were from performing the above-described standardized peel test on samples that had not been subjected to treatment by ink.

The results in Table 1 labeled "wet peel test" were from performing the standard peel test on samples that had been immersed in alkaline liquid ink for 3days at a temperature of 85 degrees C.

For each of these two tests, Table 1 shows the results for Ex. 6-10, and their average result. The results for C.E. B are the average of 5 samples. The numbers in Table 1 are the peel strength, measured in pounds (lbs) (one pound is 4.45N).

	Example Number					Average	Comparative Example B
	6	7	8	9	10		
Dry Peel Test	1.314	1.968	1.394	1.724	1.297	1.54	0.75
Wet Peel Test	1.417	1.311	1.243	1.268	1.437	1.34	0.4

Table 1

The results revealed that in both the dry and wet peel cases, the embodiments of the invention yielded higher peel strength than the KAPTON E based comparative example. Most importantly, the failure mode for the embodiments of the invention occured

between the adhesive and the cover film of the coverlay, showing the strong bonding strength between the adhesive and TPPI layer due to the higher roughness created by the nodular copper.

Example 11 (Ex. 11) and Comparative Example C (C.E. C)

Ex. 11 was made by taking a 10cm x 48mm section of UPISEL N available under the trade designation SE0320YSB, completely removing the laminated copper layer, and laminating a coverlay Elephane CL-XU4013 from Tomoegawa Industries Ltd where the coverlay consists of a polyamide/phenolic adhesive of thickness 40 μm coated on a cover film of 13 μm UPILEX SN where UPILEX SN films are available from Ube-Nitto Kasei Co. Ltd. The lamination of the coverlay onto the TPPI layer, after the copper is removed completely from the UPISEL N substrate, was done by applying pressure of about 200psi (1.38×10^6 Nm^{-2}) at a temperature of about 180 degrees C for about 6secs.

The laminated structures were then subjected to a curing process. The curing profile was employed with heating from about 30 degrees C to about 90 degrees C with increments of 10 degrees C per minute and allowed to stay at about 90 degrees C for about 60mins. The temperature was later ramped up to about 180 degrees C by increments of 10 degrees C per minute. After allowing the temperature to stay at about 180 degrees C for about 2hrs, the laminated structures were then slowly cooled to about 30 degrees C over a period of 2hrs.

C.E. C was made by taking a 0.51cm x 48mm section of KAPTON 2E known as KAPTON 200E available from DuPont and directly laminating the coverlay to it in the same manner as for Ex. 11, and then curing the structure in the same manner as for Ex. 11.

Both Examples were subjected to the standardized peel test described above for Ex. 1-5 and C.E. A. Because the structures had no circuits, the test on these structures is referred to as a coupon level peel test.

Ex. 11 had a coupon level peel in the dry peel test of 3.11 lbs, so it was very difficult to peel. C.E. C had a coupon level peel in the dry peel test of 0.55lbs. Each of these results is the average peel strength for three samples. Again, this demonstrates the greater peel strength provided by the rough polyimide surface of the UPISEL N.

Although specific embodiments have been illustrated and described herein for purposes of description of the preferred embodiment, it will be appreciated by those of ordinary skill in the art that a wide variety of alternate and/or equivalent implementations may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. This application is intended to cover any adaptations or variations of the preferred embodiments discussed herein. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

Claims

1. A method of forming a flexible member, the method employing a structure which comprises (i) a flexible dielectric film (1) having a first surface, (ii) a thermoplastic polyimide layer (2) carried on the first surface of the dielectric film (1), and (iii) a conductive layer (3) laminated onto the thermoplastic polyimide layer thereby roughening the thermoplastic polyimide layer,

the method comprising:

forming a patterned photo-resist layer (4) on the conductive layer;

depositing one or more elements of conductive material (5) into gaps defined by the photo-resist layer;

removing the photo-resist layer;

removing exposed portions of the conductive layer (3), the remaining portions of the conductive layer and the elements of conductive material forming conductive leads (6); and

forming a coverlay (8, 9) over the conductive leads, the conductive leads being sandwiched between the thermoplastic polyimide layer and the coverlay (8, 9).

2. A method according to claim 1, the electrodes having a thickness of at least 30 μm in a direction transverse to the first surface of the dielectric film.

3. A method according to claim 1 or claim 2 further comprising forming a plurality of holes in the flexible member, and dividing the flexible member into a plurality of flexible circuit elements.

4. A method according to claim 3 in which each flexible circuit element is a flexible circuit element for a print head assembly.

5. A flexible circuit element formed by a method according to claim 3 or claim 4.

6. A method of forming a flexible member comprising:

forming a thermoplastic polyimide layer (2) on a first surface of a flexible dielectric film (1);

laminating a conductive layer (3) onto the thermoplastic polyimide layer, thereby roughening the thermoplastic polyimide layer;

forming a patterned photo-resist layer (4) on the conductive layer;

depositing one or more elements of conductive material (5) into gaps defined by the photo-resist layer;

removing the photo-resist layer;

removing exposed portions of the conductive layer, the remaining portions of the conductive layer and the elements of conductive material forming conductive leads (6); and

forming a coverlay (8, 9) over the conductive leads, the conductive leads being sandwiched between the thermoplastic polyimide layer and the coverlay.

7. A method according to claim 6 in which during the step of laminating the conductive layer onto the thermoplastic polyimide layer, the surface roughness of the polyimide layer becomes a value in the range 0.6 μm to 3 μm.

8. A flexible circuit element comprising:

a flexible dielectric film (1) having a first surface;

a thermoplastic polyimide layer (7) bonded to the first surface of the dielectric film;

a plurality of conductive leads (6) bonded to the thermoplastic polyimide layer (7) and upstanding from the thermoplastic polyimide layer, the conductive leads comprising a lower portion laminated onto the thermoplastic polyimide layer and an upper portion formed on the lower portion, the conductive leads having side surfaces extending at an angle of at least 80 degrees to the first surface of the dielectric film, and extending to a distance of at least 30 μm from the thermoplastic polyimide film;

a coverlay (8, 9) formed over the plurality of conductive leads, the plurality of conductive leads being sandwiched between the coverlay and the thermoplastic polyimide layer.

9. A print head assembly comprising a flexible circuit element according to claim 8.

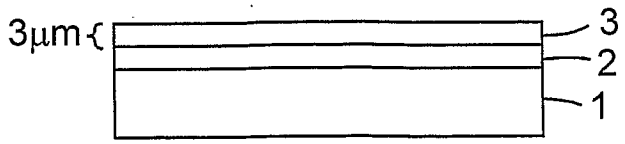


FIG. 1A

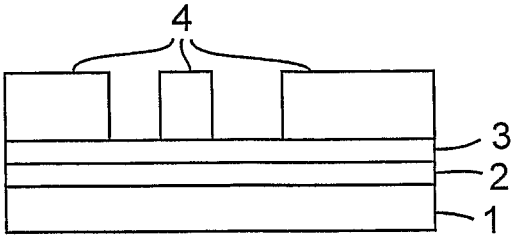


FIG. 1B

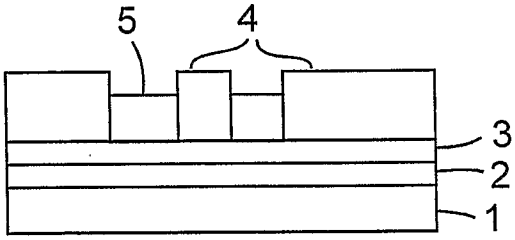


FIG. 1C

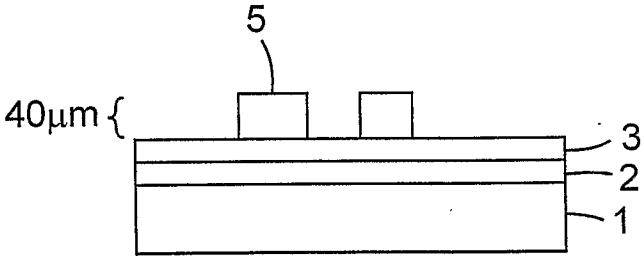


FIG. 1D

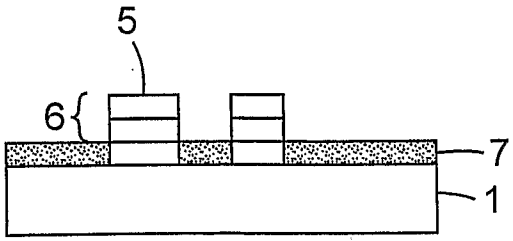


FIG. 1E

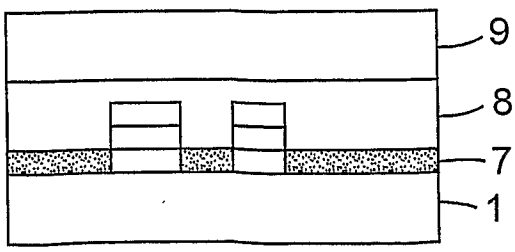


FIG. 1F

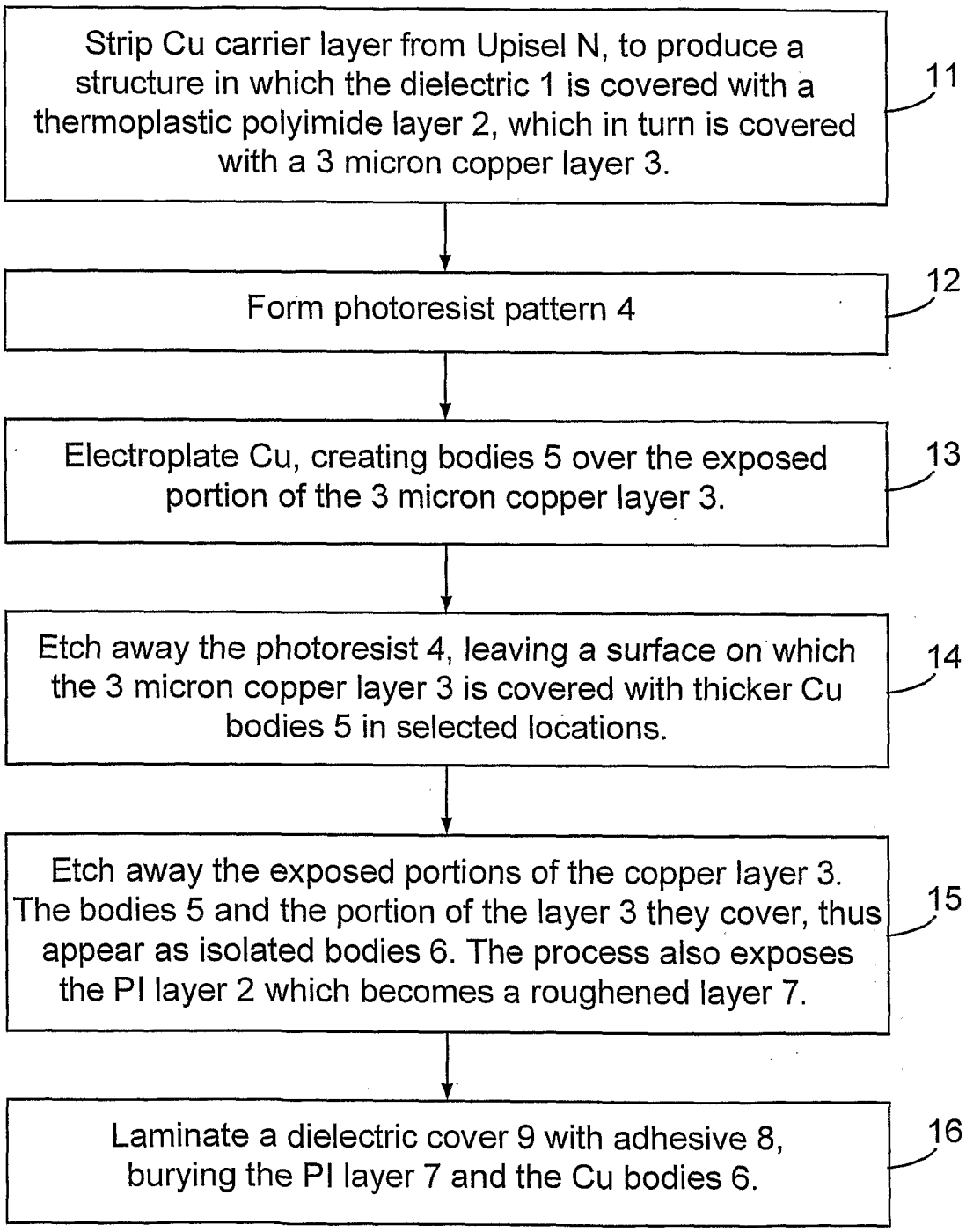

Strip Cu carrier layer from Upisel N, to produce a structure in which the dielectric 1 is covered with a thermoplastic polyimide layer 2, which in turn is covered with a 3 micron copper layer 3.
11
Form photoresist pattern 4
12
Electroplate Cu, creating bodies 5 over the exposed portion of the 3 micron copper layer 3.
13
Etch away the photoresist 4, leaving a surface on which the 3 micron copper layer 3 is covered with thicker Cu bodies 5 in selected locations.
14
Etch away the exposed portions of the copper layer 3. The bodies 5 and the portion of the layer 3 they cover, thus appear as isolated bodies 6. The process also exposes the PI layer 2 which becomes a roughened layer 7.
15
Laminate a dielectric cover 9 with adhesive 8, burying the PI layer 7 and the Cu bodies 6.
16

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2010/000303

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H05K 3/10 (2006.01) ***H01L 23/48*** (2006.01) ***H05K 3/46*** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPODOC & WPI: (flexible w circuit), polyimide, semi_additive, etc...

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1519640 A1 (NITTO DENKO CORPORATION) 30 March 2005 Refer to whole document and in particular to Fig. 1a-f, Fig. 2g-k, paragraphs [0016]-[0019], [0021], [0023], [0025]-[0028], [0037], [0040], [0047]	1-6, 8-9
X	EP 1648209 A1 (NITTO DENKO CORPORATION) 19 April 2006 Refer to whole document and in particular to Fig. 1, [0066]-[0070], [0072-[0073]).	1-6, 8-9

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 October 2010	22 OCT 2010
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. +61 2 6283 7999	Authorized officer **FIROOZEH RABBANI** AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No : +61 2 6283 2287

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/0136725 A1 (SHIMOKAWA *et. al.*) 28 May 2009 Refer to whole document and in particular to Fig. 1, paragraphs [0046]-[0058], [0098], [0101], [0207], claim 8,	1-9
X	US 5217849 A (CHONAN *et. al.*) 8 June 1993 Refer to whole document and in particular to col.1, line 10+, col. 2, lines 23-47; Fig. 1a-1h, example 1,	1-6, 8-9
X	EP 0415659 A2 (SUMITOMO METAL MINING COMPANY LTD) 6 March 1991 Refer to whole document and in particular to col. 1, line 10+, Fig. 1a-1h, col. 5-7, example 1	1-6, 8-9
A	US 5721007 A (LYNCH *et. al.*) 24 February 1998 Refer to whole document and in particular to Fig. 1-4	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/SG2010/000303

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
EP	1519640	CN	1604723	JP	2005108942	KR	20050031416
		US	2005067293	US	7323093		
EP	1648209	CN	1761379	JP	2006114631	US	2006076242
		US	7396635				
US	2009136725	CN	101449633	KR	20090004961	WO	2007111268
US	5217849	EP	0415659	JP	3083354		
US	5721007	NONE					

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX