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(54) **Title**: CARRIER MOBILITY ENHANCED CHANNEL DEVICES AND METHOD OF MANUFACTURE

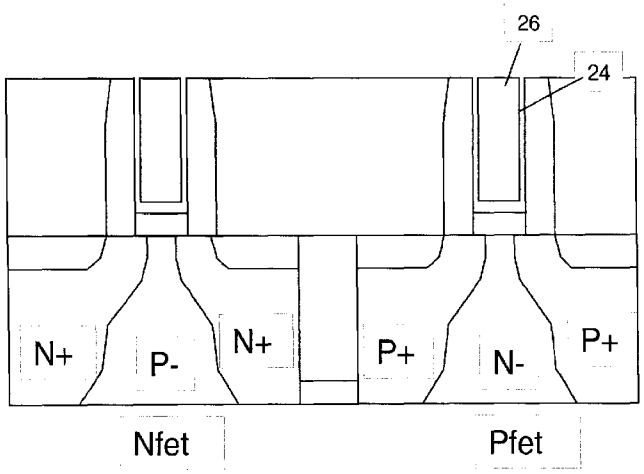


FIG. 9

(57) **Abstract**: An integrated circuit with stress enhanced channels, a design structure and a method of manufacturing the integrated circuit is provided. The method includes forming a dummy gate structure on a substrate and forming a trench in the dummy gate structure. The method further includes filling a portion of the trench with a strain inducing material and filling a remaining portion of the trench with gate material.

CARRIER MOBILITY ENHANCED CHANNEL DEVICES AND METHOD OF MANUFACTURE

FIELD OF THE INVENTION

[0001] The present invention relates to integrated circuits (ICs), a design structure and a method of manufacturing and, more particularly, to an integrated circuit with carrier mobility enhanced channels, a design structure and a method of manufacturing the integrated circuit.

BACKGROUND

[0002] CMOS technology embodied as a high performance, low-power chip, has been widely used in electronic devices because of its scaleable. However, continuing this CMOS performance trend has become extremely difficult because the industry is approaching the fundamental physical limits of CMOS scaling. For this reason, the semiconductor industry has been aggressively seeking new ways to make electric charges move faster through device channels so as to increase circuit speeds and reduce power consumption.

[0003] It has been found that a way to improve CMOS performance is to increase the mobility of its positive charges, or holes, through the device channels. For PFETs, hole mobility is known to be 2.5 times higher on (110) surface-orientation compared to that on standard wafer with (100) surface-orientation. To increase hole and electron mobility, the industry has tried to incorporate Ge materials into the semiconductor processing

methodologies; however, the presence of Ge causes material and process integration challenges to the semiconductor manufacturer.

[0004] More specifically, Ge has been used as a channel material to enhance electron and hole mobility for both NFET and PFET devices. However, due to the low melting point of Ge (e.g., about 938° C), it has a tendency to fluidize during normal annealing processes, which take place at about 1000° C. This, in turn, affects the properties and characteristics of Ge and hence the device. Also, it is difficult to form an oxide on Ge, compared to Si. Moreover, the dopant diffusion of Ge is very fast and, as such, it becomes very difficult to control the dopant profiles in the source and drain regions, as well as in the halo regions. For these and other reasons, Ge has not been integrated to standard silicon technology.

[0005] Accordingly, there exists a need in the art to overcome the deficiencies and limitations described hereinabove.

SUMMARY

[0006] In a first aspect of the invention, a method comprises forming a dummy gate structure on a substrate and forming a trench in the dummy gate structure. The method further comprises filling a portion of the trench with a high carrier mobility material and filling a remaining portion of the trench with gate material.

[0007] In another aspect of the invention, a method of forming a device comprises building a dummy gate structure on a substrate and etching at least a portion of the dummy gate structure to a channel region. This latter step results in a formation of a

trench between sidewalls of the dummy gate structure. The method further comprises depositing a high carrier mobility material on the substrate within the trench and building a gate structure over the strain inducing material.

[0008] In a further aspect of the invention, a structure comprises a germanium material formed directly on a substrate and at least within a trench defined by sidewalls of a dummy gate structure.

[0009] In yet a still further aspect of the invention, a design structure is embodied in a machine-readable medium for designing, manufacturing, or testing an integrated circuit. The design structure comprises a germanium material formed directly on a substrate and at least within a trench defined by sidewalls of a dummy gate structure. The design structure further comprises a dielectric material that lines inner portions of the sidewalls, and a metal or metal alloy that contacts with the dielectric material.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0010] The present invention is described in the detailed description which follows, in reference to the noted plurality of drawings by way of non-limiting examples of exemplary embodiments of the present invention.

[0011] FIGS. 1-8 show intermediate structures and respective processing steps in accordance with a first aspect of the invention;

[0012] FIG. 9 shows a final structure and respective processing steps according to the first aspect of the invention;

[0013] FIGS. 10 and 11 show intermediate structures and respective processing steps in accordance with a second aspect of the invention;

[0014] FIG. 12 shows a final structure and respective processing steps in accordance with the second aspect of the invention;

[0015] FIGS. 13 and 14 show intermediate structures and respective processing steps in accordance with a third aspect of the invention;

[0016] FIG. 15 shows a final structure and respective processing steps in accordance with the third aspect of the invention; and

[0017] FIG. 16 is a flow diagram of a design process used in semiconductor design, manufacture, and/or test.

DETAILED DESCRIPTION

[0018] The present invention relates to integrated circuits, a design structure and a method of manufacturing an integrated circuit and, more particularly, to an integrated circuit with a stress enhanced channel, a design structure and a method of manufacturing the integrated circuit. In implementation, the present invention provides a process to integrate Ge into a channel region of the device using a conventional flow to form both an NFET and PFET device, simultaneously. Advantageously, the present invention does not suffer from the drawbacks of known integration methods and provides enhanced device performance. The devices manufactured using the processes of the present invention will benefit from strained Si mobility enhancement.

FIRST ASPECT OF THE INVENTION

[0019] FIGS. 1-8 show intermediate structures and respective processing steps in accordance with a first aspect of the invention. In particular, FIG. 1 shows a starting structure in accordance with the invention. In this starting structure, a dummy gate structure 14 is formed on a substrate 10 using conventional deposition, lithographic and etching processes and as such an explanation of the manufacturing processes is not required herein for one of skill in the art to understand the invention. The dummy gate structure 14 includes a polysilicon layer 14b formed on a thin oxide layer 14a (e.g., about 10Å to 20Å). Sidewalls 14c are formed on the side of the polysilicon layer 14b and thin oxide layer 14a, which may comprise nitride or oxide or a combination thereof. A nitride cap 14d is formed on the gate structure and more particularly on the polysilicon layer. For purposes of discussion, the polysilicon layer 14b and oxide layer 14a may be defined as a body portion of the gate, in addition to, in embodiments, the capping layer.

[0020] A shallow trench isolation (STI) structure 12 is formed between the dummy gates 14. In embodiments, the STI structure 12 can be formed using a conventional lithographic and etching process. The STI structure 12 is filled with an oxide material.

[0021] In FIG. 2, NFET and PFET devices are formed using conventional doping processes. For example, in an NFET device, a lightly doped P- region is formed under the gate structure 14. The lightly doped P- region may be formed using a low concentration of boron in the range of, for example, 1E17 to 1E19/cm^3. The N+ regions of the NFET device can be formed by heavily doping these regions with Arsenic or

Phosphorous or a combination thereof. The concentration of such dopants may be in the range of, for example, 1E20 to 5E21/cm^3.

[0022] FIG. 2 also shows the formation of the PFET. For the PFET device, a lightly doped N- region is formed under the gate structure 14. The lightly doped N- region may be formed using a low concentration of Arsenic or Phosphorous or a combination thereof in the range of, for example, 1E17 to 1E19/cm^3. The P+ regions of the PFET device can be formed by heavily doping these regions with Boron. The concentration of Boron may be in the range of, for example, 1E20 to 5E21/cm^3.

[0023] FIG. 3 shows a dopant activation anneal process. In this processing step, the structure of FIG. 2 undergoes an anneal process at a temperature of about 1000° C. This anneal process can range from a few seconds to a flash annealing process. The anneal may also be a laser anneal.

[0024] In FIG. 4, the structure of FIG. 3 undergoes a Salicide formation. In this process, cobalt, nickel or nickel platinum, or other alloys, for example, can be deposited and annealed at a temperature of about 300° C to about 700° C. In embodiments, this results in metal contact regions 16 formed of a metal silicide. In embodiments, the structure will undergo a wet etching process to remove any excess metal, e.g., non-reactive metal.

[0025] In FIG. 5, an interlevel dielectric 18 is deposited on the structure of FIG. 4. In embodiments, the interlevel dielectric 18 is deposited using a conventional chemical

vapor deposition (CVD) process. The interlevel dielectric 18 may be an oxide-based material or low-K material.

[0026] FIG. 6 shows a gate removal process. In particular, an upper layer of the interlevel dielectric 18 and the nitride cap is removed using, for example, a CMP process. In embodiments, the nitride cap can also be etched using a reactive ion etching (RIE). In further processing steps, the polysilicon layer of the gate structure 14 is removed using a wet etch process selective to polysilicon. A dilute HF etch is then used to remove the thin oxide layer of the gate structure 14. These processes form trenches 20 which expose the channel region (Si layer) between the sidewall structures 14c of the gate structure 14.

[0027] In FIG. 7, a high carrier mobility material such as germanium (Ge) 22 is deposited in the trenches 20, e.g., channel region, using conventional deposition processes. The Ge can be grown using epitaxial CVD or ALD process. In embodiments, the Ge 22 is deposited in the channel region directly on (contacting) the substrate 10 to a thickness ranging from about 1 nm to 10 nm and preferably 5 nm to 10 nm. This thickness range of the Ge material 22 ensures that there is no decoupling of the device.

[0028] In FIG. 8, a high K dielectric material 24 is blanket deposited on the structure of FIG. 7, including over the Ge material 22 and sidewalls of the trenches. In embodiments, the high K dielectric material 24 is about 1 nm to 3 nm in thickness. A metal gate layer 26 is deposited on the high K dielectric material 24. The metal gate layer 26 may be, for example, TiN, TaN, WN, other known metal gates or any combination thereof. The metal gate layer 26 may also be a layered metal combination. In further embodiments, a

metal poly gate combination can be used with the invention, with the metal contacting to the Ge material 22.

[0029] FIG. 9 shows final processing steps and a final structure in accordance with a first aspect of the invention. In FIG. 9, the structure of FIG. 8 is planarized using, for example, a conventional CMP process.

SECOND ASPECT OF THE INVENTION

[0030] FIGS. 10 and 11 show intermediate structures and respective processing steps in accordance with a second aspect of the invention. In particular, FIG. 10 shows an intermediate structure similar to that shown in FIG. 6, with the addition of a recess 28 formed in the channel region of the substrate 10. By way of example, using conventional deposition, lithographic and etching processes a dummy gate structure 14 is formed on the substrate which includes a polysilicon layer formed on a thin oxide layer (e.g., about 10Å to 20Å). Sidewalls 14c are formed on the side of the polysilicon layer and thin oxide layer, which may comprise nitride or oxide or a combination thereof. A nitride cap is formed on the dummy gate structure 14 and more particularly on the polysilicon layer. A shallow trench isolation (STI) structure 12 is formed between the dummy gate structures.

[0031] Similarly to that described above, NFET and PFET devices are formed using conventional processes, including a dopant activation anneal process. The structure also undergoes a Salicide formation to form metal contact regions 16. An interlevel dielectric 18 is deposited on the structure using, for example, a conventional chemical vapor deposition (CVD) process. The interlevel dielectric 18 may be an oxide-based material

or low-K material. In further processing steps, the nitride cap and the upper layer of the interlevel dielectric 18 is removed using, for example, a CMP process. In embodiments, the nitride cap can also be etched using a reactive ion etching (RIE). In further processing steps, the polysilicon layer of the gate structure is removed using a wet etch process selective to polysilicon. An HF etch is used to remove the thin oxide layer of the dummy gate structure 14.

[0032] Particular to the second aspect of the invention, a recess 28 (e.g., extension of the trench) is formed in the substrate 10 using a RIE or wet etch process, selective to the substrate 10. The recess 28 is about 1 nm to 10 nm in depth, and preferably about 5 nm to 10 nm in depth.

[0033] In FIG. 11, a strain inducing material such as Ge material 30 is deposited in the recess 28 (in the channel region directly on the substrate 10). In embodiments, the Ge material can be co-planar with the surface of the substrate 10, or above or below the surface of the substrate 10. Ge thickness can be in the range between 5nm and 30nm.

[0034] FIG. 12 shows a final structure in accordance with the invention and respective processing steps. Similar to that discussed above, a high K dielectric material 24 is blanket deposited on the structure of FIG. 11, including over the Ge material 30. In embodiments, the high K dielectric material 24 is about 1 nm to 3 nm in thickness. A metal gate layer 26 is deposited on the high K dielectric material 24. The metal gate layer 26 may be, for example, TiN, TaN, WN, other known metal gates or any combination thereof. The metal gate layer 26 may also be a layered metal combination.

In further embodiments, a metal poly gate combination can be used with the invention, with the metal connecting the Ge material 30. The structure is planarized using, for example, a conventional CMP process.

THIRD ASPECT OF THE INVENTION

[0035] FIGS. 13 and 14 show intermediate structures and respective processing steps in accordance with a third aspect of the invention. In particular, FIG. 13 shows an intermediate structure similar to that shown in FIG. 6, with the addition of a recess 32 formed in the channel region of the substrate 10 and under portions of the sidewall structures 14c.

[0036] By way of example, using conventional deposition, lithographic and etching processes a dummy gate structure 14 is formed on the substrate which includes a polysilicon layer formed on a thin oxide layer (e.g., about 10Å to 20Å). Sidewalls 14c (shown in FIG. 10) are formed on the side of the polysilicon layer and thin oxide layer, which may comprise nitride or oxide or a combination thereof. A nitride cap is formed on the dummy gate structure 14 and more particularly on the polysilicon layer. A shallow trench isolation (STI) structure 12 is formed between the dummy gate structures.

[0037] Similarly to that described above, NFET and PFET devices are formed using conventional processes, including a dopant activation anneal process. The structure also undergoes a Salicide formation to form metal contact regions 16. An interlevel dielectric 18 is deposited on the structure using, for example, a conventional chemical vapor deposition (CVD) process. The interlevel dielectric 18 may be an oxide-based material

or low-K material. In further processing steps, an upper layer of the interlevel dielectric 18 and the nitride cap is removed using, for example, a CMP process. In embodiments, the nitride cap can also be etched using a reactive ion etching (RIE). In further processing steps, the polysilicon layer of the gate structure is removed using a wet etch process selective to polysilicon. An HF etch is used to remove the thin oxide layer of the gate structure.

[0038] Particular to the third aspect of the invention, a recess 32 (e.g., extension of the trench) is formed in the substrate 10 using an isotropic etching process, selective to the substrate 10. The recess 32 is about 1 nm to 10 nm in depth, and preferably about 5 nm to 10 nm in depth, and extends to underneath the sidewalls 14c.

[0039] In FIG. 14, a strain inducting material such as Ge material 34 is deposited in the recess 32 (in the channel region directly on the substrate 10), including under the sidewalls 14c. In embodiments, the Ge material 34 is preferably lower than the surface of the substrate 10. This provides better control to the channel, as the channel is "wrapped" around the gate. In alternative embodiments, the Ge material 34 can be above or below the surface of the substrate 10. The Ge thickness is between 5nm and 30nm.

[0040] FIG. 15 shows a final structure in accordance with the invention and respective processing steps. Similar to that discussed above, a high K dielectric material 24 is blanket deposited on the structure of FIG. 14, including over the Ge material 34. In embodiments, the high K dielectric material 24 is about 1 nm to 3 nm in thickness. The metal gate layer 26 may be, for example, TiN, TaN, WN, other known metal gates or any

combination thereof. The metal gate layer 26 may also be a layered metal combination. In further embodiments, a metal poly gate combination can be used with the invention, with the metal connecting the Ge material 34. The structure is planarized using, for example, a conventional CMP process.

[0041] The resulting integrated circuit chips of each aspect of the invention can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. In the latter case, the chip is mounted in a single chip package (e.g., a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (e.g., a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard or other input device, and a central processor.

DESIGN STRUCTURE

[0042] FIG. 16 shows a block diagram of an exemplary design flow 900 used for example, in semiconductor design, manufacturing, and/or test. Design flow 900 may vary depending on the type of IC being designed. For example, a design flow 900 for building an application specific IC (ASIC) may differ from a design flow 900 for designing a

standard component. Design structure 920 is preferably an input to a design process 910 and may come from an IP provider, a core developer, or other design company or may be generated by the operator of the design flow, or from other sources. Design structure 920 comprises an embodiment of the invention as shown in FIGS. 9, 12 and 15 in the form of schematics or HDL, a hardware-description language (e.g., Verilog, VHDL, C, etc.).

[0043] Design structure 920 may be contained on one or more machine-readable medium. For example, design structure 920 may be a text file or a graphical representation of an embodiment of the invention as shown in FIGS. 9, 12 and 15. Design process 910 preferably synthesizes (or translates) an embodiment of the invention as shown in FIGS. 9, 12 and 15 into a netlist 980, where netlist 980 is, for example, a list of wires, transistors, logic gates, control circuits, I/O, models, etc. that describes the connections to other elements and circuits in an integrated circuit design and recorded on at least one of machine readable medium. This may be an iterative process in which netlist 980 is resynthesized one or more times depending on design specifications and parameters for the circuit.

[0044] Design process 910 may include using a variety of inputs; for example, inputs from library elements 930 which may house a set of commonly used elements, circuits, and devices, including models, layouts, and symbolic representations, for a given manufacturing technology (e.g., different technology nodes, 32nm, 45 nm, 90 nm, etc.), design specifications 940, characterization data 950, verification data 960, design rules 970, and test data files 985 (which may include test patterns and other testing information).

[0045] Design process 910 may further include, for example, standard circuit design processes such as timing analysis, verification, design rule checking, place and route operations, etc. One of ordinary skill in the art of integrated circuit design can appreciate the extent of possible electronic design automation tools and applications used in design process 910 without deviating from the scope and spirit of the invention. The design structure of the invention is not limited to any specific design flow.

[0046] Design process 910 preferably translates an embodiment of the invention as shown in FIGS. 9, 12 and 15, along with any additional integrated circuit design or data (if applicable), into a second design structure 990. Design structure 990 resides on a storage medium in a data format used for the exchange of layout data of integrated circuits (e.g. information stored in a GDSII (GDS2), GL1, OASIS, or any other suitable format for storing such design structures). Design structure 990 may comprise information such as, for example, test data files, design content files, manufacturing data, layout parameters, wires, levels of metal, vias, shapes, data for routing through the manufacturing line, and any other data required by a semiconductor manufacturer to produce an embodiment of the invention as shown in FIGS. 9, 12 and 15. Design structure 990 may then proceed to a stage 995 where, for example, design structure 990: proceeds to tape-out, is released to manufacturing, is released to a mask house, is sent to another design house, is sent back to the customer, etc.

[0047] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless

the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0048] The corresponding structures, materials, acts, and equivalents of all means or step plus function elements, if any, in the claims below are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the invention. The embodiments were chosen and described in order to best explain the principles of the invention and the practical application, and to enable others of ordinary skill in the art to understand the invention for various embodiments with various modifications as are suited to the particular use contemplated.

INDUSTRIAL APPLICABILITY

[0049] This invention finds utility in the manufacture of integrated circuits having carrier mobility enhanced channels.

CLAIMS

What is claimed is:

1. A method comprising:

forming a dummy gate structure (14) on a substrate (10);

forming a trench (20) in the dummy gate structure (14);

filling a portion of the trench (20) with a high carrier mobility material (22); and

filling a remaining portion of the trench (20) with gate oxide (24) and gate conductor material (26).

2. The method of claim 1, wherein the filling a portion of the trench (20) with a high carrier mobility material (22) includes depositing Ge material (22).

3. The method of claim 1, wherein the forming the trench (20) comprises removing a nitride cap layer (14d), a poly material (14b) and oxide material (14a) of the dummy gate structure (14).

4. The method of claim 1, wherein the forming the trench (20) includes etching a recess (28) into the substrate (10).

5. The method of claim 4, wherein the filling includes filling the recess (28) with Ge material (30).

6. The method of claim 4, wherein the forming the trench (20) includes extending a recess (32) into the substrate (10) and under sidewalls (14c) of the dummy gate structure (14).

7. The method of claim 6, wherein the filling includes filling the recess (32) under the sidewalls (14c) of the dummy gate structure (14) with Ge material (34).

8. The method of claim 1, wherein the filling the remaining portion of the trench (20) with gate material includes depositing a liner of high K dielectric (24) on the strain material and a gate metal or metal alloy (26) on the liner.

9. The method of claim 8, further comprising planarizing the gate metal or metal alloy (26) to a surface coplanar with a dielectric material (18).

10. The method of claim 1, wherein the trench (20) extends to a channel region of the dummy gate structure (14).

11. A method of forming a device, comprising:

building a dummy gate structure (14) on a substrate (10),

etching at least a portion of the dummy gate structure (14) to a channel region which results in a formation of a trench (20) between sidewalls (14c) of the dummy gate structure (14);

depositing a high carrier mobility material (22) on the substrate (10) within the trench (20); and

building a gate structure (24, 26) over the high carrier mobility material (22).

12. The method of claim 11, wherein the building the gate structure includes depositing a dielectric material (24) on the high carrier mobility material (22) and a metal gate material (26) on the liner.

13. The method of claim 11, wherein the depositing a high carrier mobility material on the substrate (10) within the trench (20) includes depositing Ge material (22).

14. The method of claim 11, wherein the etching comprises removing a nitride cap layer (14d), a poly material (14b) and oxide material (14a) of the dummy gate structure (14).

15. The method of claim 14, wherein the etching includes etching a recess (28) into the substrate (10).

16. The method of claim 15, wherein the depositing includes filling the recess (28) in the substrate (10) with Ge material (30).

17. The method of claim 14, wherein the etching includes extending a recess (32) into the substrate (10) and under the sidewalls (14c) of the dummy gate structure (14).

18. The method of claim 17, wherein the depositing includes filling the recess (32) under the sidewalls (14c) of the dummy gate structure (14) with Ge material (34).

19. The method of claim 11, wherein the building a gate structure over the high carrier mobility material (22) includes depositing a layer of high K dielectric (24) on the high carrier mobility material (22) and a metal or metal alloy (26) on the high K layer (24).

20. A structure comprising a germanium material (22) formed directly on a substrate (10) and at least within a trench (20) defined by sidewalls (14c) of a dummy gate structure (14).

21. The structure of claim 20, wherein the germanium material (30) is formed in the substrate (10).

22. The structure of claim 21, wherein the germanium material (34) is formed in the substrate (10) below the sidewalls (14c) of the dummy gate structure (14).

23. The structure of claim 20, wherein the dummy gate structure (14) is filled with a dielectric material (24) that lines inner portions of the sidewalls (14c) and a metal or metal alloy (26) that contacts with the dielectric material (24).

24. A design structure (920) embodied in a machine readable medium for designing, manufacturing, or testing an integrated circuit, the design structure comprising:

a germanium material (22) formed directly on a substrate (10) and at least within a trench (20) defined by sidewalls (14c) of a dummy gate structure (14);

a dielectric material (24) that lines inner portions of the sidewalls (14c); and

a metal or metal alloy (26) that contacts with the dielectric material (24).

25. The design structure of claim 24, wherein one of:

the design structure comprises a netlist (980);

the design structure (990) resides on storage medium as a data format used for the exchange of layout data of integrated circuits; and

the design structure resides in a programmable gate array.

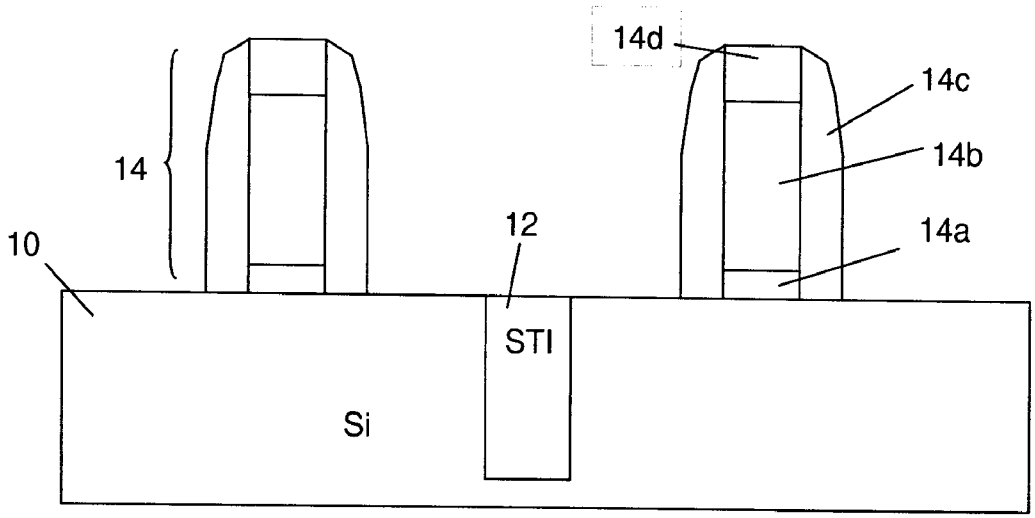


FIG. 1

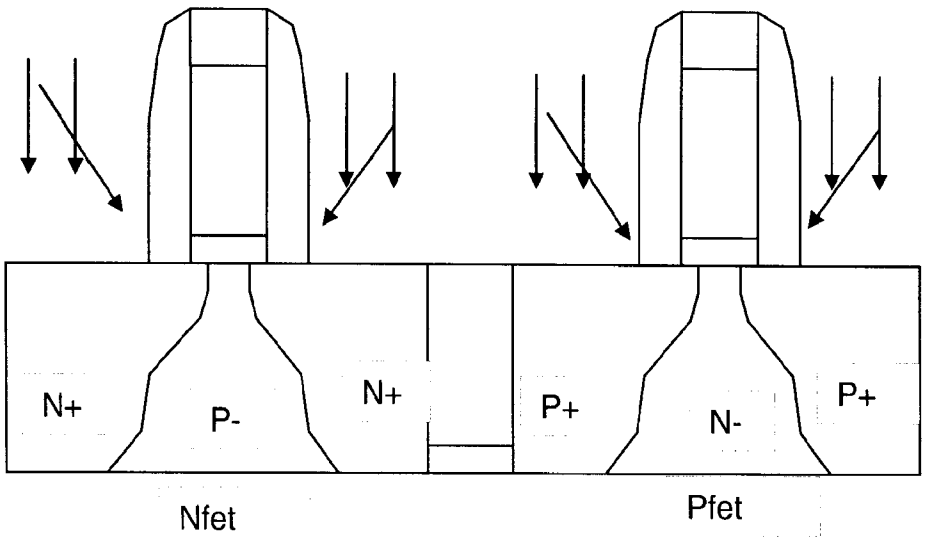


FIG. 2

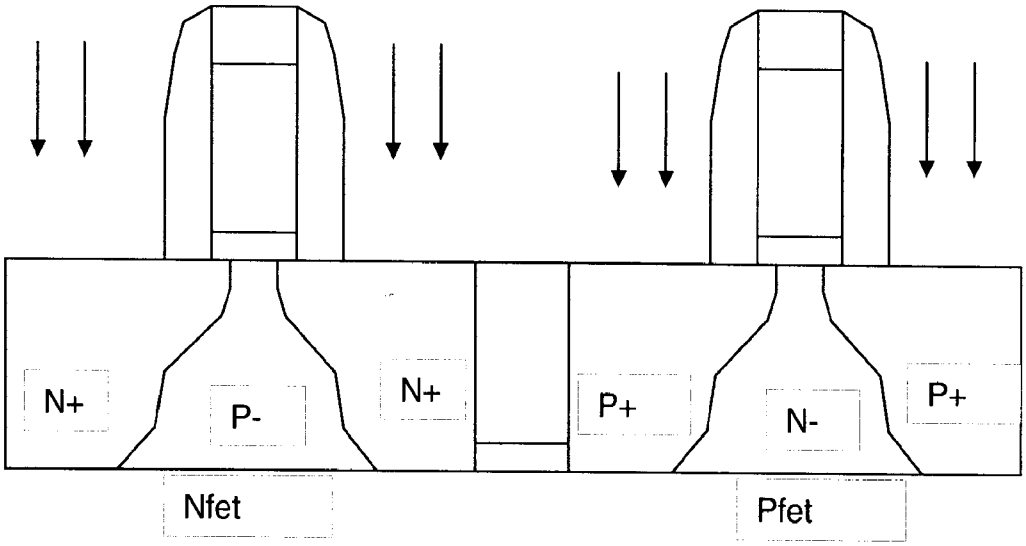


FIG. 3

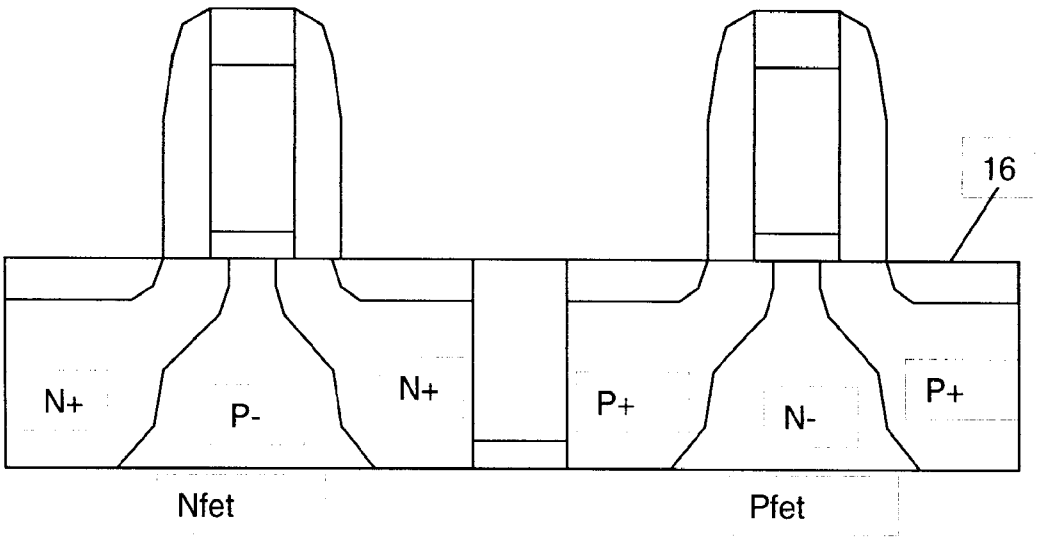


FIG. 4

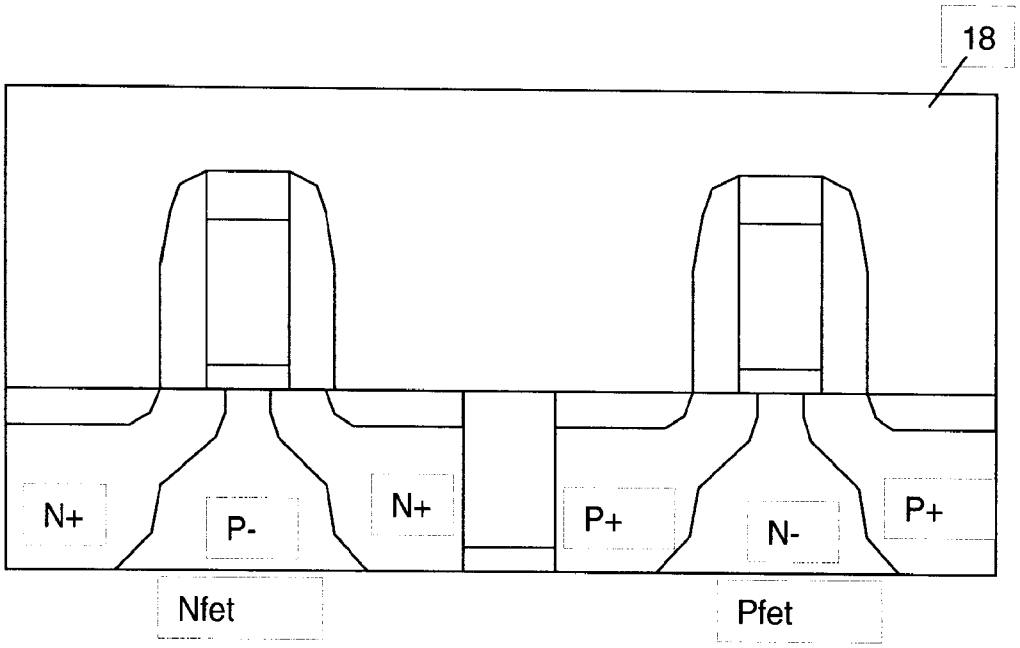


FIG. 5

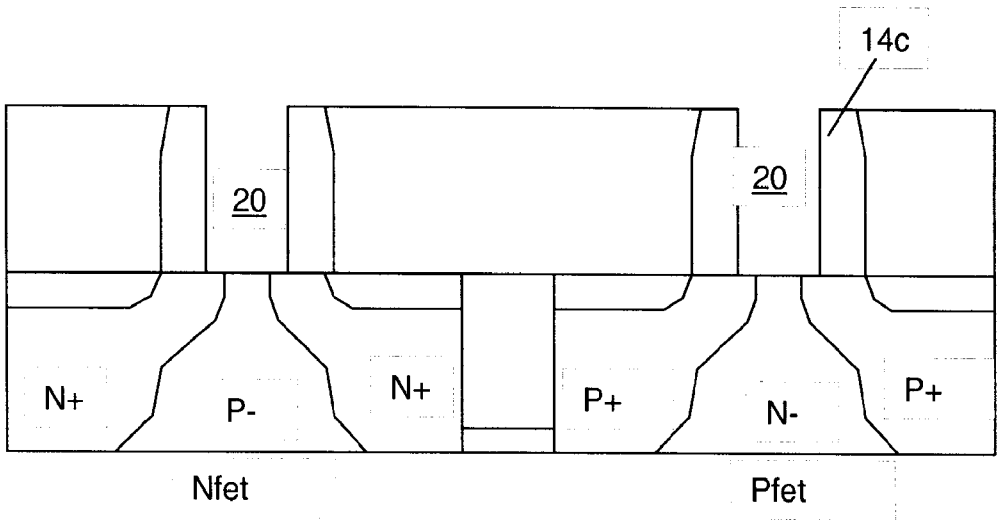


FIG. 6

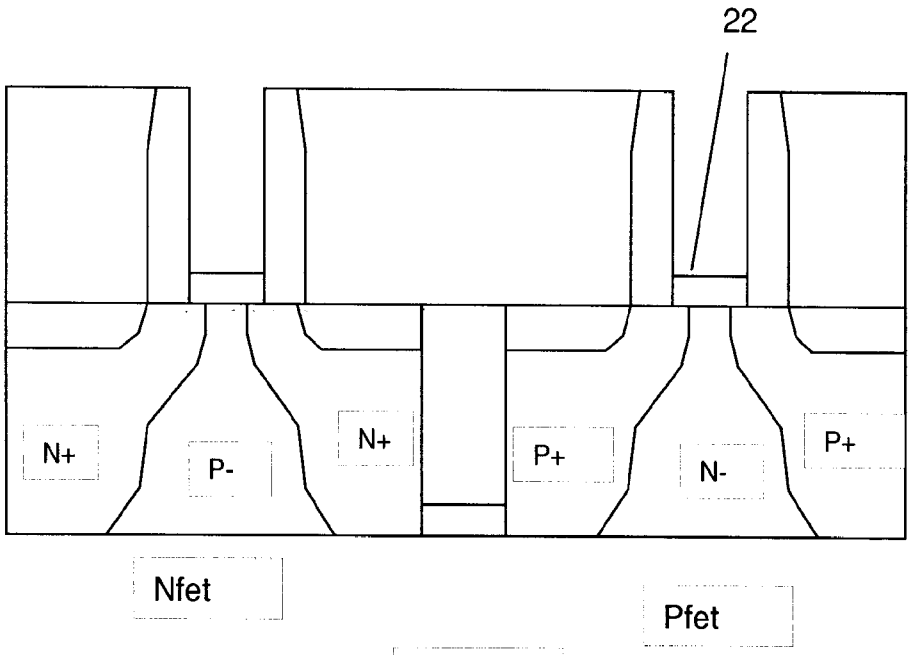


FIG. 7

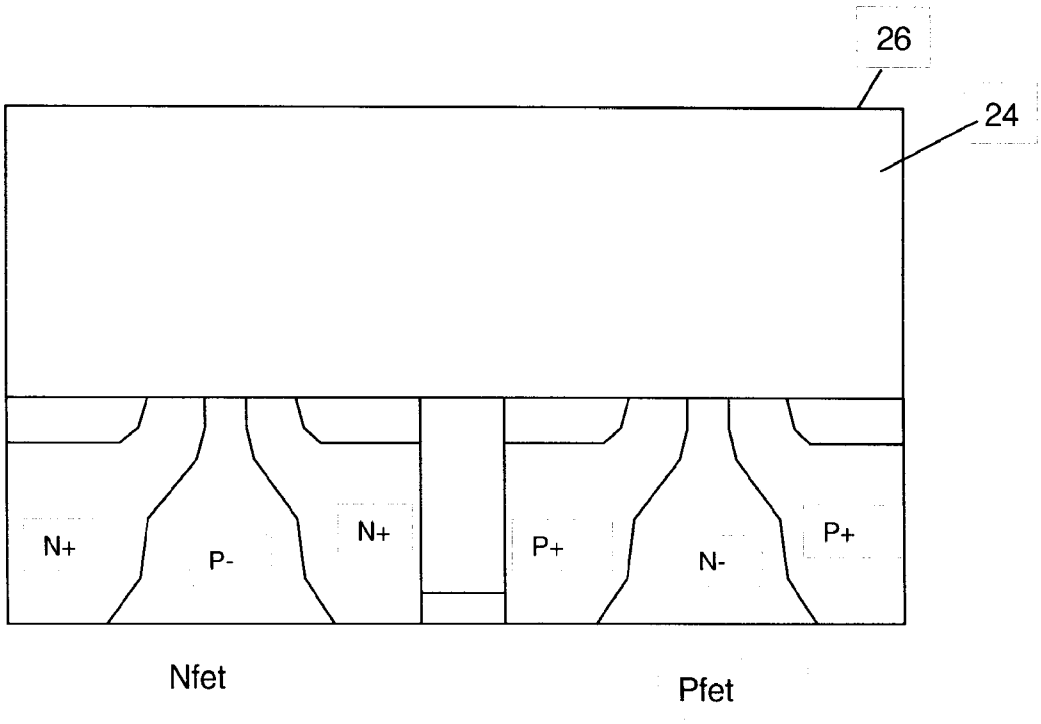


FIG. 8

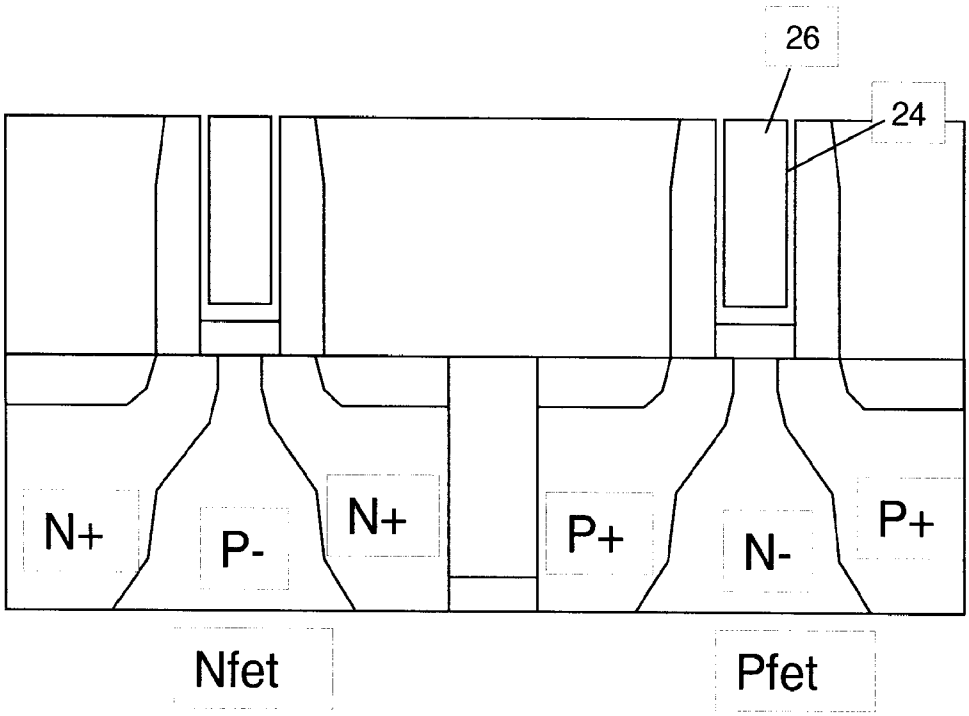


FIG. 9

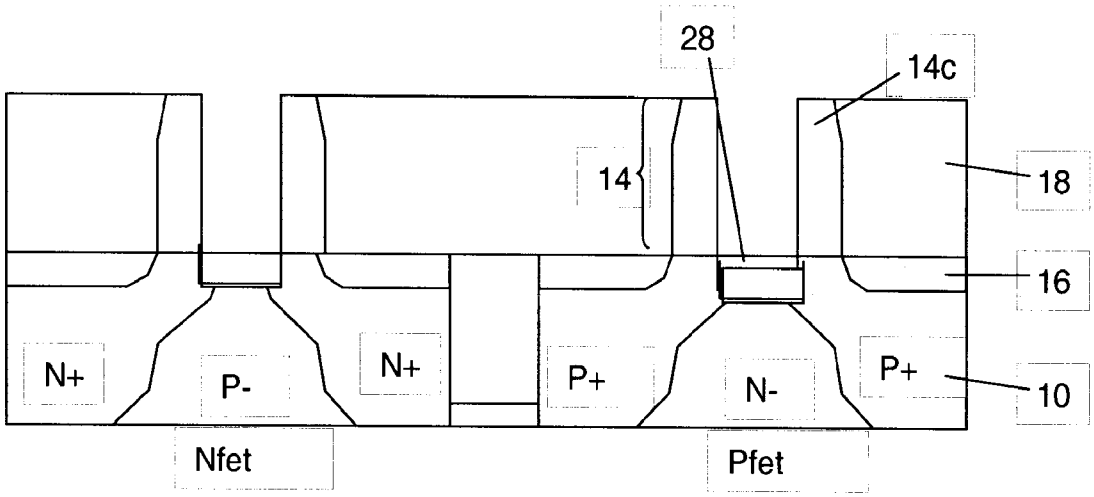


FIG. 10

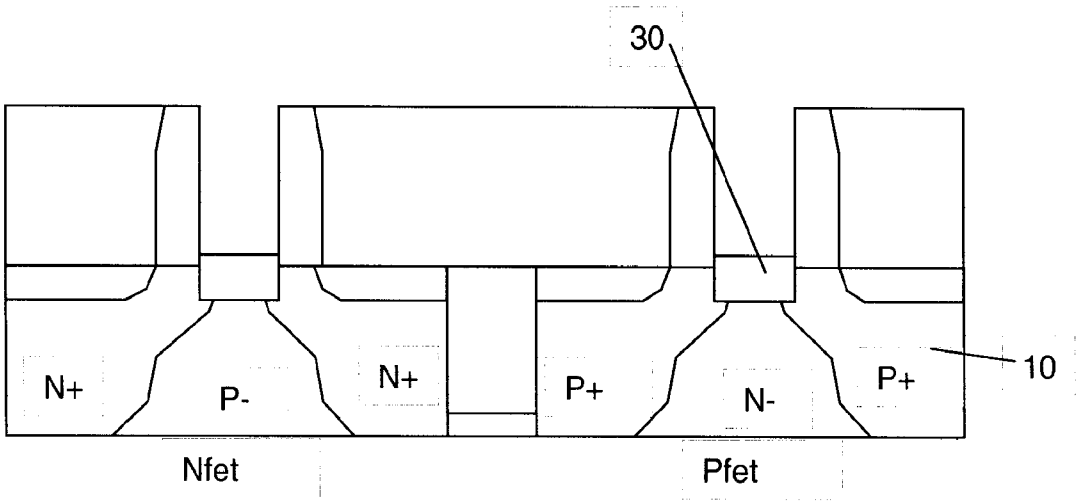


FIG. 11

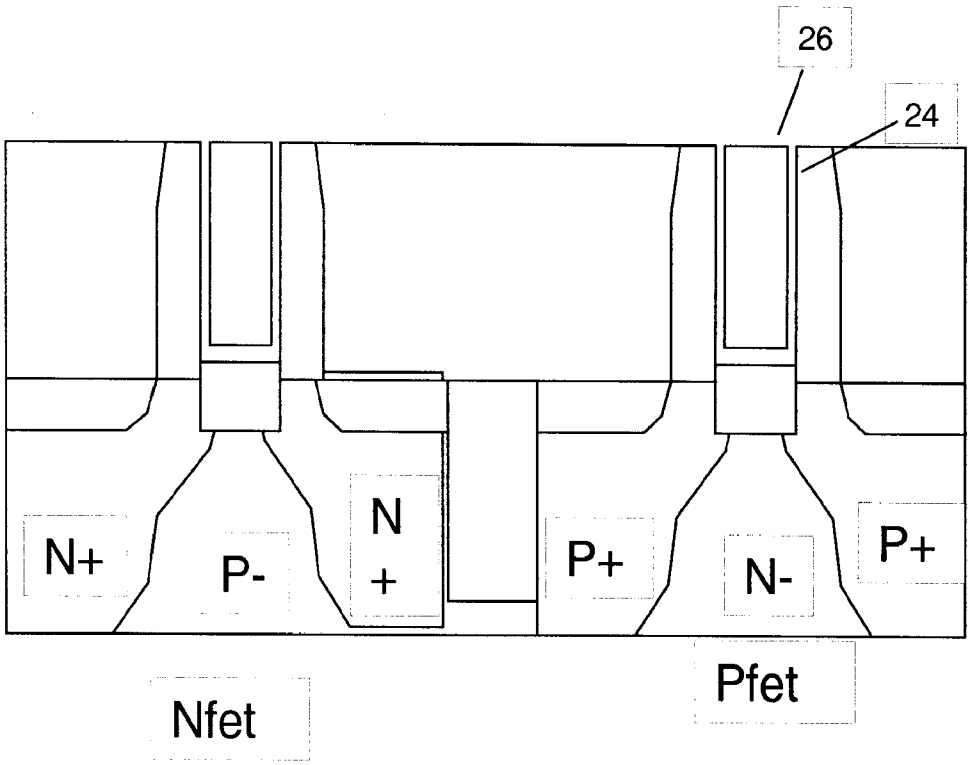


FIG. 12

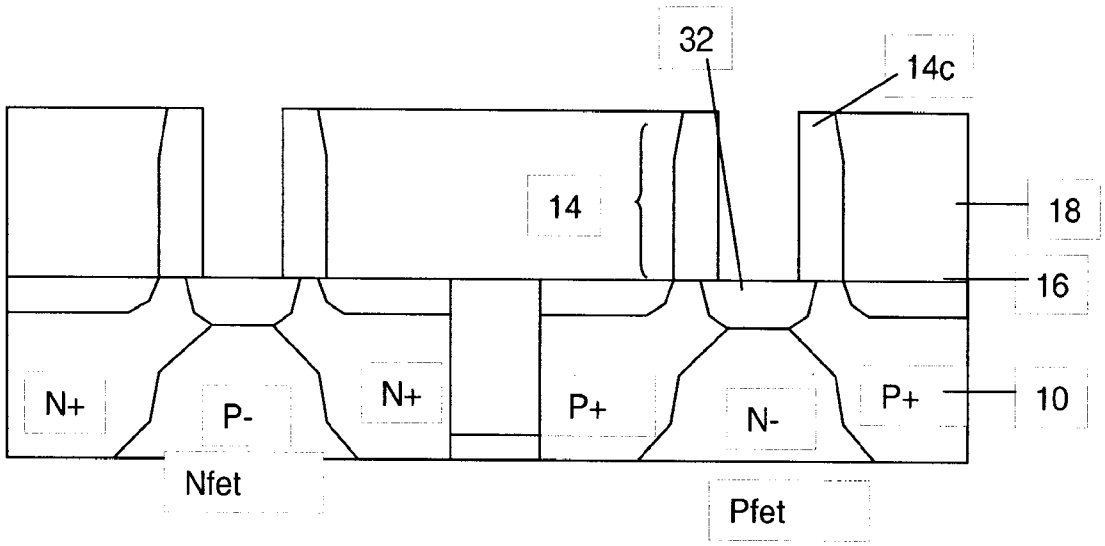


FIG. 13

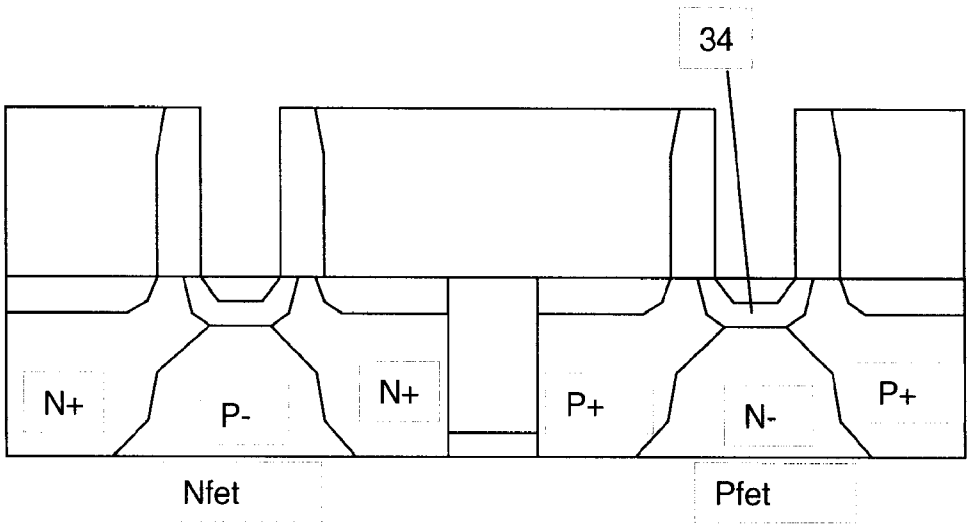


FIG. 14

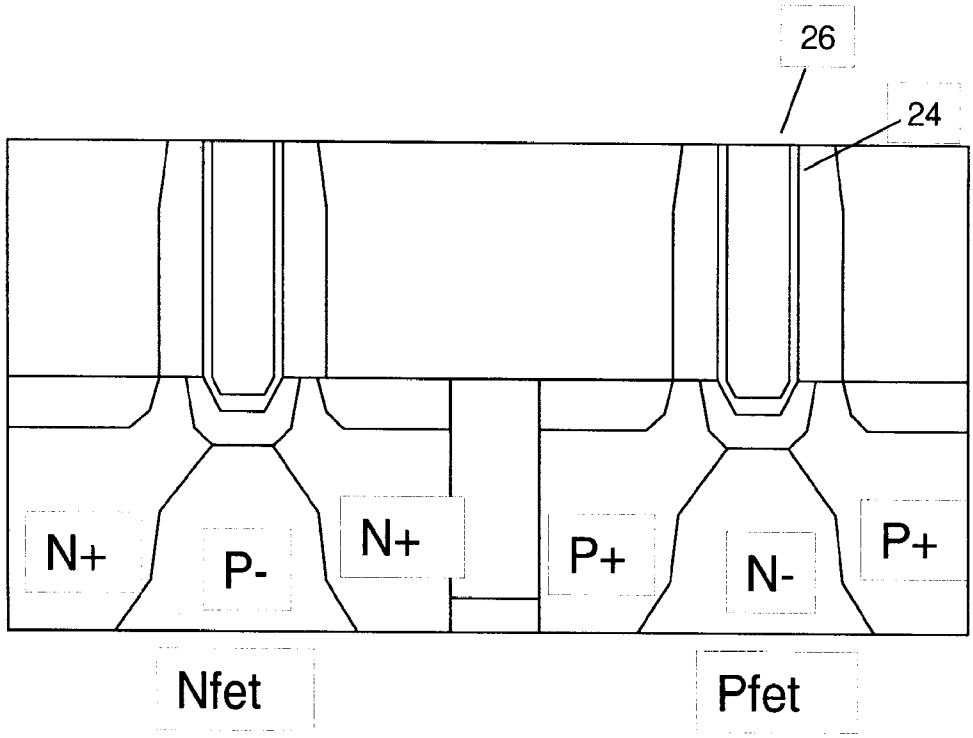


FIG. 15

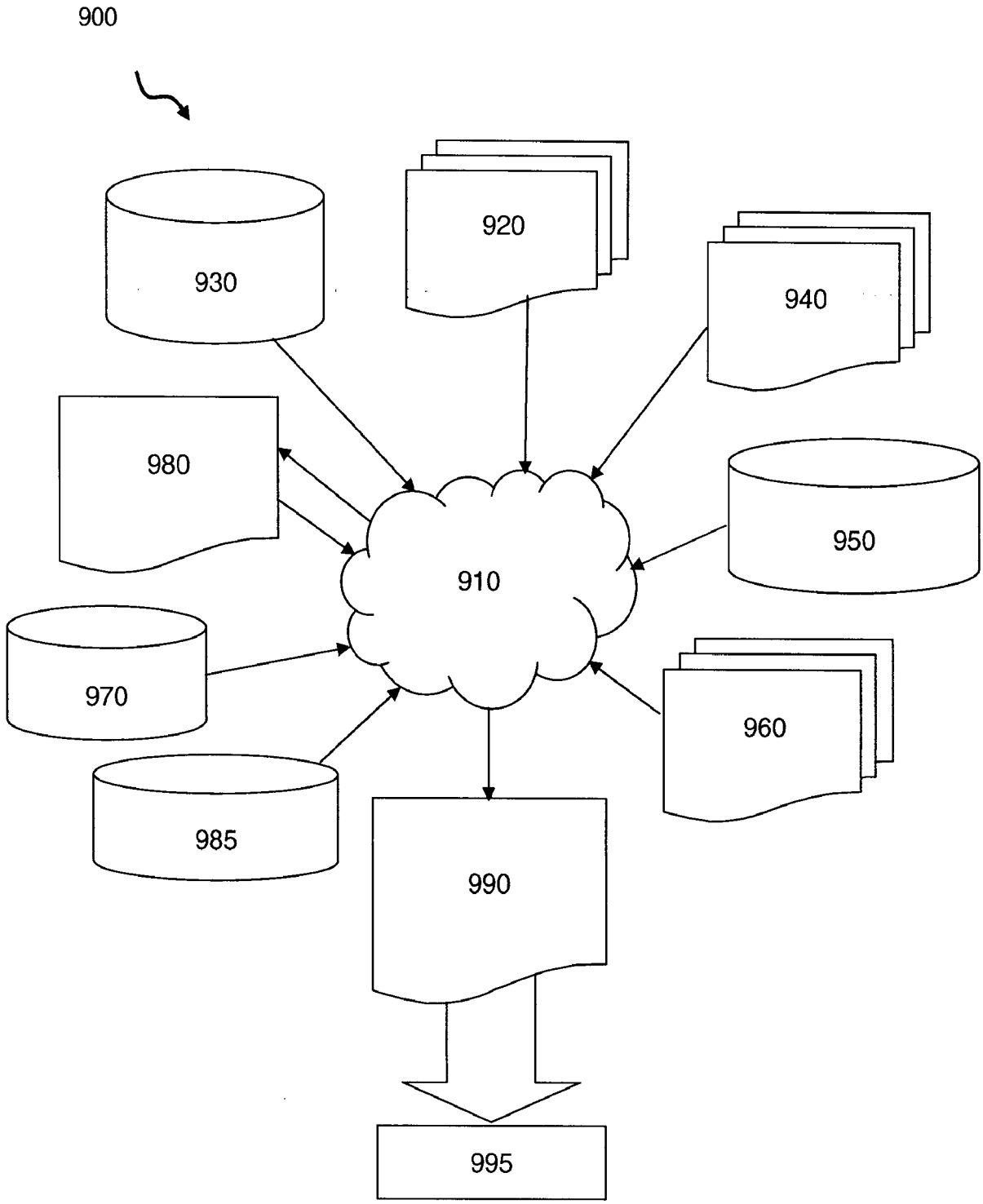


FIG. 16

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 09/45788

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/8238; 27/118 (2009.01)
USPC - 257/369; 257/E21.632
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 21/8238; 27/118 (2009.01)
USPC - 257/369; 257/E21.632

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
257/E27.108, 438/199 (keyword limited:see terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Google, Google Patents, PUBWEST (PGPB, USPT, USOC, EPAB, JPAB)
Search Terms Used: Transistor, field effect, dummy, gate, trench, Ge, channel, high-k, dielectric, oxide, electrode, metal, recessed, substrate, strain, semiconductor, germanium, dummy, liner, dummy gate.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ------ Y	US 2007/0032009 A1 (CURRIE et al.) 08 February 2007 (08.02.2007) para [0072], para [0075], para [0097], para [0100] - para [0103], para [0107], Figure 8a - Figure 8c.	1, 2, 8, 10-13, 19, 20 ---------- 3-7, 9, 14-18, 21-25
Y	US 6,664,592 B2 (INUMIYA et al.) 16 December 2003 (16.12.2003) col 31, ln 5 - ln 8, col 31, ln 30 - ln 34.	3, 14-18
Y	US 6,225,173 B1 (YU) 01 May 2001 (01.05.2001) col 2, ln 26 - ln 36, Figure 3 - Figure 5, col 4, ln 27 - ln 64.	4-7, 15-18, 21, 22
Y	US 6,278,164 B1 (HIEDA et al.) 21 August 2001 (21.08.2001) ol 5, ln 14 - ln 24, col 6, ln 54 - ln 58, Figure 5A - Figure 5E, col 5, ln 38 - ln 41, col 6, ln 24 - ln 28.	9, 23-25
Y	US 2008/0030254 A1 (ARSOVSKI et al.) 07 February 2008 (07.02.2008) para [0066] - para [0068].	24, 25

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
07 July 2009 (07.07.2009)	21 JUL 2009
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (April 2007)