



US 20030038356A1

(19) **United States**

(12) **Patent Application Publication**
Derderian

(10) **Pub. No.: US 2003/0038356 A1**

(43) **Pub. Date: Feb. 27, 2003**

(54) **SEMICONDUCTOR DEVICES INCLUDING STACKING SPACERS THEREON, ASSEMBLIES INCLUDING THE SEMICONDUCTOR DEVICES, AND METHODS**

(57) **ABSTRACT**

(76) Inventor: **James M. Derderian, Boise, ID (US)**

Correspondence Address:
TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110 (US)

A method for assembling semiconductor devices includes providing a first semiconductor device, securing spacers to noncircuit bond pads of the first semiconductor device, and positioning a second semiconductor device on the spacers. Adhesive material may be applied to a surface of one or both of the first and second semiconductor devices prior to positioning of the second semiconductor device, or introduced between first and second semiconductor devices. The noncircuit bond pads may be electrically isolated from other structures of the first semiconductor device or communicate with a ground or reference voltage plane, in which case the back side of the second semiconductor device may communicate with the ground or reference voltage plane upon being positioned against the spacers. Additional semiconductor devices may be added to the assembly. The first semiconductor device may be associated with a substrate. Assemblies and packages at least partially fabricated by the method are also disclosed.

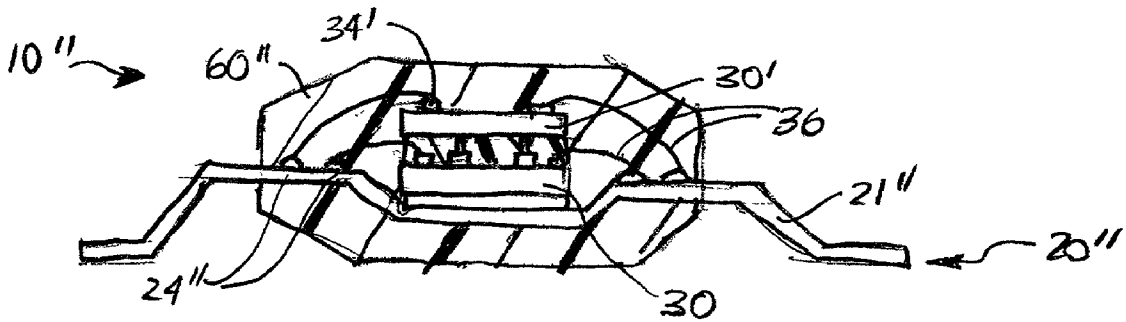
(21) Appl. No.: **09/939,258**

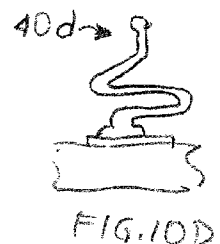
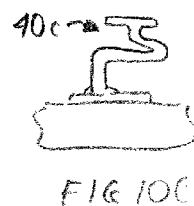
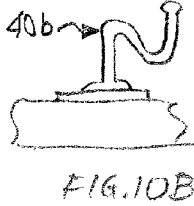
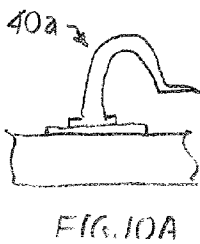
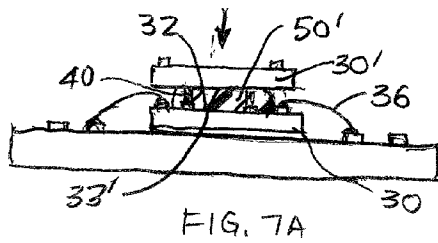
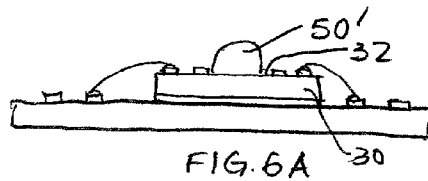
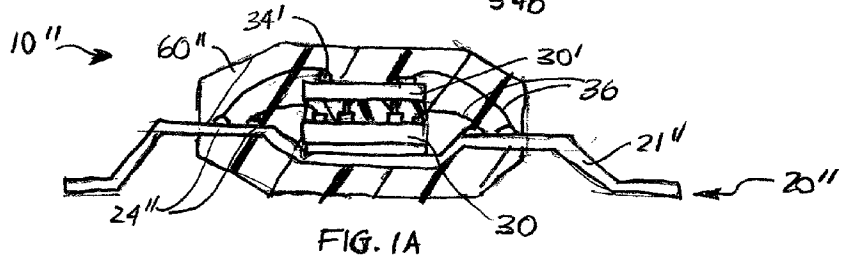
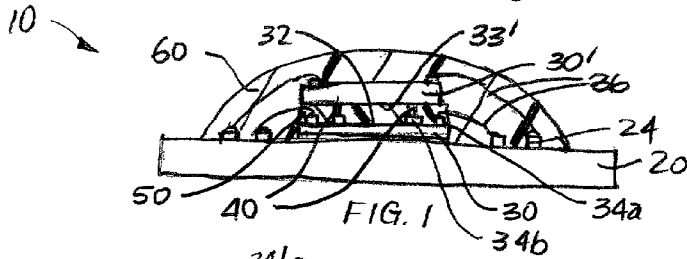
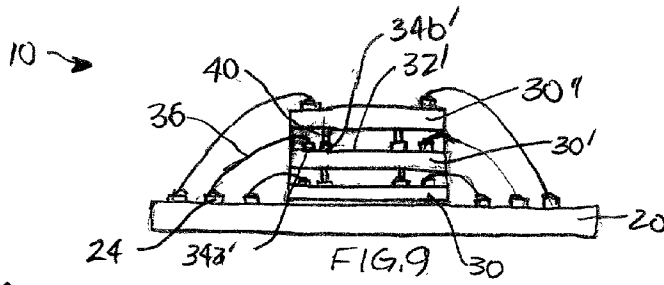
(22) Filed: **Aug. 24, 2001**

Publication Classification

(51) **Int. Cl.⁷ H01L 23/02**

(52) **U.S. Cl. 257/686**





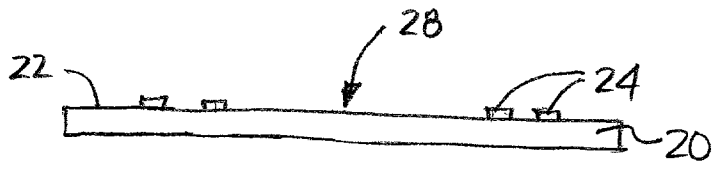


FIG. 2

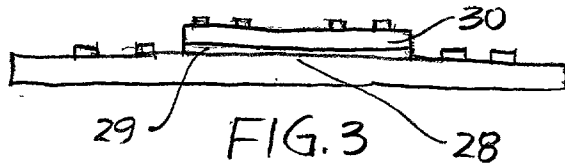


FIG. 3

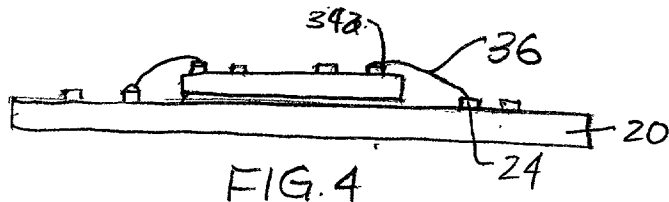


FIG. 4

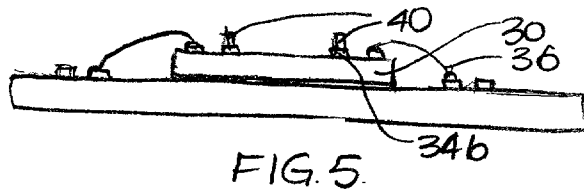


FIG. 5

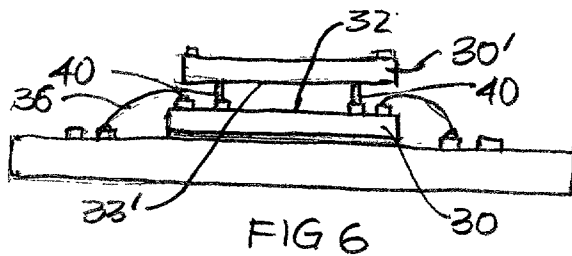


FIG. 6

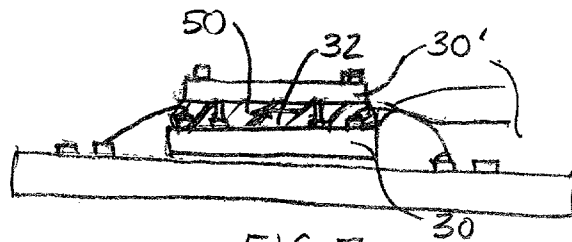


FIG. 7

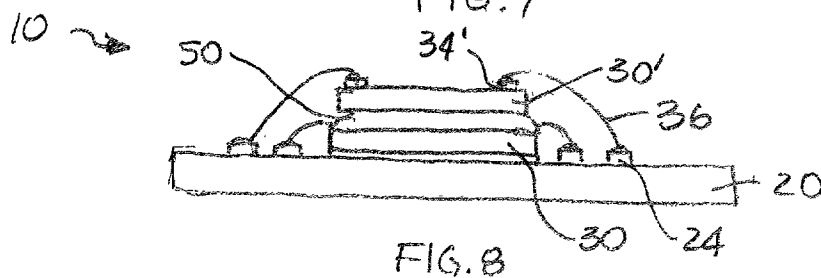


FIG. 8

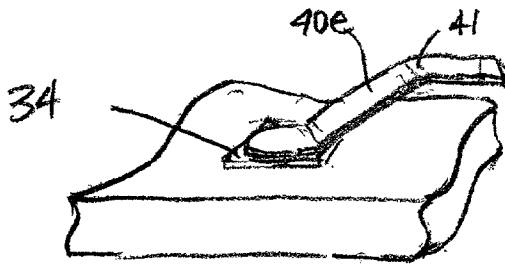


FIG. 11A

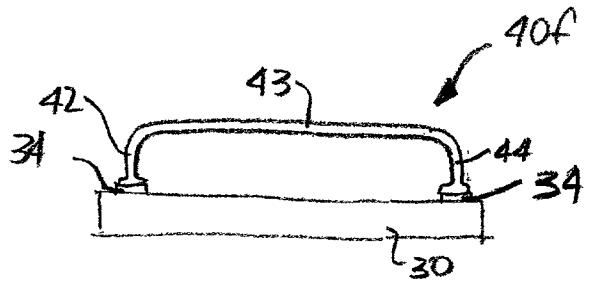


FIG. 11B

**SEMICONDUCTOR DEVICES INCLUDING
STACKING SPACERS THEREON, ASSEMBLIES
INCLUDING THE SEMICONDUCTOR DEVICES,
AND METHODS**

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to semiconductor device assemblies, or so-called “multi-chip modules”, in which two or more semiconductor devices are stacked relative to one another. More specifically, the present invention relates to semiconductor device assemblies in which the distances between adjacent stacked semiconductor devices are determined, at least in part, by the heights of structures protruding from bond pads on an active surface of the lower of the adjacent stacked semiconductor devices.

[0003] 2. Background of Related Art

[0004] In order to conserve the amount of surface area, or “real estate”, consumed on a carrier substrate, such as a circuit board, by semiconductor devices connected thereto, various types of increased density packages have been developed. Among these semiconductor device packages are the so-called multi-chip module (MCM), which includes assemblies of semiconductor devices that are stacked one on top of another. The amount of surface area on a carrier substrate that may be saved by stacking semiconductor devices is readily apparent—a stack of semiconductor devices consumes roughly the same amount of real estate on a carrier substrate as a single, horizontally oriented semiconductor device or semiconductor device package.

[0005] Due to the disparity in processes that are used to form different types of semiconductor devices (e.g., the number and order of various process steps), it has proven very difficult to actually incorporate different types of functionality into a single semiconductor device. Even in cases where semiconductor devices that carry out multiple functions can be fabricated, multi-chip modules that include semiconductor devices with differing functions (e.g., memory, processing capabilities, etc.) are often much more desirable since the separate semiconductor devices may be fabricated and assembled with one another much more quickly and cost-effectively (e.g., lower production costs due to higher volumes and lower failure rates).

[0006] Multi-chip modules may also contain a number of semiconductor devices that perform the same function, effectively combining the functionality of all of the semiconductor devices thereof into a single package.

[0007] An example of a conventional, stacked multi-chip module includes a carrier substrate, a first, larger semiconductor device secured to the carrier substrate, and a second, smaller semiconductor device positioned over and secured to the first semiconductor device. The second semiconductor device does not overlie bond pads of the first semiconductor device and, thus, the second semiconductor device does not cover bond wires that electrically connect bond pads of the first semiconductor device to corresponding contacts or terminals of the carrier substrate. Such a multi-chip module is disclosed and illustrated in U.S. Pat. No. 6,212,767, issued to Tandy on Apr. 10, 2001 (hereinafter “the ‘767 patent”). As the sizes of the semiconductor devices of such a multi-chip module continue to decrease as they are positioned increas-

ingly higher on the stack, the obtainable heights of such multi-chip modules become severely limited.

[0008] Another example of a conventional multi-chip module is described in U.S. Pat. No. 5,323,060, issued to Fogal et al. on Jun. 21, 1994 (hereinafter “the ‘060 patent”). The multi-chip module of the ‘060 patent includes a carrier substrate with semiconductor devices disposed thereon in a stacked arrangement. The individual semiconductor devices of each multi-chip module may be the same size or different sizes, with upper semiconductor devices being either smaller or larger than underlying semiconductor devices. Adjacent semiconductor devices of each of the multi-chip modules disclosed in the ‘060 patent are secured to one another with an adhesive layer. The thickness of each adhesive layer exceeds the loop heights of bond wires protruding from a semiconductor device upon which that adhesive layer is to be positioned. Accordingly, the presence of each adhesive layer prevents the back side of an overlying, upper semiconductor device from contacting bond wires that protrude from an immediately underlying, lower semiconductor device of the multi-chip module. The adhesive layers of the multi-chip modules disclosed in the ‘060 patent do not encapsulate or otherwise cover any portion of the bond wires that protrude from any of the lower semiconductor devices. The multi-chip modules of the ‘060 patent may be undesirably thick due to the large vertical distance between each adjacent pair of semiconductor devices that ensures that the back side of each upper semiconductor device is electrically isolated from the bond wires protruding over the active surface of the next, lower semiconductor device, which may result in wasted adhesive and excessive stack height.

[0009] A similar but more compact multi-chip module is disclosed in U.S. Pat. Re. No. 36,613, issued to Ball on Mar. 14, 2000 (hereinafter “the ‘613 patent”). The multi-chip module of the ‘613 patent includes many of the same features as those disclosed in the ‘060 patent, including adhesive layers that space vertically adjacent semiconductor devices apart a greater distance than the loop heights of bond wires protruding from the lower of the adjacent dice. The use of thinner bond wires with low loop profile wire bonding techniques permits adjacent semiconductor devices of the multi-chip module disclosed in the ‘060 patent to be positioned more closely to one another than adjacent semiconductor devices of the multi-chip modules disclosed in the ‘060 patent. Nonetheless, additional space remains between the tops of the bond wires protruding from one semiconductor device and the back side of the next higher semiconductor device of such a stacked multi-chip module.

[0010] Preformed silicon spacers are typically used to separate stacked semiconductor devices a sufficient distance from one another that the back side of an upper semiconductor device will not contact underlying bond wires or other discrete conductive elements protruding above an active surface of a next lower semiconductor device. The use of silicon, polymeric films, or other preformed spacers is somewhat undesirable from the standpoint that each time a preformed spacer is used, additional alignment and assembly steps are required. For example, a preformed spacer must be positioned on an active surface of a semiconductor device in such a manner that the bond pads thereof or discrete conductive elements extending thereover are exposed beyond an outer periphery of the spacer. Further, when silicon spacers are used, adhesive material must be

applied to either the spacer or the semiconductor devices the spacer is to be positioned between. As is well understood by those in the art of semiconductor device fabrication, additional alignment and assembly steps may decrease product yields and consequently increase production costs.

[0011] The vertical distance that adjacent semiconductor devices of a stacked type multi-chip module are spaced apart from one another may be reduced by arranging the semiconductor devices such that upper semiconductor devices are not positioned over bond pads of immediately underlying semiconductor devices or the bond wires or other discrete conductive elements protruding from these bond pads. Thus, adjacent semiconductor devices may be vertically spaced apart from one another a distance that is about the same as or less than the loop heights of the bond wires that protrude above the active surface of the lower semiconductor device. U.S. Pat. No. 6,051,886, issued to Fogal et al. on Apr. 18, 2000 (hereinafter "the '886 patent") discloses such a multi-chip module. According to the '886 patent, wire bonding is not conducted until all of the semiconductor devices of such a multi-chip module have been assembled with one another and with the underlying carrier substrate. The semiconductor devices of the multi-chip modules disclosed in the '886 patent must have bond pads that are arranged on opposite peripheral edges. Semiconductor devices with bond pads positioned adjacent the entire peripheries thereof could not be used in the multi-chip modules of the '886 patent. This is a particularly undesirable limitation due to the ever-increasing feature density of state-of-the-art semiconductor devices, which is often accompanied by a consequent need for an ever-increasing number of bond pads on semiconductor devices, as well as arrangement of bond pads over greater portions of the active surfaces of semiconductor devices.

[0012] In view of the foregoing, it appears that stacked assemblies in which an upper semiconductor device could be stacked over bond pads of an adjacent, lower semiconductor device to provide flexibility in bond pad number and placement would be useful, as would methods for forming such stacked assemblies. It also appears that methods and structures that reduce the number of different steps required in forming assemblies of stacked semiconductor devices would also be useful.

SUMMARY OF THE INVENTION

[0013] The present invention includes an assembly of stacked semiconductor devices in which a first semiconductor device may be secured to or otherwise associated with a substrate, such as a circuit board, an interposer, another semiconductor device, or a lead frame. Bond pads of the first semiconductor device may be electrically connected to corresponding contact areas of the substrate by way of discrete conductive elements or otherwise, as known in the art. A second semiconductor device of the assembly is positioned over and secured to the first semiconductor device and may overlie at least some discrete conductive elements protruding above the active surface of the first semiconductor device.

[0014] The back side of the second semiconductor device may be spaced apart from the active surface of the first semiconductor device, bond pads thereof, and any underlying discrete conductive elements by way of spacers that

protrude from noncircuit, or "dummy", bond pads of the first semiconductor device. Alternatively, the spacers may protrude from and communicate with bond pads that communicate with a ground or reference voltage plane for the first semiconductor device. The distance between the first semiconductor device and the second semiconductor device is determined, at least in part, by the heights the spacers protrude over the active surface of the first semiconductor device.

[0015] Spacers that comprise either substantially linear or nonlinear elements of substantially uniform height may be formed on so-called "dummy" or grounded bond pads, which are also referred to herein as noncircuit bond pads, of the first semiconductor device by wire bond formation techniques. Nonlinear spacers may be shaped in such a manner as to impart them with some resilient compressibility upon receiving a force in the directions of the lengths thereof. The thicknesses (e.g., diameters) of the spacers may impart them with sufficient strength to collectively withstand the weight of a second semiconductor device resting thereon, as well as the force that may be applied thereto as the second semiconductor device is placed thereon. Alternatively, or in addition, the spacers may be coated with one or more materials that enhance their strengths.

[0016] While it is preferred that the discrete conductive elements that extend between the first and second semiconductor devices be spaced apart from the back side of the second semiconductor device, other means for electrically isolating the discrete conductive elements from the back side of an immediately overlying, second semiconductor device are also within the scope of the present invention. By way of example only, the discrete conductive elements may be electrically isolated from the back side of the second semiconductor device by way of a dielectric coating on at least contacting portions of one or both of the discrete conductive elements and the back side.

[0017] The second semiconductor device, which may be larger, smaller, or the same size as the underlying, first semiconductor device, is secured over the first semiconductor device by way of an adhesive material, which may comprise a dielectric material, disposed between the first and second semiconductor devices.

[0018] In one exemplary embodiment of an assembly including stacked semiconductor devices, the adhesive material may fill the entire gap between the first and second semiconductor devices, substantially encapsulating the portion of each discrete conductive element located therebetween. The adhesive material may have a low enough viscosity (high liquidity), that air or other gases located between the first and second semiconductor devices is readily displaced, reducing the tendency of voids to form around discrete conductive elements or between the first and second semiconductor devices.

[0019] When a low viscosity material, such as a conventional underfill material, is used to space the first and second semiconductor devices apart from one another, the second semiconductor device is positioned over the first semiconductor device, resting on and supported collectively by the spacers protruding from the active surface of the first semiconductor device. The second semiconductor device may be at least temporarily secured to the first semiconductor device by way of a small quantity of adhesive material,

such as an adhesive polymer, solder flux, or the like, which may, for example, be placed on a surface of the first semiconductor device, the second semiconductor device, one or more discrete conductive elements, and/or one or more spacers prior to positioning the second semiconductor device over the first semiconductor device. The low viscosity adhesive material may then be introduced between the first and second semiconductor devices.

[0020] The wetting properties of a low viscosity adhesive material may facilitate spreading thereof over the active surface of the first semiconductor device and the back side of the second semiconductor device, as well as capillary action or "wicking" thereof through the spaces between the first and second semiconductor devices and around the portions of discrete conductive elements located between the first and second semiconductor devices. Spreading of the adhesive material may be aided by application of heat thereto or by mechanical vibration of the assembly. When a fixed quantity of adhesive material that is smaller than the volume between the first and second semiconductor devices is used, the surface tension of the adhesive material may cause the distance between the first and second semiconductor devices to decrease as the adhesive material spreads therebetween, thereby decreasing the overall height of the assembly. If the adhesive material is used to decrease the distance between the first and second semiconductor devices in this manner, it is preferred that the spacers be configured to compress somewhat and that a sufficient amount of adhesive material be used to prevent delicate, raised discrete conductive elements, such as bond wires, from being bent, distorted, or collapsed onto one another.

[0021] An adhesive material that has a relatively higher viscosity may be used in another exemplary embodiment of assembly including stacked semiconductor devices. Due to its high viscosity, such an adhesive material may be applied over a portion of the active surface of the first semiconductor device prior to positioning the second semiconductor device thereover. Alternatively, the second semiconductor device may be positioned over the first semiconductor device, then a high viscosity adhesive material introduced therebetween.

[0022] When a high viscosity adhesive material is used, a controlled amount of force or loading may be applied to one or both of the active surface of the second semiconductor device or the bottom of the first semiconductor device or a substrate, if any, to which the first semiconductor device is secured in such a manner that the first semiconductor device and second semiconductor device are biased toward one another. In this manner, the distance between the first and second semiconductor devices may be controlled. Force or loading may also be applied to the active surface of the second semiconductor device to facilitate spreading of a high viscosity adhesive material between the first and second semiconductor devices. If such force or loading is used, it is preferred that the force or loading not be sufficient to undesirably deformably stress (e.g., bend, kink, distort, or collapse) the spacers that protrude from the active surface of the first semiconductor device or the first semiconductor device itself.

[0023] Once the adhesive material cures, it may provide some additional physical support to the second semiconductor device. The adhesive material may also serve as a dielectric coating for the discrete conductive elements or the

back side of the second semiconductor device. Bond pads of the second semiconductor device may also be electrically connected to one or both of corresponding contact areas of the substrate and corresponding bond pads the first semiconductor device.

[0024] Of course, assemblies incorporating teachings of the present invention may include more than two semiconductor devices in stacked arrangement.

[0025] Once the semiconductor devices of such an assembly have been secured to one another and electrically connected with a substrate or with one another, the assembly may be packaged, as known in the art.

[0026] Other features and advantages of the present invention will become apparent to those of ordinary skill in the art through consideration of the ensuing description, the accompanying drawings, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] In the drawings, which illustrate exemplary embodiments of various aspects of the present invention:

[0028] **FIG. 1** is a cross-sectional representation of a first semiconductor device assembly incorporating teachings of the present invention, in which semiconductor devices are positioned in a stacked arrangement and at least one of the semiconductor devices is electrically connected to a circuit board;

[0029] **FIG. 1A** is a cross-sectional representation of a second semiconductor device assembly according to the present invention, wherein semiconductor devices are stacked and at least one of the semiconductor devices is electrically connected to leads;

[0030] **FIG. 2** is a side view of an exemplary substrate;

[0031] **FIG. 3** is a side view of a first semiconductor device disposed on the substrate of **FIG. 2**;

[0032] **FIG. 4** is a side view depicting electrical connection of the semiconductor device of **FIG. 3** to the substrate;

[0033] **FIG. 5** is a side view depicting formation of spacers on noncircuit or grounded bond pads of the semiconductor device of **FIG. 3**;

[0034] **FIG. 6** is a side view that illustrates positioning of a second semiconductor device over the first semiconductor device and placement of the second semiconductor device on the spacers of **FIG. 5**;

[0035] **FIG. 7** is a cross-sectional representation of the assembly of **FIG. 6**, showing the introduction of an adhesive material between the first and second semiconductor devices;

[0036] **FIG. 6A** is a side view that illustrates the alternate disposal of a quantity of adhesive material onto the semiconductor device of **FIG. 5**;

[0037] **FIG. 7A** is a side view depicting the positioning of a second semiconductor device over the first semiconductor device and contacting a back side of the second semiconductor device with the adhesive material of **FIG. 6A**;

[0038] **FIG. 8** is a side view that illustrates electrical connection of the second semiconductor device with the substrate;

[0039] FIG. 9 is a side view which shows that additional semiconductor devices may be stacked over the first and second semiconductor devices and electrically connected to the substrate;

[0040] FIGS. 10A-10D schematically depict exemplary compressible spacers that may be used in accordance with teachings of the present invention; and

[0041] FIGS. 11A and 11B schematically depict other configurations of spacers that may be used in accordance with teachings of the present invention.

DETAILED DESCRIPTION

[0042] With reference to FIG. 1, an exemplary embodiment of semiconductor device assembly 10 is illustrated. As depicted, semiconductor device assembly 10 includes a first semiconductor device 30 and a second semiconductor device 30' positioned over and spaced apart from first semiconductor device 30 by way of spacers 40.

[0043] Semiconductor device assembly 10 may also include a substrate 20, such as the depicted circuit board, an interposer, another semiconductor device, leads, or other suitable, known substrates.

[0044] First semiconductor device includes first and second sets of bond pads 34a, 34b, respectively, on an active surface 32 thereof. Bond pads 34a communicate with circuitry of first semiconductor device 30 and, therefore, may also be referred to as "circuit bond pads". Accordingly, and as depicted, bond pads 34a are configured to be secured to discrete conductive elements 36, such as bond wires, tape-automated bond (TAB) elements comprising conductive traces carried on a flexible dielectric film, thermocompression bonded leads, or the like. When included in semiconductor device assembly 10, discrete conductive elements 36 electrically connect and, thus, establish electrical communication between bond pads 34a and corresponding contact areas 24 of a substrate 20 of semiconductor device assembly 10.

[0045] Bond pads 34b, which are also referred to herein as "noncircuit bond pads", are either bond pads that do not communicate with internal circuitry of first semiconductor device 30, or bond pads that communicate with a ground plane of first semiconductor device 30. Communication of noncircuit bond pads 34b with the ground or reference voltage plane of semiconductor device 30 is schematically represented by broken line G.

[0046] Spacers 40, which may comprise wire or other conductive elements, are secured to noncircuit bond pads 34b of first semiconductor device 30. Structural support may be imparted to each spacer 40 by use of thicker conductive elements, stronger materials, coatings that strengthen the conductive elements thereof, or as otherwise known in the art.

[0047] The height of each spacer 40 separates a back side 33' of second semiconductor device 30' a sufficient distance from active surface 32 of the underlying first semiconductor device 30 to prevent any discrete conductive elements 36 protruding above active surface 32 from electrically shorting against back side 33'. Thus, the heights of spacers 40 may prevent back side 33' of second semiconductor device 30' from contacting discrete conductive elements 36. Alternatively,

if at least portions of one or both of discrete conductive elements 36 that contact back side 33' and portions of back side 33' that contact discrete conductive elements 36 are coated with an electrically insulative material (e.g., dielectric polymer, nonconductive oxide, such as a metal oxide, silicon oxide, or glass, etc.), the heights of spacers 40 may prevent discrete conductive elements 36 from being undesirably distorted or from collapsing onto one another when second semiconductor device 30' is placed over first semiconductor device 30.

[0048] Although spacers 40 are depicted in FIG. 1 as comprising substantially linear members that protrude from noncircuit bond pads 34b in a direction that is substantially perpendicular to the plane in which active surface 32 is located, spacers of other configurations are also within the scope of the present invention. By way of example only, the structures disclosed in U.S. Pat. Nos. 5,476,211; 5,832,601; 5,852,871; 5,864,946; and 5,884,398, each of which has been assigned to Form Factor, Inc. of Livermore, Calif. (hereinafter collectively referred to as "the Form Factor patents"), the disclosures of each of which are hereby incorporated in their entireties by this reference, may also be employed as spacers 40. FIGS. 10A-10D depict exemplary, resiliently compressible spacers 40a-40d, respectively, that may be used in the present invention.

[0049] A quantity of adhesive material 50 may be located between first semiconductor device 30 and second semiconductor device 30'. Adhesive material, which is preferably electrically nonconductive, or dielectric, may adhere to at least portions of active surface 32 of first semiconductor device 30, as well as to all or part of second semiconductor device 30' to secure first semiconductor device 30 and second semiconductor device 30' to one another. Exemplary adhesive materials that are useful in semiconductor device assembly 10 include low viscosity materials, such as thermoset resins, two-stage epoxies, or the like, as well as higher viscosity materials including, but not limited to, epoxies, silicones, silicone-carbon resins, polyimides, polyurethanes, and parylenes.

[0050] As depicted in FIG. 1, semiconductor device assembly 10 may also include a protective encapsulant 60. As shown, protective encapsulant 60 comprises a so-called "glob top". Protective encapsulant 60 may cover and, thus protect, at least portions of one or more of second semiconductor device 30', first semiconductor device 30, discrete conductive elements 36, and portions of substrate 20 located adjacent to first semiconductor device 30. Alternatively, protective encapsulant 60 may comprise a molded structure, such as is formed by transfer or pot molding processes.

[0051] FIG. 1A depicts another embodiment of semiconductor device assembly 10" in which semiconductor devices 30 and 30' are in stacked arrangement. Semiconductor device assembly 10" also includes a substrate 20" in the form of leads 21". Bond pads 34a of first semiconductor device and bond pads 34' of second semiconductor device 30' are electrically connected to corresponding contact areas 24" of the leads of substrate 20" by way of discrete conductive elements 36. As an alternative, leads 21" may comprise leads-over-chip (LOC) type leads that extend partially over an active surface 32 of first semiconductor device 30. Such leads 21" may be electrically connected to corresponding bond pads 34a by way of discrete conductive

elements 36. Alternatively, LOC type leads 21" may extend over corresponding bond pads 34a and be secured thereto by way of thermocompression bonds, direct-attach conductive structures that may, for example, be formed from solder, z-axis conductive elastomer, conductive epoxy, or conductor-filled epoxy, or otherwise, as known in the art.

[0052] In addition, and as depicted, semiconductor device assembly 10" may include a protective encapsulant 60". One or more of first semiconductor device 30, second semiconductor device 30', and discrete conductive elements 36 may be packaged by protective encapsulant 60". Portions of substrate 20" that are located adjacent to first and second semiconductor devices 30, 30' may also be enveloped by protective encapsulant 60". As shown, protective encapsulant 60" comprises a molded structure (e.g., a transfer molded or pot molded structure), although other types of protective encapsulants (e.g., glob-top encapsulants), or packages, are also within the scope of the present invention.

[0053] Turning now to FIGS. 2-9, exemplary embodiments of forming semiconductor device assemblies are depicted.

[0054] As shown in FIG. 2, a substrate 20 is provided. Although substrate 20 is depicted as a circuit board, which includes one or more external connective elements (not shown) in the form of pins, solder balls, plug-in members, or the like, other types of substrates and their accompanying external connective elements are also within the scope of the present invention, including, without limitation, interposers, other semiconductor devices, and leads. The depicted substrate 20 includes conductive areas 24, in the form of terminals, which are positioned on an upper surface 22 thereof adjacent a die-attach location 28 of upper surface 22.

[0055] In FIG. 3, a first semiconductor die 30 is positioned over die-attach location 28 and secured thereto with an adhesive element 29, such as an adhesive material (e.g., a conventional die attach material), an adhesive coated film (e.g., a polyimide film), or the like.

[0056] As shown in FIG. 4, discrete conductive elements 36 may be formed or placed between and secured to bond pads 34a of first semiconductor device 30 and their corresponding contact areas 24 of substrate 20. Each discrete conductive element 36 electrically connects and, thus, establishes electrical communication between a bond pad 34a and its corresponding contact area 24. By way of example only, discrete conductive elements 36 may comprise bond wires that are formed between bond pads 34a and contact areas 24 with wire bonding equipment. As another example, each discrete conductive element 36 may comprise a TAB element or a lead that is placed between and in contact with a bond pad 34a and its corresponding contact area 24 and secured thereto by thermocompression bonding processes.

[0057] FIG. 5 illustrates the placement or formation of spacers 40 on noncircuit bond pads 34b of first semiconductor device 30. Spacers 40 may be secured to or formed on noncircuit bond pads 34b before, after, or during the formation or placement and securing of discrete conductive elements 36. As an example, and not to limit the scope of the present invention, spacers 40 may be fabricated on noncircuit bond pads 34b by use of wire bonding equipment and accompanying wire bonding techniques, such as conventional wire bonding processes or those disclosed in the Form

Factor patents. Alternative types of spacers 40, such as balls, bumps, pillars, or columns, may be formed and/or secured to noncircuit bond pads 34b by appropriate techniques known in the art. For example, a solder mask and solder reflow techniques may be used to form and secure solder balls or bumps to noncircuit bond pads 34b. Other types of spacers 40 may be positioned on a noncircuit bond pad 34b and secured thereto by use of a conductive adhesive or by heating or otherwise reflowing adjacent portions of one or both of spacer 40 and noncircuit bond pad 34b. Of course, the manner in which a spacer 40 is formed and secured to a noncircuit bond pad 34b depends, at least in part, upon the type of spacer 40 being used.

[0058] Once spacers 40 have been formed, a second semiconductor device 30' may be positioned over first semiconductor device 30, as depicted in FIG. 6. Back side 33' of second semiconductor device 30' rests upon uppermost portions of spacers 40. As depicted, the heights of spacers 40 may prevent discrete conductive elements 36 from contacting back side 33' of second semiconductor device 30', electrically isolating discrete conductive elements 36 and back side 33' from one another. If spacers 40 are connected to a ground plane, back side 33' of second semiconductor device 30' is thus also grounded by contact with spacers 40.

[0059] Prior to introduction of an adhesive material between at least portions of active surface 32 of first semiconductor device 30 and back side 33' of second semiconductor device 30', a position of second semiconductor device 30' may be maintained by way of adhesive material (not shown), such as a pressure-sensitive adhesive material, solder flux, or the like, disposed on either back side 33' of second semiconductor device 30', on an active surface 32 of first semiconductor device 30, and/or on uppermost portions of spacers 40.

[0060] As depicted in FIG. 7, when second semiconductor device 30' has been properly positioned over first semiconductor device 30, at least partially unconsolidated adhesive material 50 may be introduced between first and second semiconductor devices 30 and 30'. Adhesive material 50 preferably has a low enough viscosity and high enough surface tension to facilitate introduction thereof by capillary action, or wicking, between first and second semiconductor devices 30 and 30'. The viscosity of adhesive material 50 may also be low enough to prevent bond wire sweep. Nonetheless, the viscosity and/or surface tension of adhesive material 50 may be sufficient to prevent flowing thereof off of active surface 32 of first semiconductor device 30. By way of example only, adhesive material 50 may comprise an epoxy, a silicone, a silicone-carbon resin, a polyimide, a polyurethane, or a parylene.

[0061] FIGS. 6A and 7A illustrate an alternative to the processes discussed herein with reference to FIGS. 6 and 7.

[0062] In FIG. 6A, a higher viscosity adhesive material 50' is disposed on active surface 32 of first semiconductor device 30. Adhesive material 50' has a higher viscosity and/or surface tension than adhesive material 50, which allows adhesive material 50' to form a raised structure prior to being cured to an at least semisolid state without flowing.

[0063] Next, as depicted in FIG. 7A, a second semiconductor device 30' is positioned over first semiconductor

device **30**, as well as over adhesive material **50'** on active surface **32** thereof. As one or both of first semiconductor device **30** and second semiconductor device **30'** are moved toward one another (e.g., by die attach equipment), back side **33'** of second semiconductor device **30'** contacts adhesive material **50'**, causing adhesive material **50'** to spread somewhat over back side **33'**, as well as active surface **32** of first semiconductor device **30**. First and second semiconductor devices **30** and **30'** are moved toward one another at least until back side **33'** of second semiconductor device **30'** contacts upper portions of spacers **40**. If spacers **40** are somewhat compressible, first and second semiconductor devices **30** and **30'** may be moved even more closely toward each other. Adhesive material **50'** may spread to a lateral location beyond which discrete conductive elements **36** are exposed, or may partially or fully encapsulate portions of discrete conductive elements **36** that are located between first semiconductor device **30** and second semiconductor device **30'**.

[0064] Adhesive material **50, 50'** may then be fully or partially hardened to an at least semisolid state, as appropriate for the type of material employed, securing first and second semiconductor devices **30** and **30'** to one another. By way of example, thermoplastic adhesive materials **50, 50'** may be cooled or permitted to cool. Other types of adhesive materials **50, 50'** may be cured by processes such as heat curing, snap curing, UV curing, catalytic curing, or appropriate combinations thereof. As an example of the use of a combination of curing processes, some known adhesive materials **50, 50'**, such as some of the die attach and thermal adhesives marketed as QUANTUM adhesives by Dexter Corporation of Industry, California, may be cured by both UV curing and heat or snap curing processes. Exposed, edge portions of these adhesive materials **50, 50'** may be UV-cured to form an external fillet which contains internal, unconsolidated adhesive material **50, 50'**, which may then be cured by heat or snap curing processes.

[0065] If spacers **40** comprise somewhat compressible structures, such as those depicted in FIGS. **10A-10D** and described in the Form Factor patents, an adhesive material **50, 50'** that shrinks somewhat upon cured may be employed.

[0066] Alternative configurations of spacers **40e** and **40f** are shown in FIGS. **11A** and **11B**. Spacer **40e** of FIG. **11A** includes a ribbon wire **41** that is secured to a bond pad **34** by way of a wedge bond, while spacer **40f** of FIG. **11B** is a structure that includes opposite end portions **42** and **44** that are secured to different bond pads **34** of a semiconductor device **30** and a central portion **43** located between end portions **42** and **44** and extending over a portion of a semiconductor device **30**.

[0067] Once adhesive material **50** has cured sufficiently to secure the relative positions of first semiconductor device **30** and second semiconductor device **30'**, discrete conductive elements **36** may be formed between bond pads **34a'** of second semiconductor device **30'** and corresponding contact areas **24** of substrate **20**, as depicted in FIG. **8**. Discrete conductive elements **36** may comprise bond wires, TAB elements, thermocompression bonded leads, or any other suitable, known type of discrete conductive element. Discrete conductive elements **36** are formed by suitable techniques which, of course, depend upon the particular type of discrete conductive element **36** used in assembly **10**.

[0068] In the event that assembly of additional semiconductor devices **30''** over semiconductor devices **30** and **30'** is desired, as shown in FIG. **9**, second semiconductor device **30'** may include noncircuit bond pads **34b'** on an active surface **32'** thereof, upon which additional spacers **40** may be formed. These additional spacers **40** may be formed prior to, concurrently with, or subsequent to the formation of discrete conductive elements **36** between bond pads **34a'** of second semiconductor device **30'** and their corresponding contact areas **24** of substrate **20**. The processes described herein with reference to FIGS. **6-8** may be repeated until assembly **10** includes a desired number of semiconductor devices.

[0069] Although the foregoing description contains many specifics, these should not be construed as limiting the scope of the present invention, but merely as providing illustrations of some exemplary embodiments. Similarly, other embodiments of the invention may be devised which do not depart from the spirit or scope of the present invention. Features from different embodiments may be employed in combination. The scope of the invention is, therefore, indicated and limited only by the appended claims and their legal equivalents, rather than by the foregoing description. All additions, deletions, and modifications to the invention, as disclosed herein, which fall within the meaning and scope of the claims are to be embraced thereby.

What is claimed is:

1. A semiconductor device assembly, comprising:
 - at least one semiconductor device; and
 - a plurality of mutually laterally spaced discrete spacers protruding from a surface of said at least one semiconductor device, said spacers defining a distance said surface of said at least one semiconductor device is to be spaced apart from another semiconductor device to be positioned in superimposed relation with said at least one semiconductor device.
2. The semiconductor device assembly of claim 1, wherein at least one of said spacers is resiliently compressible.
3. The semiconductor device assembly of claim 1, wherein at least one of said spacers protrudes from an active surface of said at least one semiconductor device.
4. The semiconductor device assembly of claim 3, wherein each of said spacers protrudes from an active surface of said at least one semiconductor device.
5. The semiconductor device assembly of claim 4, wherein said plurality of spacers are arranged to stably support said another semiconductor device.
6. The semiconductor device assembly of claim 1, further comprising:
 - said another semiconductor device positioned adjacent said spacers, opposite from said at least one semiconductor device.
7. The semiconductor device assembly of claim 6, further comprising:
 - adhesive material between said at least one semiconductor device and said another semiconductor device.
8. The semiconductor device assembly of claim 7, wherein said adhesive material is located between adjacent spacers.

9. The semiconductor device assembly of claim 6, wherein said spacers are electrically isolated from internal circuitry of said at least one semiconductor device.

10. The semiconductor device assembly of claim 1, wherein said spacers comprise electrically conductive material.

11. The semiconductor device assembly of claim 10, wherein said spacers communicate with a ground plane of said at least one semiconductor device.

12. The semiconductor device assembly of claim 1, further comprising:

a substrate with which at least one semiconductor device is associated.

13. The semiconductor device assembly of claim 12, wherein said substrate comprises at least one of a circuit board, an interposer, a semiconductor device, and leads.

14. The semiconductor device assembly of claim 12, wherein at least one bond pad of said at least one semiconductor device is in communication with a corresponding contact area of said substrate.

15. The semiconductor device assembly of claim 14, further comprising:

at least one discrete conductive element extending from said at least one bond pad, over an active surface of said at least one semiconductor device, to said corresponding contact area.

16. The semiconductor device assembly of claim 15, wherein heights of said spacers exceed a maximum height said at least one discrete conductive element protrudes above said active surface.

17. The semiconductor device assembly of claim 1, wherein said spacers are secured to noncircuit bond pads of said at least one semiconductor device.

18. A semiconductor device assembly, comprising:

a substrate;

a first semiconductor device associated with said substrate, bond pads of said first semiconductor device in communication with corresponding contact areas of said substrate;

mutually laterally spaced discrete spacers positioned on and protruding from an active surface of said first semiconductor device; and

a second semiconductor device comprising a back side positioned on said mutually laterally spaced discrete spacers.

19. The semiconductor device assembly of claim 18, wherein said substrate comprises one of a circuit board, an interposer, another semiconductor device, and leads.

20. The semiconductor device assembly of claim 18, wherein said bond pads and said corresponding contact areas communicate by way of discrete conductive elements positioned therebetween.

21. The semiconductor device assembly of claim 20, wherein said discrete conductive elements comprise at least one of bond wires, tape-automated bond elements, and thermocompression bonded leads.

22. The semiconductor device of claim 18, wherein said mutually laterally spaced discrete spacers are secured to noncircuit bond pads of said first semiconductor device.

23. The semiconductor device assembly of claim 22, wherein said laterally discrete spacers comprise conductive material.

24. The semiconductor device assembly of claim 23, wherein said mutually laterally spaced discrete spacers are electrically isolated from internal circuitry of said first semiconductor device.

25. The semiconductor device assembly of claim 23, wherein said mutually laterally spaced discrete spacers are in communication with a ground or reference voltage plane of said first semiconductor device.

26. The semiconductor device assembly of claim 25, wherein said back side of said second semiconductor device is also in communication with said ground or reference voltage plane.

27. The semiconductor device assembly of claim 20, wherein heights of said laterally discrete spacers exceed a maximum height said discrete conductive elements protrude above said active surface.

28. The semiconductor device assembly of claim 18, wherein at least one of said laterally discrete spacers is compressible.

29. The semiconductor device assembly of claim 18, wherein said second semiconductor device comprises a dielectric layer on at least portions thereof that contact said laterally discrete spacers.

30. The semiconductor device assembly of claim 18, wherein bond pads of said second semiconductor device communicate with corresponding contact areas of said substrate by way of discrete conductive elements positioned therebetween.

31. The semiconductor device assembly of claim 18, further comprising:

an adhesive layer between said first semiconductor device and said second semiconductor device.

32. The semiconductor device assembly of claim 31, wherein at least some of said mutually laterally spaced discrete spacers extend through said adhesive layer.

33. The semiconductor device assembly of claim 18, further comprising: at least one additional semiconductor device positioned over said second semiconductor device.

34. The semiconductor device assembly of claim 18, further comprising: an encapsulant material substantially covering said first semiconductor device, said second semiconductor device, said discrete conductive elements, and portions of said substrate located adjacent to said first semiconductor device.

35. The semiconductor device assembly of claim 18, further comprising: at least one external connective element carried by said substrate and in electrical communication with at least one corresponding contact area of said substrate.

36. A method for assembling semiconductor devices in stacked arrangement, comprising:

providing a substrate;

securing a first semiconductor device to said substrate;

electrically connecting bond pads of said first semiconductor device to corresponding contact areas of said substrate;

positioning discrete spacers at mutually laterally spaced positions on at least one of an active surface of said first semiconductor device and a back side of said second semiconductor device;

positioning a second semiconductor device over said first semiconductor device, said spacers separating said first semiconductor device from said second semiconductor device.

37. The method of claim 36, wherein said providing comprises providing at least one of a circuit board, an interposer, another semiconductor device, and leads.

38. The method of claim 36, wherein said electrically connecting comprises placing discrete conductive elements between bond pads of said first semiconductor device and corresponding contact areas of said substrate.

39. The method of claim 38, wherein said placing comprises wire bonding.

40. The method of claim 38, wherein said placing comprises tape-automated bonding.

41. The method of claim 38, wherein said placing comprises thermocompression bonding leads between said bond pads and said corresponding contact areas.

42. The method of claim 36, wherein said positioning spacers comprises positioning resilient compressible spacers.

43. The method of claim 36, wherein said positioning spacers comprises securing spacers to noncircuit bond pads.

44. The method of claim 43, wherein said positioning spacers comprises positioning said spacers in electrical isolation from internal circuitry of said first semiconductor device.

45. The method of claim 43, wherein said positioning spacers comprises positioning spacers in communication with a ground plane of said first semiconductor device.

46. The method of claim 36, wherein said positioning said second semiconductor device comprises positioning said second semiconductor device with a back side thereof facing an active surface of said first semiconductor device.

47. The method of claim 36, further comprising:

electrically connecting bond pads of said second semiconductor device and corresponding contact areas of said substrate.

48. The method of claim 36, further comprising:

applying adhesive material at least to a surface of said first semiconductor device.

49. The method of claim 48, wherein said applying adhesive material comprises introducing adhesive material between said first and second semiconductor devices.

50. The method of claim 36, further comprising:

positioning at least one additional semiconductor device over said second semiconductor device.

51. The method of claim 36, further comprising:

substantially encapsulating said first semiconductor device, said spacers, said second semiconductor device, and portions of said substrate located laterally adjacent said first semiconductor device.

52. The method of claim 36, further comprising:

placing at least one external conductive element in communication with at least one corresponding contact area of said substrate.

* * * * *