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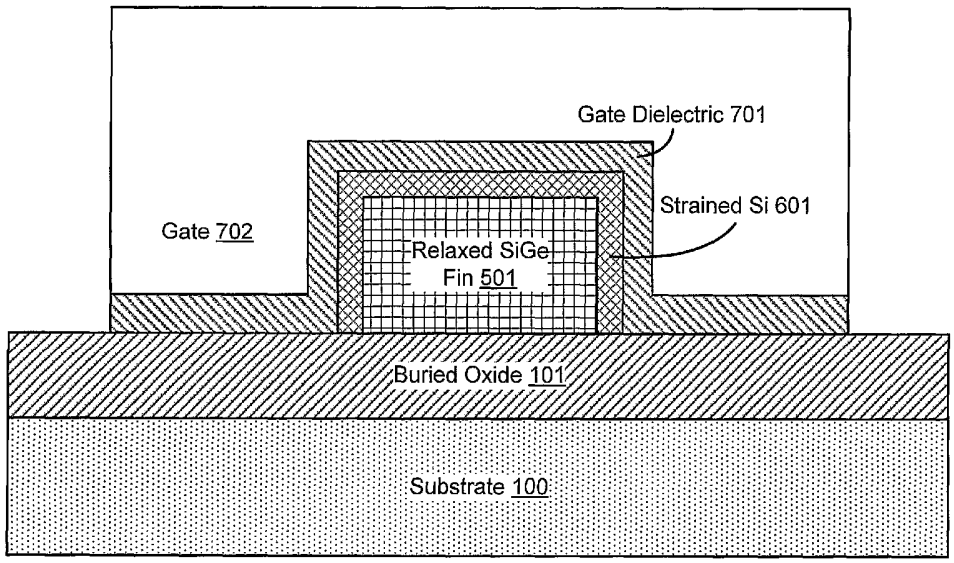
(54) **Title:** NON-PLANAR MOS STRUCTURE WITH A STRAINED CHANNEL REGION



(57) **Abstract:** An embodiment is a non-planar MOS transistor structure including a strained channel region. The combination of a non-planar MOS transistor structure, and in particular an NMOS tri-gate transistor, with the benefits of a strained channel yields improved transistor drive current, switching speed, and decreased leakage current for a given gate length width versus a non-planar MOS structure with an unstrained channel or planar MOS structure including a strained channel.

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NON-PLANAR MOS STRUCTURE WITH A STRAINED CHANNEL REGION

FIELD

[0001] Embodiments of the invention relate to a transistor structure and in particular to a non-planar transistor structure that incorporates a strained channel.

BACKGROUND

[0002] Traditional planar metal oxide semiconductor (MOS) transistor technology is approaching fundamental physical limits for certain transistor features past which it will be necessary to employ alternate materials, processing techniques, and /or transistor structure to support continued transistor performance improvement according to Moore's Law.

[0003] One such paradigm shift is a non-planar MOS structure. One particular non-planar MOS structure is a non-planar tri-gate transistor. A tri-gate transistor employs a three-dimensional gate structure that permits electrical signals to conduct along the top of the transistor gate and along both vertical sidewalls of the gate. The conduction along three sides of the gates enables, among other improvements, higher drive currents, faster switching speeds, and shorter gate lengths, simultaneously increasing the performance of the transistor while occupying less substrate area versus a planar MOS structure. The tri-gate structure further decreases the amount of current leakage, a problem to which ever shrinking planar MOS devices are prone, by improving the short channel characteristics of the transistor.

[0004] Another paradigm shift involves using strained semiconductor material for various portions of a transistor. Adding tensile or compressive strain to a semiconductor (depending on the particular application) lattice increases the carrier mobility within the strained semiconductor. In particular, for an NMOS device imparting tensile strain to a semiconductor increases the electron mobility (i.e., dominant charge carrier in an NMOS device). The increased carrier mobility in turn allows for higher drive current and corresponding faster switching speeds.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1: illustration of cross section of a silicon on insulator (SOI) substrate

[0006] FIG. 2: illustration of the substrate of Figure 1 and strained silicon germanium and silicon with a hydrogen implant for Smart Cut process

[0007] FIG. 3: illustration of a cross section of the substrate of Figure 2 following the Smart Cut formation of strained silicon germanium and silicon

[0008] FIG. 4: illustration of a cross section of the substrate of Figure 3 following an anneal to form relaxed silicon germanium

[0009] FIG. 5: illustration of a cross section of the substrate of Figure 4 following the patterning of the relaxed silicon germanium

[0010] FIG. 6: illustration of a cross section of the substrate of Figure 5 following the formation of strained silicon on the relaxed silicon germanium

[0011] FIG. 7: illustration of a cross section of the substrate of Figure 6 following the formation of a gate dielectric and gate to form a non-planar MOS structure including a strained channel

[0012] FIG. 8: illustration of a perspective view of the substrate of Figure 7

[0013] FIG. 9: illustration of the perspective view of Figure 8 following an implant to form source and drain regions

DETAILED DESCRIPTION

[0014] Embodiments of a non-planar MOS transistor structure with a strained channel region will be described. Reference will now be made in detail to a description of these embodiments as illustrated in the drawings. While the embodiments will be described in connection with these drawings, there is no intent to limit them to drawings disclosed herein. On the contrary, the intent is to cover all alternatives, modifications, and equivalents within the spirit and scope of the described embodiments as defined by the accompanying claims.

[0015] Simply stated, an embodiment is a non-planar MOS transistor structure including a strained channel region. The combination of a non-planar MOS transistor structure, and in particular an NMOS tri-gate transistor, with the benefits of a strained channel yields

improved transistor drive current, switching speed, and decreased leakage current for a given gate length, gate width, and operating voltage versus a non-planar MOS structure with an unstrained channel or planar MOS structure including a strained channel.

[0016] Figure 1 illustrates a cross section of a silicon on insulator (SOI) substrate. SOI substrates are well known in the art to increase transistor performance by, among other features, reducing the capacitance that develops in a junction capacitance layer between impurity layers (e.g, impurity doped source and drain regions of a planar MOS structure) and a substrate. For example, in an embodiment, substrate 100 comprises silicon. Atop substrate 100 is a buried oxide 101. In an embodiment, the buried oxide comprises silicon dioxide. Atop the buried oxide 101 is silicon 102. Commercially available, the SOI substrates generally include silicon 102 layers that are approximately 500 angstroms thick. An embodiment, to further reduce the junction capacitance area, planarizes and polishes (e.g., by chemical mechanical polishing or CMP) the silicon 102 to approximately between 20 and 100 angstroms. It is to be understood, however, that the SOI combination of substrate 100, buried oxide 101 and silicon 102 may also be prepared by separation by implanted oxygen (SIMOX), bonded and etched back (BESOI) or hydrogen implant before BESOI process (Smart Cut) as is understood in the art.

[0017] Figure 2 illustrates the substrate 100 cross section of Figure 1 including strained silicon germanium 201 and silicon 202 prior to Smart Cut transfer of each to silicon 201 as is well known in the art and has been developed by SOITEC. A particular application of the Smart Cut method involves growing a layer of strained silicon germanium 201 on silicon 202 as a separate substrate that includes a large sacrificial silicon 202 layer as illustrated by Figure 2. A high dose (i.e., 10^{17} /cm^2) of hydrogen is implanted to a depth

either in the silicon 202 adjacent to the strained silicon germanium 201 or to a depth within the silicon germanium layer 201 as illustrated by hydrogen implant 203 (shown deposited within silicon 202). The separate substrate comprised of silicon 202 and strained silicon germanium 201 is brought into contact with the substrate 100 that includes buried oxide 101 and silicon 102. In particular, the surfaces of silicon 102 and strained silicon germanium 201 are joined by chemical hydrophobic bonding after a high temperature anneal. Said differently, the strained silicon germanium 201 bonds by covalent forces to the silicon 102. In an embodiment, the anneal is approximately between 800°C and 900°C for approximately 1 hour. The anneal further produces, based on the high dose hydrogen implant 203 in silicon 202, an in-depth weakened layer of silicon 202. As the bonding forces between the silicon 102 and strained silicon germanium 201 are stronger than what the in-depth hydrogen implant 203 weakened region of silicon 202 can support, the sacrificial portion of silicon 202 (or of silicon germanium 201 and silicon 202 if the hydrogen implant 203 resides in the silicon germanium 201) can be cleaved, leaving behind the structure illustrated by Figure 3. In an embodiment, the remaining silicon 202 (or silicon germanium 201) may be chemically mechanically polished to form a suitable silicon 202 (or silicon germanium 201) surface for subsequent processing steps.

[0018] Silicon and germanium have the same lattice structure; however, the lattice constant of germanium is 4.2% greater than the lattice constant of germanium (the lattice constant of silicon is 5.43 angstroms while the lattice constant of germanium is 5.66 angstroms). A silicon germanium alloy $Si_{1-x}Ge_x$, x = 0.0 to 1.0, has a monotonically increasing lattice constant a x increases from 0.0 to 1.0. Depositing a thin layer of silicon over silicon germanium produces, as the underlying silicon germanium lattice structure coerces the lattice thinly deposited layer of silicon, a silicon layer with tensile strain as the

smaller silicon lattice aligns with the larger silicon germanium lattice. Similarly, a thin silicon germanium layer can be grown with compressive strain on a layer of silicon. However, as the deposited layers of strained materials thicken, they tend to relax to their intrinsic lattice structure.

[0019] Figure 4 illustrates the substrate 100 cross section of Figure 3 following a high temperature, long duration anneal. In an embodiment, the anneal is approximately between 800°C and 1100°C for approximately 1 second to 3 hours. In an anneal of an embodiment, the temperature is approximately 1000°C and the duration is approximately 2 hours. During the high temperature, long duration anneal, the germanium in the strained silicon germanium 201 diffuses into the silicon 102 and silicon 202. As the germanium diffuses to an approximate constant concentration throughout the strained silicon 201, silicon 102, and silicon 202, it forms relaxed silicon germanium 401. No longer compressively strained by adjacent silicon, the lattice constant of the relaxed silicon germanium 401 increases based on the germanium concentration in the relaxed silicon germanium 401. In an embodiment, the relaxed silicon germanium 401 has a germanium concentration range of approximately 5% to 80% (i.e., approximately 5% to 80% of the silicon lattice sites are occupied by germanium). In an embodiment, the relaxed silicon germanium 401 has a germanium concentration approximately 15%. The relaxed silicon germanium 401 may, based on the pre-anneal doping of silicon 102, strained silicon germanium 201, silicon 202, or a combination thereof (or in an embodiment, a separate relaxed silicon germanium 401 doping process) may be p-doped with any p-dopant known in the art. The p-dopant concentration level of a relaxed silicon germanium 401 embodiment may be

approximately between undoped and $6*10^{19}/cm^3$. In an embodiment, the p-type dopant concentration level of relaxed silicon germanium 401 is approximately $10^{17}/cm^3$.

[0020] Figure 5 illustrates a cross section of the substrate 100 of Figure 4 following the lithographic patterning of the relaxed silicon germanium 401 to form a relaxed silicon germanium fin 501. The relaxed silicon germanium fin 501 may be patterned by any method known in the art to pattern silicon germanium. In an embodiment, the relaxed silicon germanium fin is patterned by any dry silicon etch process known in the art. Following the lithographic patterning, relaxed silicon germanium fin 501 of an embodiment has an approximately rectangular cross section as the lithographic patterning is substantially anisotropic and creates substantially vertical relaxed silicon germanium fin 501 sidewalls. In a further embodiment, though not illustrated, the relaxed silicon germanium fin 501 has a substantially trapezoidal cross section, with its top surface spanning a smaller lateral distance than its base adjacent to the buried oxide 101. For both the substantially rectangular and substantially trapezoidal embodiments, the relaxed silicon germanium fin 501 comprises a top and two sidewalls whose width and height dimensions are approximately between 25% and 100% of the transistor gate length, and can have any shape from substantially tall and thin to substantially short and wide. In yet further embodiments, also not illustrated, the relaxed silicon germanium fin 501 has other geometrical cross sections that may include additional sidewalls or may be substantially hemispherical.

[0021] Figure 6 illustrates a cross section of the substrate 100 of Figure 5 following the deposition of strained silicon 601. As noted above, the lattice constant of the relaxed silicon germanium fin 501 is larger than the lattice constant of silicon. When a thin layer

of silicon is formed atop the relaxed silicon germanium fin 501, provided the silicon has a sufficiently small thickness, the silicon lattice will align with the relaxed silicon germanium fin 501 lattice to form strained silicon 601. As the relaxed silicon germanium fin 501 lattice constant is larger than that of silicon, the subsequently formed strained silicon 601 exhibits tensile strain as the smaller silicon lattice stretches to conform with the relaxed silicon germanium fin 501 lattice. As noted, the tensile strain increases the carrier mobility in the strained silicon 601 that comprises the channel region of a non-planar MOS transistor of an embodiment.

[0022] Strained silicon 601 can be deposited by any method known in the art to deposit crystalline silicon. In an embodiment, the strained silicon 601 is deposited with selective epitaxy such that the silicon grows only on the surface of the relaxed silicon germanium fin 401 and not on the surface of the buried oxide 101 exposed during the pattering of relaxed silicon germanium fin 501. For example, in an embodiment a low pressure chemical vapor deposition process of an embodiment utilizes silane (SiH_4), disilane (Si_2H_4), dichlorol silane (SiH_2Cl_2), and trichlorol silane ($SiHCl_3$) as a silicon source and HCL as an etching gas for selective growth. In an embodiment, the pressure of the deposition chamber is approximately between 500 millitorr and 500 torr, the temperature of the substrate 100 is approximately between 400°C and 1100°C, and the total precursor gas flow rate is approximately between 10 sccm and 1000 sccm. It is to be understood that the deposition conditions may vary depending on the size of the deposition chamber. It is to be further understood that the epitaxial deposition forms substantially a single crystal stained silicon 601.

[0023] In an embodiment, the strained silicon 601 is doped with a p-type dopant. In an embodiment the p-type dopant concentration level of strained silicon 601 ranges from approximately undoped to $6*10^{19}/cm^3$. It is to be understood that the strained silicon 601 may be doped by any doping method known in the art. In particular, the strained silicon 601 may be doped in situ during its deposition by incorporating dopant precursors in the low pressure chemical deposition process of an embodiment. The strained silicon 601 may alternatively be doped by out diffusion or implant.

[0024] As noted, the cross section of the relaxed silicon germanium fin 501 of an embodiment has a top and two sidewalls. It is important to note that the strained silicon 601 be deposited on the top and on both sidewalls of relaxed silicon germanium fin 501 with substantially uniform thickness for each surface. The strained silicon 601 of an embodiment on the top and sidewalls has a substantially uniform thickness of approximately between 2 nanometers and 10 nanometers In an embodiment, the strained silicon 601 thickness is approximately between 4 and 5 nanometers. In an embodiment, the strained silicon 601 thickness permits deeply depleted or fully depleted channel conditions as is understood in the art.

[0025] Figure 7 illustrates a cross section of the substrate 100 of Figure 6 following the deposition of a gate dielectric 701 and gate 702 to illustrate a non-planar, tri-gate transistor cross section. In an embodiment, gate dielectric 701 comprises silicon dioxide. In a further embodiment, gate dielectric 701 comprises a high dielectric constant material like hafnium oxide, hafnium silicate, lanthanum oxide, lanthanum aluminate, zirconium oxide, zirconium silicate, tantalum oxide, titanium oxide, barium strontium titanate, barium titanate, strontium titanate, yttrium oxide, aluminum oxide, lead scandium tantanate, or

lead zinc niobate. The gate dielectric 701 may be deposited my any method known in the art to deposit a gate dielectric 701 material.

[0026] In an embodiment, the gate dielectric 701 deposition is a blanket deposition. Following the deposition of gate dielectric 701, a gate 702 is deposited. In an embodiment the gate 702 comprises polysilicon, polysilicon with a layer of metal at the high-k gate dielectric 701 interface, or a complete metal gate. In an embodiment, the gate 702 deposition is a blanket deposition. In an embodiment for which the gate dielectric 701 and gate 702 depositions are blanket depositions, each is etched to expose areas of strained silicon 601 that will thereafter form the source and drain of the tri-gate non-planar transistor of an embodiment. Of note is that the gate 702 and underlying gate dielectric 701 of an embodiment extend over all sides (in an embodiment, the top and both sidewalls) of the relaxed silicon germanium fin 501 including strained silicon 601 formed thereon.

[0027] In an alternate embodiment (not illustrated), the gate 702 is only adjacent to the sidewalls of the relaxed silicon germanium fin 501 and does not extend across the top of the relaxed silicon germanium fin 501. The strained silicon 601 may be formed over the entire exposed surface (i.e., top and both sidewalls) of the relaxed silicon germanium fin 501 or may just be formed on the two sidewalls of the silicon germanium fin 501. Similarly, the gate dielectric 701 may be formed over the entire exposed surface (i.e., top and both sidewalls) of the strained silicon 601 formed atop the relaxed silicon germanium fin 501 or may just be formed on the two sidewalls of strained silicon 601. With such an arrangement, the non-planar transistor of an embodiment resembles a FinFET including strained silicon 601 channel regions.

[0028] Figure 8 is an illustration of a perspective view of the substrate 100 of Figure 7 including buried oxide 101, relaxed silicon germanium fin 501, strained silicon 601, gate dielectric 701 and gate 702. In an embodiment, the blanket deposition of gate dielectric 701 and gate 702 have been etched to expose the relaxed silicon germanium fin 501 as described above. It is to be understood that one relaxed silicon germanium fin 501 can operate for many gates 702 and one gate 702 may operate with many relaxed silicon germanium fins 501 to create an array of non-planar, tri-gate MOS transistors.

[0029] Figure 9 is an illustration of the perspective view of Figure 8 including an implant 901 to form a source 902 and a drain 903. Well known in the art to form a source and drain for a MOS transistor, the implant 901 (e.g., an n-type dopant implant for an NMOS device) further decreases the contact resistivity between both the source 902 and drain 903 with subsequently fabricated metal contacts to improve the performance of the non-planar, tri-gate MOS transistor of an embodiment.

[0030] The resulting structure of an embodiment is a non-planar, tri-gate MOS transistor that includes a strained silicon 601 channel. As noted, the tensile strain on the strained silicon 601 lattice increases the electron and hole mobility within the strained silicon 601 lattice to fabricate an NMOS device with improved performance characteristics. Further, in an embodiment, the strained silicon 601 thickness permits deeply depleted or fully depleted conditions to mitigate leakage current while the NMOS device is in an off state (i.e., enhancement mode with zero gate voltage).

[0031] One skilled in the art will recognize the elegance of an embodiment as it combines a non-planar MOS transistor structure with a strained channel material to improve transistor performance.

What is claimed is:

1. A non-planar transistor comprising:

a silicon germanium body formed on a substrate and electrically isolated from the substrate;

a strained silicon formed on the silicon germanium body;

a gate dielectric formed on the strained silicon;

a gate formed on the gate dielectric; and

a source and a drain formed in the strained silicon.

2. The non-planar transistor of claim 1, the silicon germanium body comprising a germanium concentration of approximately between 5% and 80%.

3. The non-planar transistor of claim 2, the silicon germanium body comprising a germanium concentration of approximately 15%.

4. The non-planar transistor of claim 1, the gate dielectric comprising a material selected from the group consisting of silicon dioxide, hafnium oxide, hafnium silicate, lanthanum oxide, lanthanum aluminate, zirconium oxide, zirconium silicate, tantalum oxide, titanium oxide, barium strontium titanate, barium titanate, strontium titanate, yttrium oxide, aluminum oxide, lead scandium tantanate, and lead zinc niobate.

5. The non-planar transistor of claim 1, the gate comprising a material selected from the group consisting of polysilicon, metal, and a combination thereof.

6. The non-planar transistor of claim 1 wherein the silicon germanium body has a substantially rectangular cross section and the strained silicon is formed on a top and both sidewalls of the silicon germanium body.

7. The non-planar transistor of claim 1 wherein the silicon germanium body has a substantially trapezoidal cross section and the strained silicon is formed on a top and both sidewalls of the silicon germanium body.

8. The non-planar transistor of claim 1 wherein the strained silicon has a thickness of approximately between 2 nanometers and 10 nanometers.

9. The non-planar transistor of claim 8 wherein the strained silicon has a thickness of approximately between 4 nanometers and 5 nanometers.

10. A tri-gate transistor comprising:

a silicon germanium fin formed on an insulator, the silicon germanium fin including a top surface and two sidewall surfaces;

a strained silicon film formed on the top surface and two sidewall surfaces of the silicon germanium fin;

a gate dielectric formed on the strained silicon film;

a gate formed on the gate dielectric wherein the gate extends over the top surface of the silicon germanium fin; and

a source and a drain formed in the strained silicon film.

11. The tri-gate transistor of claim 10, the silicon germanium fin comprising a germanium concentration of approximately between 5% and 80%.

12. The tri-gate transistor of claim 11, the silicon germanium fin comprising a germanium concentration of approximately 15%.

13. The tri-gate transistor of claim 10 wherein the strained silicon film has a thickness of approximately between 2 nanometers and 10 nanometers.

14. The tri-gate transistor of claim 13 wherein the strained silicon film has a thickness of approximately between 4 nanometers and 5 nanometers.

15. A method comprising:

forming silicon germanium on a silicon on insulator substrate;

annealing the silicon germanium to relax the silicon germanium;

forming a fin in the relaxed silicon germanium, the fin including a top surface and two sidewall surfaces; and

forming strained silicon on the top surface and two sidewall surfaces of the fin.

16. The method of claim 15, annealing the silicon germanium further comprising diffusing germanium into the silicon of the silicon on insulator substrate.

17. The method of claim 16 further comprising:

forming a gate dielectric on the strained silicon film, the gate dielectric material selected from the group consisting of silicon dioxide, hafnium oxide, hafnium

silicate, lanthanum oxide, lanthanum aluminate, zirconium oxide, zirconium silicate, tantalum oxide, titanium oxide, barium strontium titanate, barium titanate, strontium titanate, yttrium oxide, aluminum oxide, lead scandium tantanate, and lead zinc niobate.

18. The method of claim 17 further comprising:

forming a gate on the gate dielectric, the gate material selected from the group consisting of polysilicon, metal, and a combination thereof.

19. The method of claim 18 further comprising:

doping the strained silicon to form a source and a drain.

20. An apparatus comprising:

a tri-gate transistor including a strained silicon channel region.

21. The apparatus of claim 20 wherein the strained silicon channel region has a thickness of approximately between 2 nanometers and 10 nanometers.

22. The apparatus of claim 21 wherein the strained silicon channel region has a thickness of approximately between 4 nanometers and 5 nanometers.

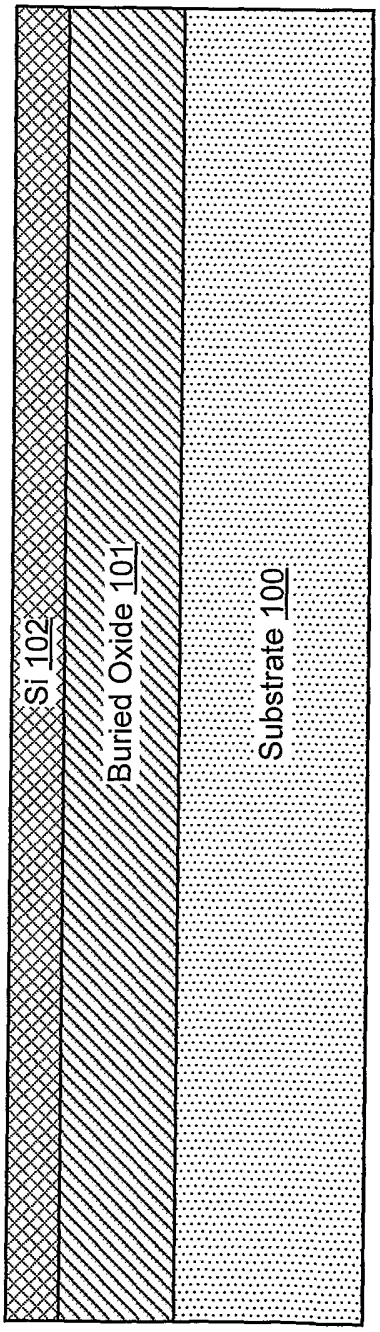
Si 102
Buried Oxide 101
Substrate 100

FIG. 1

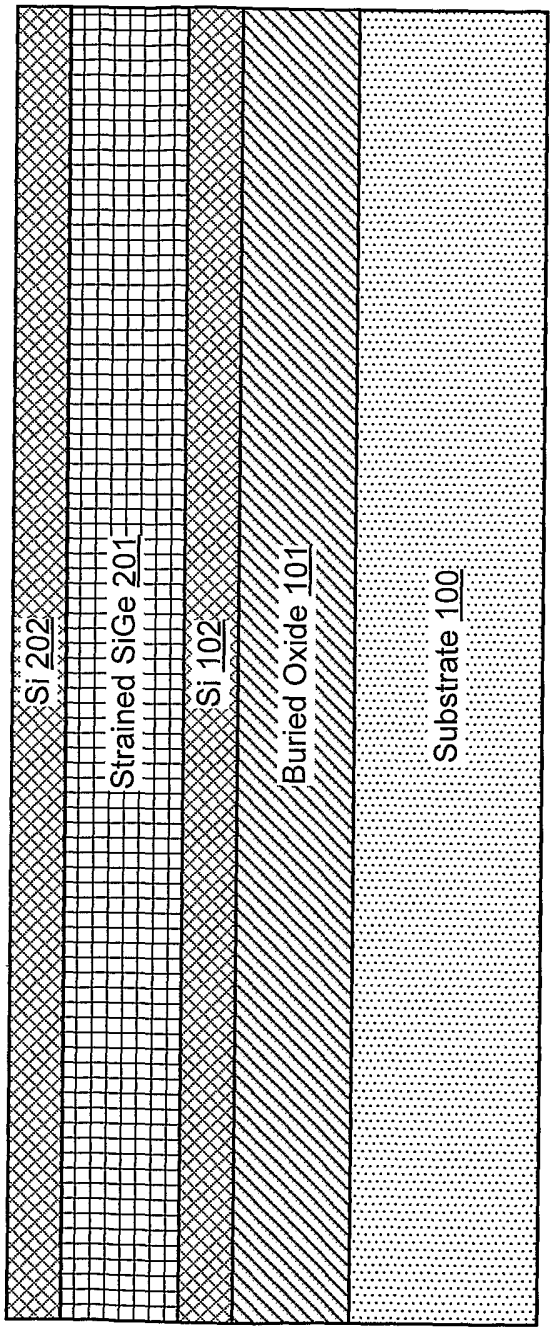
Si 202
Strained SiGe 201
Si 102
Buried Oxide 101
Substrate 100

FIG. 3

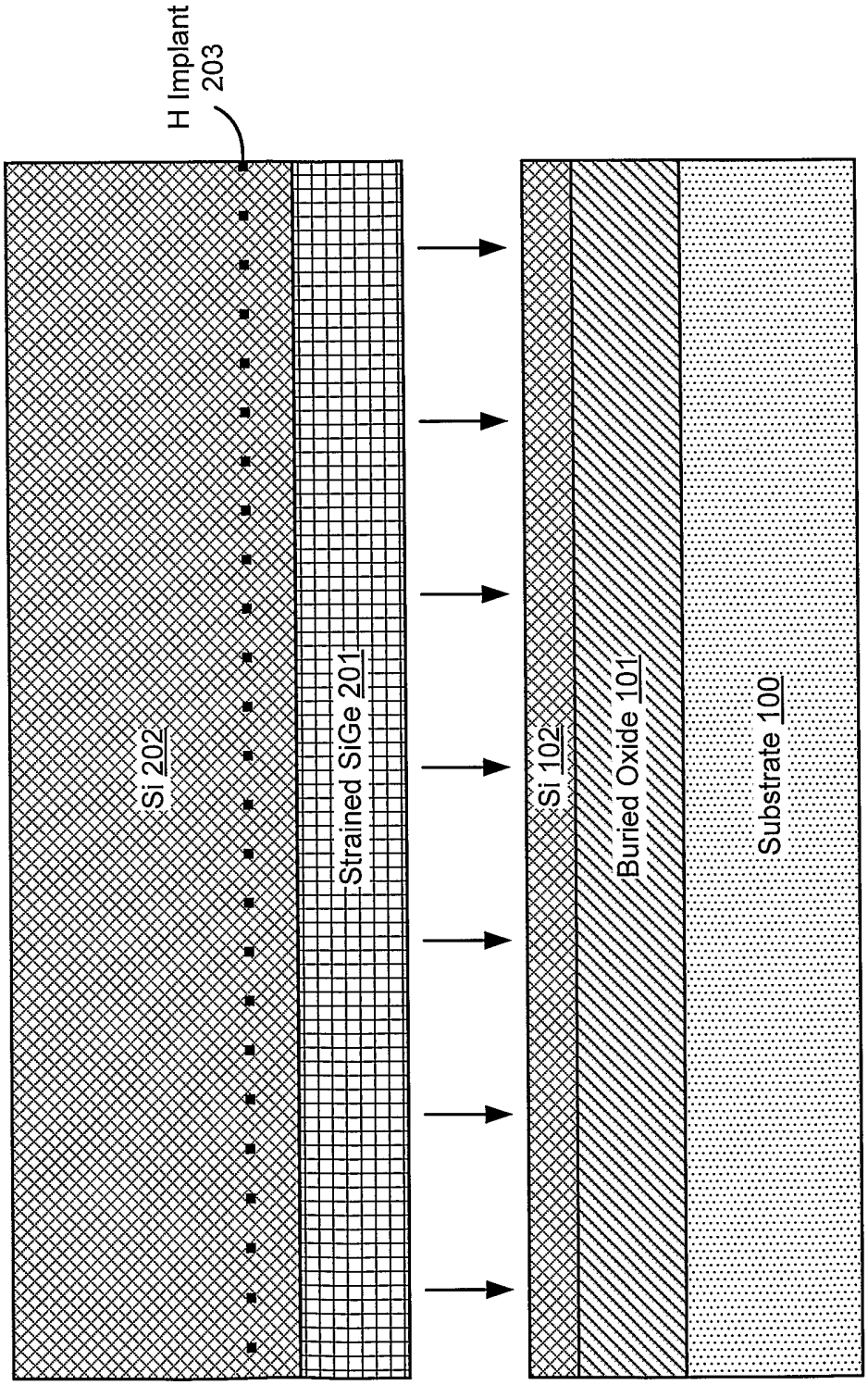
H Implant
203
Si 202
Strained SiGe 201
Si 102
Buried Oxide 101
Substrate 100

FIG. 2

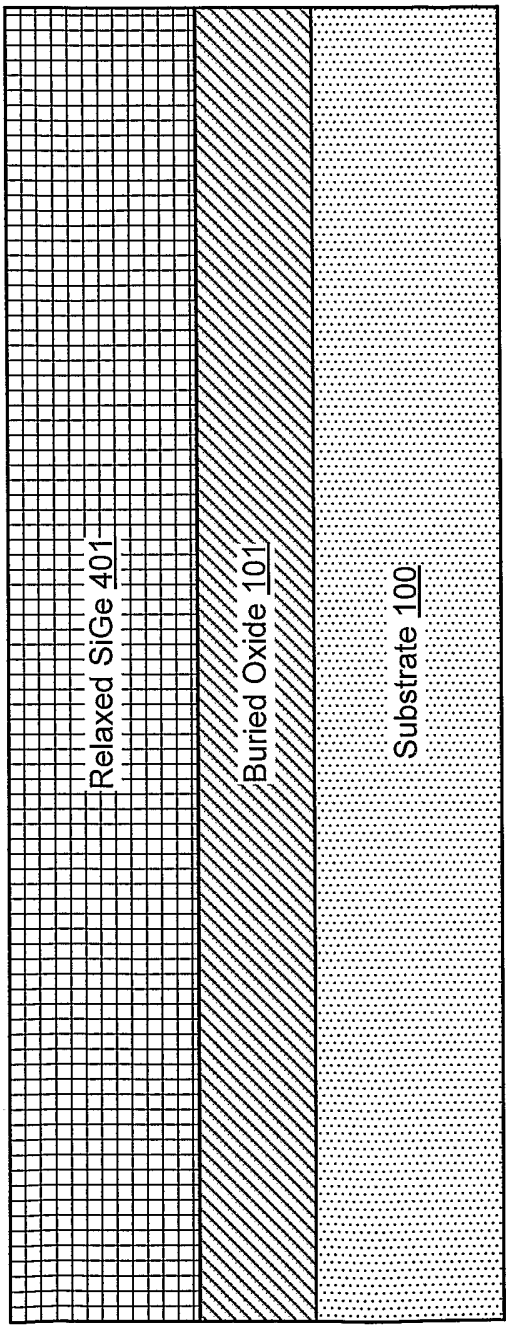
Relaxed SiGe 401
Buried Oxide 101
Substrate 100

FIG. 4

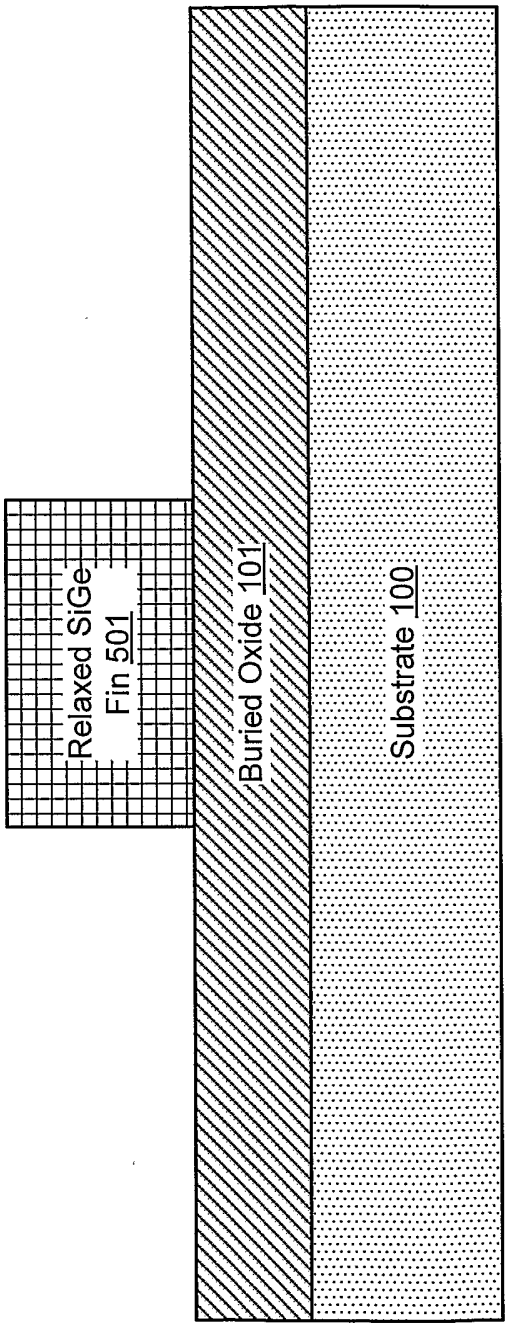
Relaxed SiGe Fin 501
Buried Oxide 101
Substrate 100

FIG. 5

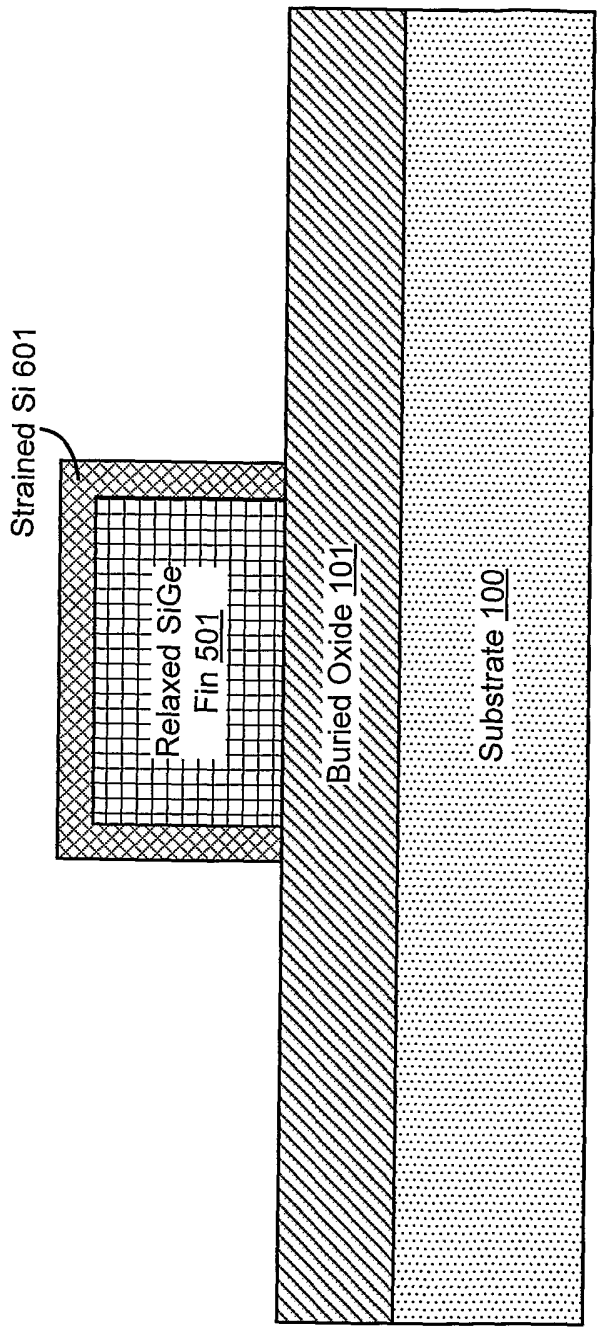
Strained Si 601
Relaxed SiGe Fin 501
Buried Oxide 101
Substrate 100

FIG. 6

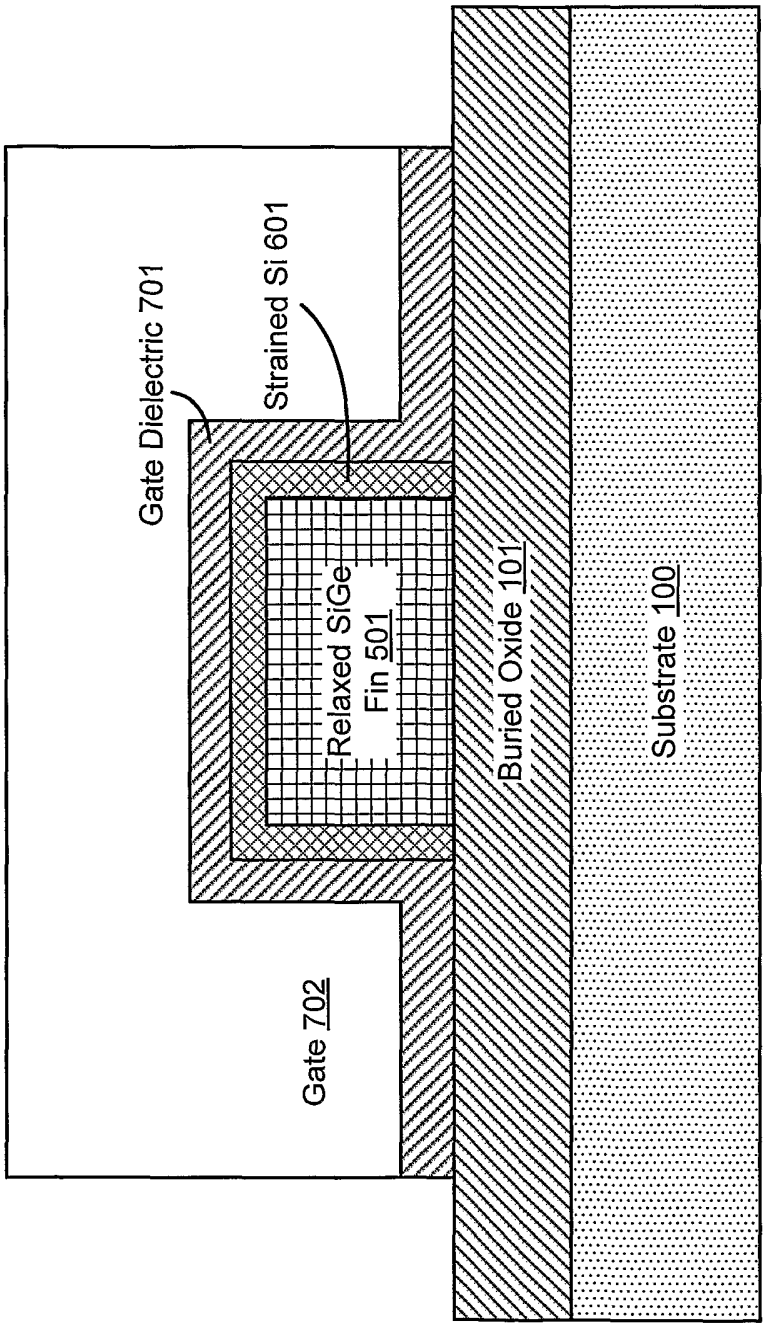
Gate Dielectric 701
Strained Si 601
Relaxed SiGe
Fin 501
Buried Oxide 101
Substrate 100
Gate 702

FIG. 7

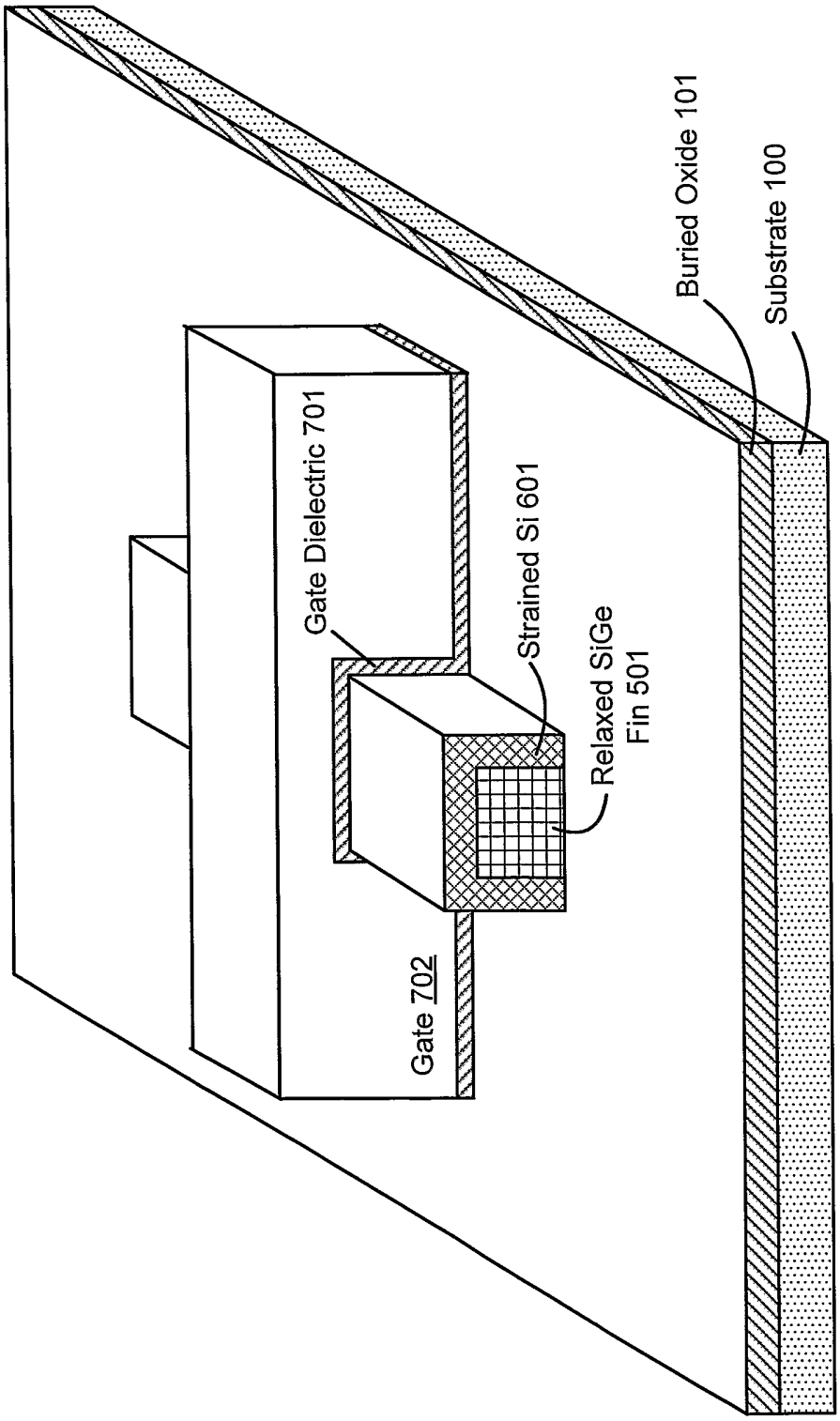
Buried Oxide 101
Substrate 100
Gate Dielectric 701
Strained Si 601
Relaxed SiGe
Fin 501
Gate 702

FIG. 8

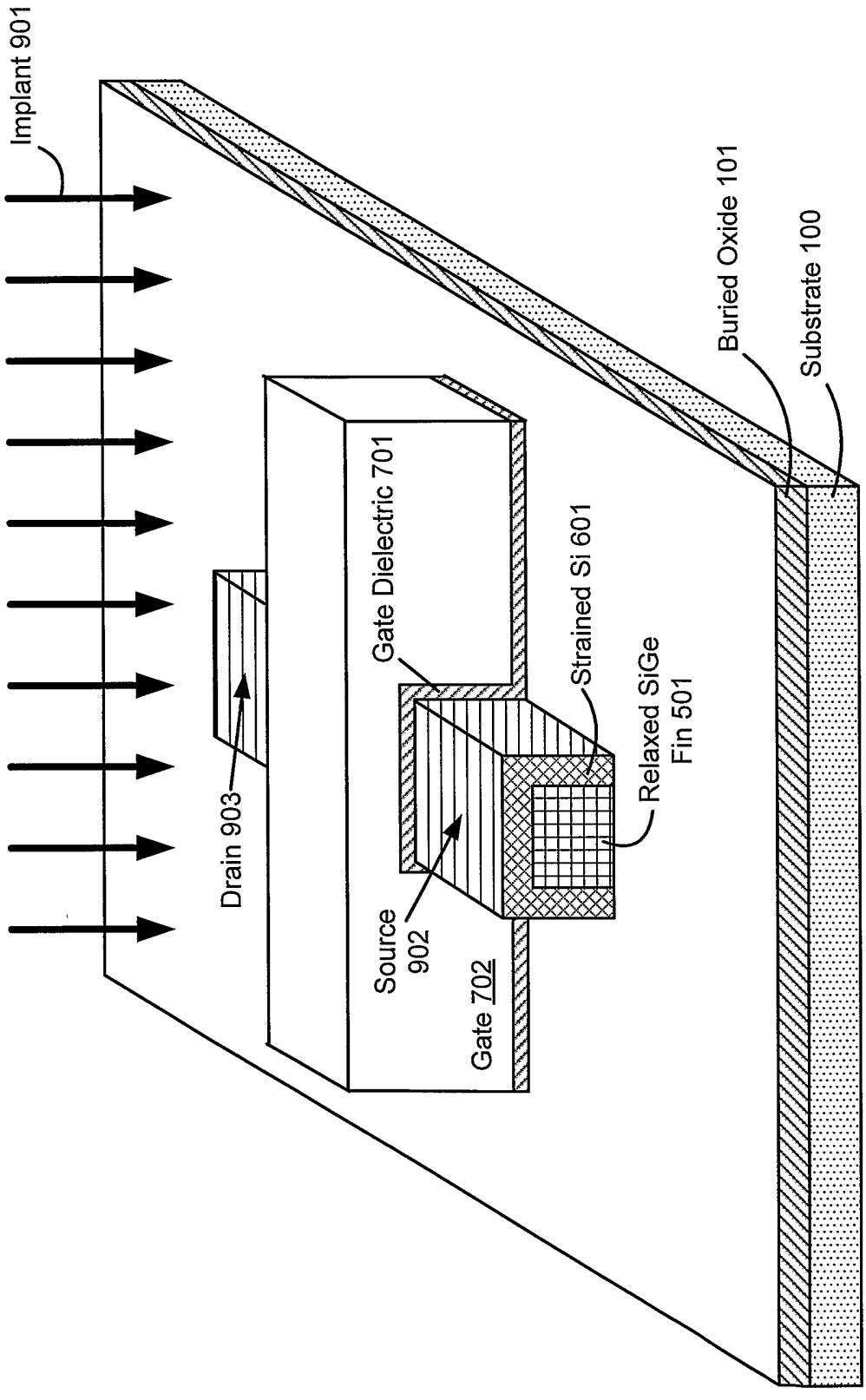
Implant 901
Buried Oxide 101
Substrate 100
Gate Dielectric 701
Strained Si 601
Relaxed SiGe Fin 501
Drain 903
Source 902
Gate 702

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/000378

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/786 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/227036 A1 (SUGIYAMA NAOHARU ET AL) 11 December 2003 (2003-12-11) the whole document	1-22
X	US 2004/145019 A1 (DAKSHINA-MURTHY SRIKANTESWARA ET AL) 29 July 2004 (2004-07-29) paragraph [0022] - paragraph [0028]; figures 4A,4B	1-14, 20-22
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2006/000378

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