

United States Patent

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**[54] METHOD AND APPARATUS FOR SUB-PERIOD
MEASUREMENT OF SUCCESSIVE VARIABLE
TIME PERIODS
15 Claims, 4 Drawing Figs.**

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G04f 9/00,
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324/68, 70;
328/129, 130, 138, 165; 235/92 T; 307/232, 234

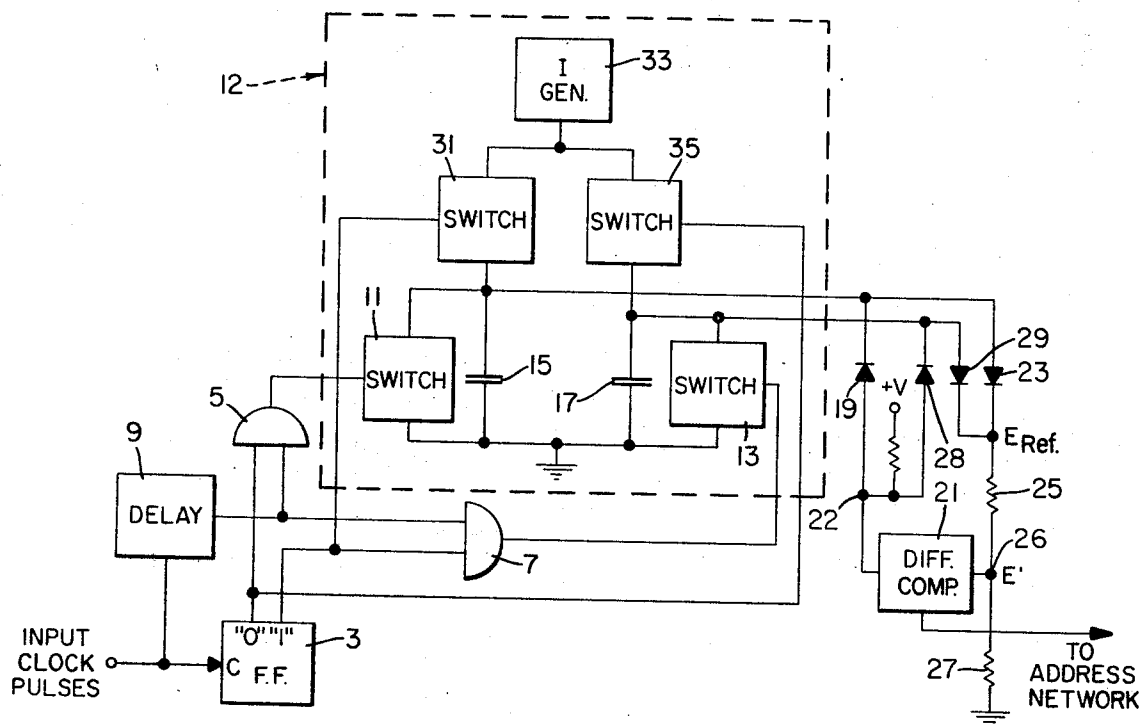
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ABSTRACT: Self-clocking method and apparatus for continuously detecting desired subperiods of time periods between successive pulses where the time periods may vary. The successive pulses indicate the start and stop of each time period. A switching network responds to the start-stop indications to generate a responsive signal, e.g. a ramp function signal. The characteristics of the ramp are dependent upon the start and stop indications. A comparator network compares the magnitude of the responsive signal to a reference signal stored from the preceding period.

The invention herein described was made in the course of performance of a contract with the Department of the United States Army.



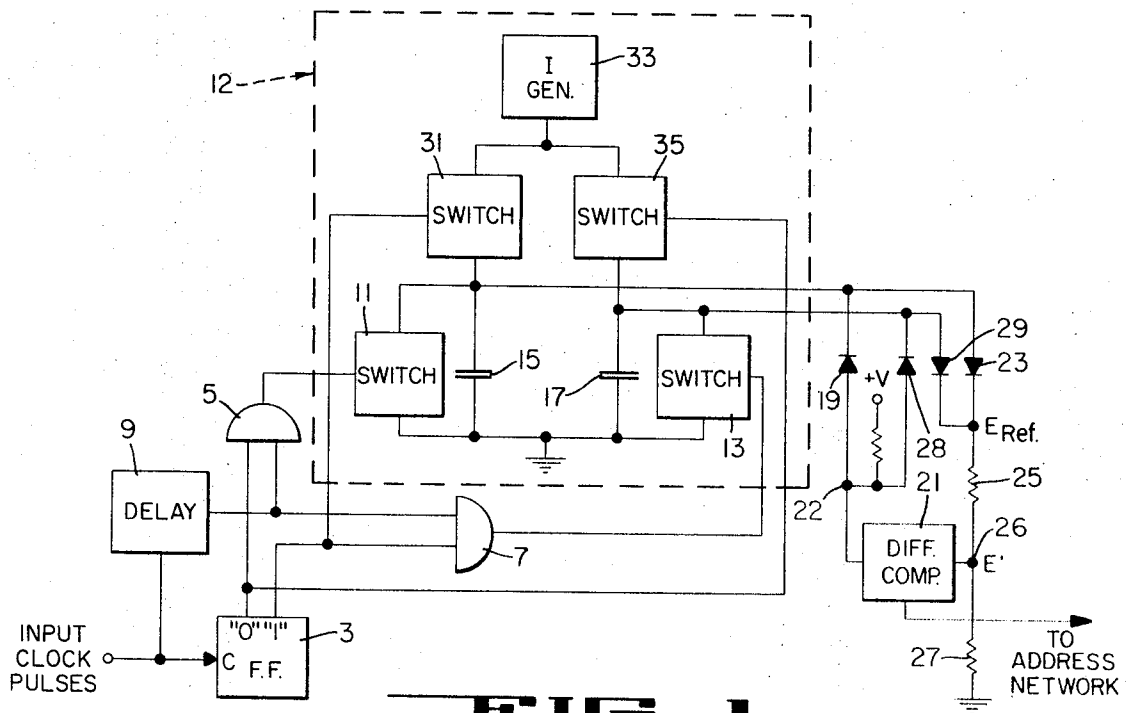


FIG. 1

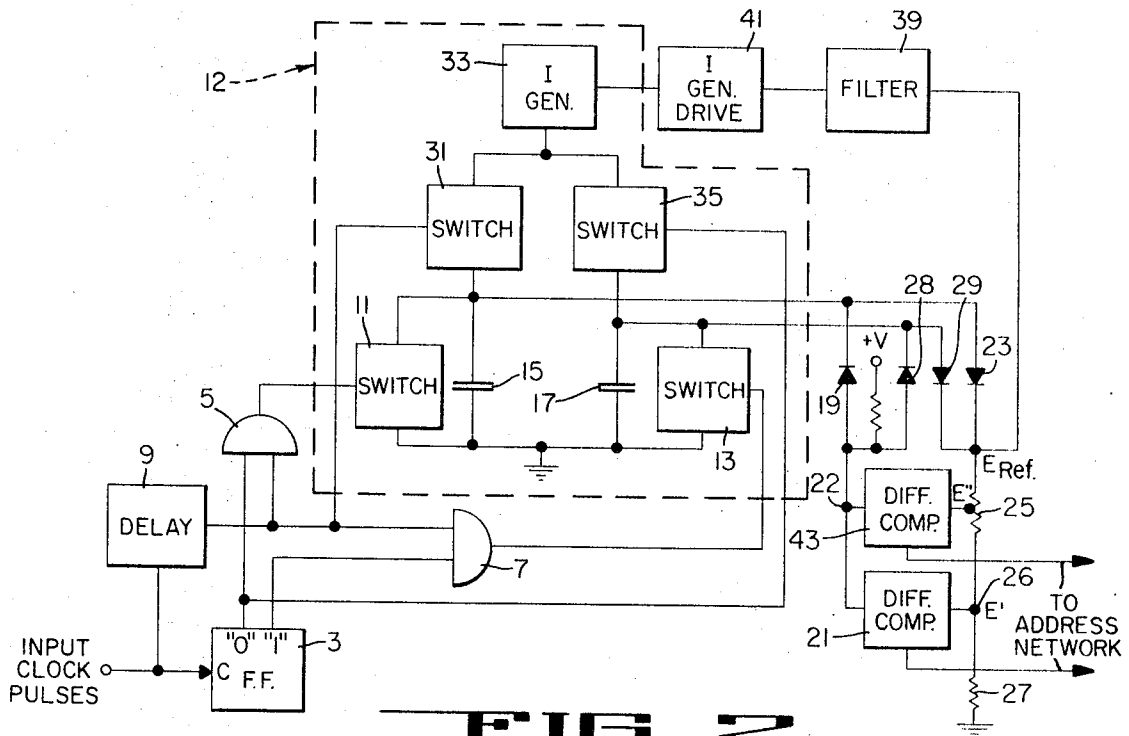


FIG. 2

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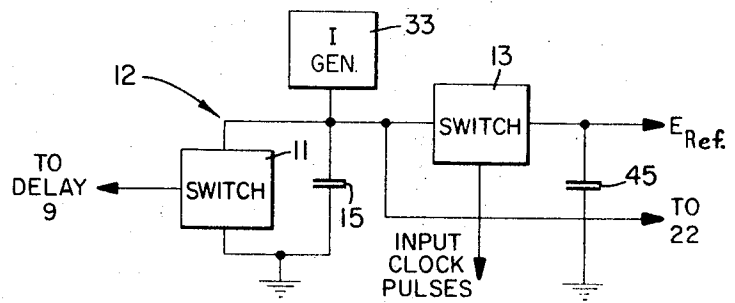


FIG. 3

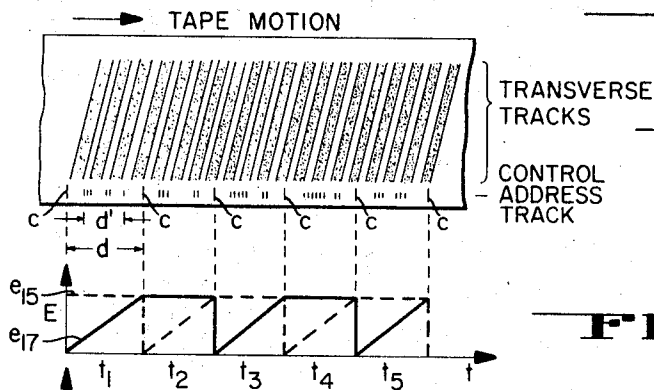


FIG. 4

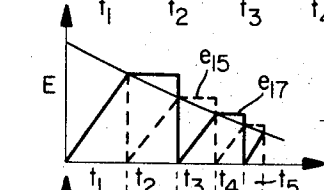


FIG. 5A

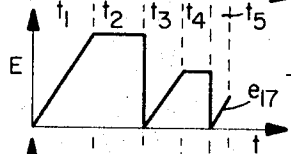


FIG. 5B

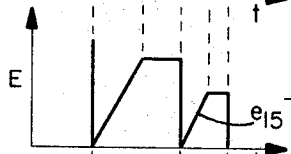


FIG. 5C

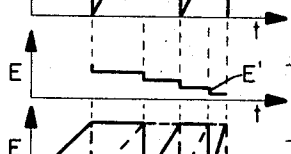


FIG. 5D

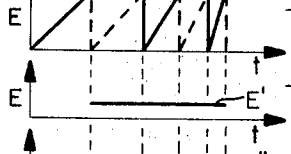


FIG. 5E

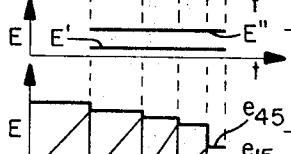


FIG. 5F

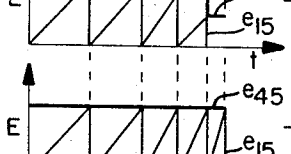


FIG. 5G

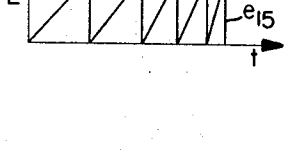


FIG. 5H



FIG. 5I



FIG. 5J

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METHOD AND APPARATUS FOR SUB-PERIOD MEASUREMENT OF SUCCESSIVE VARIABLE TIME PERIODS

BACKGROUND OF THE INVENTION

The present invention relates to the detection of a desired percentage of a time period where the time period may vary over a large range of values. Though there will be various recognized applications, the invention provides a highly satisfactory solution to a problem encountered in magnetic tape information storage and retrieval systems storing large volumes of information. In such systems it is desirable to have selective rapid access to all segments of the tape for retrieval, modification or erasure of the information recorded at a select segment of block. For example, in magnetic tape document storage and retrieval systems numerous documents are recorded on the tape. It may be desired after reading or recording a document of one segment of the tape, to read or record another document on another segment of the same tape displaced several hundred feet from the first document. Also, as certain documents become obsolete, it is desirable to erase that recorded document and replace it with another. In such systems during the record or reading mode tape speed is relatively slow, e.g. 5 inches per second (ips), and during the search mode of transporting between remote locations, the tape velocity is relatively high, e.g. 500—1000 ips. It is essential that the transport continuously identify the tape location so that during search the transport speed be reduced when the select segment or document is neared and/or reached. Also, during record or playback of the select block or document there need be control over actual speed for minimizing the effects of time base errors.

Identification of the actual longitudinal position of the tape and the tape itself are realized through use of a tape addressing subsystem. Unique address pulses are recorded for each block of intelligence to identify its actual location on the tape. Also, one approach to tape speed control is to record on a longitudinal track of the tape a clock reference pulse train or evenly spaced pulses. Then in the playback and record modes the velocity is determined by sensing these pulses. The physical distance between reference clock pulses being substantially constant, the time period between successive pulses is a function of tape speed with the timer period substantially less in the high speed search mode than in the record or playback modes. Generally, the control track and address track signals are recorded prior to the recording of any documents or intelligence and then as the documents are recorded each is referenced to the unique block or blocks.

In recording the address pulses, they may be referenced to the clock pulses on the control track such that during a sub-clock period the address information appears identifying the block. For example, the address code may be recorded on the middle X percent of successive clock pulses. Therefore, during the middle X percent of the time period the address information identifying the block is available. The clock and address data may be recorded on separate longitudinal tracks or possibly the same track with the address data intermediate successive clock pulses. Obviously, it further becomes necessary to differentiate between the clock reference and address data. Thus, the tape velocity is sensed by the clock reference pulse and the position by unique address pulses identifiable with individual blocks. During the search mode with the desired block remote, tape speed may be maximum and as the select block or document is neared tape speed decreased. When the select block is reached, the transport may be at stop or operating at the record or playback speed.

An object of the present invention is to teach a self-clocking method and apparatus for monitoring, tracking and detecting reference clock and subclock periods notwithstanding wide variations in the block periods.

SUMMARY OF THE PRESENT INVENTION

The method and apparatus of monitoring, tracking and detecting reference clock and subclock periods of the present invention utilizes features of electrical excitation, storage and feedback. The change in clock periods may be viewed as a continuous function. A switching network extending to an electrical charge storage means responds to the start and stop pulses of each clock period to control excitation to the charge storage means. The charge storage means may be such that part of it holds a charge while another part is being charged. Detecting means, such as voltage comparators, respond to the charge level on the holding and charging parts. The subperiod of the clock period is selected by detecting the actual charge on the charging part relative to the reference level set by the charge on the holding part. The time for said charging part to reach the reference level establishes the subperiod. As the time period between successive pulses varies there are corresponding variations in the charging time of the charging means. Thus, the detecting means compares a relatively constant percentage of the time duration between successive switching signals notwithstanding variations in successive time durations. As used in magnetic tape recording and retrieval, the address data, which may be recorded within a select percentage of the clock period of successive control track pulses, may be interrogated and extracted by an address reading means operational during the subperiod.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a generalized block diagram of a circuit in accordance with the present invention;

FIG. 2 is a further embodiment incorporating the teachings of the present invention;

FIG. 3 is an alternate embodiment of the ramp generator network of FIGS. 1 and 2;

FIG. 4 is a generalized diagram of a segment of a recorded magnetic tape and illustrating the recording of intelligence clock reference and address information in accordance with the principles of rotary-head magnetic tape recorders; and

FIGS. 5A—5J graphically illustrate the electrical charge of the capacitors of the various charging circuits and the detecting voltage levels of the networks of FIGS. 1—3 with and without feedback and with changing time periods.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The generalized circuitry of FIG. 1 illustrates apparatus for practicing a method for generating the interrogating signals of a changing time period and for providing an output signal during a subperiod of each time period. For example, in the magnetic tape recorder art the change in time or clock period between successive recorded clock pulses may be due to tape acceleration and deceleration. The network of FIG. 1 is designed to sense a subperiod of each successive time period notwithstanding changes in the time periods. The network includes a binary counter or a flip-flop circuit 3 receiving input clock pulses, e.g. those originating from the recorded longitudinal clock track of a magnetic tape. The "zero" output terminal of the flip-flop 3 extends to the first AND gate 5 and the "one" output extends to a second AND gate 7. The inputs of the AND gates 5 and 7 are also common to a delay network 9 which receives the input clock pulses. The AND gate 5 is tied to a first shorting switch 11 of a ramp signal generator switch stage referred to by the general reference character 12. The AND gate 7 is common to a second shorting switch 13. Across the first switch 11 is a charging capacitor 15. Across the switch 13 is a charging capacitor 17. The charging capacitor 15 extends through a diode 19 to a differential comparator 21. The cathode of the diode 19 is common to the switch 11 and the capacitor 15 while the anode is common to a first input terminal 22 common to the differential comparator 21 and a bias potential source +V. The switch 11 also extends through a diode 23 and a resistance source 25 to a second input ter-

terminal 26 of the differential comparator 21 and to a reference plane (ground) through a resistance 27. The anode of the diode 23 is common to the switch 11 and the capacitor 15 while the cathode is common to the resistance source 25. The switch 13 extends through a diode 28 to the input terminal 22 of the differential comparator 21 with the anode tied to the comparator and the cathode to the switch. The switch 13 also extends through a diode 29 and the resistance 25 to the reference terminal 26 of the comparator 21. The cathode of the diode 29 is tied to the resistance source 25 and the anode to the switch 13 and the capacitor 17. The cathode of the diodes 23 and 29, regardless of which capacitor 15 or 17 is "holding," serves as a reference level E_{ref} from which the voltage detecting level E' for the comparator 21 is established.

The "one" output terminal of the flip-flop 3 is also common to a third switch 31. The switch 31 is intermediate the first capacitor 15 and a current generator 33. The "zero" output terminal of the flip-flop 3 is common to a fourth switch 35. The switch 35 is intermediate the second capacitor 17 and the current generator 33. Obviously, all switches included herein may be of the electronic type.

The theoretical operation of the network of FIG. 1 is believed to be as follows. Referring to FIGS. 4 and 5A—5E, FIG. 4 depicts a segment of a magnetic tape recorded with a format compatible with rotary head transverse scan recorders. Various transverse tracks are depicted. A longitudinal control-address track is depicted including a train of evenly spaced pulses C with unique address pulses intermediate. The control track pulses are generally incorporated to provide reference signals for servocontrolling the speed of the tape drive system and providing time base stability. The distance d between successive clock pulses C is equal with the time period between the pulses dependent upon tape velocity. As tape velocity varies the time period also varies. The address pulses for unique individual increments of recorded data are referenced to the clock pulses. A predetermined distance d' between control track pulses C is reserved for the address data. Thus, in essence, the control-address track provides information as to tape velocity, tape address clock and tape address. This recorded information is extracted during all tape speeds and all modes of operation. The tape speeds which depend on the operational mode may vary over a large range. For example, in present day digital tape data storage and retrieval systems, the range may vary in the order of 1000 to 1. For rapid access to and retrieval of any select decoded document, the tape is transported at a high rate, e.g. 500—1000 ips, until the select segment is neared. During this mode, commonly referred to as the "search mode," the address track is continuously read to "inform" the transport control subsystem of the actual location. When the select segment is reached the speed is slowed to the read or write speed, e.g. 5 ips. During the read or write mode the address track is read so that the transport control subsystem is informed that the actual tape segment coincides with the selected.

The transport includes a control track head (not shown) positioned to sense the control track signals C. The tape velocity is determined by the rapidity with which the pulses C pass the head. Address read and write heads may also be positioned so as to write or read the address data. Since the address data is referenced to the clock data on the control track and occurs during a subperiod of the clock periods, the address circuitry is referenced to the control track signals. Coding of the address data pulses requires comparison of each data period to the associated clock period. For example, the address data may be in the X middle percent of successive control track signals C. It then becomes necessary to maintain cognizance of the time periods as they change due to the changing tape velocity.

The method of the present invention for generating or interrogating signals at a changing clock rate and as realized from the circuitry of FIG. 1 utilizes alternate charge of the capacitors 15 and 17 through the current source 33 to form a ramp function signal to the differential comparator 21. The final

level of the ramp voltage produced across each capacitor is determined by the time period between successive input clock pulses to the flip-flop 3. Viewing FIG. 5A there is illustrated the charge potential e_{15} and e_{17} across the capacitors 15 and 17, respectively, at constant tape speed. The charge rate of the capacitors remains the same while the charge period is dependent upon the time period between successive clock pulses C. Since the tape speed is constant, the time periods are equal. The switching arrangement is such that the ramp voltage level is held across one of the capacitors while the other is charging. While the capacitor 17 is charging, the capacitor 15 is holding. When a clock pulse is sensed the holding capacitor is discharged and commences charging while the other holds. The capacitors maintain this status until the next clock pulse. The potential on the holding capacitor serves as a reference E_{ref} for the voltage comparator 21 and the ramp function potential across the other capacitor is supplied to the terminal 22 common to the input of the comparator 21. The voltage divider network of the resistors 25 and 27 divide E_{ref} so that it may be used as the desired detecting level E' . The output of the comparator 21, which determines the state of the interrogate pulses controlling the address circuitry network (not shown) thus commences when the ramp signal equals and exceeds E' . The comparator output stops when the next clock pulse from the tape is detected coinciding with discharge of the holding capacitor and removal of ramp signal to the terminal 22. The cycle is then repeated with the capacitors switching their respective operational functions.

The change in clock period may be viewed as a continuous function. For example, the change in clock periods between pulses C of the tape segment of FIG. 4 results during tape acceleration or deceleration. FIG. 5B represents the charge potential e_{15} and e_{17} of the capacitors 15 and 17 graphically superimposed while FIGS. 5C and 5D represent the charges individually for the network of FIG. 1 during changing time periods. The curve of FIG. 5E illustrates the response detecting level E' which is reduced from E_{ref} due to the voltage dividing action of the resistors 25 and 27. In analyzing the graphs, assume the capacitor 17 is charging when the next input clock pulse is received. The flip-flop 3 opens the switch 35 to terminate further charging of the capacitor 17. The capacitor 17 holds its charge. The gate 5 momentarily closes the shunting switch 11 to discharge the capacitor 15 which was previously in the "hold" state. The capacitor 15 then commences charging through switch 31 which closed when the switch 35 opened. The condition is now a "hold" voltage on the capacitor 17 and an increasing voltage on the capacitor 15. The potential on the diode 29 is now higher than that on the diode 23. Voltage reference E_{ref} is thus derived from the capacitor 17 through the diode 29. The resistors 25 and 27 determine the percent of decrease of the potential E_{ref} to set the detecting level E' at the terminal 26. The +V potential determines which diode 19 or 28 conducts by selecting the one with the lowest potential on the cathode. In this case it is the diode 19. As the charge on the capacitor 15 increases, an output indication from the comparator 21 is generated dependent on the potential e_{15} and E' relationship. The differential comparator 21 generates an output until the next clock pulse.

FIG. 2 is a generalized modified circuit network of FIG. 1 providing a plurality of output signals indicative of a percent of a time period. It further includes a feedback network from the reference potential E_{ref} to the current generator 33. The resistance 25, which is at the capacitor charge value, is tied through a filter network 39 and a current generator drive 41 to the current generator 33. The filter network 39 is included to remove undesired frequency components, for example, those due to the switching action of the capacitors 15 and 17. The feedback network provides for maintaining the maximum charge across the capacitors 15 and 17 constant notwithstanding changes in charge time. The charging current from the current generator 33 is controlled with respect to the charge voltage E_{ref} . Whereas without feedback the charging current rate was constant and amplitude varied, with feedback the

rate changes and the amplitude varied, with feedback the rate changes and the amplitude constant. Thus, if the voltage E_{ref} tends to decrease, the charging current is increased and vice versa to maintain a constant E_{ref} .

FIG. 5F illustrates the "charge" of the capacitors 15 and 17 with the feedback network. It may be noted that during the "charge" cycle the rate of charge changes with corresponding changes in the time period. FIG. 5G illustrates the detecting level potential E' which is a substantially constant value.

FIG. 2 further illustrates the inclusion of a second differential comparator 43. The comparator 43 is common to the first input terminal 22. The detecting level to the comparator 43 is common to the resistance 25 but at a potential level E'' different from that of the comparator 21. Thus, the comparator 43 provides an output indication at a different percent of the time period (charge on charging capacitor) from that of the comparator 21. The use of multiple outputs at different percents of the time period may be put to use in various ways depending upon the applications. For example, viewing FIG. 4, the address data is within the middle segment between successive pulses C. Thus, it may be desirable to turn the address circuitry "on" when the address data block starts and turn it "off" when the address data stops. In FIG. 2, by knowing that the address data is within the middle X percent of the tape segment between successive pulses, the detecting level potentials E' and E'' may be selected within this percentage by proper selection of the resistors 25 and 26 and tapping of the resistor 25 for the differential comparator 43. The output from the comparator 21 may turn the address circuitry "on" and the output from the comparator 41 turn it "off." FIG. 5H illustrates graphically the two detecting levels E' and E'' which may be used to turn "on" and "off" the address circuitry.

Fig. 3 depicts generalized circuitry for another embodiment for a ramp generator switching stage 12. In this embodiment, rather than use four switches, only two are necessary. The switch 13 is placed intermediate the charging capacitor 15 and storage capacitor 45. Thus, when capacitor 15 is charging, the switch 13 is open. Upon completion of the charge of capacitor 15, the switch 13 is closed and the charge transferred to the storage capacitor 45. The switch 13 is then opened and the capacitor 45 provides the reference level E_{ref} . The charging capacitor 15 is discharged by closing the shorting switch 11 responsive to a sigma; from the delay 9. The capacitor 15 is again charged during the next period. The idealized charging waveforms of the capacitors 14 and 45 are depicted in FIG. 5I. The network of FIG. 3 can also be used with feedback as in FIG. 2 in which case the waveforms take the form of FIG. 5J.

I claim:

1. A method for detecting a percentage portion of each of successive time periods whose durations may vary comprising the steps of:

- detecting the duration of each of the successive time periods;
- resolving from the duration of each detected time period the beginning and ending times of the percentage portion of the detected time period; and
- examining each of the succeeding ones of the successive time periods to provide indications at times thereof corresponding to the beginning and ending times of the percentage portion resolved from the immediately previous detected time period.

2. A self-clocking network for detecting a subperiod of each period of successive time periods whose durations may vary over a wide range comprising:

- timing means responsive to the start and stop of each one of the successive time periods to generate a discrete signal representative of the duration of each one of the successive time periods;
- storage means for storing the discrete duration representative signal generated during each time period while the timing means is generating another discrete signal representative of the duration of the immediately successive time period;

means responsive to the discrete signal stored during each time period to provide a discrete reference signal representative of a particular segment of a selected percentage of the duration represented by the stored signal; and

comparator means for receiving the discrete signal being generated by the timing means and the discrete reference signal to provide a responsive indication when the signal being generated by the timing means represents a time within the particular selected percentage segment of the duration represented by the discrete reference signal.

3. The network according to claim 2 further comprising means responsive to the stored discrete duration representative signal for controlling the timing means to issue duration representative signals whose absolute magnitude stored for initiating the generation of the reference signal is not greater than a predetermined absolute magnitude regardless of changes in the duration of successive time periods.

4. The network according to claim 2 wherein successive pulses indicate the start and stop of the successive time periods, the timing means is a ramp signal generating means for generating successive ramp signals in response to successive pulses, each ramp signal having a final level from which the duration of the time period during which the ramp signal was generated can be determined, the storage means stores a discrete signal representative of the final level of the ramp signal generated during each time period, and the discrete reference signal provided by the reference signal generating means represents a particular level segment of a selected percentage of the final level of the generated ramp signal.

5. The network according to claim 4 wherein the discrete reference signal provided by the reference signal generating means represents a particular level less than the final level of the ramp signal, and the comparator means provides the responsive indication when the ramp signal being generated by the timing means reaches a level corresponding to the particular level represented by the discrete reference signal.

6. The network according to claim 4 further comprising means responsive to the stored discrete signal for controlling the ramp signal generating means to change the slope of the ramp signal generated thereby to maintain the final level of each ramp signal constant regardless of changes in the duration between successive pulses.

7. The network according to claim 4 wherein the reference signal generating means provides a discrete reference signal representative of a first particular level and of a second particular greater level of the ramp signal, and the comparator means provides a first indication when the ramp signal being generated by the timing means reaches a level corresponding to the first particular level and a second indication when the ramp signal reaches a level corresponding to the second particular level.

8. The network according to claim 7 further comprising means responsive to the stored discrete signal for controlling the ramp signal generating means to change the slope of the ramp signal generated thereby to maintain the final level of each ramp signal constant regardless of changes in the duration between successive pulses.

9. The network according to claim 2 wherein the timing means includes a switching means and a charging means, the storage means is a charge holding means, the charging means is responsive to the switching means to initiate at the start of each time period charging for the duration of each time period, the charge holding means is responsive to the switching means at the stop of each time period to hold charge indicative of the maximum level of the charge of the charging means during the preceding time period, the held charge representative of the duration of the preceding time period, the reference signal generating means is a voltage divider means providing a voltage reference signal representative of the particular segment of the duration represented by the held charge, and the comparator means provides the responsive indication when the charge of the charging means is within the segment represented by the voltage reference signal.

10. The network according to claim 9 wherein successive pulses indicate the start and stop of the successive time periods, the charging means and charge holding means each includes one of a pair of capacitors each extending to a current generator source through the switching means, the switching means responds to successive pulses to couple the current source to one of the capacitors during alternate time periods and to the other of the capacitors during the remaining time periods whereby each of the capacitors alternately serves as the charging means and as the charge holding means, and further comprising means for coupling the capacitors serving as the charge holding means to the voltage divider means for the duration of the time period said capacitor serves as the charge holding means.

11. The network according to claim 10 further comprising a second switching means extending across each of said capacitors, the second switching means responding to successive pulses and momentarily shorting the capacitor serving as the charge holding means to discharge the held charge prior to charging the capacitor during the succeeding time period.

12. The network according to claim 11 further comprising means responsive to the level of charge held by the charge holding capacitor for controlling the current generator source to change the level of held charge provided during each time period constant regardless of changes in the duration between successive pulses.

13. The network according to claim 9 wherein the voltage

divider means provides a first voltage representative of a first particular level of charge and a second voltage representative of a particular second greater level of charge, and the comparator means includes a pair of comparators, each of the comparators referenced to the charge on the charging means, and one of the comparators coupled to receive the first voltage and the other of the comparators coupled to receive the second voltage provided by the voltage divider means whereby the one comparator provides a first indication when the level of the charge on the charging means reaches that corresponding to the first voltage and the other comparator means provides a second indication when the level of the charge on the charging means reaches that corresponding to the second voltage.

14. The network according to claim 13 further comprising means responsive to the level of charge held by the charge holding means for controlling the rate of charge of the charging means to maintain the level of held charge provided during each time period constant regardless of changes in the duration of successive time periods.

15. The network according to claim 14 further comprising a second switching means responsive to the start of each successive time period to discharge the charge holding means prior to initiating the charge of the charging means during the succeeding time period.

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