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(54) Title: SELECTOR WITH POROUS OXIDE LAYER

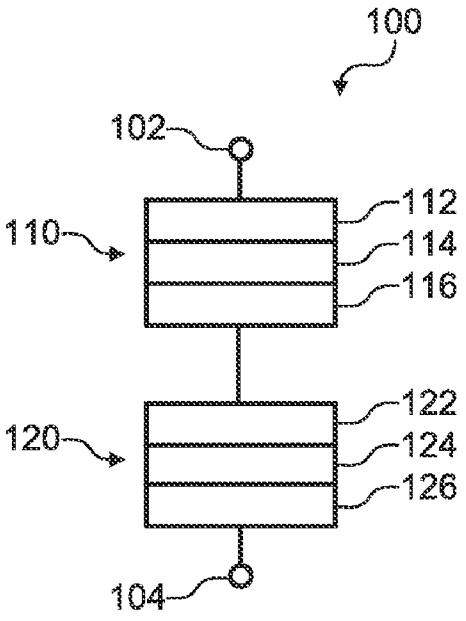


FIG. 1A

(57) Abstract: In one example, a selector device includes a first electrode, a second electrode, and a porous oxide layer. The first electrode may include cation metal. The porous oxide layer may be disposed between the first and second electrodes. The porous oxide layer may include a framework supporting a porous structure. The cation metal from the first electrode may drift into the porous structure of the porous oxide layer upon application of a threshold voltage across the first and second electrodes so as to provide a conductive path through the porous oxide layer.

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SELECTOR WITH POROUS OXIDE LAYER

Background

[0001] Memory devices are used to store data. A memory device may be made up of multiple memory cells. In some cases, a memory cell may be a semiconductor device that can have two different states. The two different states can be associated with a respective binary logic value, such as 0 or 1. Data may be stored to a memory cell by assigning a logic value to that memory cell, and manipulating the memory cell to cause it to take the associated state. Further, the logic value of the memory cell may be queried by determining its state. Data assignment and query operations may be referred to as write and read operations, respectively. A group of memory cells can be used to store a binary dataset by assigning a respective logic value to each cell in the group such that each cell stores a bit of the dataset.

[0002] Various technologies have been used in the design and implementation of memory devices. In some cases, a chip includes multiple semiconductor memory cells that are connected to a set of driving and measurement lines that can be used to address individual memory cells or subsets of the memory cells. A control system can then use those lines to perform read and write operations by applying energy to the individual cells via the lines. For example, reading data from a memory cell may involve applying a read voltage to that memory cell while measuring current (or vice versa) to determine the state of the cell. Similarly, writing data to a memory cell may involve applying a write voltage (or current) to that memory cell which sets the memory cell's state.

Brief Description of the Drawings

[0003] The following detailed description references the drawings, wherein:

[0004] FIG. 1A is a block diagram of an example memory cell including a selector in series with a memristor;

[0005] FIG. 1B is a chart of an example current and voltage for an example memory cell;

[0006] FIG. 2 is a block diagram of an example crossbar array having multiple memory cells that each have a selector in series with a memristor;

[0007] FIG. 3A is a flowchart of an example process for writing data to a memory cell;

[0008] FIG. 3B is a flowchart of an example process for reading data from a memory cell;

[0009] FIG. 4A is a diagram of a side cross-sectional view of an example selector in a non-conductive state;

[0010] FIG. 4B is a diagram of a side cross-sectional view of an example selector in a conductive state;

[0011] FIG. 5A is a flowchart of an example process for fabricating a selector; and

[0012] FIG. 5B is a flowchart of an example process for fabricating a selector.

DETAILED DESCRIPTION

[0013] The following description makes reference to the accompanying drawings, in which similar symbols identify similar components, unless context dictates otherwise. The descriptions herein, as well as the drawings, present examples of the subject matter of the present disclosure and are in no way limiting in regard to the subject matter disclosed herein. Throughout the description, the singular forms of "a", "an", and "the" mean "one or more". Thus, various examples in which a component is described in singular form also apply to examples having multiple of those components. Moreover, some aspects of the examples presented herein may be modified, re-arranged, re-ordered substituted, combined, and/or separated in a variety of different configurations without departing from the subject matter of the present disclosure.

[0014] A memory device may include an array of memory cells. A crossbar array of memory cells may include a grid of control lines arranged in rows and columns. Memory cells may be situated at the intersections of the row and column lines such that a given memory cell can be addressed by a combination of the row and column lines. One example of a memory cell that may be used in such a crossbar array is a memristor.

[0015] A memristor is a passive, non-volatile device with an electrical resistance that depends on the history of current conveyed through the memristor. A memristor may be used to store data using its resistance state. For example, a low-resistance state of the memristor may be associated with a first logical value and a high-resistance state of the memristor may be associated with a second logical value. Thus, a memristor may be used to store a bit of data (e.g., a logical 0 or 1). The resistance state may be modified to write data to the memristor by applying sufficient energy to the memristor. For example, applying a voltage pulse may place the memristor in a low-resistance state and applying a voltage pulse of a different polarity, or different value, may place the memristor in a high-resistance state. In some examples, applying a voltage between about 1-2 volts (V) may cause a memristor to switch its resistance state. The energy to change the state of the memristor may also be provided by a current source. To determine the resistance state of a memristor, a read voltage may be applied to the memristor. A current may be collected and used to determine the resistance state of the memristor. In some examples, the determination may involve comparing the measured current to a reference current. For example, if the output current is greater than the reference current, then the memristor may be determined to be in a low resistance state. On the other hand, if the output current is less than the reference current, then the memristor may be determined to be in a high resistance state.

[0016] Memristors may be implemented using a number of different materials and fabrication techniques. As used herein, the term “memristor” may refer to a

passive two-terminal circuit element that changes its electrical resistance under sufficient electrical bias. A memristor may receive a read voltage to generate a current that can be measured to determine the resistance state of the memristor. A memristor may also receive a write voltage that sets the resistance state of the memristor. In one example, a memristor may have two layers: one that includes an electrically insulating material and one that includes an electrically conductive material. As used herein, the terms insulating and conductive are relative terms. That is, they refer to relative extents of electrical conductivity between the two materials. Thus, the two layers of the memristor include one that is more conductive than the other. In operation, a memristor may transition between states of resistivity via drift of ions or vacancies between the two layers. For example, the two layers may be oxide films in which one is more conductive than the other due to oxygen vacancies providing a conductive channel through the depleted layer. Under sufficient bias, oxygen vacancies may form in the non-depleted layer so as to effectively decrease the thickness of the conductive layer relative to the insulating layer. The resistance of the memristor can then be approximated as the tunneling resistance through the non-depleted oxide layer, which decreases with the decreasing thickness of the insulating layer. Other examples of non-volatile, variable-resistance materials that transition between resistance states in response to application of an electrical bias or other transition energy may also be used to implement a memristor.

[0017] In a crossbar array of memristors, the term “target” may refer to a memristor that is to be written to or read from. A target row line and a target column line may be the row and column lines that correspond to the target memristor in a crossbar array. Non-target row lines and non-target column lines may be row lines and column lines that are not the target row or column line. The terms “row lines” and “column lines” may refer to distinct conductive lines, such as conductive traces, wires, etc., that are used to apply voltages to memristors in a crossbar array and/or to measure currents through memristors.

[0018] In some examples, row lines and column lines for non-selected memristors may be held at a fixed voltage, and the row and column lines for the target memristor can be set to apply a voltage across the target memristor. Applying voltage(s) to the target row line and target column line may cause other memristors coupled to the same row/column lines to experience a voltage change. For example, a read voltage V_R may be applied to a target memristor by setting the target row and target column lines to -½ V_R and +½ V_R, respectively, with the remaining lines set to 0. In such an example, the non-target memristors on the same column and row as the target may experience a bias of about half that applied to the target (e.g., about ½ V_R). While the voltage change is generally less than the voltage applied to the target memristor, the voltage across these partially-selected, non-target memristors may induce current that reaches the target column line. Such current paths that do not pass through the target memristor are referred to as sneak currents. Sneak currents may lead to a number of issues such as inaccurate memristor queries due to sneak current contributions from neighboring low resistance state memristors, saturating the current of driving transistors, and increasing power consumption. In some examples, noise from sneak currents may cause inaccurate or ineffective memory reading and writing operations.

[0019] In some examples, a selector may be coupled serially with a memristor. The selector may be a two-terminal highly non-linear circuit element that becomes conductive upon application of a threshold voltage. Below the threshold voltage, current flow through the selector, and the memristor, is minimal. To help mitigate the effect of sneak currents, the selector may have a threshold voltage that is not activated by the voltages applied to non-target memristors on the same row or column as a target memristor. As such, while some sneak current may be inevitable, series-coupled selectors may help mitigate the sneak current from non-target memristors described above. In some systems, a memory device includes a crossbar array of row and column lines arranged in a grid. A selector and a

memristor coupled in series can be situated at intersections of the row and column lines.

[0020] The present disclosure relates to an arrangement for a selector that may be coupled in series with a memristor. The selector may be a metal-insulator-metal semiconductor device. For example, the selector may include conductive top and bottom electrodes that sandwich an insulator layer. The insulator layer may be an oxide film or another material that transitions between a non-conductive state and a conductive state. The insulator layer becomes conductive in response to a threshold voltage being applied across the top and bottom electrodes. When the applied voltage is less than the threshold voltage, the insulator layer does not allow current to flow between the top and bottom electrodes.

[0021] In some examples, one or both of the selector electrodes may include cation metal and/or cation metal oxides that can migrate into the insulator layer. Upon application of sufficient voltage, the cation metal may be driven into the insulator layer and become arranged within the insulator layer so as to create a conductive channel for a current path between the electrodes. The insulator layer may be a porous oxide layer having a lattice structure that supports the porous material. In some examples, the porous oxide may be nano-porous silicon dioxide. The porous structure may allow cation metal and/or cation metal oxide to migrate into the insulator layer. For instance, in comparison with a dense oxide layer, cation metal and/or cation metal oxides may migrate into a porous oxide layer to a greater depth and/or in greater numbers at a given electrical bias. The porous oxide layer may include vacant defect centers distributed throughout its lattice framework, and the defects may help facilitate passage of diffusing and/or drifting cation metal.

[0022] The disclosed selector device may allow for design trade-offs to adjust the threshold voltage. For instance, increasing the thickness of the porous oxide layer may increase the threshold voltage required to transition the selector to a

conductive state. Further, doping the porous oxide with a conductive material may decrease the threshold voltage.

[0023] FIG. 1A is a block diagram of an example memory cell 100 including a selector 110 electrically coupled in series with a memristor 120. In some examples, the memory cell 100 may be coupled between control lines at nodes 102 and 104. For example, the control lines may be lines in a crossbar array that includes many additional memory cells, such as at each intersection of the control lines.

[0024] The selector 110 includes a first electrode 112, a selector layer 114, and a second electrode 116. The memristor 120 includes a first electrode 122, a variable resistance layer 124, and a second electrode 126. In some examples, the first 112, 116 and second electrodes 122, 126 may be referred to as top and bottom electrodes, respectively. The selector 110 may exhibit a non-linear change in its conductivity in response to changing an applied voltage. For instance, the selector layer 114 may be characterized by a high-resistance state (low conductivity state) when the applied voltage is less than a threshold voltage, and a low-resistance state (high conductivity state) when the applied voltage exceeds the threshold voltage.

[0025] The selector layer 114 of the selector 110 may include a porous oxide material that receives drifting cation metal and/or cation metal oxides from one or both electrodes 112, 116 upon application of an electrical bias. When the applied voltage reaches a threshold voltage, the drifting cation metal and/or cation metal oxides may become arranged within the porous oxide selector layer 114 so as to create a conductive channel between the electrodes 112, 116. In some examples, the selector layer 114 may be a layer of nano-porous silicon dioxide or another porous oxide that provides a lattice framework with defect centers distributed throughout the layer. Cation metals may occupy defects within such lattice or otherwise become arranged within the material of the selector layer. In some cases, the selector layer 114 may be an insulating material that is doped with conductive material, for example. At voltages less than the threshold voltage, the

cation metal ions do not create significant conductive channels through the selector layer 114. Although in some examples, some current flow through the selector layer 114 may occur at voltages less than the threshold voltage of the selector 110, such sub-threshold current flow may be due to fewer conductive channels and/or channels with less current-carrying capacity than occurs above the threshold voltage. As a consequence, the selector 110 may be substantially non-conductive (e.g., have a high resistance) for voltages below its threshold voltage and be substantially conductive (e.g., have a low resistance) for voltages above its threshold voltage.

[0026] Electrode 112 and/or electrode 116 may include cation metal such as Cu, Au, Ag, Ni and/or their oxides which can then diffuse and/or drift into the porous oxide of the selector layer 114. In some examples, electrode(s) 112 and/or 116 may include a layer or film of cation metal disposed on a surface that faces the insulator layer 114. In some examples, electrode(s) 112 and/or 116 may be substantially formed of cation metal. Electrode 112 and/or 116 therefore provide a source of cation metal and/or cation metal oxides that diffuse and/or drift into the porous oxide of the selector layer 114 to cause the selector 110 to transition from non-conductive to conductive. Additional details of an example arrangement for a selector including a porous oxide selector layer are provided in connection with FIGS. 4A and 4B.

[0027] The memristor 120 may have a resistance that depends on the history of energy applied across its electrodes 122, 126. For instance, the variable resistance layer 124 may transition between a high-resistance state and a low-resistance state upon application of state-changing energy, such as a voltage pulse of sufficient magnitude and/or duration. Further, the variable resistance layer 124 may remain in its most-recently established resistance state until application of a subsequent state-changing voltage pulse. As such, the resistance state may be used for non-volatile information storage with the two possible resistance states corresponding to a binary bit of information.

[0028] Both the selector 110 and the memristor 120 are two-terminal devices and they are coupled in series between nodes 102 and 104. As shown in the block diagram of FIG. 1A, node 102 is electrically coupled to the first electrode 112 of the selector 110. The second electrode 116 of the selector 110 is electrically coupled to the first electrode 122 of the memristor 120. The second electrode 126 of the memristor 120 is coupled to the node 104. FIG. 1A illustrates these electrical couplings schematically as wires, however the electrical couplings between electrodes and other components may be implemented in a various ways depending on fabrication, materials, and other factors. For instance, in some examples, the electrodes 116 and 122 of the selector 110 and memristor 120 may be implemented as a single layer of conductive material situated between the selector layer 114 and the variable resistance layer 124. In some examples, the electrodes 112 and 126 proximate the nodes 102 and 104, respectively, may be implemented as control lines with multiple selector layers and/or variable resistance layers patterned thereon.

[0029] FIG. 1B is a chart of an example current and voltage for an example memory cell. The current-voltage chart of FIG. 1B schematically illustrates an example relationship between current passed through the memory cell 100 and the voltage applied across the memory cell 100. Referring to the positive voltage region of the chart, right of the axis, it can be seen that the current remains very low below a threshold voltage V_T. The threshold voltage V_T may be the threshold voltage of the selector 110, which exhibits a high electrical resistance for voltages below V_T, but transitions to a conductive state at voltages above V_T. Moreover, at sub-threshold voltages, the resistance of the selector 110 may be greater than the resistance of the memristor 120 such that the selector 110 dominates the resistance of the memory cell 100 for voltages below V_T. In some examples, the selector 110 may exhibit similar behavior at negative voltages: high resistance for voltages greater than $-V_T$ and conductive for voltages less than $-V_T$, which is portrayed in the example

relationship shown in FIG. 1B. The region of the chart in which the behavior of the memory cell 100 is dominated by the selector is labelled as the "Selector Region."

[0030] For voltages above V_T (or less than $-V_T$) the selector 110 is conductive, and so the resistance of the memory cell is dominated by the memristor 120. As shown in FIG. 1B, above V_T, the I-V curve may proceed along two different paths, depending on whether the memristor 120 is in a high resistance state (HRS) or a low resistance state (LRS). To distinguish between the two paths in FIG. 1B, the paths are shown with dashed line for the HRS behavior and a solid line for the LRS behavior. Thus, if the memristor 120 is in the HRS, current through the memory cell 100 follows the dashed path at voltages above V_T. On the other hand, if the memristor 120 is in the LRS, current through the memory cell follows the solid path at voltages above V_T.

[0031] As noted above, to determine the state of the memristor 120, a read voltage V_R may be applied to the memory cell 100. As shown in FIG. 1B, if the memristor 120 is in HRS (dashed path), then applying V_R results in a first current I_1. On the other hand, if the memristor 120 is in LRS (solid path), then applying VR results in a second current I_2. Reading the resistance state may be performed by measuring the current through the memory cell 100 while V_R is applied across the terminals 102, 104. For instance, the resulting current may be collected and compared to a reference current value, which reference may be between I_1 and I_2, and the state of the memory cell 100 may be determined based on the comparison.

[0032] In some examples, V_R may be applied by setting one terminal of a target memory cell to about ½ V_R and the other terminal to about -½ V_R. In a crossbar array, applying V_R in this way using a target row line and target column line, with all other row/column lines set to 0 results in all non-target memory cells that share either the target row or target column receiving a voltage of ½ V_R. As such, many memory cells in a crossbar array will regularly receive a voltage of about ½ V_R. Current drawn at ½ V_R may contribute to sneak current, introduce noise in the current measurement, and cause excess power consumption. Reducing current at ½ V_R to near zero may

help mitigate these issues. In practice, this may be achieved by selecting V_R to be less than 2 V_T, such that ½ VR is within the Selector Region shown in FIG. 1B. In addition, the value of V_R may be selected to be greater than V_T by some margin to ensure that the two currents I_1 and I_2 are measurable and distinguishable from one another. Balancing these concerns may result in selecting V_R to satisfy the following relation: $½ V_R < V_T < V_R$.

[0033] Further, to set the resistance state of the memristor 120, a set voltage V_S may be applied to the memory cell 100. The set voltage V_S may be a voltage that causes the memristor to transition from HRS to LRS, as illustrated by the arrow in FIG. 1B from the HRS dashed path to the LRS solid path. For example, the transition between states may involve a change in distribution of ions, vacancies, and/or defects within the variable resistance layer 124 of the memristor 120. Applying a pulse at the set voltage V_S may set the memristor 120 to LRS and applying a pulse at a reset voltage voltage $-V_S$ may reset the memristor 120 to HRS. Other examples of hysteresis curves are possible in which a given memristor's resistance state may be set and/or reset by application of suitable voltage pulses.

[0034] Note that the I-V chart described above in connection with FIG. 1B is provided for example purposes only to illustrate one example of behavior that may be exhibited by some memory cells. Other memristor devices may exhibit different hysteresis curves, including some in which the transition between resistance states may be initiated by voltages of the same polarity. The chart in FIG. 1B is therefore provided for example purposes only. Other examples applicable to the present disclosure may include memory cells that exhibit alternative hysteresis curves to that shown in FIG. 1B.

[0035] FIG. 2 is a block diagram of an example crossbar array 200 having multiple memory cells that each have a selector 110 in series with a memristor 120 in 1S1R configuration. Each of the selectors 110 include a selector layer 114 situated between two electrodes. The selector layers 114 of the selectors 110 may be similar to the selector layer described above in connection with FIGS. 1A-1B. For example,

the selector layers 114 of the selectors 110 may each include a porous oxide material that receives drifting cation metal and/or cation metal oxides from one or both electrodes upon application of an electrical bias. Upon application of a threshold voltage across a given selector layer 114, the drifting cation metal and/or cation metal oxide may form a conductive channel through that selector layer 114.

[0036] The crossbar array 200 shown in FIG. 2 demonstrates a layout with two row lines 210, 212 and two column lines 220, 222. In some examples, the row lines 210, 212 may be parallel with one another and orthogonal to the conductive lines 220, 222, which are themselves parallel with one another. Memory cells are located at the intersections of the row lines and column lines such that a given memory cell is connected between one row line and one column line, which lines may be used to control that memory cell. As shown in FIG. 2, memory cell 202 is electrically coupled between row line 210 and column line 220; memory cell 204 is electrically coupled between row line 210 and column line 222; memory cell 206 is electrically coupled between row line 212 and column line 220; and memory cell 208 is electrically coupled between row line 212 and column line 222. Each of the -memory cells 202-208 includes a selector 110 electrically coupled in series with a memristor 120. Example operations that may be performed using the crossbar array -200 are described in connection with FIGS. 3A and 3B.

[0037] FIG. 3A is a flowchart of an example process 300 for writing data to a memory cell. FIG. 3B is a flowchart of an example process 310 for reading data from a memory cell. Processes 300 and 310 may be described below as being executed or performed by a system, for example, the crossbar array 200 of FIG. 2. Other suitable systems and/or computing devices may be used as well. Processes 300 and 310 may be implemented in the form of executable instructions stored on at least one machine-readable storage medium of the system and executed by at least one processor of the system. In some examples, processes 300 and 310 may be implemented in the form of electronic circuitry (e.g., hardware). The processes 300 and 310 are depicted with a series of blocks in the flowcharts of FIGS. 3A and 3B. In

some cases, one or more blocks of processes 300 and/or 310 may be executed substantially concurrently or in a different order than shown in FIGS. 3A and 3B. In some cases, processes 300 and 310 may include more or less blocks than are shown in FIGS. 3A and 3B. In some examples, one or more of the blocks of processes 300 and/or 310 may, at certain times, be ongoing and/or may repeat.

[0038] Referring to FIG. 3A, at block 302, an indication may be received to write data to a target memory cell. For example, a control system associated with the crossbar array 200 of FIG. 2 may receive an indication that a data value should be written to memory cell 202.

[0039] At block 304, a write voltage pulse may be applied to the target memory cell. The write voltage pulse may cause the memory cell to transition to a resistance state associated with the data to be written to the target memory cell. For example, a control system associated with the crossbar array 200 of FIG. 2 may select the row and column line combination that corresponds to memory cell 202: row line 210 and column line 220, and apply a write voltage pulse across those lines 210, 220 so as to set to the resistance state of memory cell 202.

[0040] Referring to FIG. 3B, at block 312, an indication to read data from a target]memory cell may be received. For example, a control system associated with the crossbar array 200 of FIG. 2 may receive an indication that a data value should be read from memory cell 202.

[0041] At block 314, a read voltage may be applied to the target memory cell. The read voltage may be greater than a threshold voltage of a selector in the memory cell to allow the resistance state of the memristor to be determined. For example, the row and column lines for the target memristor: row line 210 and column line 220 may be set to $+\frac{1}{2} V_R$ and $-\frac{1}{2} V_R$, respectively.

[0042] At block 316, the current that flows through the target memory cell may be measured while the read voltage is applied. For example, current may be collected along the column line 220.

[0043] At block 318, the data value of the target memory cell may be determined based on the measured current. For example, if the current exceeds a threshold, then the memory cell may be determined to be in a low resistance state and otherwise may be determined to be in a high resistance state.

[0044] FIG. 4A is a diagram of a side cross-sectional view of an example selector 400 in a non-conductive state. The selector 400 includes a bottom electrode 402, a selector layer 404, and a top electrode 406. The selector layer 404 may be sandwiched between the top electrode 406 and the bottom electrode 402. The selector layer 404 may be a porous oxide material, such as nano-porous silicon dioxide. The top electrode 406 may include cation metal such as Cu, Au, Ag, Ni, etc. and/or cation metal oxide. At least some of the cation metal may be situated along a surface of the top electrode 406 that faces the selector layer 404. The top electrode 406 may provide a source of cation metal and/or cation metal oxides that diffuse and/or drift into the selector layer to thereby transition the selector 400 to a conductive state. In the non-conductive state shown in FIG. 4A, cation metal from the top electrode 406 has not diffused and/or drifted into the porous oxide material enough to create conductive channels therein. In some examples, while the selector 400 is non-conductive, cation metal may remain substantially within the top electrode 406, leaving the selector layer 404 substantially void of cation metal. Without the cation metal, the porous oxide material is not a conductive material and does not allow for significant current to flow between the electrodes 402, 406.

[0045] FIG. 4B is a diagram of a side cross-sectional view of an example selector 400 in a conductive state. A voltage may be applied across the top and bottom electrodes 402, 406. The applied voltage is represented in FIG. 4B as a voltage source 418. Upon application of a threshold voltage, cation metal ions 420 from the top electrode 406 may drift into the porous oxide of the selector layer 404 so as to create conductive channels therein. In the diagram of FIG. 4B, the migrating cation metal ions 420 are depicted as circles that may occupy locations within the porous oxide of the selector layer 404 (e.g., at vacant defect centers). The cation metal ions

420 will drift into the porous oxide material so as to form a conductive channel for current to flow between the electrodes. For instance, in a case where the cation metal ions 420 are able to become aligned in a series of adjacent or near ions that stretch between the two electrodes, current may flow along the resulting conductive channel. The diagram of FIG. 4B provides a schematic illustration of two such conductive channels within the selector layer 404 formed by the diffusing and/or drifting cation metal ions 420.

[0046] In some examples, a sidewall structure may be formed around the sidewalls of the selector layer 404. The sidewall structure may be formed of an electrically insulating material that extends between the two electrodes, for example. In some cases, such a sidewall structure may insulate the selector layer 404 therein from electrical and/or thermal variations. In some examples, a sidewall may also provide some structural stability to the sandwich structure of the selector device 400.

[0047] FIG. 4A and 4B provide diagrams illustrating an example structure and arrangement for selector 400 and to help enhance understanding. However, these diagrams are not rendered to scale, and the relative thicknesses and/or dimensions of the electrodes, selector layer, and/or cation metal(s) depicted therein are not representative of a physical arrangement or in any way serve to limit the physical dimensions, ratios, etc., of selector devices presented herein.

[0048] FIGS. 5A and 5B are a flowcharts of example processes 500 and 510 for fabricating a selector. Processes 500 and 510 may be described below as being executed or performed by a system, such as a micro-fabrication system and/or computing device. Processes 500 and 510 may be implemented in the form of executable instructions stored on at least one machine-readable storage medium of the system and executed by at least one processor of the system. In some examples, processes 500 and 510 may be implemented in the form of electronic circuitry (e.g., hardware). The processes 500 and 510 are depicted with a series of blocks in the flowcharts of FIGS. 5A and 5B. In some cases, one or more blocks of

processes 500, 510 may be executed substantially concurrently or in a different order than shown in FIGS. 5A and 5B. In some cases, processes 500, 510 may include more or less blocks than are shown in FIGS. 5A and 5B. In some examples, one or more of the blocks of processes 500, 510 may, at certain times, be ongoing and/or may repeat.

[0049] At block 502, a first electrode including a cation metal and/or cation metal oxide may be formed. The electrode may be formed by a conductive material that is patterned onto a particular region at a desired thickness. For instance, the conducive material may be electroplated over a seed level. In some examples, the conductive material of the first electrode may be a cation metal, such as Cu, Au, Ag, Ni, etc. In some examples, the first electrode may include multiple layers, and the last-formed layer may include a cation metal and/or cation metal oxide. For example, the first electrode may include a layer of Ti, Pt, Ta, TiN, TaN, and/or Pd (or another conductive material), with a layer of Au (or another cation metal and/or cation metal oxide) formed thereon. As such, the top surface of the first electrode includes at least some cation metal and/or cation metal oxide, which can then be used as a source to diffuse and/or drift into the insulator layer.

[0050] At block 504, an insulator layer including porous oxide may be formed over the first electrode. The porous oxide may be a layer of nano-porous silicon dioxide, for example. In some examples, the porous oxide may be formed by depositing material over the first electrode, such as via a chemical vapor deposition process (e.g., plasma enhanced chemical vapor deposition, plasma assisted chemical vapor deposition, etc.). In some examples, the porous oxide material may be patterned to occupy a particular area and at a desired thickness using various techniques such as masking, resists, etc. In some examples, a porous oxide layer may be formed by another micro-fabrication technique, such as spin coating. In some examples, the porous oxide material may be formed directly on a surface of the first electrode that includes at least some cation metal and/or cation metal oxide material that can mobilize into the porous oxide material responsive to application of an electrical bias.

For instance, there may not be a material that impedes migration of cation metal, such as an electrode barrier or the like, that is situated between the first electrode and the insulator layer. In some examples, however, such a barrier may be placed between the insulator and the second electrode which may help prevent migrating cations from penetrating the entirety of the porous oxide insulator layer and thereby ensuring their ability to migrate back to the first electrode.

[0051] At block 506, a second electrode may be formed over the insulator layer. The second electrode may be a conductive material that is patterned on a region of the insulator layer so as to occupy a region opposite the first electrode. The second electrode may be formed by patterning a seed layer and electroplating a suitable conductive material, or by another micro-fabrication technique. The second electrode may or may not include cation metal and/or cation metal oxides. Once formed, the second electrode and the first electrode may sandwich the insulator layer.

[0052] Referring to FIG. 5B, another process 510 for fabricating an example selector is described. Process 510 is similar to process 500 in some respects, however the second-formed electrode includes cation metal and/or cation metal oxides rather than the first-formed electrode. Thus, for a selector formed according to process 510, the second-formed electrode may provide a source of cation metal and/or cation metal oxide that migrate into the insulator layer.

[0053] At block 512, a first electrode may be formed. The first electrode may be a conductive material that is patterned in a particular area and thickness. The first electrode may be formed by patterning a seed layer and electroplating a suitable conductive material, or by another micro-fabrication technique. The first electrode may or may not include cation metal and/or cation metal oxides.

[0054] At block 514, an insulator layer including porous oxide may be formed over the first electrode. The porous oxide may be a layer of nano-porous silicon dioxide, for example. In some examples, the porous oxide may be formed by depositing material over the first electrode, such as via a chemical vapor deposition process (e.g., plasma enhanced chemical vapor deposition, plasma assisted chemical vapor

deposition, etc.). In some examples, the porous oxide material may be patterned to occupy a particular area and at a desired thickness using various techniques such as masking, resists, etc. In some examples, a porous oxide layer may be formed by another micro-fabrication technique, such as spin coating.

[0055] At block 516, a second electrode including a cation metal and/or cation metal oxide may be formed over the insulator layer so as to occupy a region opposite the first electrode. The electrode may be formed by a conductive material that is patterned onto a particular region at a desired thickness. Once formed, the second electrode and the first electrode may sandwich the insulator layer. The conducive material may be electroplated over a seed level. In some examples, the conductive material of the second electrode may be a cation metal, such as Cu, Au, Ag, Ni, etc. In some examples, the second electrode may include multiple layers, and the first-formed layer may include a cation metal and/or cation metal oxide. For example, the second electrode may include a layer of Au (or another cation metal and/or cation metal oxide) formed directly on the insulator layer. A layer of Ti, Pt, Ta, TiN, TaN, Pd, etc., or another conductive material may be formed on the cation metal layer. As such, the bottom surface of the second electrode includes at least some cation metal and/or cation metal oxide, which can then be used as a source to diffuse and/or drift into the insulator layer.

[0056] In some examples, a portion of the second electrode that includes at least some cation metal and/or cation metal oxide material may be formed directly on a surface of the porous oxide material. As such, the cation metal may mobilize into the porous oxide material responsive to application of an electrical bias. For instance, there may not be a material that impedes migration of cation metal, such as an electrode barrier or the like, that is situated between the second electrode and the insulator layer. In some examples, however, such a barrier may be placed between the insulator and the first electrode which may help prevent migrating cations from penetrating the entirety of the porous oxide insulator layer and thereby ensuring their ability to migrate back to the second electrode.

[0057] Some examples disclosed here relate to selector devices for being electrically coupled in series with a memristor device to form a memory cell. However, the selector devices described herein may be used in other contexts as well. For instance, in a crossbar array, selectors that include insulator layers formed of porous oxide to receive diffusing and/or drifting cation metal and/or cation metal oxide from at least one electrode may be electrically coupled in series with other two-terminal memory elements to help inhibit application of voltage below a threshold value to such memory elements. Moreover, selectors described herein may be applied in a variety of electrical contexts to help regulate voltage(s) applied to various components and/or current(s) through various components.

CLAIMS

1. A selector device comprising:

a first electrode comprising a cation metal;

a second electrode; and

a porous oxide layer disposed between the first and second electrodes, the porous oxide layer comprising a framework supporting a porous structure.

2. The device of claim 1, wherein the porous oxide layer is to receive, in response to application of a threshold voltage across the first and second electrodes, drifting cation metal from the first electrode that form a conductive channel.

3. The device of claim 2, wherein the drifting cation metal causes the porous oxide layer to transition from a high-resistance state to a low-resistance state.

4. The device of claim 1, wherein the cation metal of the first electrode comprises a film of gold or copper disposed on a side of the first electrode facing the porous oxide layer.

5. The device of claim 1, wherein the porous oxide layer comprises a layer of nano-porous silicon dioxide having defect centers distributed throughout the layer.

6. The device of claim 1, wherein the porous oxide layer is deposited on the first or second electrode via plasma enhanced chemical vapor deposition.

7. The device of claim 1, wherein the second electrode comprises the cation metal.

8. The device of claim 1, wherein the porous oxide layer includes a conductive dopant.

9. A method of fabricating a selector device, the method comprising:

forming a first electrode;

forming a porous oxide layer over the first electrode, the porous oxide layer comprising a framework supporting a porous structure; and

forming a second electrode over the insulator layer such that the insulator layer is disposed between the first and second electrodes; and

wherein at least one of the first and second electrodes comprises a cation metal.

10. The method of claim 9, wherein forming the porous oxide layer comprises depositing a porous oxide material on the first electrode via plasma enhanced chemical vapor deposition.

11. The method of claim 9, wherein the porous oxide layer comprises a layer of nano-porous silicon dioxide having defect centers distributed throughout the layer.

12. A system comprising:

a memristor device having two terminals and a variable resistance layer disposed between the two terminals, the variable resistance layer to transition between resistance states responsive to application of a transition energy; and

a selector device electrically coupled in series with the memristor device, the selector device comprising:

(i) a first electrode comprising a cation metal;

(ii) a second electrode; and

(iii) a porous oxide layer disposed between the first and second electrodes, the porous oxide layer comprising a framework supporting a porous structure.

13. The system of claim 12, wherein the porous oxide layer is to receive, in response to application of a threshold voltage across the first and second electrodes, drifting cation metal from the first electrode.

14. The system of claim 13, wherein the drifting cation metal causes the porous oxide layer to transition from a high-resistance state to a low-resistance state.

15. The system of claim 12, wherein the porous oxide layer comprises a layer of nano-porous silicon dioxide having defect centers distributed throughout the layer.

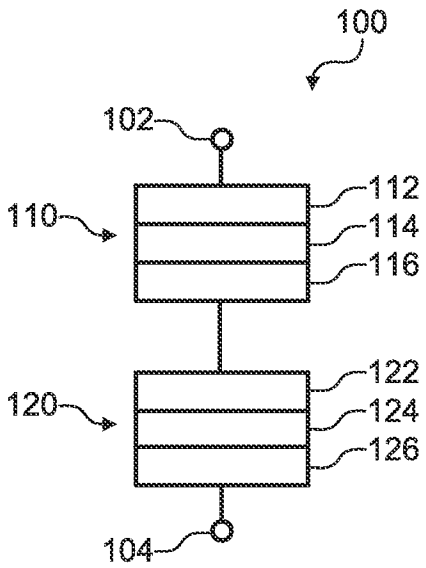


FIG. 1A

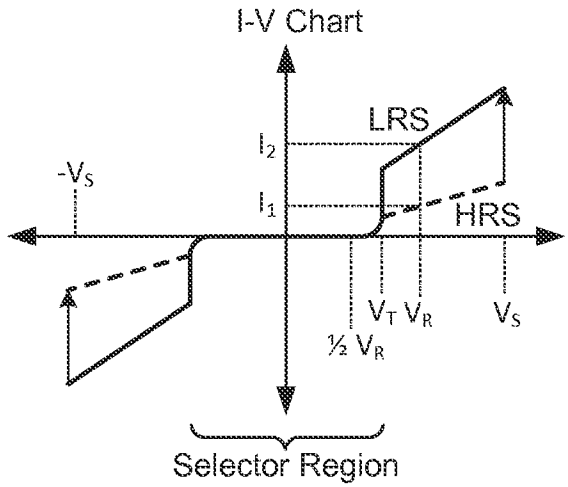


FIG. 1B

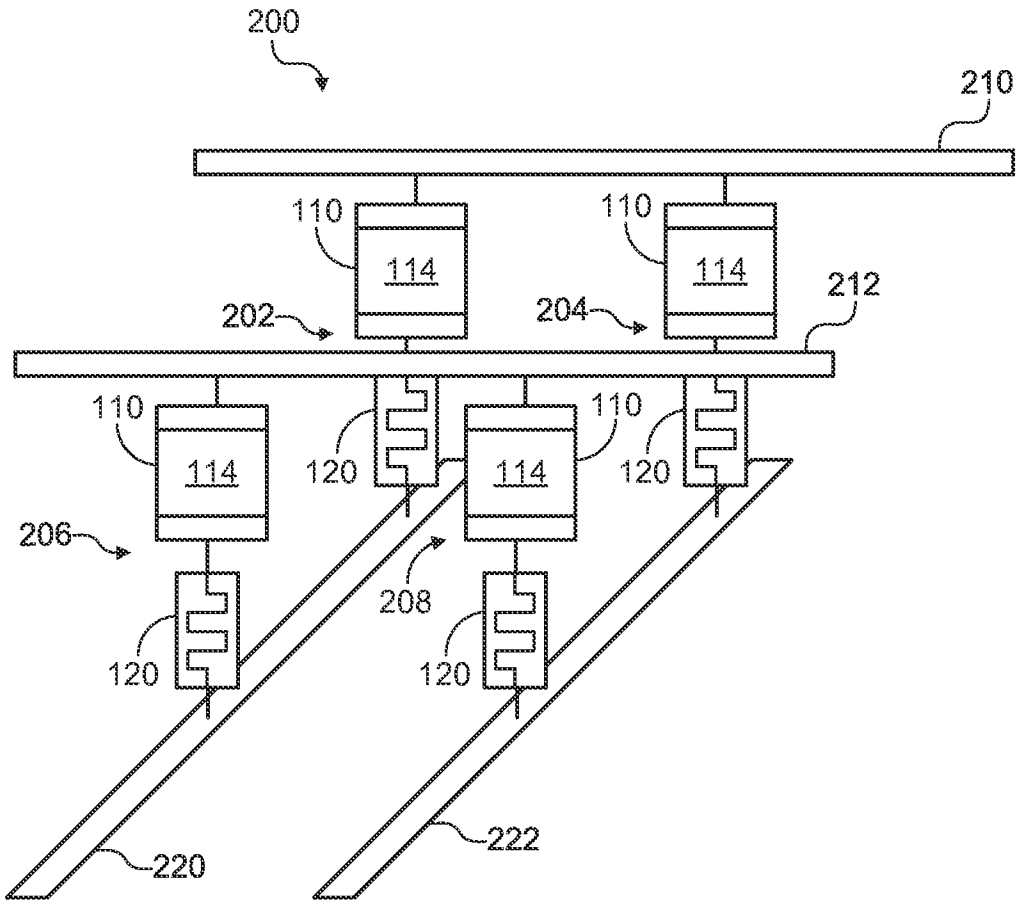


FIG. 2

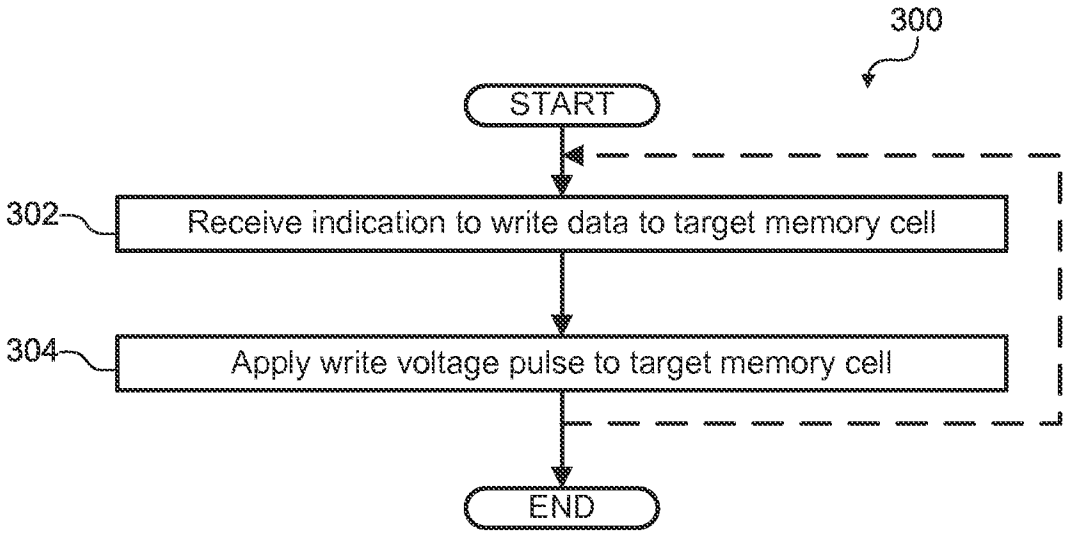

300
START
302
Receive indication to write data to target memory cell
304
Apply write voltage pulse to target memory cell
END

FIG. 3A

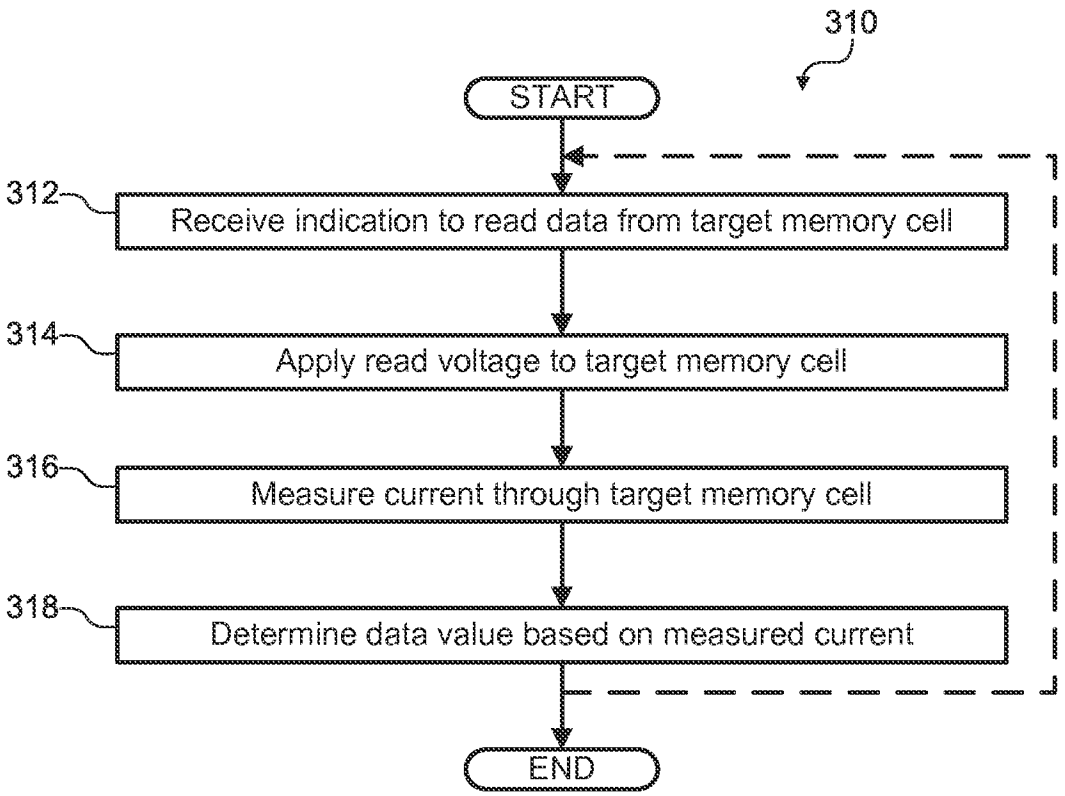

310
START
312
Receive indication to read data from target memory cell
314
Apply read voltage to target memory cell
316
Measure current through target memory cell
318
Determine data value based on measured current
END

FIG. 3B

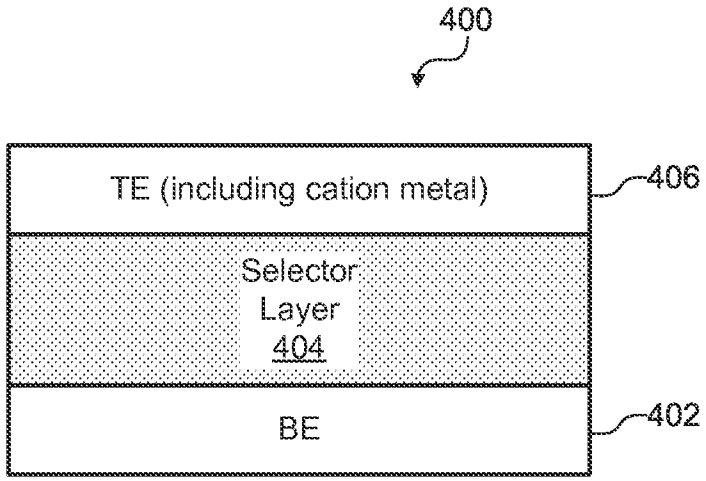

400
TE (including cation metal)
406
Selector
Layer
404
BE
402

FIG. 4A

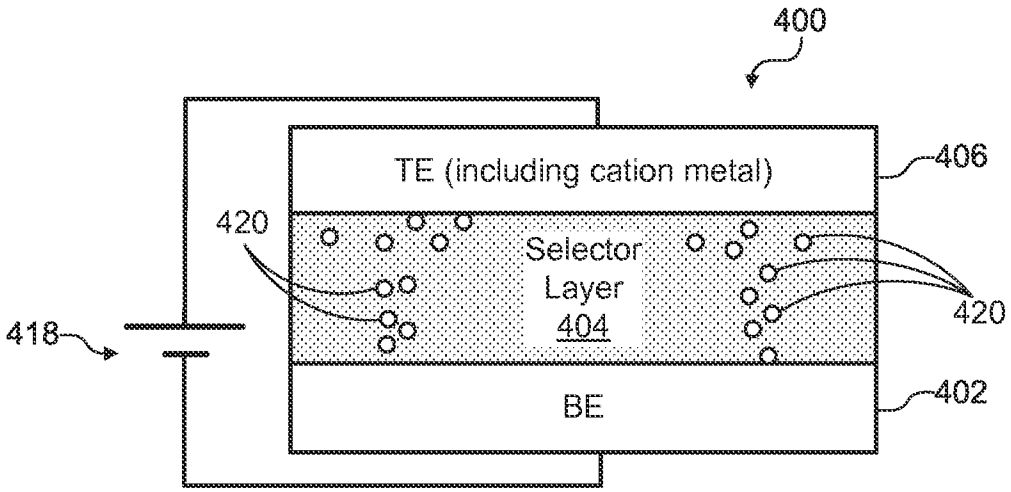

400
TE (including cation metal)
406
420
Selector
Layer
404
420
418
BE
402

FIG. 4B

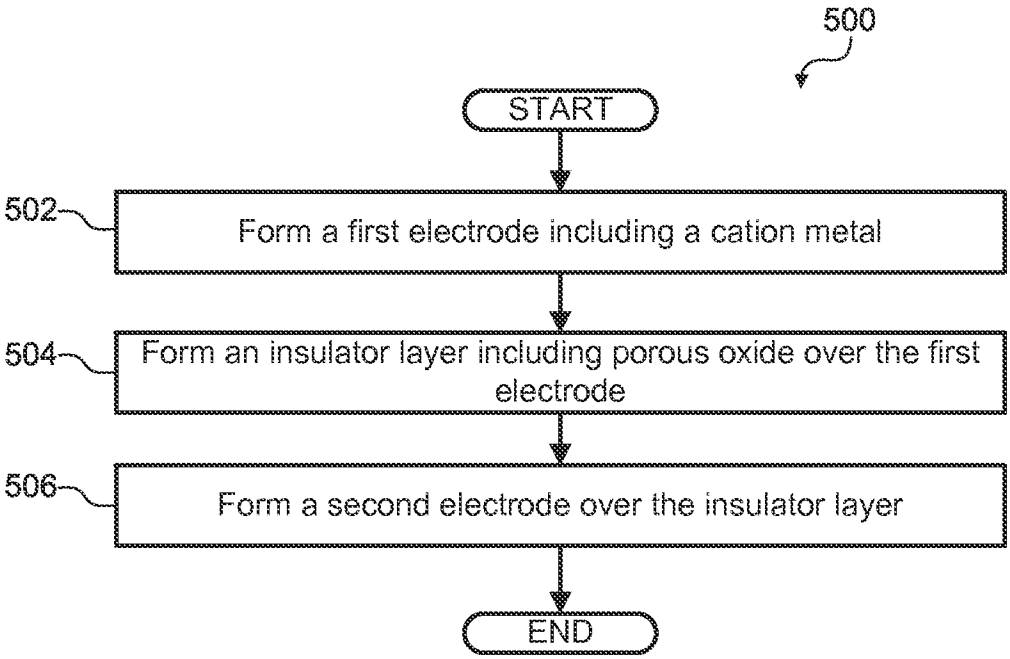

500
START
502
Form a first electrode including a cation metal
504
Form an insulator layer including porous oxide over the first electrode
506
Form a second electrode over the insulator layer
END

FIG. 5A

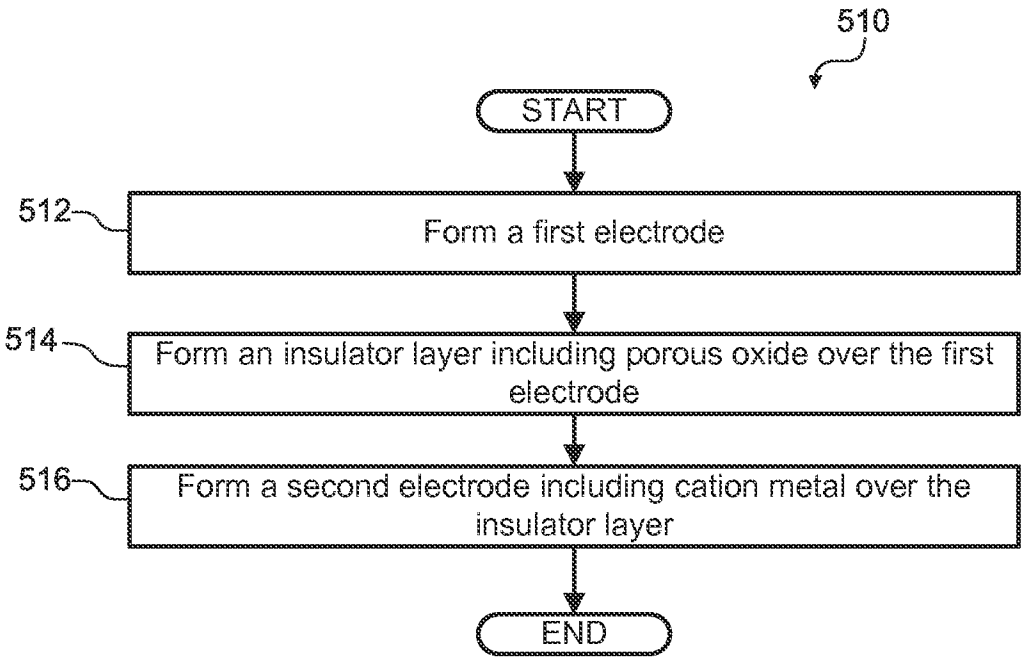

510
START
512
Form a first electrode
514
Form an insulator layer including porous oxide over the first electrode
516
Form a second electrode including cation metal over the insulator layer
END

FIG. 5B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/051882

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/316(2006.01)i, H01L 21/28(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/316; G11C 11/34; G11C 11/56; H01L 51/00; H01L 29/04; H01L 45/00; H01L 27/10; G11C 11/00; H01L 21/28

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: memory cell, porous oxide, memristor, diffusion, dopant

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y		2,3,8,12-15
Y	US 2011-0176353 A1 (ZHIYONG LI et al.) 21 July 2011 See abstract; paragraphs [0016], [0017], [0046]-[0054]; claim 1; and figure 3.	2,3,8,12-15
Y	US 2010-0008124 A1 (ROY E. SCHEUERLEIN et al.) 14 January 2010 See abstract; paragraphs [0057]-[0062]; claim 1; and figures 8-12.	12-15
A	JP 2005-500682 A (ADVANCED MICRO DEVICES INCORPORATED) 06 January 2005 See abstract; paragraphs [0021]-[0025]; claim 1; and figures 1-20.	1-15
A	US 2013-0175493 A1 (ZHITANG SONG et al.) 11 July 2013 See abstract; paragraphs [0043]-[0047]; claim 1; and figure 6.	1-15

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 May 2016 (30.05.2016)	**30 May 2016 (30.05.2016)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/051882

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