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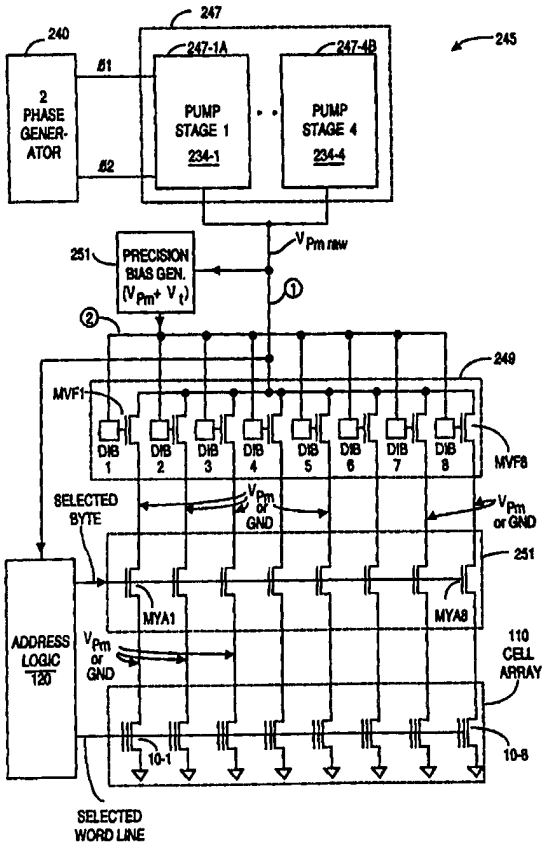
(54) Title: PRECISE MEDIUM VOLTAGE, HIGH CURRENT CHARGE PUMP SYSTEM

(57) Abstract

A medium high voltage pump system includes a two–phase raw high voltage generator circuit (247) that operates from a low voltage Vdd to output a larger magnitude V¿Pm raw?, and a voltage follower (249) whose input lead (2) receives a lower current reference voltage that is at least V_{Pm}, whose power lead (1) is coupled to said V¿Pm raw?, and whose output lead provides V_{Pm} at a current level greater than the reference voltage. The voltage follower preferably being a source follower. The raw generator comprises a plurality of series–connected charge multiplier stages (247–1A through 247–4B) that each includes a MOS transistor and a charging capacitor. One of two non–overlapping phase signals is coupled to the free end of each charging capacitor such that adjacent charging capacitors are driven by different phases, each charging stage preferably having Vt–cancellation and substrate–well protection.



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PRECISE MEDIUM VOLTAGE, HIGH CURRENT CHARGE PUMP SYSTEM

RELATIONSHIP TO PENDING APPLICATION

Applicants' co-pending U.S. patent application serial no. 08/744,200 filed on 5 November 1996, entitled POSITIVE/NEGATIVE HIGH VOLTAGE CHARGE PUMP SYSTEM discloses a number of high voltage pump circuits that may be adapted for use with the present invention.

FIELD OF THE INVENTION

The present invention relates to charge pump circuits that step-up voltage levels used to program and erase flash EPROM and EEPROM circuits, and more specifically to charge pump circuits for outputting medium voltage levels at high current.

BACKGROUND OF THE INVENTION

Flash electrically programmable read only memories ("EPROMs") and flash electrically erasable and programmable read only memories ("EEPROMs") are solid state devices that can persistently store digital data. As shown by Figure 1, an EPROM-type flash cell 10 typically has a metal-on-silicon ("MOS") structure that includes a substrate 12, source and drain regions 14, 16, a floating gate 18 overlying MOS channel region 20 but separated therefrom by a thin layer region 22 of oxide 24. A control gate 26 is formed overlying floating gate 18. For a flash EPROM, it is necessary to surround the source region with a lightly doped region 15 of like-conductivity type dopant. The substrate or bulk 12 is tied to a potential Vbb that typically is ground.

For the NMOS device depicted, substrate 12 is doped with P-type impurities, and the source and drain regions are doped with N-type impurities. For a flash EPROM, N+ source region 14 is surrounded by an N- region 15. The N- region 15 is included to protect the source junction from the large source-floating gate electric field used to electrically erase the cell. This N- region helps reduce electric field magnitude between source nodes and the first polysilicon layer (not shown) during erase operations.

Of course a PMOS device may be formed by substituting an N-type substrate, and P-type source, drain regions. Generally, NMOS devices are preferred to PMOS devices in that the majority carriers in NMOS devices, electrons, have 2.5 times the mobility of the majority carriers, holes, in PMOS devices, and thus can operate more rapidly. Although a flash-type EPROM cell is depicted, it is to be understood that the present invention may also be used with EPROM, or EEPROM type memory as well.

A Vcg voltage coupled to control gate 26 can affect charge stored on floating gate 18, which charge affects the Vt threshold voltage of MOS device 10. The magnitude of charge on the floating gate controls the minimum (or Vt) voltage Vcg that will turn-on device 10, causing drain-source current to flow across the channel region 20. Device 10 is programmed to one of two states by accelerating electrons from substrate channel region 20 through the thin gate dielectric 22 region onto floating gate 18.

The state of device 10, e.g., how much charge is stored on floating gate 18, is read by coupling an operating voltage Vds across source and drain regions 14, 16, and then reading the drain-source current Ids to determine whether the device is ON or OFF for a given control volt-

age level Vcg.

Two mechanisms are in common use to program a flash EPROM (or to erase a flash EEPROM, whose definitions of erasing and programming are opposite), namely channel-hot-electron ("CHE") injection, and Fowler-Nordheim ("FN") tunnelling. Commonly, EPROM-flash devices use FN-erase mode and CHE-program mode operations, which combination is sometimes referred to as ETOX, for EPROM tunnel oxide technology. On the other hand, EEPROM-flash devices commonly use FN-erase mode, and FN-program mode operations.

Table 1 summarizes the application of FN and CHE modes, as well as typical cell voltages for gate, source and drain nodes. As described later herein, the present invention is directed to a medium high voltage pump that can increase a lower Vdd voltage to approximately 5 VDC at high current for coupling to the source or drain of cells to be erased or programmed.

TABLE 1

	ERASE	PROGRAM
EPROM-flash	FN: G=-8V, S=5V, D=float	CHE: G=8V, S=0V, D=5V
EEPROM-flash	FN: G=12V, S=0V, D=0V	FN: G=-8V, S=5V, D=float

Thus, for the EPROM-flash cell depicted in Figure 1, channel-hot-electron injection is used to program the cell to an off-state in read mode. Using CHE technology, it is necessary to apply a positive high voltage Vcg, e.g., perhaps +8 VDC to +10 VDC to control gate 26, while applying perhaps +5 VDC to drain 16, and 0 VDC to source 14. As hot electrons are accelerated and travel from source to drain, the electric field created by the high Vgs and Vds voltages can pull some hot electrons from the drain to the floating gate. (No electrons will be pulled to the floating gate from the source, which is at ground

potential.) When using CHE injection, the drain-source channel current will be approximately 0.5 mA/cell.

Using FN technology, an EPROM-flash cell is erased by coupling perhaps -8 VDC to the control gate 26, +5 VDC to the source, and allowing the drain to float. FN-mode erasing can be accomplished with a tunnel current of approximately 10 nA/cell. (Although one can erase an EPROM-flash cell by providing positive high voltage to the source and grounding the control gate, so doing increases source region junction leak current, and increases hot-hole injection at the source region.)

To program an EEPROM-flash cell using FN technology requires applying approximately -8 VDC to control gate 26, applying +5 VDC to source 14, and grounding drain 16. The negative Vcg high voltage and Vs produce a large tunnel electric field that can push electrons from the floating gate 18 to the source 14. (No electrons are pulled out of the floating gate to the drain, as the floating drain will not generate a large electric field.) Unfortunately, this causes hole trapping, and degrades the storage capability and endurance of the memory cell. To erase an EEPROM cell using FN technology, approximately +12 VDC is applied to control gate 26, while drain 16 and source 14 are grounded. As was the case for an EPROM-flash cell, FN erasing can be accomplished with a tunnel current of approximately 10 nA/cell.

Typically the circuitry with which memory cells 10 are used is powered by a single low voltage power supply, a 3.3 VDC battery for example, although batteries ranging from perhaps 1.2 VDC to 5 VDC or higher may instead be used. Positive and negative high voltage pump circuits are commonly used to generate the ±10 V (V_{Pp}, V_{Pn}) or so high voltage necessary to program and erase memory cells from a single lower voltage power supply. In the prior

art, separate medium voltage pump circuits are used to generate the +5 V or so (V_{Pm}) that must be supplied at relatively higher current levels in the few mA range. Usually the source shares a pump circuit with the drain, as the voltages required are the same.

From the foregoing discussions of CHE and FN mechanisms, it will be appreciated that the number of cells that can be erased or programmed in parallel, e.g., simultaneously (or in a "flash"), will often be determined by the pump circuit current output characteristics. For example, if a medium voltage V_{Pm} pump circuit can provide an average 8 mA output current drain-source, 16 bits can be programmed simultaneously, whereas 100 Kbytes may be erased simultaneously. Understandably, in designing pump circuits it is important that sufficient program or erase current be provided to at least meet the cell requirements to maintain erasing and programming efficiency . In a system with a 5 VDC power supply (Vdd = 5 VDC), 32-bit programming can be achieved, but if Vdd = 3 VDC, only 8-bit programming can presently be achieved. It simply is difficult in ETOX systems to provide sufficient 0.5 mA/cell program current at 5 VDC drain voltage when Vdd is less than about 3 VDC. Further, it is necessary to pump a 3 VDC Vdd up to 5 VDC, preferably using an on-chip pump circuit, to even meet the 0.5 mA/cell programming requirements. If an externally created 5 VDC Vdd is available, it may of course provide multiple byte-programming, e.g., four-byte, without recourse to an on-chip high current pump. At present, FN-programming dominates sub-3 VDC Vdd systems, whereas CHE-programming dominates 5 VDC Vdd flash memory systems.

As shown in Figure 2, it is common to form an integrated circuit ("IC") 100 that includes a plurality of cells 10 that are arrayed in addressable rows and columns that define a storage array 110. Address logic 120 permits

accessing a specific cell in such an array. For example, during a program/read or erase operation, a given cell 10 may be accessed by applying the proper Vgs, Vd, Vs potentials to all cells in a column containing the addressed cell, and to the row containing the addressed cell. Commonly, a horizontal row of cells having their control gates tied-together defined a word line ("WL"), whereas a vertical column of cells having their drains tied-together define a bit line ("BL"). For ease of illustration, address logic 120 is shown as having a single output lead, but in practice there will be multiple output leads, including leads for Vgs, Vd, and Vs.

In Figure 2, IC 100 preferably operates from a single low voltage power supply Vdd, which may be a battery if, for example, IC 100 is a storage unit within a laptop computer. Typically the low voltage power supply magnitude is 5 VDC, although the trend has been toward lower voltage magnitudes, e.g., 3.3 VDC or 2.5 VDC, with a goal of perhaps 1.2 VDC.

To generate the high voltage necessary to program or erase the various cells, IC 100 will commonly include a positive high voltage pump circuit 130 that outputs a high positive potential V_{Pp}, and a negative high voltage pump circuit 140 that outputs a high negative potential V_{Pn}. A medium voltage circuit 145 is also used to output a medium high voltage V_{Pm}, perhaps +5 V at relatively higher current levels, e.g., $\approx$ 5 mA, than are associated with voltages V_{Pp} and V_{Pn}.

IC 100 also includes a phase generator circuit 150 that outputs a plurality of non-overlapping different phase pulse trains that drive the positive and negative pump circuits. Many prior art high voltage pump circuits require phase generators that provide at least four-phase output pulse trains, here denoted $\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$, al-

though some circuits require at least eight-phase pulse trains. It is important that phase generator 150 output non-overlapping pulse train signals for the various voltage generating circuits 130, 140, 145 to function. It will be appreciated that generating a large number of non-overlapping phase signals can require complex phase generator circuitry that will consume IC chip-area. Further, as more phases are required to be generated, the practical upper frequency of the phase generator output signals decreases, due to the necessity that the various phase signals not overlap each other at their voltage transitions.

In typical flash memory applications, an erase time of 1 second is typical, regardless of the number of flash memory cells, e.g., cells 10, being erased. However, in practice, the magnitude of the erase current can limit the number of cells or memory bits that can be erased simultaneously. A typical flash memory cell, e.g., cell 10, may require about 10 nA during erase mode operation, and about 0.5 mA during program mode operation. Stated differently, programming current required by a typical memory cell exceeds erase current by about 50,000:1. Because of this current limitation, it is common to block erase 64 Kbits simultaneously, while programming is directed to one byte (e.g., 8 bits) at a time. Typically, to program a byte requires about 0.5 mA/cell x 8 cells $\approx$ 4 mA at about 5 VDC. Approximately the same current is required to erase a block of 64 KBytes, e.g., 10 nA/cell x 64 KByte cells $\approx$ 5 mA. Since simultaneous block erase and byte programming would not occur, a single medium voltage pump circuit capable of approximately 5 mA output at V_{Pm} can suffice.

Figure 3A depicts a prior art approach used to implement medium voltage generator 145. This approach, favored by Toshiba, Inc. of Japan, implements generator 145 by com-

bining the outputs of eight precise two-stage voltage generators, 160-1 through 160-8. Each voltage generator includes two stages of pump circuitry, for example, generator 160-1 comprising a first pump stage 160-1A and a second pump stage 160-1B. Phase generator 150 must output eight phases, e.g., $\phi 1$, $\phi 2$, ... $\phi 8$ and their complements. Each phase is at a common frequency but is shifted 45° relative to an adjacent phase. In Figure 3A, the complementary phase signal is coupled to the second stage in each pump.

Figure 3B depicts a prior art two-stage positive high voltage so-called Dickson charge pump, such as might be used for pump 1, 160-1, or any other pump in Figure 3A. Details of this configuration may be found in "On-Chip High-Voltage Generation in NMOS Integrated Circuits Using an Improved Voltage Multiplier Technique", Dickson, J., IEEE J. Solid State Circuits, vol. 11, pp. 374-378, June 1976. In this configuration, a plurality of voltage pump or multiplier or rectifier stages is formed, each comprising an NMOS used as a diode, and an associated charging capacitor. (NMOS transistors in general are preferred to PMOS devices because of the higher mobility associated with electrons in NMOS transistors.)

In a Dickson configuration, each NMOS transistor has its gate and source leads coupled together, with the result that Vgs = 0 VDC. The substrate or bulk potential Vbb is typically ground, or 0 VDC, to prevent the P-substrate, N-source/drain regions from becoming a current conducting forward-biased PN junction. The gate-source of M0 may be said to define the anode node for the string of rectifier stages, and the drain of M5 may be said to define the cathode node for the string of rectifier stages. In Figure 3B, the anode node is coupled to the low voltage power supply Vdd.

Each two-stage pump stage requires two-phase non-overlapping pulse trains, here denoted $\phi 1$, $\overline{\phi 1}$, which are provided by phase generator 150. By non-overlapping it is meant that 0 to 1, and 1 to 0 voltage transitions of one phase never overlap with transitions of the other phase, although duty cycle of the two phases is not critical. Thus, while these two-phase signals are denoted with complementary nomenclature, since they must not overlap they are not complementary in the usual sense of the word. As shown in Figure 3B, each waveform has a 0 to 1 voltage differential E1 that typically is equal to Vdd. Assume that Vdd = E1 = 3.3 VDC.

In Figure 3B, node A will see a potential of (Vdd-Vt), where Vt is the threshold voltage drop of M0, typically about 1 VDC for the NMOS transistors shown. Thus if Vdd $\approx$ 3.3 VDC, node A will see perhaps 2.3 VDC. This Vt drop will always be present because the gate potential (Vdd) can never be more positive than the source potential (Vdd) (since Vgs = 0). In stating that Vt $\approx$ 1 V, a simplifying assumption is made that no MOS body effect is present. In practice, Vt will likely be higher for transistor M1, and even higher for M2, 1.5 V perhaps, due to increasing body effect induced by higher pumped voltages with respect to ground potential. Thus, where Vt $\approx$ 1 V is assumed, it must be remembered that body effect contributions are not being fully accounted for.

The rising edge of waveform $\phi 1$ AC-couples through capacitor C1 to superimpose a positive transition of magnitude E1 (e.g., +3.3 VDC) upon the 2.3 VDC potential, raising node A to a peak voltage of +5.6 V. Node B will follow the potential at node A less a Vt drop of 1 VDC, and will see (5.6-1) = 4.6 VDC. However the positive-going transition of the $\overline{\phi 1}$ waveform AC-couples through capacitor C2 to initially superimpose an E1 = 3.3 V transition upon node B, increasing the peak node potential to (4.6+3.3) =

7.9 VDC. Node C will follow this potential, less a 1 VDC drop, which puts the peak node C potential at 6.9 VDC, or V_{Pm}. Thus, node C will be at about +6.9 VDC in this example. (In practice, body effect in the various transistors will reduce the output voltage seen by the load capacitor, C_{LOAD}.

In the configuration of Figure 3B, typically coupling capacitors C1 and C2 are in the 10-20 pF range, depending upon the driving current requirements and magnitude of load capacitor C_{LOAD}, which is typically in the 50 pF range.

Although the Dickson configuration of Figure 3B works, it is not very efficient because of the diode drop associated with each stage. More stages may be added to boost the output voltage even higher, but on a relative basis even coupling capacitors in the 2 pF to 10 pF range require not insubstantial IC chip area.

Other design approaches are known in the art. For example, U.S.patent no. 5,126,808 to Montalvo discloses a single-stage charge pump that can output 6V, but requires Vdd = 5 VDC to do so. A two-stage pump circuit shown in International Solid-State Circuits Conference Digest of Technical Papers, 1996 IEEE, Vol. 39, sect. 2, TP 2.6 is said to output $V_{Pm} \approx 5$ VDC from a Vdd = 3.3 VDC power source. Unfortunately, if Vdd drops to 2.4 VDC, V_{Pm} drops sufficiently low to require a drastically lengthened programming time. Even at 2.4 VDC Vdd, the theoretical output voltage V_{Pm} is 2Vdd or barely 4.8 VDC. While many of these prior art circuits attempt to improve efficiency by using native transistors (e.g., MOS devices whose Vt is less than about $\pm$0.2 VDC) to minimize Vt loss, such devices are relatively costlier to manufacture reliably.

It will be appreciated that to output a precise value of V_{Pm} requires that the phase generator output waveforms be precisely maintained. For example, the circuits disclosed in the Montalvo patent and in the TP 2.6 IEEE reference each require 8-phase pulse trains. The need for so many pulse trains arises because when the charge pump circuit in question delivers current to a load capacitor, the output voltage increases. But when current is not being output, the voltage across the load capacitor will reduce to the current consumed by the erased or programmed cells, and output voltage ripple will be seen.

Figure 3C depicts voltage waveforms for a prior art pump circuit such as that of Figure 3B. Waveform 1 evidences substantial AC-clock ripple and represents a very low output current state in which relatively large ripple and poor voltage regulation is seen. Waveform 2 shows a somewhat idealized output voltage V_{Pm}, which approaches the desired, ripple-free, value shown by the horizontal dashed line. However, improving voltage regulation and reducing the magnitude of the ripple, requires a substantial number, e.g., eight, of parallel pump circuits and an 8-phase pulse train generator. As a result, the period between adjacent phases is reduced, as is the time during which output current is not being delivered by a given pump. It will be appreciated from Figure 3C that there is really not much margin for error in that at best, the prior art circuit of Figure 3B barely meets specification.

Further complicating the charge pump design is the fact that the individual memory cells 10 are not perfect, and will have associated leakage currents. In practice, the magnitude of V_{Pm} will represent a ratio between the high output voltage the medium voltage pump circuit can generate, and ground, without leakage current. If the ratio is permitted to drop too low, programming and erasing

efficiency can be unacceptably low.

It is known in the art to cancel Vt for the series-coupled transistors in a pump circuit by breaking the gate-source connection at each transistor, and inserting an additional transistor in series between gate and source. One such technique is disclosed in U.S. patent no. 5,077,691 to Haddad et al., wherein a minimum of four phases must be used. But while eliminating Vt improves charge pump efficiency, unfortunately four non-overlapping phase signals, $\phi 1$, $\phi 2$, $\phi 3$, $\phi 4$, required by the Haddad et al. circuit add to the complexity of phase generator 150.

Understandably, as phase generator 150 design becomes more complex, additional IC chip area is required to implement the design. Further, as more phases are added, the maximum frequency of each phase signal is reduced. Further, the configuration of Figure 3A is likely too complex to economically implement Vt-cancellation. Even if a complex phase generator were implemented, the phase frequency typically varies as a function of Vdd magnitude, MOS and capacitor device process variations including Vt values, impedance values and capacitance values. Further, ambient operating temperature can also vary the operating frequency of the phase generator.

In summary, what is needed is a medium voltage high current pump circuit that can rapidly boost low voltage Vdd ($\approx$ +2.5 VDC) to about $V_{Pm} \approx$ +5 VDC at current levels sufficient to program a byte-block of memory cells, e.g., current in the 5 mA range. Preferably such output voltage should be sufficiently ripple-free to maintain program and erase efficiency. For ease of implementing the phase generator and to conserve IC chip area, preferably such medium voltage high current pump circuit should be implemented with as few as two phases, and should prefer-

ably include Vt-cancellation. Further, such circuit should function without using expensive native MOS devices. Finally, such circuit should provide a margin of at least 3 VDC and preferably about 5 VDC.

The present invention discloses such a medium voltage charge pump circuit.

SUMMARY OF THE PRESENT INVENTION

The present invention provides a two-phase medium high voltage generator circuit that preferably includes Vt-cancellation, and can be fabricated without native MOS devices. Rather than attempt to output a precision magnitude of V_{Pm} directly, the present invention uses the voltage generator circuit to provide a voltage $V_{Pm\ raw}$ voltage that may permissibly have several volts peak-to-peak ripple.

In one embodiment, the raw voltage is used to generate a low-current precision voltage (V_{Pm} + Vt), for example using a Zener diode and a MOS follower. This precision voltage is then used to provide power to data in buffer latches that are is coupled to the gates of source-follower MOS devices. The drain leads of the source followers are coupled to $V_{Pm\ raw}$, which as noted is a relatively unregulated higher voltage that may include ripple. It suffices if the highest positive ripple on $V_{Pm\ raw}$ does not breakdown MOS devices in the circuit, and providing the most negative ripple is not less than the desired V_{Pm} output voltage. The desired V_{Pm} output voltage is taken from the source of the source-follower MOS device and is coupled, preferably through byte select switches, to the group of cells to be programmed or erased.

An alternative embodiment is somewhat similar, except that the data in buffer latches are powered by the raw

voltage $V_{Pm\ raw}$. In this embodiment, source leads of the voltage followers are clamped to individual precision bias clamp circuits at a potential not exceeding V_{Pm}.

Either embodiment can output $V_{Pm} \approx +5$ VDC from Vdd $\approx$ 2.5 VDC at approximately 5 mA current levels, e.g., current levels sufficient to erase a block of 64 Kbits simultaneously, or to program up to 8 cells simultaneously.

The relatively unregulated $V_{Pm\ raw}$ voltage is provided by a charge pump circuit, preferably as disclosed in applicants' above-referenced pending U.S. patent application. Each stage in the charge pump circuit includes a plurality of series-connected charge multiplier or rectifier stages and comprises at least a MOS transistor and a charging capacitor. One of two non-overlapping phase signals is coupled to the free end of each charging capacitor such that adjacent charging capacitors are driven by different phases. Preferably NMOS devices are used, with the NMOS substrates coupled to Vdd to prevent substrate-source/drain current flow. Optionally, pre-charge circuitry pulls up the relatively unregulated drain voltage Vdd-Vtn to save charge time.

Preferably Vt cancellation is provided for each series-connected MOS transistor in the rectifier stages by connecting cross-coupled diodes implemented as charge-switching MOS transistors between the gate and source leads of the rectifying MOS. The gate and source of the first charge-switching MOS transistor and the drain of the second are AC-coupled through a separate charge capacitor to the complement of the non-phase signal that is AC coupled to the gate of the rectifying MOS. The gate and source of the second charge-switching MOS transistor and the drain of the first are coupled to the gate of the rectifying MOS transistor. Preferably the series-connected rectifying transistors and the charge-switching

transistors are all NMOS devices whose substrates are tied to a common substrate node.

Other features and advantages of the invention will appear from the following description in which the preferred embodiments have been set forth in detail, in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 depicts a conventional EPROM/EEPROM-type storage cell, according to the prior art;

FIGURE 2 depicts an IC including positive and negative high voltage pump circuits, a multi-phase generator, and an array of storage cells, according to the prior art;

FIGURE 3A depicts a Toshiba-type configuration for generating precise V_{Pm}, according to the prior art;

FIGURE 3B depicts a Dickson-type two-phase driven positive voltage pump circuit, according to the prior art;

FIGURE 3C depicts an idealized voltage output from the 8-phase configuration of Figure 3A, according to the prior art;

FIGURE 4A depicts an IC including a medium high voltage pump system according to the present invention and a less complex two-phase phase generator, in which more IC chip area is available for an expanded array of storage cells;

FIGURES 4B and 4C depict exemplary non-overlapping two-phase pulse trains $\phi 1$, $\phi 2$, such as may be used with the present invention;

FIGURE 5A is a generic block diagram of a two-phase medium high voltage pump system, according to a first

embodiment of the present invention;

FIGURE 5B is a generic block diagram of a two-phase medium high voltage pump system, according to a first embodiment of the present invention;

FIGURE 5C depicts raw and regulated voltage waveforms for the circuit of Figure 5A and Figure 5B;

FIGURE 6A-1 depicts a five-stage two-phase pump circuit with four-stage Vt cancellation, which circuit may be used as a positive/negative high voltage pump circuit 230 and/or as a medium high voltage pump circuit 247, according to the present invention;

FIGURE 6A-2 depicts a four-stage two-phase pump with Vt cancellation circuit that is preferred for use as medium high voltage pump circuit 247, according to the present invention;

FIGURE 6B depicts one charging stage and associated Vt-cancelling components from the circuit of Figures 6A-1 or 6A-2;

FIGURES 6C-6E depict typical phase waveforms for the circuit of Figures 6A-1 or 6A-2;

FIGURE 6F depicts voltage waveforms for the charging stage NMOS shown in Figure 6B before saturation, when the circuit of Figure 6A-1 is configured to output positive high voltage, or for the circuit of Figure 6A-2;

FIGURE 6G depicts voltage waveforms for the charging stage NMOS shown in Figure 6B after saturation, when the circuit of Figure 6A-1 is configured to output positive high voltage, or for the circuit of Figure 6A-2;

FIGURE 6H depicts the positive high voltage output by the circuit of Figures 6A-1 or 6A-2 for light and heavier capacitive loading;

FIGURE 7A depicts in detail capacitor node precharging/discharging and substrate protection in a circuit 230 and/or circuit 247, according to the present invention;

FIGURE 7B depicts a first embodiment of a three-transistor precharge/discharge circuit, such as preferably is used to discharge capacitor nodes and load capacitor load, according to the present invention;

FIGURE 7C depicts a second embodiment of a three-transistor precharge/discharge circuit that discharges trapped capacitor voltages to Vtp, according to the present invention;

FIGURE 8 depicts a four-stage two-phase NMOS pump circuit with full Vt-cancellation, with capacitor node precharging/discharging and substrate protection, suitable for use as circuit 230 and/or circuit 247, according to the present invention;

FIGURE 9A depicts a four-stage two-phase PMOS pump circuit with full Vt-cancellation for each stage, with capacitor node precharging/discharging and substrate protection, suitable for use as circuit 230 and/or circuit 247, according to the present invention;

FIGURE 9B depicts a preferred circuit for generating a VNWELL bias for the embodiment of Figure 9A, according to the present invention;

FIGURE 10 depicts the multi-well fabrication preferably used to implement NMOS pump devices, according to the

present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 4A depicts an IC 200 that includes a plurality of cells 10 that are arrayed in addressable rows and columns that define a storage array 210. Similar to what was described with respect to prior art Figure 2, address logic 220 permits accessing a specific cell in such an array. For ease of illustration, IC 200 is shown as including a single high voltage pump circuit 230 that can output positive high voltage or negative high voltage, depending upon whether a program/read or erase operation is to be undertaken. Such a dual-mode high voltage pump system was disclosed in applicants' said pending U.S. patent application. For purposes of the present invention, however, dual-mode circuit 230 could be replaced with prior art separate positive and negative high voltage circuits 130, 140 as shown in prior art Figure 1. So doing would require more than two-phase signals into the circuits generating V_{Pp} and V_{Pn}, however, and would use more IC chip area.

Figure 4A depicts the present invention, a two-phase medium high voltage pump system 245 that outputs V_{Pm}. Note too that phase generator 240 now outputs only two phases, $\phi 1$, $\phi 2$, to drive the positive/negative high voltage pump circuit 230.

For purposes of the present invention, e.g., medium high voltage pump system 245, the size of two-phase phase generator 240 is symbolically shown smaller than what was shown for the four-phase phase generator 150 of prior art Figure 2. Because applicants' system 245 can operate efficiently from two-phase drive signals, generator 240 advantageously may be less complex and can be fabricated on less IC chip area than if system 245 required four or eight or more phase signals. Note too that symbolically,

array 210 now includes more cells 10. Array 210 can be larger, or alternatively IC 200 can be smaller, because IC chip area is reduced because of the presence of two-phase system 245 and a preferably less complex phase generator 240.

Figures 4A and 4B depict generic non-overlapping two-phase pulse trains $\phi 1$, $\phi 2$, such as may be used to drive medium high voltage pump system 245. (These same two phases may also be used to drive positive/negative high voltage pump circuit 230, if such a dual-mode circuit is used.) Each of these pulse trains has a 0 to 1 amplitude differential of E1 volts, where E1 $\approx$ Vdd. In practice, Vdd may range from as low as about 1.2 VDC to 5 VDC or higher. Because more circuitry is designed to be battery operated, laptop computers for example, the trend is to operate ICs from as low a magnitude Vdd as is feasible, to reduce switching currents, and to extend battery life-time. Duty cycle of $\phi 1$, $\phi 2$ is relatively unimportant providing waveform transitions of one pulse train do not coincide with waveform transitions of the other pulse train. Further, the two pulse trains may have dissimilar duty cycles. In the preferred embodiment, the repetition rate frequency of each pulse train may range from about 10 MHz to 20 MHz or higher. This frequency range is twice as fast as what is permissible using the four-phase Haddad et al. configuration shown in Figure 3A.

Figures 5A and 5B discloses two preferred embodiments of medium high voltage pump system 245. In contrast to prior art approaches such as described in Figure 3A, system 245 does not attempt to directly generate a precisely controlled V_{Pm}. Instead, a raw high voltage generator comprising two-phase multi-stage pump 247 generates a raw V_{Pm}, which may be as high as perhaps +10 VDC and may include substantial ripple. This +10 VDC magnitude is substantially higher than the +5 VDC used in

prior art approaches, such as shown in Figure 3A.

Preferably pump 247 comprises four sub-stages, 234-1, 234-2, 234-3 and 234-4. Each of these stages is driven by a two-phase phase generator 240, which outputs non-overlapping pulse trains $\phi 1$ and $\phi 2$. Preferably pump 247 is implemented using circuits disclosed in applicants' referenced co-pending application. However, description of preferred circuitry will also be provided herein.

In the embodiments shown in Figures 5A and 5B, system 245 includes a voltage-follower stage 249, which comprises a plurality of preferably identical voltage followers, denoted MVF1, MVF2, ... MVF8. It will be appreciated that although description of the preferred embodiments is given with respect to a byte-wide operation, although more or less than 8 bits might be programmed or erased simultaneously.

In the preferred embodiments, the logical input to each voltage follower device is provided by an associated data in buffer latch, denoted DIB. Thus, DIB1 is coupled to the gate node of MVF1, DIB2 to MVF2, and so on. The "0" or "1" contents of each data in buffer latch store the pattern of the new byte data to be written into the associated memory cells. (For ease of illustration, logic connections to the data in buffer latches is not shown.)

In the embodiment of Figure 5A, the data input buffer latches receive operating voltage from precision bias generator 251, whereas in Figure 5B, these latches operate from $V_{Pm\ raw}$ potential from circuit 257. However, in Figure 5B, separate precision bias clamp circuits ("CLPs") are coupled to the source of the source follower devices. Thus, the positive most excursion of the output of device MVF1 is clamped by voltage clamp

CLP1 to a potential not exceeding V_{Pm}, the output of MVF2 is clamped by CLP2, and so on.

In Figure 5A, the magnitude of the generator 251 output preferably is 1 Vt ≥ V_{Pm}. Thus, if the desired level of V_{Pm} is +5 VDC, then generator 251 should output a minimum of +6 VDC, and preferably at least +6.5 VDC, to provide a greater margin to account for fabrication tolerances, Vdd tolerances, ambient temperature changes, and the like. Details are not provided for generator 251 in that there are many ways to generate a precision voltage from a raw voltage source $V_{Pm\ raw}$. For example, a 6.5 VDC zener diode could be coupled between ground and a constant current source, the zener diode node outputting $V_{Pm\ raw}$. Temperature compensation could be provided by generating this precision voltage using MOS devices as series-coupled diodes, or a precision voltage generator circuit could be used. In any event, the voltage tolerance on the output of precision bias generator 250 should be about ±500 mV at a current level of about 0.5 mA.

In the embodiment of Figure 5B, the various precision bias clamps could also be zener diodes, a series string of MOS diodes, voltage regulator and diode clamps, and the like. Preferably the tolerance on the clamped V_{Pm} voltage levels in Figure 5B is also about ±500 mV at about 0.5 mA.

In Figure 5A, by way of example, if the data in DIB1 is "1", the signal provided to the gate of MVF1 will be high, namely V_{Pm}+Vt. When the gate of MVF1 is V_{Pm}+Vt, then the drain node of associated cell device 10-1 is at V_{Pm}, which potential enables programming of the data stored in DIB1. But if DIB1 stores a "0", the buffer latch output it "0", the drain of cell 10-1 is ground and programming will not occur. As shown in Figure 5A, address logic 120 receives high operating potential V_{Pm}

$_{raw}$, as devices MYA1, MYA2, ... MYA8 and cells 10-1, 10-2, ... 10-8 require high voltage during program and erase mode operations. Operation in Figure 5B is somewhat similar except that the voltage output from MVF1, MVF2, ... MVF8 could exceed V_{Pm} (when the gate input to such transistors is high), but for the clamp presence of CLP1, CLP2, etc.

It will be appreciated from Figure 5A and Figure 5B that the highest positive magnitude of $V_{Pm\ raw}$ can be many voltage greater than the desired magnitude of V_{Pm}, as long as such raw positive voltage does not breakdown or damage MOS devices in pump 247 or in voltage followers 249. Similarly, the lowest (or negative most) magnitude of $V_{Pm\ raw}$ must be sufficiently positive to exceed the desired magnitude of V_{Pm}. Thus, there can be a volt or more of peak-to-peak ripple on $V_{Pm\ raw}$, without substantial adverse effect on the output voltage V_{Pm}.

Looking at Figure 5A, it is seen that the output voltages V_{Pm}, available from the source leads of MOS voltage followers MVF1, MVF2, ... MVF8 will be one Vt voltage drop less than the precision output of generator 251. Thus, V_{Pm} will be $(V_{Pm} + Vt) - Vt = V_{Pm}$. In Figure 5B, the action of the various clamps CLP1, CLP2, etc. will also ensure that the source lead potential at MVF1, MVF2, etc. cannot exceed V_{Pm}. In either embodiment, this output voltage preferably will be approximately +5 VDC at about 5 mA. This is sufficient voltage and current to reliably block erase a 64 KByte block of memory, or to program one byte of memory.

In Figures 5A and 5B, the various medium high voltage pump output nodes are coupled to switch transistors MYA1, MYA2, ... MYA8 in a bitline select circuit 251, that may be implemented as part of address logic 120 if desired. Circuit 251 selects eight addressed bitlines for coupling

to V_{Pm}. If a selected cell is to be programmed, e.g., cell 10-1 in cell array 110, then switch transistor MYA1 will be turned on by a logic signal from address logic 120 (or the equivalent). When MYA1 is turned on, the gate node of storage cell 10-1 is coupled to V_{Pm}. If cell 10-1 is not to be programmed, then the relevant bitline is not selected, and transistor MYA-1 will turn off, isolating cell 10-1 from the source of V_{Pm}. The cells shown in array 110 are the eight selected cells. These eight bitlines may be adjacent or in separate columns within the entire cell array 110, depending upon configuration of select circuitry 251.

Figure 5C graphically depicts the advantages of medium high voltage pump system 245 for the embodiments shown in Figures 5A or 5B. Trace 1 represents $V_{Pm\ raw}$, which is available at the output of pump circuit 247 and is provided to the drain leads of voltage follower devices MVF1 ... MVF8. Trace 2 represents the magnitude of V_{Pm} delivered to bitline select circuit transistors MYA1 ... MYA8, assuming that precision bias generator is, intentionally, outputting a conservative higher-than-needed voltage magnitude. The dashed line in Figure 5C depicts the minimum specification for V_{Pm}. It is seen that considerable ripple can be tolerated on the raw (larger magnitude) voltage before either breakdown or insufficient output voltage to meet the required V_{Pm} occurs. This is in stark contrast to prior art systems that require 8-phase phase generators 240 and tight control over the direct output voltage from their multi-phase pump stages.

Figure 6A-1, which is fully described in applicants' referenced co-pending patent application, shows a preferred embodiment of a two-phase positive/negative high voltage pumping circuit 230 that may be adapted for use as pump circuit 247 (see Figures 4A, 5A, 5B). As

described below, Vt cancellation is provided for each series-coupled NMOS transistor in the string of rectifier stages. NMOS transistors M1, M2, M3, M4 and M5 together with capacitors C1, C2, C3, C4, C5 comprise an N=5 stage pump circuit. However, when implemented as a pump circuit 247, a four-stage configuration will suffice, even when Vdd ≈ 2.5 VDC.

In Figure 6A-1, one of two non-overlapping phase signals $\phi 1$, $\phi 2$ is coupled to the free end of each charging capacitor such that adjacent charging capacitors are driven by different phases. The transition edges of the phase signals are AC-coupled through the capacitors and are peak-rectified by the associated MOS-device, which acts as a diode D that turns on when forward biased, and is otherwise off. The anode and cathode of a given MOS device diode are subjected to AC-coupled signals having different phases. The AC-coupled created voltage differential between a MOS device diode's anode and cathode will determine whether current flows. The diode biasing ensures current flow, if any, is unidirectional, such that voltage across the diode-capacitor nodes changes in a common direction, e.g., more positive. Any floating DC potential at the top lead of the capacitor will be coupled through the diode, subject to a Vt threshold drop (unless additional components are provided to cancel such drop). Because the peak voltage waveform on the various capacitors decays with time, it is advantageous to operate the various phase signals with a high repetition rate, perhaps 10 MHz to 20 MHz. Understandably, the faster the repetition rate, the less voltage decay before the arrival of the next voltage-enhancing transition edge on the associated phase signal.

More specifically, the circuit of Figure 6A-1 includes a plurality of series-connected rectifier or pump stages, each stage comprising a MOS transistor and a charging

capacitor, and also includes an input multiplexer MUX1 comprising M-MUX1A and M-MUX1B, and an output multiplexer MUX2 comprising M-MUX2A and M-MUX2B. Each multiplexer has nodes identified as nodes 1, 2 and 3. In the embodiment shown, all transistors are NMOS except for MUX transistors M_{MUX1B} and M_{MUX2B}. The use of NMOS transistors in the string of rectifier stages is advantageous in that hole mobility of PMOS transistors is substantially less than electron mobility in NMOS transistors. Whether the circuit shown in Figure 6A-1 outputs positive or negative high voltage is determined by the on/off state of the various MUX transistors, as described below.

The circuit of Figure 6A-1 further includes a Vt-cancellation pair of transistors MnA, MnB (that function as cross-coupled diodes to dynamically control the ultimate voltage differential between the drain and gate of associated transistor Mn to within |Vtn|), and associated capacitor CnA for each of devices M1, M2, M3 and M4, to boost voltage-multiplication efficiency. Typically, for a configuration having N stages of rectification, there will be (N-1) pairs of Vt-cancelling transistors, and (N-1) capacitors CnA that mainly function to generate voltage peaks employed in cancelling Vt of associated rectifier stage NMOS transistors. The value of these Vt-cancellation capacitors C1A ... C(N-1)A preferably will be in the few pF range, whereas charge pumping capacitors C1, C2, C3 ... CN will be about 10 pF. The channel width/length ("W/L") ratios for the Vt cancelling transistors, e.g., M1A, M1B, etc. will be about 30/1.2, whereas W/L for the charge pumping transistors in the rectification stage (e.g, M1, M2, ...MN) will be about 90/1.2.

Figure 6A-1 also depicts several nodes at which a symbolic switch denoted P/D is shown, whereat precharge/discharge circuits may be coupled to speed

circuit operation. The various MUX connections in Figure 6A-1 also provide substrate bias protection. The substrates of transistors M0 and well as all NMOS transistors in the rectifier string are coupled together to a common substrate node, shown as node 3, which is also the anode node for the series-coupled string of rectifier stages. Substrate-source/drain junction current flow is prevented by MUX-switching the substrates to Vdd when outputting positive high voltage (or MUX-switching to V_{Pn} when outputting negative high voltage.)

Naturally when used to implement medium voltage pump system 247, there is no need to output a negative voltage such as V_{Pn}. Thus, when used in system 245, nodes 1 and 3 in MUX1 are coupled together (e.g., MOS device M-MUX1B is turned on) and node 1 is coupled to Vdd. Within MUX2, nodes 2 and 3 are coupled together (device M-MUX2A is turned on), and $V_{Pm\ raw}$ is available from MUX2 node 2. (If used to generate negative high voltage V_{Pn}, the POS/NEG node 1 of MUX 1 would be grounded, nodes 2 and 3 in MUX1 would be coupled together (e.g., device M-MUX1A is turned on), nodes 1 and 2 in MUX2 would be coupled together (e.g., device M-MUX2B is turned on), and V_{Pn} would be output at MUX1 node 2.) Further, in positive voltage mode, transistors M-MUX1B and M-MUX2B preferably precharge the V_{Pp} node to Vdd-Vtn rather than ground, which significantly reduces charging time. During precharge, the gate voltage to transistor M-MUX1A is set to PRE = Vdd, and is ground otherwise. In this fashion, performance is enhanced, and no dedicated pull-up or pull-down transistors are required. (If the MUXes were configured to output negative high voltage, during precharge, the V_{Pn} node would be charged by transistors M-MUX1A and M-MUX1B would be charged to a PMOS Vtp.)

Several factors determine the number N of rectifying or pumping stages required to achieve a desired magnitude of

output high voltage. One factor is the magnitude of the low voltage power supply Vdd, which typically determines the voltage transition E1 associated with the phase signals. A large magnitude of E1 can reduce the number of required stages N. The number of stages N will increase as output load current and/or magnitude of C_{LOAD} increase. Increasing the magnitude of the individual capacitors C1, C2 ... CN+1 and to a lesser extent the magnitude of any Vt-cancellation capacitors C1A, C2A ... CNA can decrease N, but at the expense of devoting more IC chip area to fabricating larger capacitors. Increasing the frequency of the phase waveforms enhances pump efficiency and can decrease N. Further, the magnitude of the Vt threshold voltage associated with each rectification stage (unless Vt cancellation is provided) affects N in that larger uncancelled Vt voltage dictate a larger N.

The AC load current provided to C_{LOAD} will vary as a function of time, as a function of phase operating frequency, magnitude of C_{LOAD}, magnitude of capacitors used to implement the circuit, MOS fabrication process variations, ambient temperature, among other variables. However, scaled simulations predict that the preferred embodiment can deliver load current in the few mA range, e.g., perhaps 5 mA or more.

Figure 6A-2 depicts a preferred embodiment of pump circuit 247, in which four pump stages have been found sufficient to provide adequate $V_{Pm\ raw}$, even with Vdd ≈ 2.5 VDC. Circuit 247 in Figure 6A-2 is similar to what was depicted in Figure 6A-1. The MUX transistors have been eliminated since this circuit is dedicated to unipolar positive output. In essence, M-MUX1B is permanently "on" such that Vdd is permanently coupled to what was the POS/NEG input port in Figure 6A-1, and M-MUX1A is permanently "off", or simply omitted. M-MUX2B is permanently "off", or simply omitted, and M-MUX2A is

permanently "on", such that the output voltage from M5A is permanently coupled to the $V_{Pm\ raw}$ output port. In this embodiment, C_{LOAD} was about 50 pF, the various other capacitors were in the 10 pF to 20 pF range, and Vdd was 2.5 VDC. This four-stage two-phase circuit was adequate in SPICE (Simulation Program with Integrated Circuit Emphasis) simulation to ensure a V_{Pm} of 5 VDC at 5 mA for the configuration of Figure 5A or 5B.

More specifically, SPICE simulation analysis for Vdd = 2.5 V showed +3.9 VDC at the node defined by M1-C2, +6.4 VDC at the M3-C3 node, +8.9 VDC at the M4-C4 node, +11.4 VDC at the M5-C5 node. Thus, $V_{Pm\ raw}$ is conservatively over +10 VDC, even from Vdd = 2.5 VDC. In the SPICE simulations, the various capacitors (other than C_{LOAD}) were about 10 pF. Fabrication of the capacitors was assumed to be convention polysilicon level two over polysilicon level one with an oxide-nitride-oxide ("ONO") dielectric, or a level of polysilicon over a well having an oxide dielectric.

Figure 6B replicates one stage of Figure 6A-1 or 6A-2, showing one NMOS transistor (M1) and its associated cross-coupled diode Vt-cancelling transistors M1A, M1B, and capacitors C1, C1A, and C2. Figures 6C-6H depict voltage waveforms for various nodes of the circuit. In Figure 6B, the gate, source and node designations refer to the rectifying or charging transistor M1. As shown by Figures 6C and 6E, the two phase waveforms $\phi 1$, and $\phi 2$ (and their respective complements) are non-overlapping in that voltage waveform transitions do not coincide between the phases. It will be assumed that the 0 to 1 voltage peak of each waveform is E1 volts, and that E1 $\approx$ Vdd, where Vdd may have a magnitude between 1.2 VDC to about 5 VDC or higher. In the preferred embodiment, Vdd $\approx$ 2.5 VDC.

Referring to Figures 6B and 6F, before V_{Pp} saturation occurs, the waveforms in Figure 6F reflect that for one-half a charge pump cycle, high voltage charge will pass from source-to-drain in the rectification stage NMOS transistors. For the next-half pump cycle, the charge at the source will remain trapped, to await the next half-pump cycle.

The gate node is coupled to $\phi 1$, and on 0 to 1 $\phi 1$ transitions, the gate node voltage is raised higher than the drain node. As a result, charge can flow through diode M1B from the gate to the drain node until the gate node is Vtn more positive than the drain node. (At "steady state", $Q = C\Delta V/\Delta t = 0$, where Q is transferred charge, C is effective capacitance gate-to-source, and t is time.) As the gate node rises due to the positive $\phi 1$ transition, the source node falls due to the negative complement signal $\overline{\phi 1}$ transition. Thus, the gate of M1 is more positive than the drain, which is more positive than the source. As a result, M1 turns on and transfers charge from drain to source.

As the charge transfers, the drain voltage drops. This implies that charge is also transferred from gate to drain to maintain gate potential at least Vtn higher than drain potential, to ensure M1 can conduct high drain-source current. The gate, source and drain nodes of M1 will experience automatic charge flow until the source and drain voltages of M1 equalize. Stated differently, the described two-phase Vt-cancellation indeed results in zero voltage drop across the source and drain of transistor M1.

Note in Figure 6F that pre-saturation, the source node is pumped-up one Vdd (or E1) magnitude higher than the drain node, providing that capacitors C1, C2 are sufficiently large to accommodate 100% coupling. Thus, when the M1

drain node is pumped-up positively (e.g., by $\overline{\phi 2}$), the source node will be pumped sufficiently negatively (e.g., by $\overline{\phi 1}$) to dump charge from drain to source. This transfer is accomplished as the gate node voltage will have been pumped sufficiently high (e.g, by $\phi 1$) to fully pass the charge on the drain node to the source node.

During the next-half pumping cycle, when the drain is pulled negatively while the source is pulled positively, the gate voltage will turn-off pump transistor M1. With M1 now off, charge at capacitor C1 at the drain, and charge at capacitor C2 at the source are trapped or stored. However, on the next half-cycle, M1 turns on, and the storage charge results in a transfer from drain to source. The resultant drain-source current flow (i) pumps-up the voltage (V) across C2, e.g., $i = C2\Delta V/\Delta t$.

After a time period that typically is less than 1 ms, the output voltage V_{Pp} saturates in that it can go no more positive. The relevant waveforms for saturation mode are shown in Figure 6G.

As shown in Figure 6H, the voltage V_{Pp} appearing across the load capacitor will start out low, at Vdd-VtM0, where VtM0 is the source-drain threshold voltage drop for transistor M0, here assumed to be about 1 V. Thus, if Vdd is 2.5 VDC, the starting value for V_{Pp} will be about 1.5 VDC. As the circuit operates, V_{Pp} will increase with each charge cycle until after a time period, typically less than 1 ms, saturation occurs and the maximum output voltage is attained. For the N=5 stage configuration shown in Figure 6A, the maximum output voltage will be $\{(N \times Vdd - VtNM0) + (Vdd - VtNM5)\} \approx 12$ VDC, where $VtNM0 \approx 1$ V and where $VtNM5 \approx 2$ V (due to higher voltage-induced body effects). This relatively high output voltage results from the above-described Vt, with the sole VtN loss arising from the cathode-node NMOS transistor M5, which has

no Vt voltage cancellation. The two waveforms shown in Figure 6H reflect larger and smaller values of C_{LOAD}. The larger values of load capacitor provide better low pass filtering, and the V_{Pp} waveform is smoother. By contrast, smaller values of C_{LOAD} provide less filtering, as shown by the "spikier" waveform in Figure 6H.

As noted, Vt cancellation in the present invention is achieved with two-phase drive waveforms, as opposed to the four-phase waveforms required by prior art Figure 3C. The embodiment of Figures 6A-1 and 6A-2 use one pair of cross-coupled diodes implemented as parallel-coupled Vt-cancelling transistors per pump stage, whereas prior art Figure 3C used only a single Vt-cancelling transistor per pump stage. However whereas prior art Figure 3C required four-phases, the embodiment of Figure 6A can cancel Vt using only two-phases. Two-phase operation is cost-efficient in that design of phase generator 240 is simplified, and higher repetition rate operation is achieved as well. A higher repetition frequency for the non-overlapping two-phase phase signals implies that the various capacitances used for pump 247 (and indeed circuit 230 as well) could themselves be reduced somewhat, which further saves IC chip area.

Of course circuit 247 (and/or circuit 230) in Figure 6A-1 or 6A-2 could be implemented with other Vt-cancellation techniques, or indeed with no Vt-cancellation. Of course, eliminating Vt-cancellation would decrease voltage multiplication in that the number of stages N would have to be increased to compensate for the NxVt voltage drops that would be present.

Figure 7A depicts a four-stage Vt-compensated circuit similar to that of Figure 6A-2, in which precharging and substrate bias protection are shown (as well as an option to output positive or negative voltage). The

configuration of Figure 7A can output a positive voltage equal to about 5xVdd, or about +12.5 V for Vdd = 2.5 V. (In negative voltage mode, this circuit can output -12.5 V, again for Vdd = 2.5 V.) Similar to the description of Figure 6A-2, in positive-only mode, the multiplex devices may be replaced by short or open circuits, as required.

In Figure 7A, the capacitor nodes are identified as 0A, 1A, 2A, 3A, 4A, 1B, 2B, 3B and 4B. Preferably coupled to each of these nodes is the output terminal of a precharge/discharge circuit 250 such as shown in Figure 7B or a precharge/discharge circuit 270 such as shown in Figure 7C. Further, the output terminal of a circuit 250 or 270 is also coupled to the V_{Pp}/V_{Pn} output node to discharge the load capacitor.

As shown in Figure 7B, circuit 250 includes PMOS transistor M70 and NMOS transistors M72, M74. Inputs to circuit 250 are a precharge/discharge logic signal ("PD") at input port 252, and voltages V1 and V2 at ports 254, 256. Circuit 250 output an output signal at port 258 that is coupled to one of the capacitor nodes in Figure 7A, and outputs an N-well potential at port 260. The N-well potential is coupled to node 3 associated with transistor M4 in Figure 7A. Table 2 below depicts the logical functioning of precharge/discharge circuit 250.

TABLE 2

PD/V1/V2	Positive Voltage	Negative Voltage
Precharge	0 V / Vdd / Vdd	Vdd / 0V/ 0V
Discharge	0 V / Vdd / 0 V	0 V / Vdd / 0 V

For the configuration of Figure 7A, it is understood that preferably there will be nine circuits 250, e.g., one circuit for each of the nine nodes 0A, 1A ... 3B, 4B, and a tenth circuit to the output node, coupled to the load capacitor.

Referring to Table 2 and Figure 7B, during precharge for V_{Pp} generation, logic signal PD will be ground, and V1 and V2 will each be Vdd, whereas for V_{Pn} generation, PD will be Vdd, and V1 and V2 will each be ground. In positive mode, for example when outputting $V_{Pm\ raw}$ as circuit 247, the output signal from a circuit 250 will precharge the associated node, e.g., node 0A, to Vdd-Vtn before voltage pumping voltage. (If the circuit of Figure 7A is used in negative mode, the various circuits 250 will precharge their associated node to Vtp before pumping voltage.) It will be appreciated that such voltage presetting or precharging advantageously saves time in that the maximum peak output voltage will be attained in less time.

In discharge, for V_{Pp} or for V_{Pn} generation, PD and V2 will be ground, and V1 will be Vdd. Discharge operation is such that the output ports 258 of the various circuits 250 will discharge the potential at the associated node (e.g., node 0A, or node 1B, etc.) to ground, 0 V, when pump circuit 240 is inactive. Such discharging removes the positive or negative charge that would otherwise remain trapped in capacitors C0A, C1A, C2A, C3A, C4A, C1, C2, C3, and C4. Understandably, such trapped charges can create undesired high potential differences between nodes and peripheral circuitry, and can subject associated MOS devices to voltage breakdown.

An alternative precharge/discharge circuit 270 is shown in Figure 7C as including NMOS transistors M80 and M82, and PMOS transistor M84. Inputs to circuit 270 are first and second precharge/discharge logic signals ("PD1" and "PD2") at input ports 272, 274, and voltages V1 and V2 at ports 276, 278. Circuit 270 provides an output signal at port 280 that is coupled to one of the capacitor nodes in Figure 7A, and outputs N-well and P-well potentials at ports 282, 284. The N-well and P-well potentials are

coupled to the corresponding well nodes in Figure 7A. One advantage of the configuration of Figure 7C is that trapped positive or negative charges are discharged to Vtp rather than to ground (as was the case for the circuit of Figure 7B). Table 3 below depicts the logical functioning of precharge/discharge circuit 270.

TABLE 3

PD1/PD2/V1/V2	Positive Voltage	Negative Voltage
Precharge	0 V/ Vdd/ Vdd/ Vdd	0 V/ Vdd/ Vdd/ 0V
Discharge	Vdd/ 0 V/ 0 V/ 0 V	0 V/ 0 V/ Vdd/ 0 V

Similar to the above description of circuit 250, for the configuration of Figure 7A, it is understood that preferably there will be nine circuits 270, e.g., one circuit for each of the nine nodes 0A, 1A ... 3B, 4B, and a tenth circuit to discharge the load capacitor. Such precharging advantageously also used when the described pump circuits are used to output $V_{Pm\ raw}$.

It will be appreciated from the above descriptions that precharge/discharge circuit 250 or 270 advantageously can use input signals (e.g., PD, PD1, PD2, V1, V2) that are ground or at Vdd potential. As such, no boost circuitry is required to provide these input signals, which may be generated from ordinary logic associated with the system of Figure 4A, or may be generated elsewhere, off-chip for example. When discharging positive voltage, preferably the P-well is discharged before the voltage nodes are discharged. This discharge sequence avoids the problem of undesired forward current from P-well to N+ source/drain regions. Similarly, when discharging negative voltage, preferably the voltage nodes are discharged before the P-well.

Adding precharge/discharge circuits such as shown in Figures 7B, 7C to circuit 240 in Figure 7A, or to circuit 230 in Figure 6A can introduce some well-current diffi-

culties. In Figure 6A-1, for example, P-well potential to NMOS devices M0 ... M5 is accomplished through node 3 associated with M-MUX1A and M-MUX1B. When the circuit of Figure 6A-1 outputs V_{Pp}, P-well potential is presented by M-MUX1B, whose node 1 is coupled to Vdd. If precharge/discharge circuitry such as circuit 240 is used, source/drain nodes (in Figure 7A denoted 1B, 2B, 3B, 4B) will be precharged to Vdd-Vtn, which can permit forward current to flow from the P-well of the NMOS devices to the N+ source/drain regions. Although any such forward current would occur only at the start of pumping, such current can create a risk of MOS latch-up.

Such latch-up risk is reduced using circuit 290, whose configuration is depicted in Figure 8. In this configuration, P-well potential for NMOS devices M0 ... M4 is not directly coupled to node 3 (associated with M-MUX1A, M-MUX1B, but instead is coupled via transistor M6. In this embodiment, devices M0 - M4 preferably are fabricated within a common P-well. Precharge/discharge circuits are again coupled to each capacitor node, to the load capacitor, and preferably also to node 00 in Figure 8A.

Thus, in positive mode (e.g., when the circuit outputs V_{Pp} or $V_{Pm\ raw}$), the precharge/discharge circuit across node 00 is turned on, and NMOS M6 is turned off. This permits grounding the P-well while still permitting Vdd at node 1 of M-MUX1B to be applied to node 3 associated with M-MUX1A and M-MUX1B. If, for example, circuit 250 (Figure 7B) is used with circuit 290 (Figure 8), PD=ground, V1=Vdd, V2=Vdd will produce the desired positive voltage precharge condition (see Table 2).

(If the circuit of Figure 8 is used in negative mode, the gate of M6 is coupled to PRE=Vdd to discharge the P-well potential from POS/NEG potential via transistor M-MUX1B to ground. The M6 gate is then coupled to ground to

avoid voltage breakdown resulting from a too strong electric field across the associated gate oxide. The pump circuit 290 is then activated. Transistor M6 is on, as its associated node 3 becomes pumped toward a negative voltage, and as a result the common P-well is coupled to the node 3 potential, which avoids forward current flow. If the precharge/discharge circuit shown in Figure 7B is used, the precharge, negative mode voltage conditions will be PD=Vdd, V1 = V2 = ground (see Table 2). As seen from circuit 250 in Figure 7B, the voltages V1, V2 are isolated from the P-well potential.)

Figure 9A depicts a PMOS version of a pump circuit 300 that is somewhat similar to NMOS circuit 290, depicted in Figure 8. Preferably the PMOS transistors are fabricated in a common N-well which is coupled via transistor M5 to node 3, associated with MUX2 transistors M-MUX2A and M-MUX2B. This construction helps avoid forward current flow from the PMOS transistors' P+ source/drain regions to the N-well. The circuit of Figure 9A may be used to output $V_{Pm\ raw}$ as circuit 247, if the multiplexer transistors nodes are properly connected as earlier described, where Vdd is coupled to MUX1 node 1, and where the desired output higher raw voltage is available from MUX2 node 2. Of course, fewer stages could be utilized, and indeed four Vt-compensated pump stages have been found to output sufficiently high $V_{Pm\ raw}$, even from Vdd = +2.5 VDC.

Preferably the various capacitor voltage nodes in circuit 300, including the load capacitor node, are provided with precharge/discharge circuits such as described with respect to Figures 7B and 7C. Such precharge/discharge circuits, used with the embodiment of Figure 9A or other embodiments, can advantageously initially discharge voltage nodes to ground during negative mode operation. (It will be appreciated that 0 V is a more advantageous

starting point than is a potential of VtN.) Then, when the pump circuit actively pumps each node negatively, the precharge/discharge circuits can switch back to precharge bias conditions, which can substantially shorten the time needed for the pump circuit to reach maximum output potential.

A circuit 450 (shown in Figure 9B) outputs a VNWELL potential that is presented to the VNWELL port of circuit 300. NMOS transistor M5 can isolate this potential, however, from the preferably common N-well associated with the PMOS transistors in circuit 300.

In positive mode operation (which includes outputting $V_{Pm\ raw}$), node 3 (associated with MUX22 transistors M-MUX2A and M-MUX2B) will be pumped to positive high voltage V_{Pp}, and PMOS transistor M5 will be turned on. With M5 on, the N-well potential is coupled to node 3, which helps avoid forward current from the PMOS transistors' P+ source/drain regions to the preferably common N-well. When this is occurring, the gate of M6 is at ground, which turns-off M6, thus isolating the N-well from the VNWELL potential.

In negative mode operation, the POS/NEG node at the left side of Figure 9A is ground, and 0 V will be coupled via transistor M-MUX2B to node 3 on the right side of Figure 9A, associated with MUX2. Transistor M5 is now off, and the gate of M6 is coupled to Vdd, which turns-on M6, and couples VNWELL potential to the preferably common N-well. In terms of timing, preferably VNWELL causes Vdd to first be applied before 0 V is coupled to MUX2 node 3, to avoid forward current and device junction breakdown.

Figure 9B depicts a preferred embodiment of a switching circuit 450 for generating the VNWELL potential, referred to above. Referring back briefly to prior art Figure 3C,

it has been common practice to couple the N-well of PMOS devices to Vdd in negative high voltage pump circuits. However, when the P+ source/drain regions of the PMOS devices are pumped to negative high voltage the PN junction at the source/drain and well regions may breakdown due to the strong electric field.

Circuit 450 reduces such electric field problems by providing well potential in two steps. Initially during an inactive ("INACT") stage, the N-well of PMOS devices (e.g., those shown in Figure 9A) is coupled to Vdd, to avoid forward current from source/drain regions to the well. Pump circuit (e.g., circuit 300 in Figure 9A) is activated (e.g., complement of INACT), and in the second step, after a desired level of negative pumped potential is detected at the source/drain regions, the N-well is switched to ground. Grounding the N-well will now reduce electric fields between the junction of source/drain regions and the N-well, to minimize the risk of junction breakdown.

Circuit 450 also includes a bias generator, shown as 450, which here comprising devices M24, M25, M26, and also includes a logic element 470, comprising devices M27, M28, M29. The output from logic element 470 is buffered by a pair of inverters and is the VNWELL potential that is coupled to circuit 300 in Figure 9A.

In Figure 9B, when pump circuit 300 is inactive, the status signal INACT = Vdd, which charges the signal provided to the gate of transistor M28 to Vdd, turning off M28. But in charge pump active mode, INACT = ground, which discharges the gate potential of M28 to Vtp.

More specifically, circuit 450 includes a series-string of devices M20, and diode-coupled devices M21, M22, and M23. Collectively, M21, M22, M23 establish a potential

of 3xVpt, which when added to potential VDETECT, presents 3Vpt+VDETECT to the gate of M29. (VDETECT can correspond to a magnitude of detected PMOS P+ region source/drain voltage in circuit 300.) For example, if node 2B in Figure 9A is detected (VDETECT), when the voltage of this node decreases to about - 4.5 V, the gate voltage at M29 in Figure 9B will be about 0 V. This gate potential turns-on M29, which switches the output potential VNWELL from Vdd to ground. Bias generator 460 provides a bias voltage to the gate of M5, which bias voltage is used to adjust a trip point for circuit 450.

As noted, for reasons of higher mobility the use of NMOS devices is preferred to PMOS devices, yet it is important to avoid a substrate-source/drain current flow. Figure 10 depicts a portion of an IC 500 that includes a PMOS transistor 510 and an NMOS transistor 520, formed on a common P-substrate 12. NMOS transistor 520 is formed in an N-well 530A that contains a P-well 540. PMOS transistor 510 is formed within an N-well 530B that may be separate from N-well 530A (as shown), or indeed may be a portion of the same N-well 530A. NMOS transistor 520 has N+ source and drain regions 550S, 550D and a gate 560 overlying a thin oxide 24. PMOS transistor 510 has P+ source and drain regions 570S, 570D and a gate 580, also overlying a thin gate oxide 24. If desired, a positive/negative charge pump 230 may be fabricated using NMOS and PMOS transistors, in which the NMOS transistors have a double-well configuration as shown in Figure 10. In the present invention, a medium high voltage generator 247 may be similarly fabricated. In such fashion, substrate to drain/source current is avoided, when outputting $V_{Pm\ raw}$ or V_{Pp} (or when outputting V_{Pn}).

Modifications and variations may be made to the disclosed embodiments without departing from the subject and spirit of the invention as defined by the following claims.

WHAT IS CLAIMED IS:

1. A medium high voltage charge pump system operable from low voltage Vdd and outputting a higher magnitude controlled voltage V_{Pm}, comprising:

a raw high voltage generator including a number (N) of series-coupled charge pump stages that collectively define an anode node coupled to receive said Vdd, and a cathode node outputting a raw high voltage $V_{Pm\ raw}$ whose magnitude is at least said V_{Pm}, each of said stages coupled to receive one of two non-overlapping phase pulse train signals whose amplitude is E1, where E1 ≤ Vdd, such that adjacent said stages receive different ones of said phase pulse train signals;

wherein said pump stages multiply a said AC-coupled E1 amplitude signal to create a larger magnitude potential $V_{Pm\ raw}$ therefrom; and

a voltage follower having an input lead coupled to receive a lower current regulated reference voltage whose magnitude approximates said V_{Pm}, a power lead coupled to receive said $V_{Pm\ raw}$, and an output lead whereat a potential appears that follows said regulated reference voltage and is said V_{Pm}.

2. The medium high voltage charge pump system of claim 1, wherein each of said stages in said raw high voltage generator includes at least a charge pump device coupled to a first capacitor having a capacitor node adapted to receive and to AC-couple to said charge pump device one of said phase pulse train signals.

3. The medium high voltage charge pump system of claim 2, wherein at least one of said charge pump devices is selected from the group consisting of (a) a PMOS transistor, (b) an NMOS transistor, and (c) a diode.

4. The medium high voltage charge pump system of claim 1, wherein adjacent said stages in said series are

coupled to receive different ones of said phase pulse trains signals.

5. The medium high voltage charge pump system of claim 1, wherein said system includes a generator outputting said regulated reference voltage.

6. The medium high voltage charge pump system of claim 1, wherein said voltage follower includes a MOS device source follower, wherein said regulated reference voltage is coupled to a gate lead of said MOS device source follower, said $V_{Pm\ raw}$ potential is coupled to a drain lead of said MOS device source follower, and said V_{Pm} is output from a source lead of said MOS device source follower.

7. The medium high voltage charge pump system of claim 6, wherein:

said system includes a generator outputting said regulated reference voltage; and

said regulated reference voltage has a magnitude $V_{Pm}+Vt$, where Vt is a threshold voltage drop of said MOS device source follower.

8. The medium high voltage charge pump system of claim 1, further including a switching mechanism that precharges said output port to a potential approximating (Vdd-Vt), where Vt is a voltage equal to a MOS device threshold voltage.

9. The medium high voltage charge pump system of claim 1, wherein in said raw high voltage generator each said pump stage includes a MOS device coupled to a first capacitor having a capacitor node adapted to receive and to AC-couple to said MOS device one of said phase pulse train signals; and

wherein a substrate node of each said MOS device is

coupled to a first potential.

10. The medium high voltage charge pump system of claim 1, wherein in said raw high voltage generator each said pump stage includes a MOS device coupled to a first capacitor having a capacitor node adapted to receive and to AC-couple to said MOS device one of said phase pulse train signals; and

each said pump stages includes a mechanism for cancelling a Vt threshold drop otherwise present in each said MOS device such that when said MOS device is turned on, there is zero voltage loss from source to drain.

11. The medium high voltage charge pump system of claim 1, wherein said raw high voltage generator includes N=4 stages.

12. The medium high voltage charge pump system of claim 1, wherein said V_{Pm} is approximately +5 VDC.

13 The medium high voltage charge pump system of claim 1, wherein said V_{Pm} is approximately +5 VDC at a current level of at least 4 mA.

14. The medium high voltage charge pump system of claim 1, wherein said system is fabricated on a single integrated circuit chip.

15. The medium high voltage charge pump system of claim 5, wherein said system is fabricated on a single integrated circuit chip.

16. The medium high voltage charge pump system of claim 1, where N=4

17. The medium high voltage charge pump system of claim 1, further including a phase generator outputting

said two non-overlapping phase pulse train signals;

wherein said system is fabricated on a single integrated circuit.

18. A method of generating a medium high voltage of controlled magnitude V_{Pm} from a low voltage Vdd, comprising the following steps:

(a) generating a raw high voltage $V_{Pm\ raw}$ whose magnitude is at least said V_{Pm} by providing a number (N) of series-coupled charge pump stages that collectively define an anode node coupled to receive said Vdd, and a cathode node outputting said $V_{Pm\ raw}$, each of said stages coupled to receive one of two non-overlapping phase pulse train signals whose amplitude is E1, where E1 ≤ Vdd, such that adjacent said stages receive different ones of said phase pulse train signals;

(b) coupling said non-overlapping phase pulse train signals to said pump stages such that said pump stages multiply a said AC-coupled E1 amplitude signal to create a larger magnitude potential therefrom;

(c) providing a lower current regulated reference voltage whose magnitude approximate said V_{Pm};

(d) providing a voltage follower having an input lead coupled to receive said lower current regulated reference voltage, having a power lead coupled to receive said $V_{Pm\ raw}$, and an output lead whereat a potential appears that follows said regulated reference voltage and is said V_{Pm}.

19. The method of claim 18, wherein:

step (a) includes implementing each of said pump stages with a MOS device and an associated capacitor; and said method further includes:

(a-1) providing for at least (N-1) of the MOS devices a threshold voltage cancelling mechanism such that when turned on, said (N-1) MOS devices do not exhibit a

threshold voltage loss between source and drain.

20. The method of claim 18, wherein step (c) includes generating said lower current regulated reference voltage from said $V_{Pm\ raw}$, and wherein step (d) includes providing a MOS source follower as said voltage follower, wherein said input lead is a gate lead, said power lead is a drain lead, said output lead is a source lead of said MOS source follower.

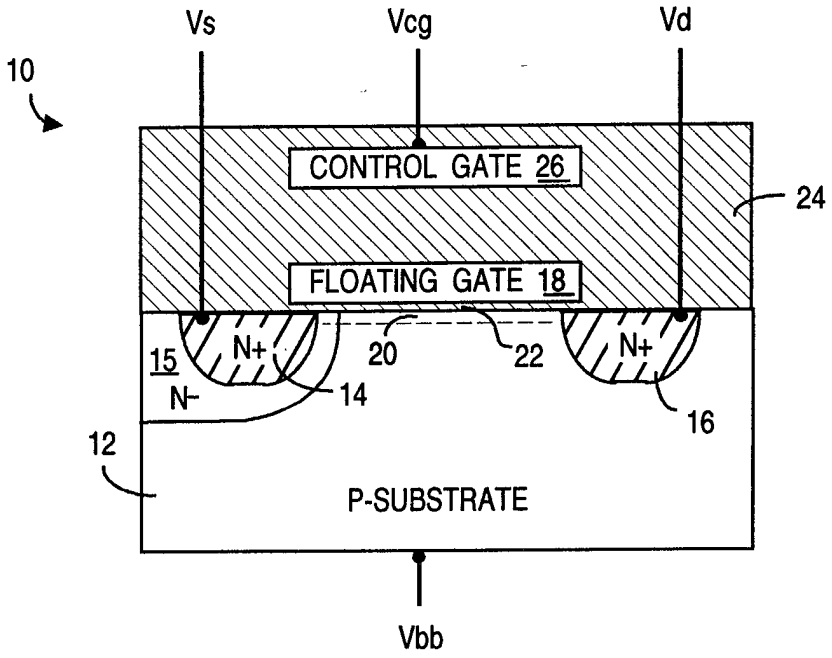

FIGURE 1 (PRIOR ART)

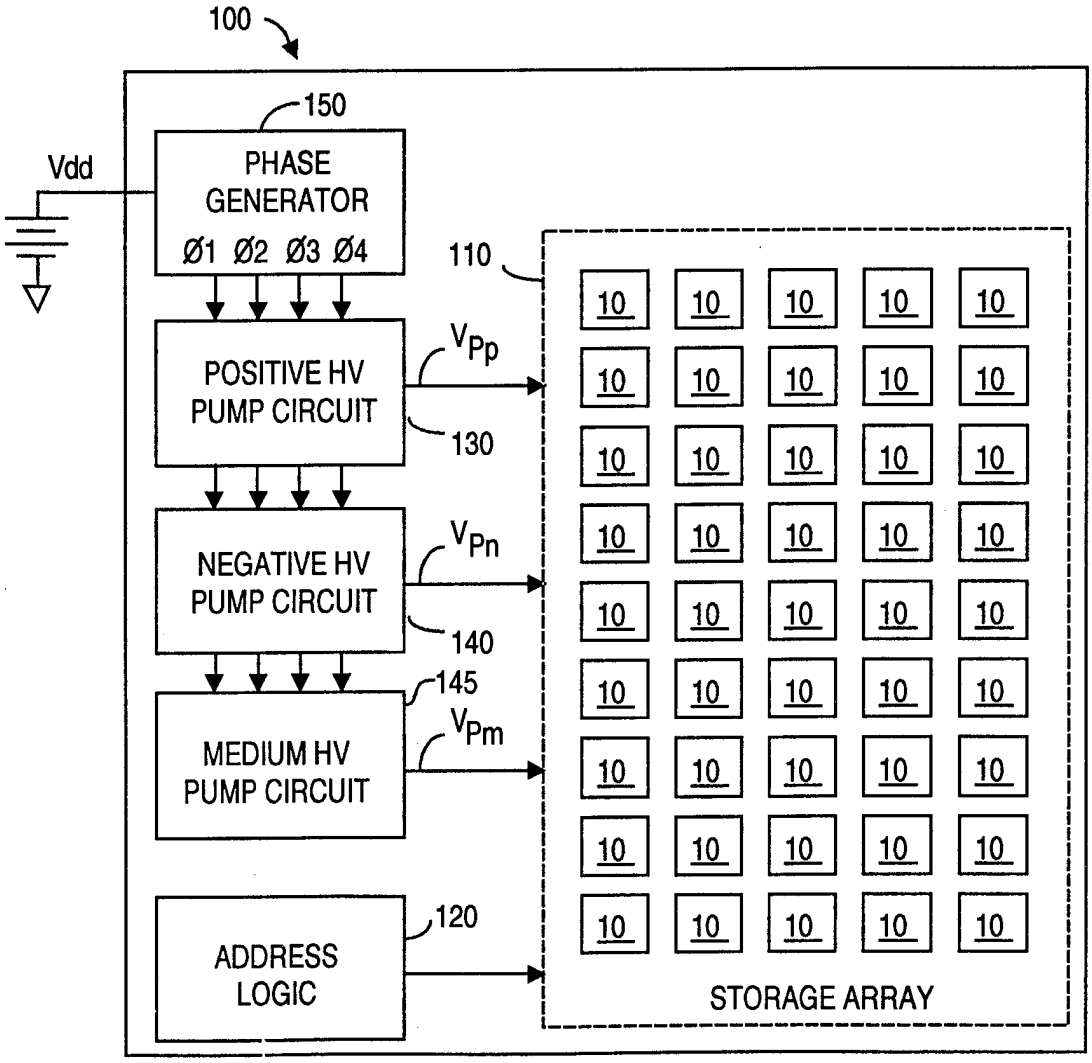

FIGURE 2 (PRIOR ART)

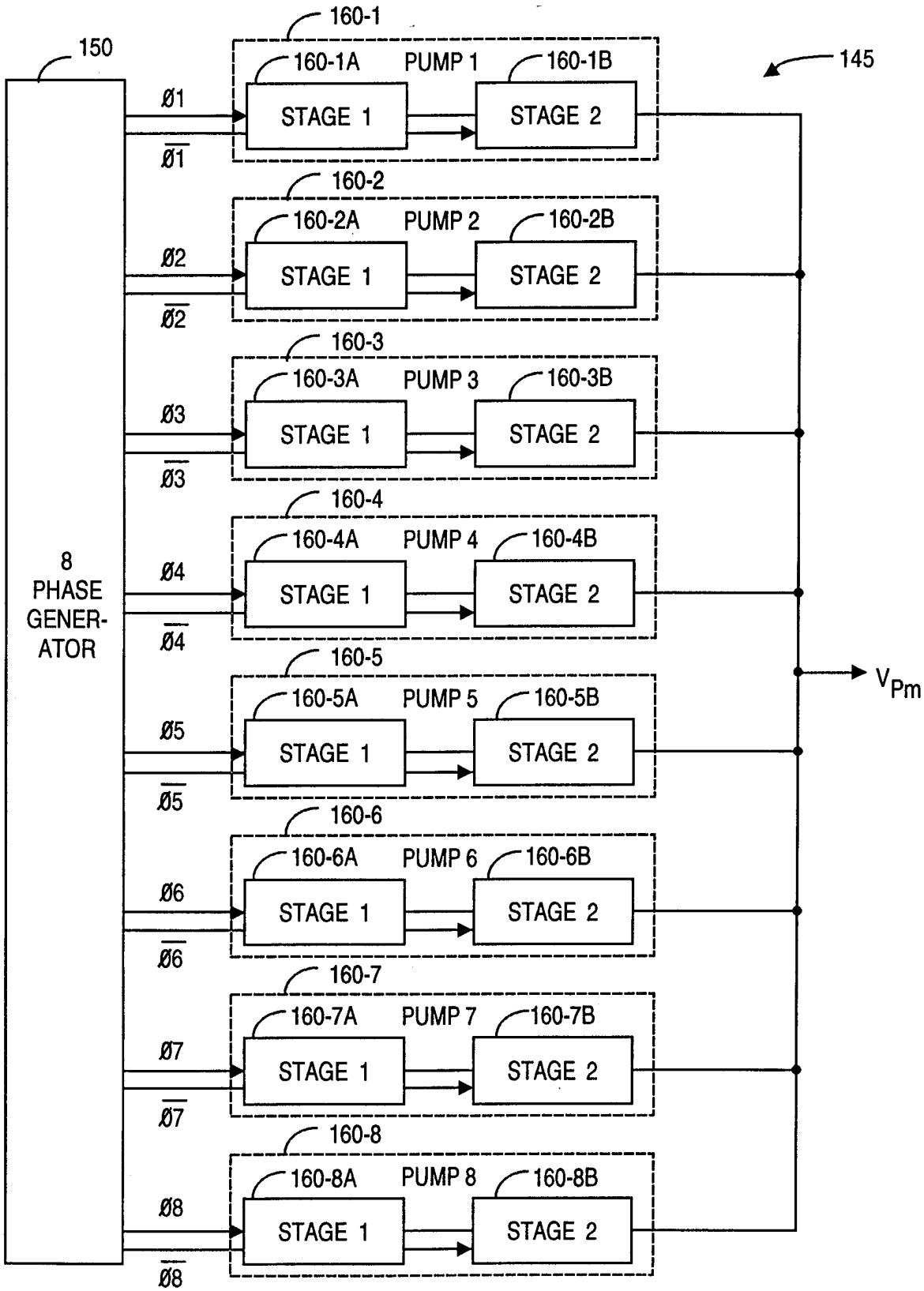

FIGURE 3A (PRIOR ART)

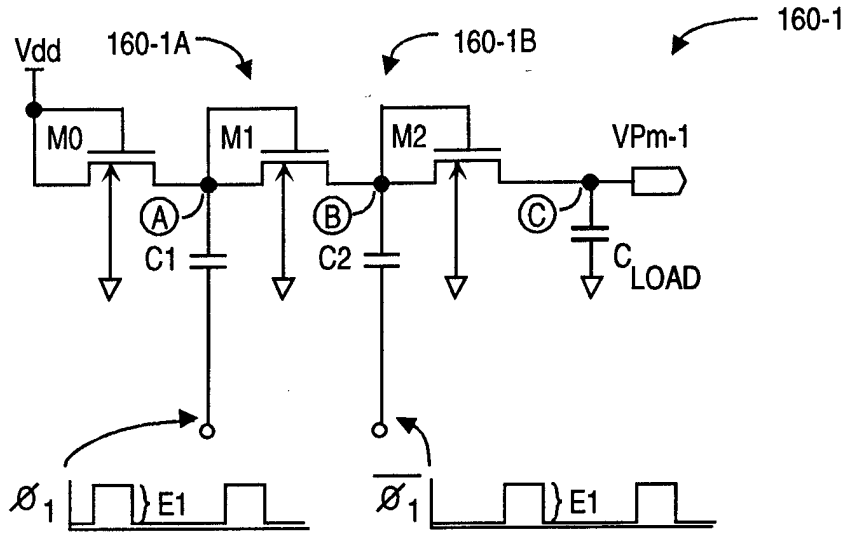

FIGURE 3B (PRIOR ART)

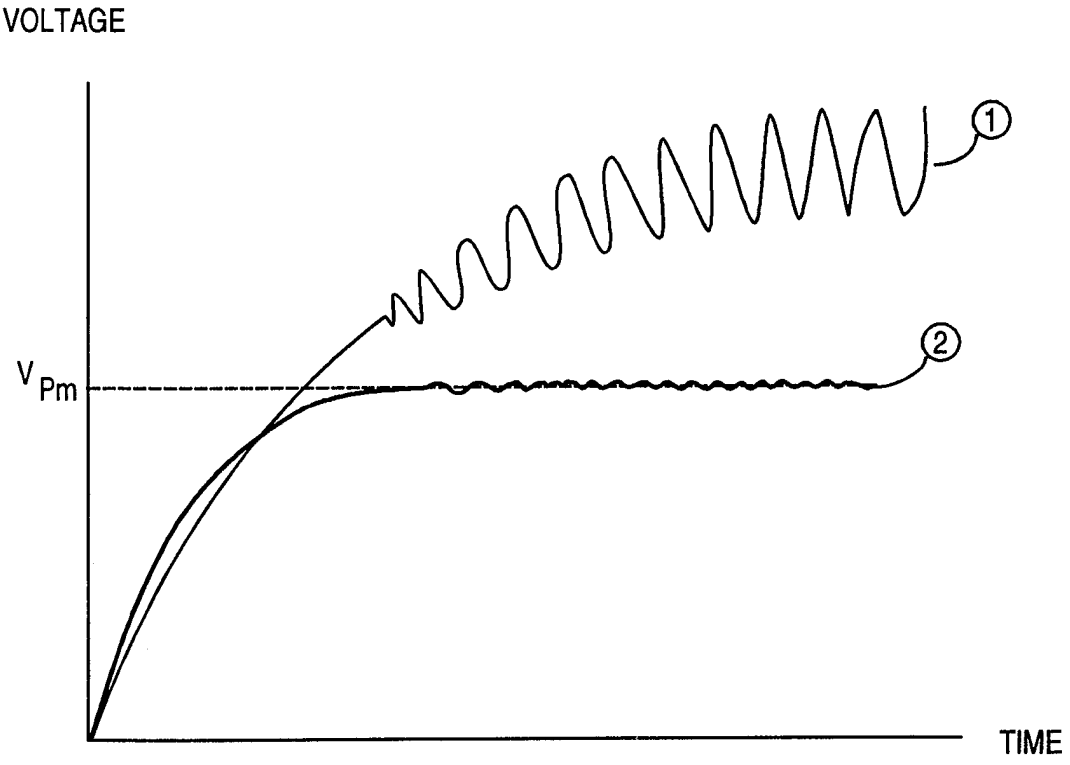

FIGURE 3C (PRIOR ART)

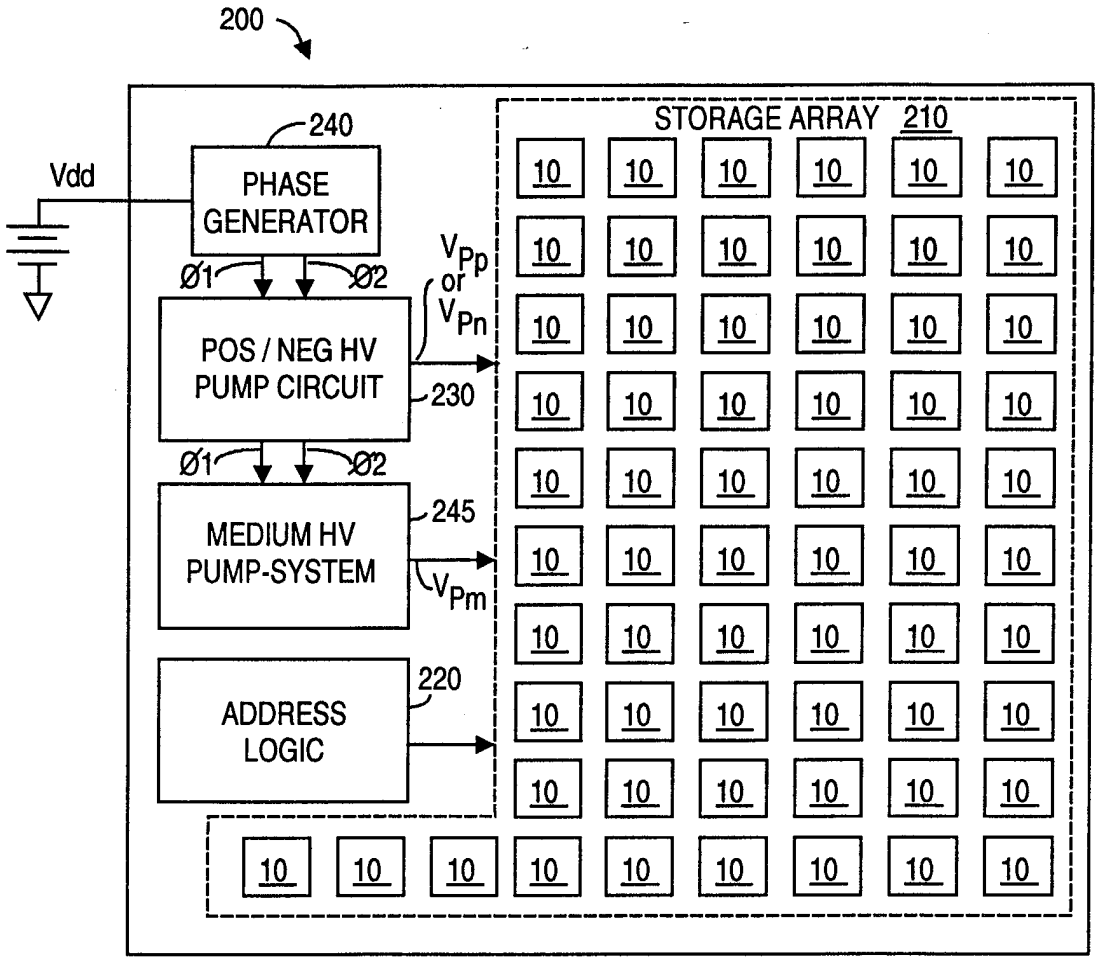

FIGURE 4A

FIGURE 4B

FIGURE 4C

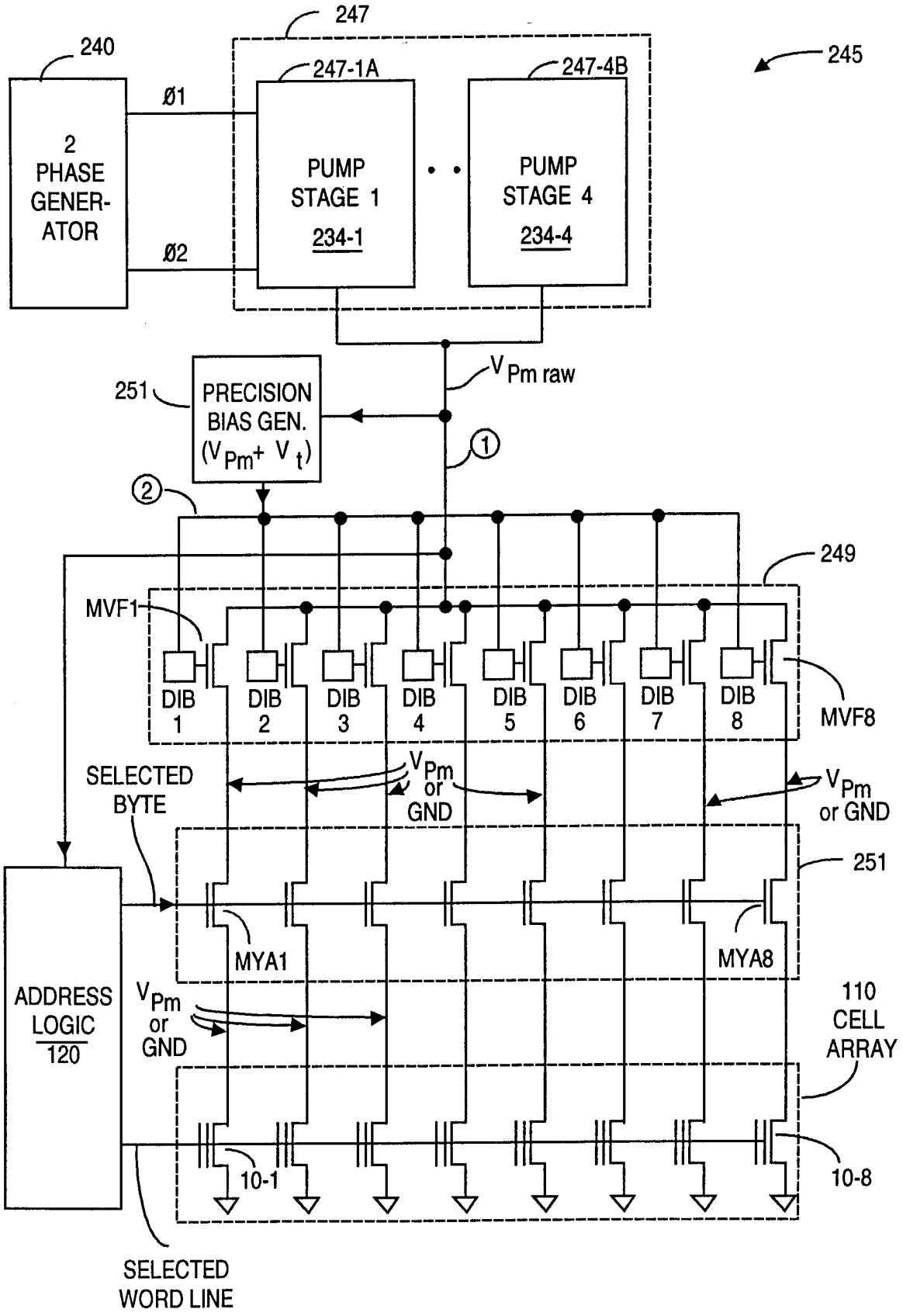
247
240
245
247-1A
247-4B
Ø1
2 PHASE GENER-ATOR
PUMP STAGE 1
234-1
PUMP STAGE 4
234-4
Ø2
V Pm raw
251
PRECISION BIAS GEN. (V Pm+ V t)
1
2
249
MVF1
DIB 1
DIB 2
DIB 3
DIB 4
DIB 5
DIB 6
DIB 7
DIB 8
MVF8
SELECTED BYTE
V Pm or GND
V Pm or GND
251
MYA1
MYA8
ADDRESS LOGIC 120
V Pm or GND
110 CELL ARRAY
10-1
10-8
SELECTED WORD LINE

FIGURE 5A

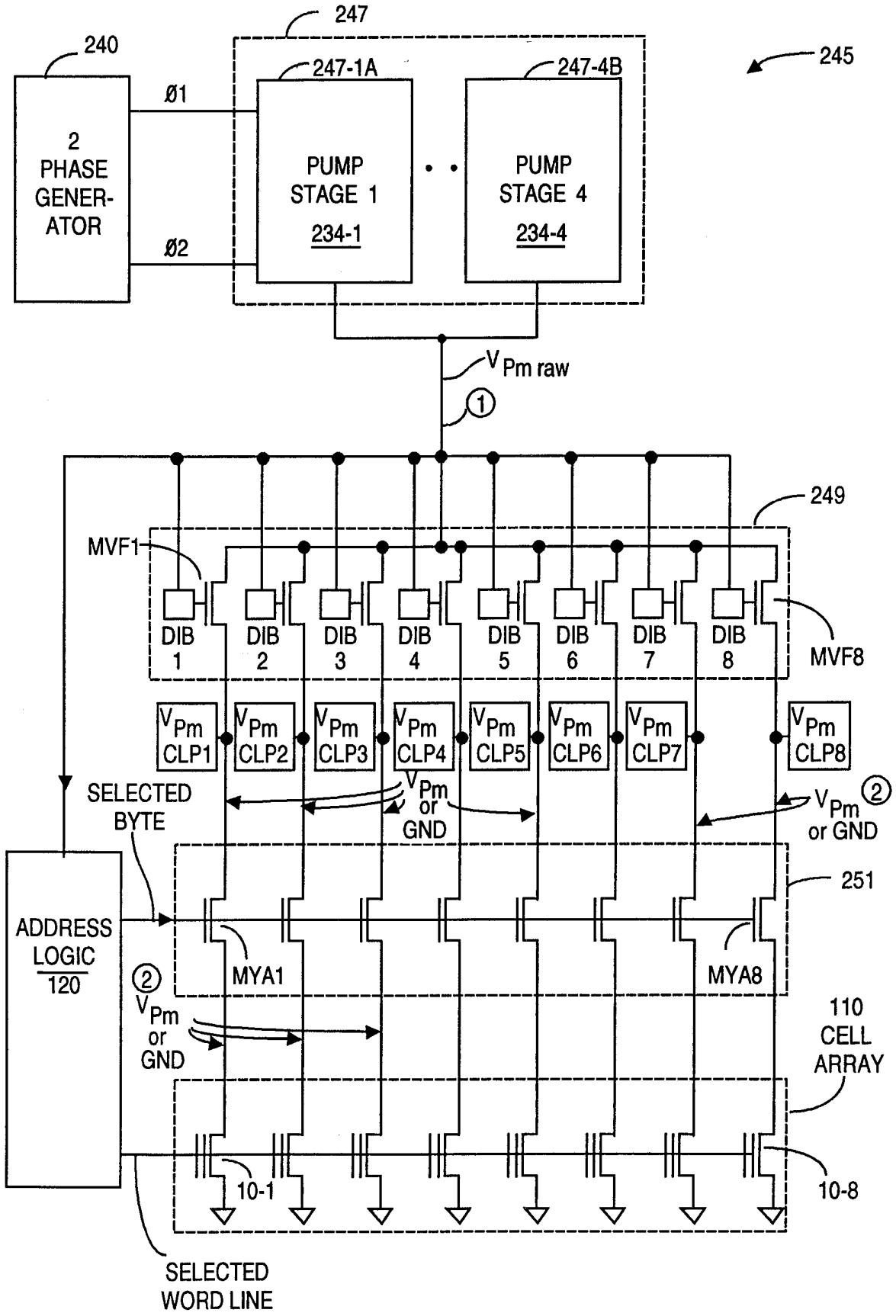
247
240
247-1A
247-4B
245
Ø1
2
PHASE
GENER-
ATOR
PUMP
STAGE 1
234-1
PUMP
STAGE 4
234-4
Ø2
V Pm raw
1
249
MVF1
DIB 1
DIB 2
DIB 3
DIB 4
DIB 5
DIB 6
DIB 7
DIB 8
MVF8
V Pm CLP1
V Pm CLP2
V Pm CLP3
V Pm CLP4
V Pm CLP5
V Pm CLP6
V Pm CLP7
V Pm CLP8
SELECTED BYTE
V Pm or GND
2
V Pm or GND
251
ADDRESS LOGIC 120
MYA1
MYA8
2
V Pm or GND
110 CELL ARRAY
10-1
10-8
SELECTED WORD LINE

FIGURE 5B

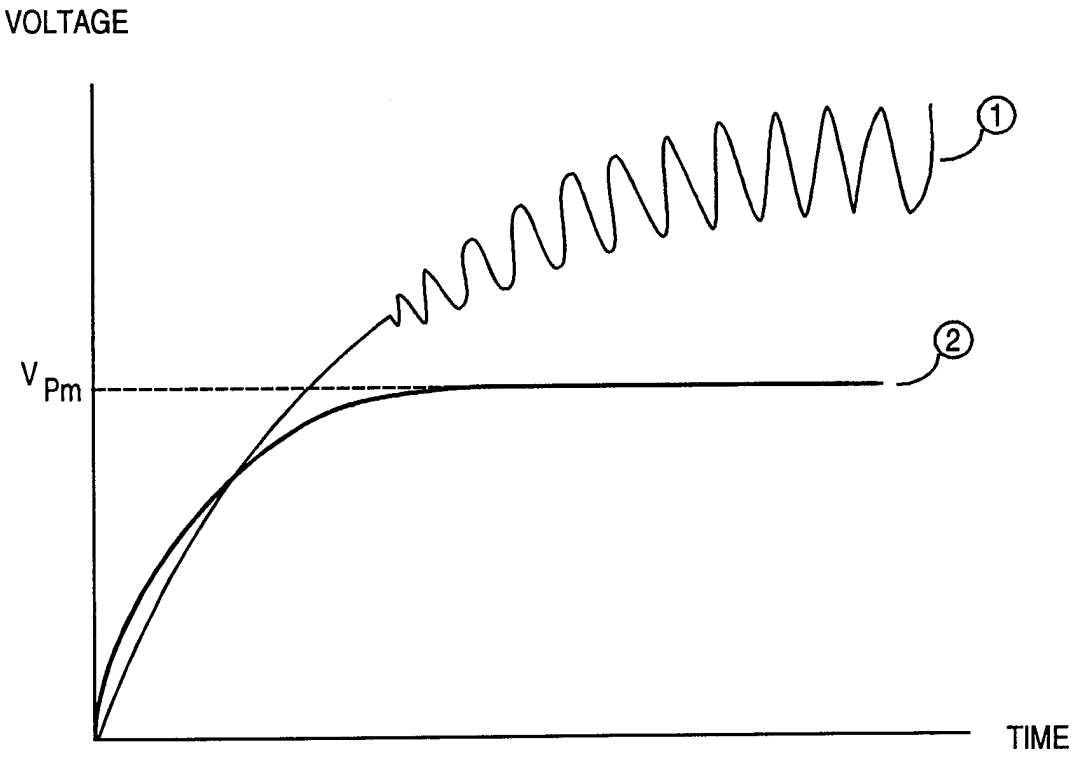

FIGURE 5C

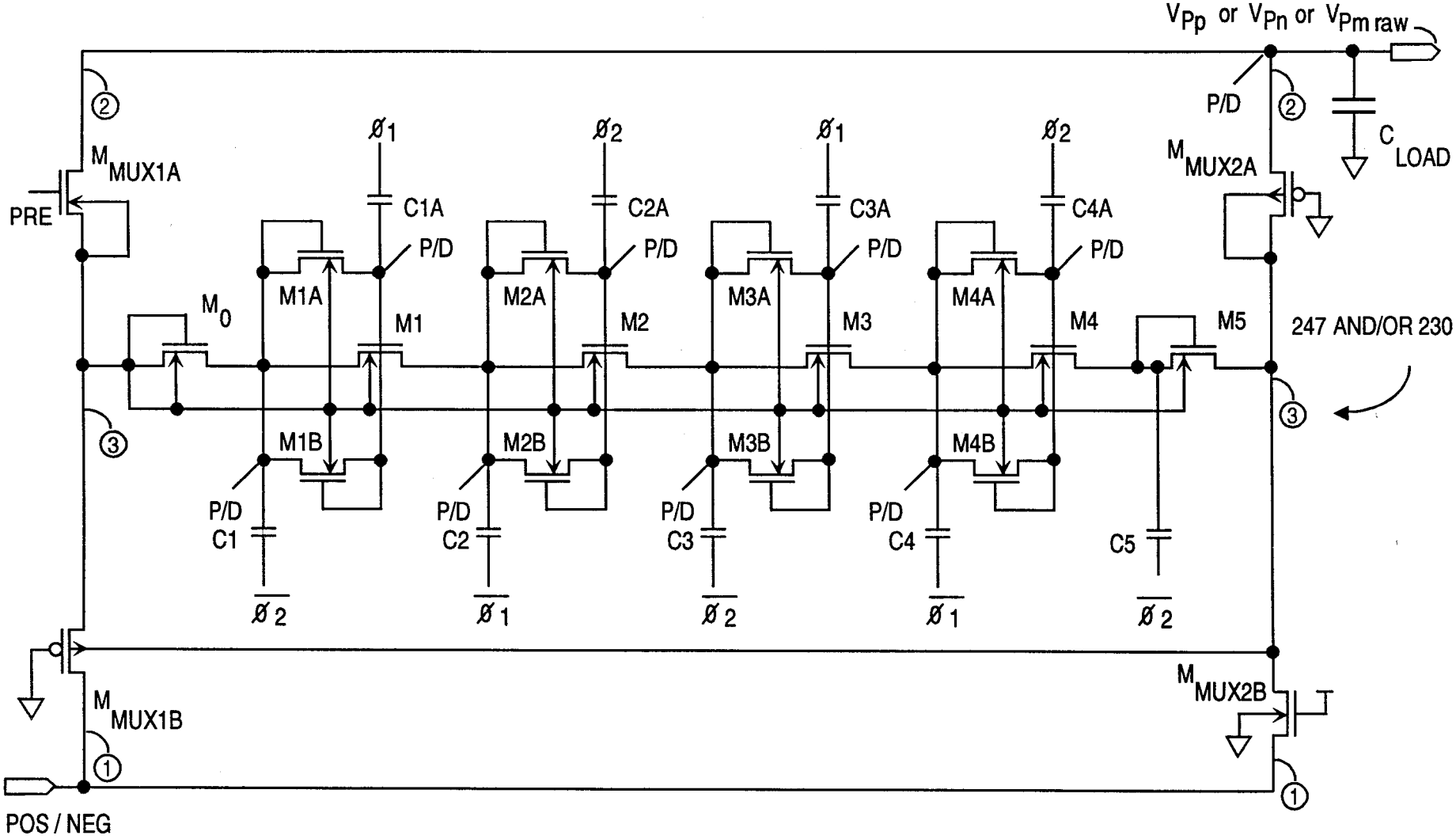
V_{Pp} or V_{Pn} or V_{Pm} raw
P/D
C LOAD
M_{MUX2A}
M_{MUX1A}
PRE
M_0
M1A
M1
M2A
M2
M3A
M3
M4A
M4
M5
C1A
C2A
C3A
C4A
M1B
M2B
M3B
M4B
C1
C2
C3
C4
C5
247 AND/OR 230
M_{MUX1B}
M_{MUX2B}
POS / NEG

FIGURE 6A-1

Vdd
M1A
M1B
M1
C1A
P/D
Ø1
C2
P/D
Ø1
M2A
M2B
M2
C2A
P/D
Ø2
C3
P/D
Ø2
M3A
M3B
M3
C3A
P/D
Ø1
C4
P/D
Ø1
M4A
M4B
M4
C4A
P/D
Ø2
C5
P/D
Ø2
M5A
M5B
M5
C5A
P/D
Ø1
C LOAD
V Pm raw OUT
247

FIGURE 6A-2

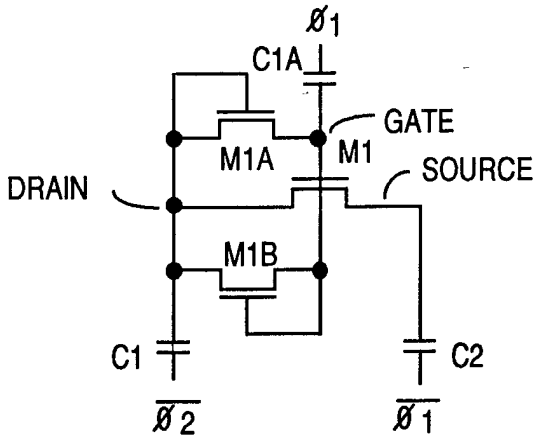

FIGURE 6B

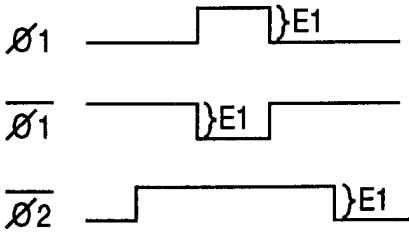

FIGURE 6C

FIGURE 6D

FIGURE 6E

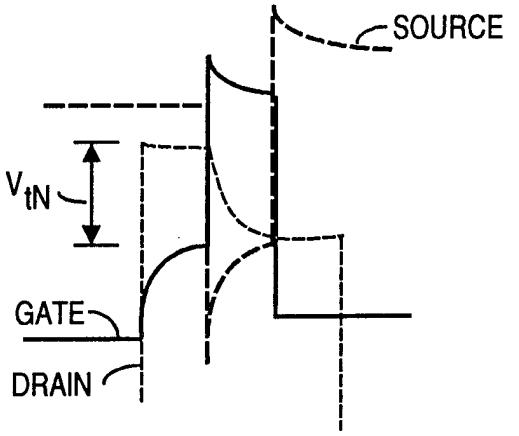

FIGURE 6F

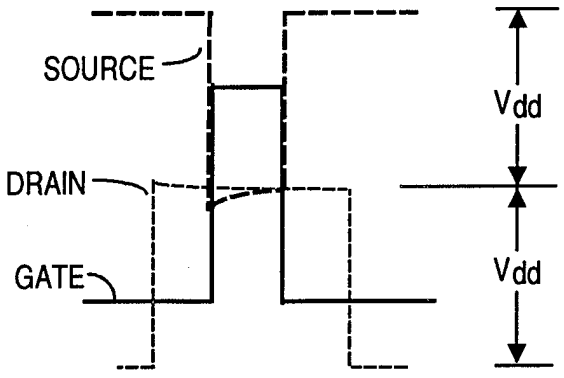

FIGURE 6G

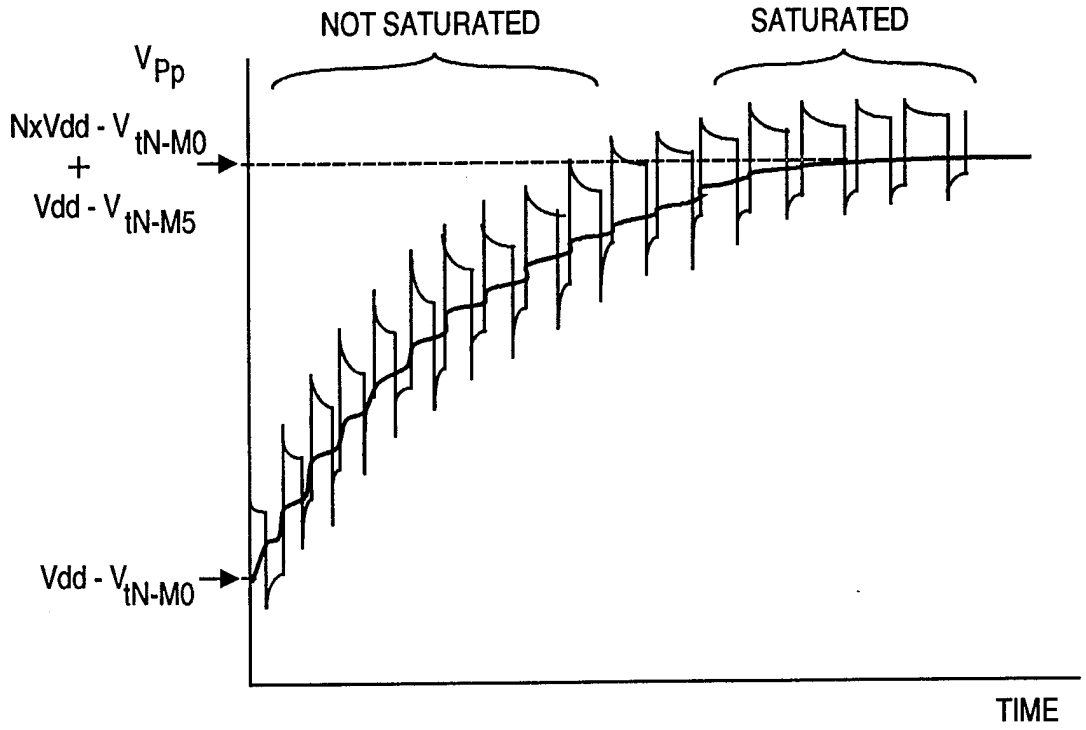
NOT SATURATED
SATURATED
V_{Pp}
NxVdd - V_{tN-M0}
+
Vdd - V_{tN-M5}
Vdd - V_{tN-M0}
TIME

FIGURE 6H

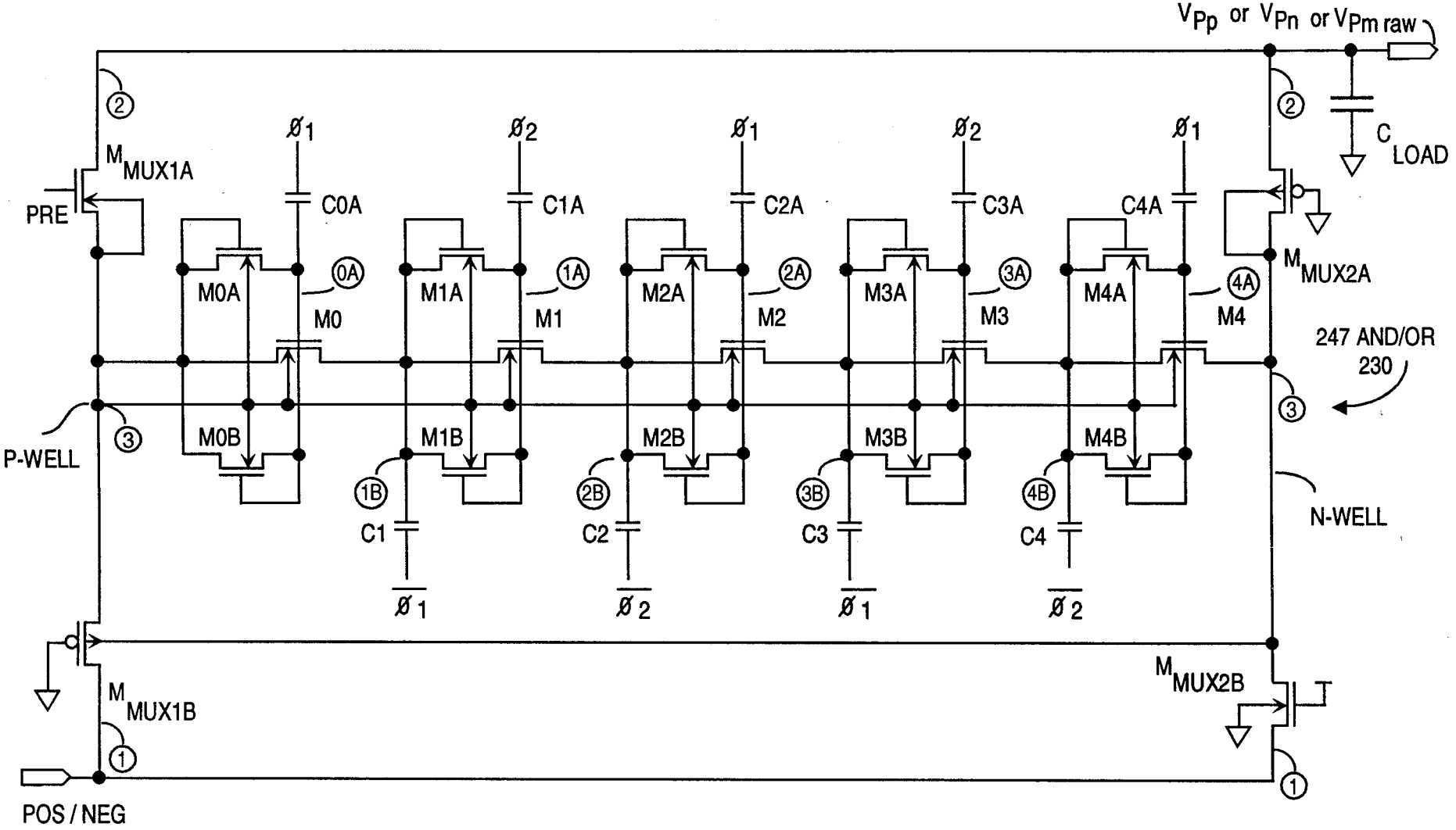
V_{Pp} or V_{Pn} or V_{Pm} raw
C_{LOAD}
M_{MUX1A}
PRE
M_{MUX2A}
M_{MUX1B}
M_{MUX2B}
Ø1
Ø2
C0A
C1A
C2A
C3A
C4A
M0A
M1A
M2A
M3A
M4A
M0
M1
M2
M3
M4
0A
1A
2A
3A
4A
M0B
M1B
M2B
M3B
M4B
1B
2B
3B
4B
C1
C2
C3
C4
247 AND/OR 230
P-WELL
N-WELL
POS / NEG

FIGURE 7A

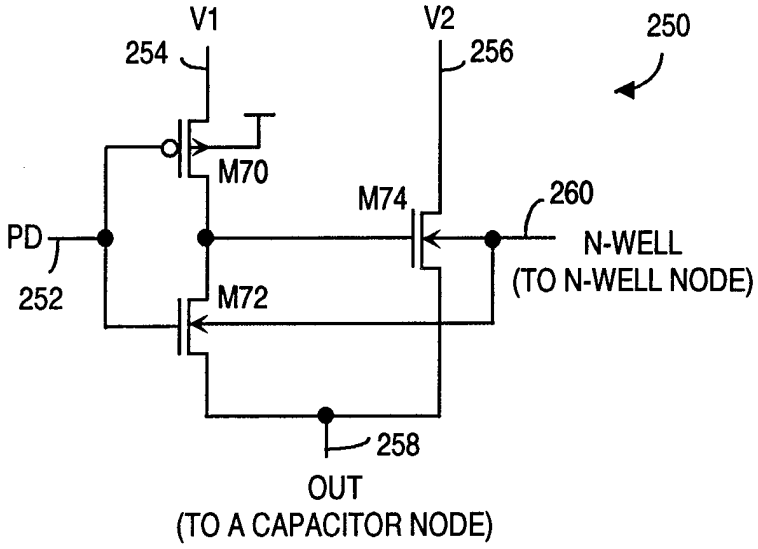

FIGURE 7B

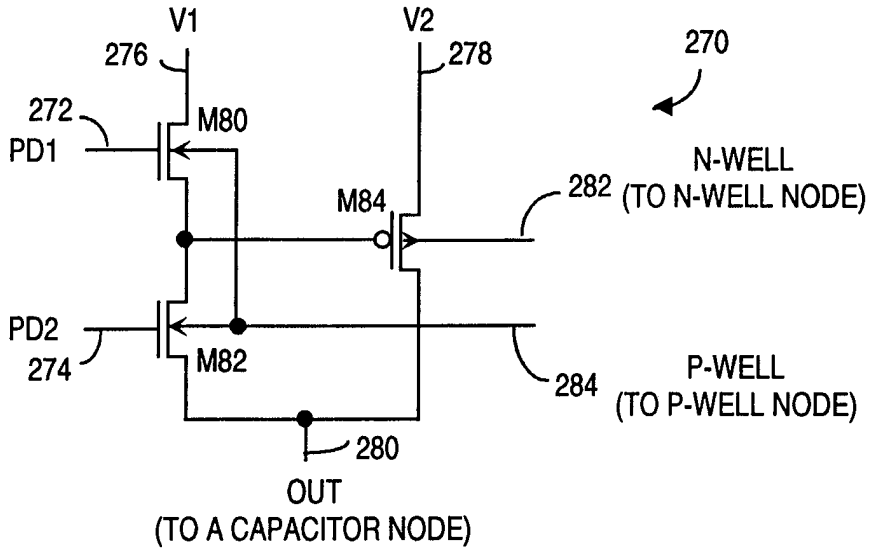

FIGURE 7C

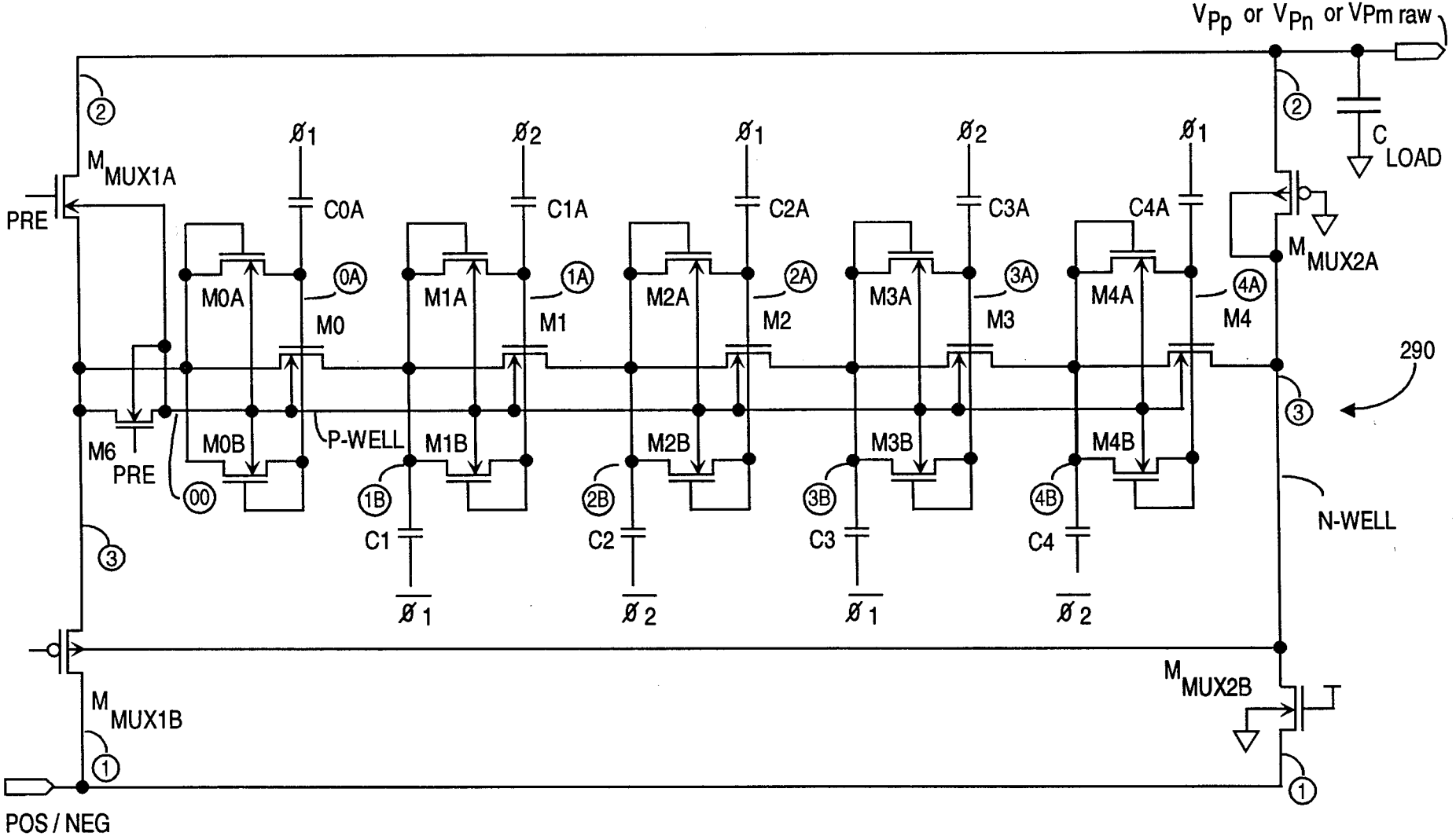
V_{Pp} or V_{Pn} or VPm raw
C LOAD
M_{MUX1A}
M_{MUX2A}
M_{MUX1B}
M_{MUX2B}
PRE
M6 PRE
C0A
C1A
C2A
C3A
C4A
M0A
M1A
M2A
M3A
M4A
M0
M1
M2
M3
M4
M0B
M1B
M2B
M3B
M4B
P-WELL
N-WELL
290
C1
C2
C3
C4
POS / NEG

FIGURE 8

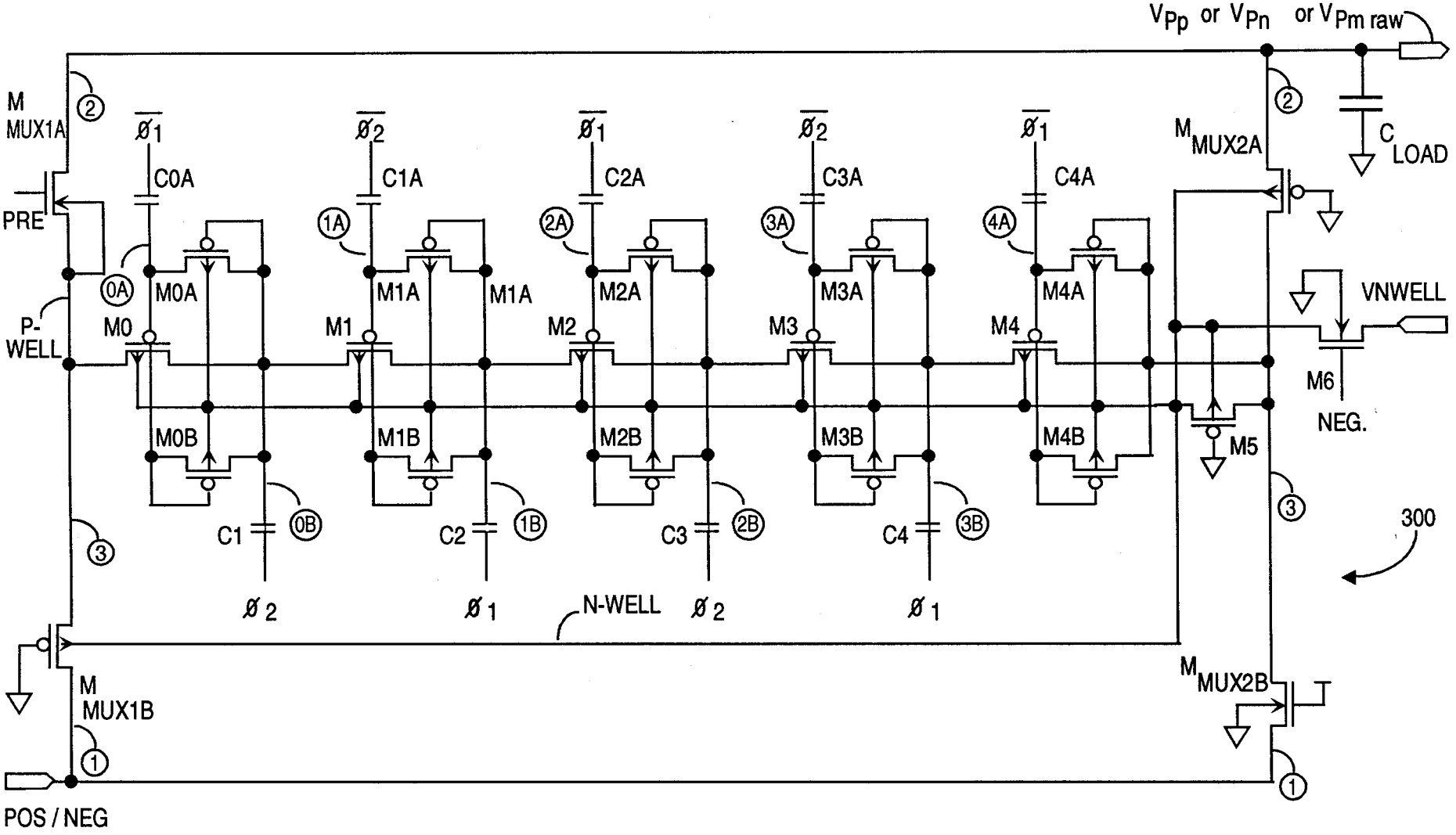
V_{Pp} or V_{Pn} or V_{Pm} raw
M MUX1A
PRE
P-WELL
POS / NEG
M MUX1B
C0A
C1A
C2A
C3A
C4A
M0A
M1A
M2A
M3A
M4A
M0B
M1B
M2B
M3B
M4B
M0
M1
M2
M3
M4
C1
C2
C3
C4
N-WELL
M_{MUX2A}
M_{MUX2B}
C LOAD
VNWELL
M6
NEG.
M5
300

FIGURE 9A

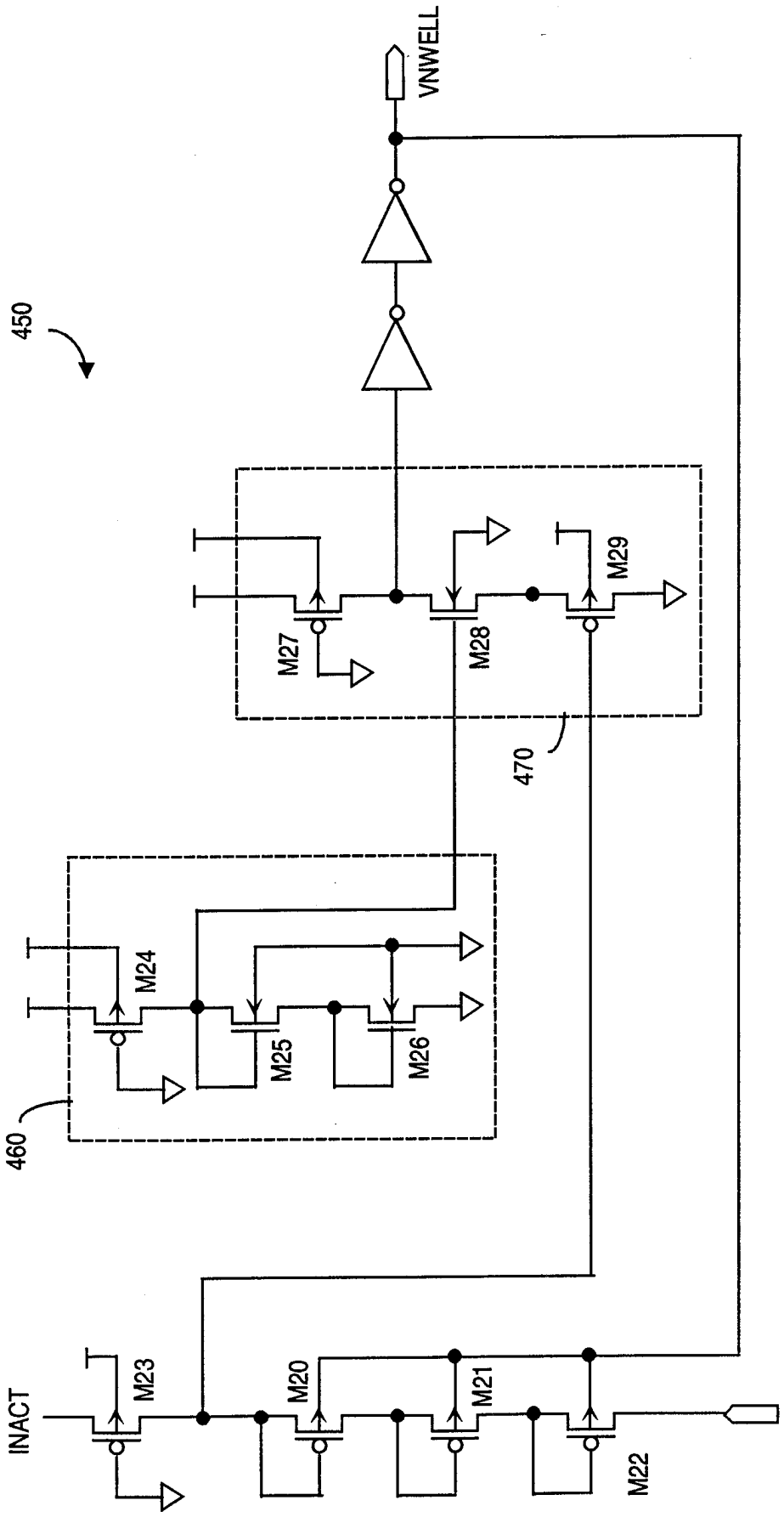
VNWELL
450
M29
M27
M28
470
M24
M25
M26
460
INACT
M23
M20
M21
M22
VDETECT

FIGURE 9B

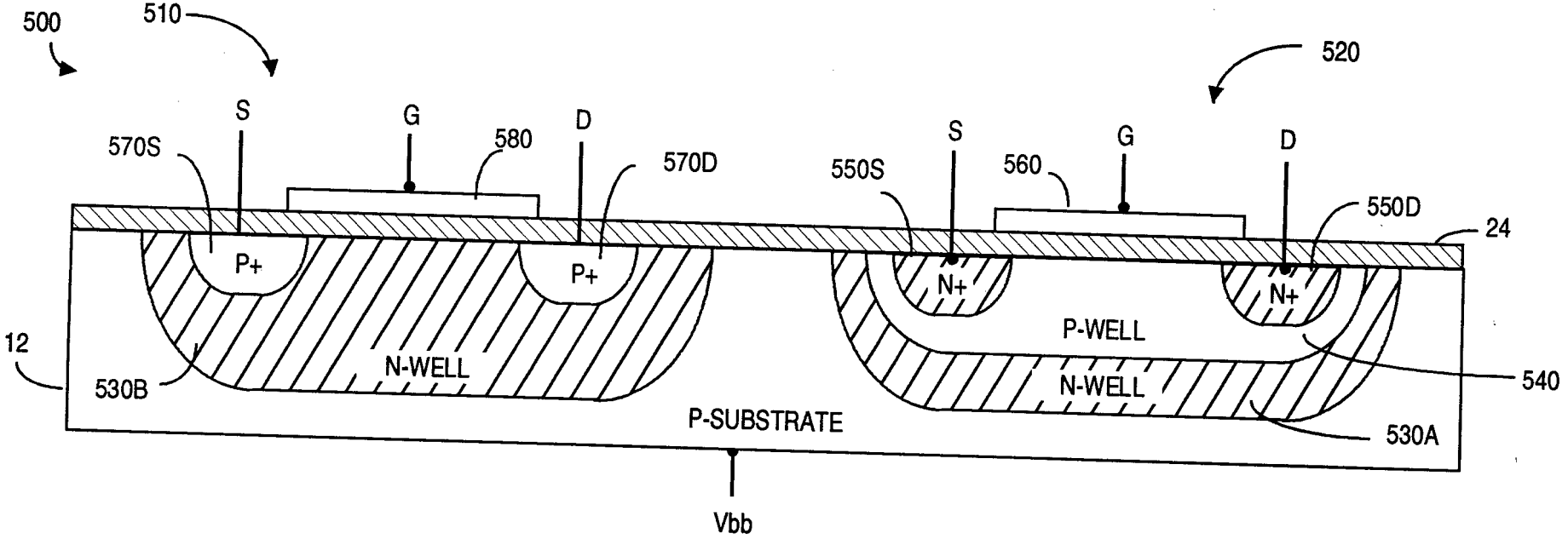
500
510
520
S
G
D
570S
580
570D
550S
560
550D
24
P+
P+
N+
N+
12
530B
N-WELL
P-WELL
N-WELL
540
P-SUBSTRATE
530A
Vbb

FIGURE 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/23085

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G05F 3/02
US CL :327/537, 536

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 327/535, 536, 537

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P ----- Y,P	US 5,699,018 A (YAMAMOTO ET AL.) 16 December 1997 (16.12.97), see Fig. 2.	1-5, 18 ---------- 9, 11-17
X,P ----- Y,P	US 5,642,072 A (MIYAMOTO ET AL.) 24 June 1997 (24.06.97), see Figs. 2 and 7.	1-5, 18 ---------- 9, 11-17
X --- Y	US 5,530,640 (HARA ET AL.) 25 June 1996 (25.06.96), see Fig. 5.	1-8, 10, 11, 16-18, 20 ---------- 9, 12-15
X ---- Y	US 5,388,084 A (ITOH ET AL.) 07 February 1995 (07.02.95), see Fig. 3.	1-5, 18 ---------- 9, 11-17

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

18 MARCH 1998

Date of mailing of the international search report

12 MAY 1998

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