

Nov. 10, 1959

L. L. SLATTEN, JR

2,912,601

MEANS FOR DEVELOPING ELONGATED PULSES

Filed March 10, 1958

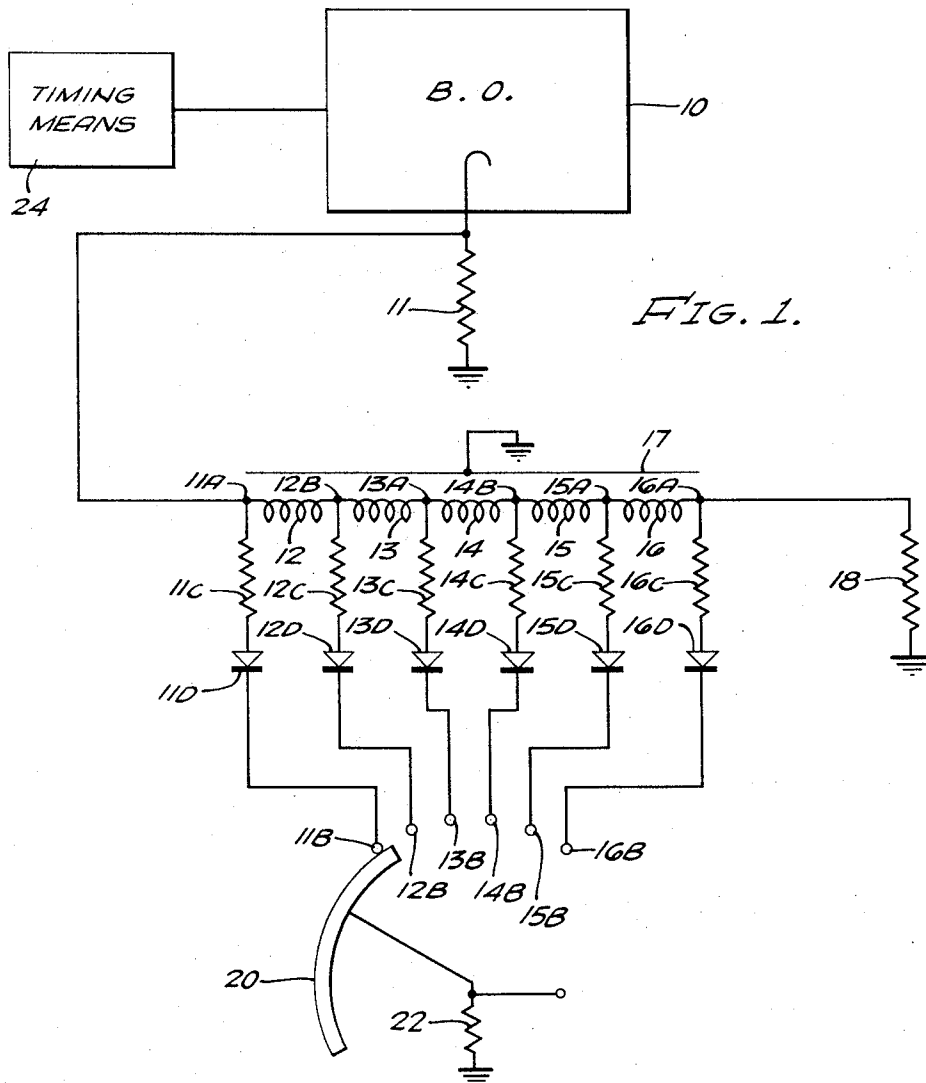
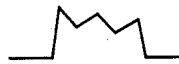
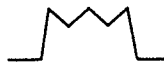
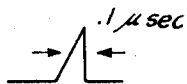


FIG. 2.

FIG. 3.

FIG. 4.

FIG. 5.



INVENTOR.
LESTER L. SLATTEN, JR.
BY *Lyon & Lyon*
ATTORNEYS

1

2,912,601

MEANS FOR DEVELOPING ELONGATED PULSES

Lester L. Slatten, Jr., Beverly Hills, Calif., assignor to
Brubaker Electronics, Inc., Los Angeles, Calif., a corporation of California

Application March 10, 1958, Serial No. 720,288

7 Claims. (Cl. 307-106)

The present invention relates to improved means and techniques for developing elongated pulses.

In general, the present arrangement involves the use of a multitapped delay line for developing elongated or "stretched" pulses that are substantially constant in height for the duration of the pulse. Elongated pulses have heretofore been produced using a blocking oscillator, but the pulses produced thereby decay in amplitude because of inherent features of the oscillator. Thus, usually a blocking oscillator which is used to develop a relatively long pulse has a long recovery time which is in proportion to the length of the pulse. This places a limitation on the rapidity with which such oscillator may develop pulses. In accordance with the present invention, elongated pulses may be developed with great rapidity and without decaying in amplitude.

An object of the present invention is to provide improved means and techniques for developing elongated pulses using a blocking oscillator of short pulse length.

Another object of the present invention is to provide improved means and techniques for developing elongated pulses of adjustable width which do not decay appreciably in amplitude.

The features of the present invention which are believed to be novel are set forth with particularity in the appended claims. This invention itself, both as to its organization and manner of operation, together with further objects and advantages thereof, may be best understood by reference to the following description taken in connection with the accompanying drawings, in which—

Figure 1 is a schematic representation of a system embodying features of the present invention.

Figure 2 represents a pulse obtained from the output of the blocking oscillator.

Figures 3 and 4 represent the shape of output pulses when the slider bridges two and three contacts, respectively.

Figure 5 represents the type of pulse produced when the slider bridges the first three contacts without any compensatory effect.

In Figure 1 the blocking oscillator 10 serves to develop a pulse having a duration of approximately one-tenth of one microsecond across its output load resistance 11 which has one of its terminals grounded.

The ungrounded terminal of resistance 11 is connected to the ungrounded terminal of resistance 18 through the series of coils 12, 13, 14, 15, 16, which are each capacitatively coupled to ground by condensers represented by the capacity plate 17, and which form therewith a tapped delay line.

The taps 11A, 12A, 13A, 14A, 15A and 16A on the delay line are connected respectively to stationary switch contacts 11B, 12B, 13B, 14B, 15B and 16B through corresponding series connected resistances and diode rectifiers 11C, 11D, 12C, 13D, 13C, 13D, 14C, 14D, 15C, 15D and 16C, 16D.

These stationary switch contacts 11B-16B are

2

adapted to be, in turn, bridges by a common slider contact 20 which is connected to the ungrounded terminal of the output resistance 22.

The resistances 11C-16C are compensating resistances and range in value uniformly from 300 ohms for the first resistance 11C to substantially zero ohms for the last resistance 16C to account for attenuation in the line.

The diodes provide for passage of pulses in one direction only and serve to prevent pulses from feeding back to the delay line.

Resistances 11, 18 may each be approximately 100 ohms in value.

Output resistor 22 should have a value approximately ten times the value of delay line termination, resistance 18.

Thus, depending upon the position of the adjustable slider 20, the pulse appearing across the output resistance 22 may be a composite of one or more time spaced .1 microsecond pulses as indicated in Figures 3 and 4. It is noted that these pulses follow one another in the elongated train by approximately .1 microsecond which is the duration of each blocking oscillator pulse and also the delay encountered by a pulse in passing through one section of the delay line.

The particular length of pulses which appears across resistance 22 may thus be selected. It is noted that the first pulse forming the composite train is attenuated in substantially equal amount as the second, third, fourth, fifth or sixth pulse comprising the train, so that the average height of all such pulses is the same as indicated in Figures 2 and 3 instead of decaying, as illustrated in Figure 5. Such uniformity in pulse height is produced by resistances of non-uniform value.

While the particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from this invention in its broader aspects and, therefore, the aim in the appended claims is to cover all such changes and modifications as fall within the true spirit and scope of this invention.

I claim:

1. The combination comprising, a source of pulses developing pulses, each of said pulses having a finite duration, a multitapped delay line having a plurality of sections defined by taps thereon, said delay line having its input coupled to said source, each of said sections producing a delay in the transmission of one of said pulses from one of said taps to a succeeding one of said taps, said delay being commensurate with the duration of said pulse an impedance coupled to the output of said delay line, an output impedance, and switching means connecting said output impedance to one or more of said taps.

2. The combination comprising, a source of pulses developing pulses, each of said pulses having a finite duration, a multitapped delay line having a plurality of sections defined by taps thereon, said delay line having its input coupled to said source, each of said sections producing a delay in the transmission of one of said pulses from one of said taps to a succeeding one of said taps, said delay being commensurate with the duration of said pulse an output impedance, a series of resistances, a series of rectifiers, switching means having a plurality of contacts, each one of said contacts being connected to a corresponding tap through a corresponding serially connected one of said resistances and one of said rectifiers, said switching means including a movable slider engageable in succession with said contacts and being connected to said output impedance.

3. An arrangement as set forth in claim 2 in which said resistances are of non-uniform value.

4. The combination comprising, delay means includ-

3

ing a multitapped delay line having a plurality of spaced taps thereon defining different sections of the delay line, an output impedance, switching means connecting said output impedance successively and jointly to different ones of said taps each of said sections imparting a finite delay to the transmission of pulses through the delay line, and a source of pulses connected to the input of said delay line and developing pulses, each of said pulses having a duration which is substantially equal to said delay.

5. Delay means as set forth in claim 4 including a series of rectifiers, a series of resistances, a corresponding one of said rectifiers and a corresponding one of said resistances being connectible by said switching means between said output impedance and a corresponding tap.

6. Delay means as set forth in claim 5 in which said resistances are of non-uniform value and decrease in value from the input to the output of the delay line.

7. A blocking oscillator developing pulses of relatively short duration, a multitapped delay line having a plurality of sections and taps thereon and having its input terminal connected to said blocking oscillator, an im-

4

pedance connected to the output terminal of said delay line, each one of said sections imposing a delay substantially equal in duration to a pulse from said oscillator, an output impedance, a series of resistances, a series of rectifiers, switching means comprising a plurality of stationary contacts engageable in succession and jointly with a movable slider, said output impedance being connected to said slider, a corresponding resistance and rectifier being serially connected between a corresponding one of said taps and a corresponding one of said contacts, said resistances being of non-uniform magnitude with the resistances connected to taps closer to the input terminal of said delay line being progressively larger in magnitude, said rectifiers being poled to prevent the passage of pulses from said slider to said taps.

References Cited in the file of this patent

UNITED STATES PATENTS

2,408,824	Varela	Oct. 8, 1946
2,418,128	Labin et al.	Apr. 1, 1947