



(43) International Publication Date
18 August 2016 (18.08.2016)

- (51) **International Patent Classification:**
H01L 21/302 (2006.01) *H01L 21/304* (2006.01)
- (21) **International Application Number:**
PCT/CN2015/073086
- (22) **International Filing Date:**
15 February 2015 (15.02.2015)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
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(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: METHOD FOR OPTIMIZING METAL PLANARIZATION PROCESS

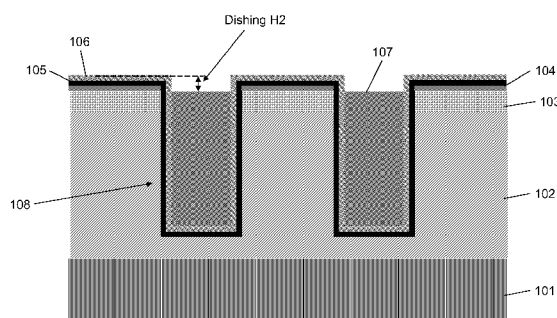


FIG 5

(57) Abstract: The present invention provides a method for optimizing metal planarization process, comprising: removing a bulk metal layer on a top surface of an interconnection structure by a stressed polishing process until the thickness of the remained metal layer reaches a predetermined value Y, the remained metal layer being a continuous layer covering the top surface of the interconnection structure, wherein the remained metal layer has a first surface mean roughness Ra1 induced by the stressed polishing process; removing the remained metal layer on the top surface of the interconnection structure by a stress free polishing process, the top surface of the metal layer in recessed areas in the interconnection structure being lower than the top surface of the interconnection structure by a dishing value H2 after the stress free polishing process, wherein the metal layer in the recessed areas has a second surface mean roughness Ra2 induced by the stress free polishing process, dividing the removing thickness of the stress free polishing process by Ra2 for obtaining a ratio a; wherein when setting a dishing value, for obtaining the minimum metal surface roughness after the stress free polishing process, the thickness of the remained metal layer after the stressed polishing process satisfies the following equation: $Y = a/6 * H2 - aRa1$.

METHOD FOR OPTIMIZING METAL PLANARIZATION PROCESS

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention generally relates to semiconductor manufacture, and more particularly relates to a method for optimizing metal planarization process.

2. The Related Art

[0002] In interconnection structure manufacturing process, with the shrinking of line width and the application of copper and low k dielectric materials, interconnection structure planarization technology has more stringent requirements compared with the past. At present, there at least two kinds of planarization technologies are used for planarizing metal on the interconnection structure, including stressed polishing process, such as CMP and stress free polishing process, such as electrochemical polishing. The CMP utilizes slurry and down force to remove the metal. Although the CMP is still the most commonly used planarization technology, however, with the development of semiconductor technology, the bottlenecks and problems existing in the CMP process are gradually exposed. The CMP has several deleterious effects on the underlying structures of the interconnection structure because of the relatively strong mechanical force involved. Especially, when the k value of the dielectric materials increasingly reduces, the mechanical force may cause permanent damage to the dielectric materials.

[0003] The electrochemical polishing utilizes charged electrolyte to remove the metal on the interconnection structure. Because there only the charged electrolyte contacts the metal surface, the electrochemical polishing process has no mechanical force and will not cause damage to the low k dielectric materials. The charged electrolyte is ejected to the metal surface and reacts with the metal. The metal ions are transferred to cathode. In the electrochemical polishing process, the metal surface

could be considered as an anode. Hence, as byproducts, huge bubbles are generated on the metal surface, which causes the metal surface roughness becomes bad. As we know, the amount of the bubbles on the metal surface is less, that after the electrochemical polishing, the metal surface roughness is better. Therefore, for improving the metal surface roughness, the amount of the bubbles on the metal surface must be controlled. The amount of the bubbles is proportional to the electrochemical polishing time. The electrochemical polishing time is shorter, that the amount of the bubbles is less. Further, the electrochemical polishing time is proportional to the electrochemical polishing removing thickness. The electrochemical polishing removing thickness is less, that the electrochemical polishing time is shorter. Based on the relationships, it is obtained that the electrochemical polishing removing thickness is less, after the electrochemical polishing, the metal surface roughness is better.

[0004] For improving planarization efficiency and reducing the electrochemical polishing removing thickness, the CMP and electrochemical polishing are combined for planarizing the metal on the interconnection structure. Firstly, remove the bulk metal on the top surface of the interconnection structure by CMP and remain a continuous metal layer covering the top surface of the interconnection structure. The continuous metal layer can resist mechanical force of CMP for protecting the low k dielectric material from damaging. Then, remove the continuous metal layer on the top surface of the interconnection structure by electrochemical polishing and expose the underlying structure of the interconnection structure, such as barrier layer. How to find an optimal remaining thickness after CMP, that is also the removing thickness of the electrochemical polishing, is very important for the final metal surface roughness and dishing control. If the thickness of the remained metal layer after CMP is too thin, it is hard to ensure whether the metal layer can fully cover the top surface of the interconnection structure, and probably the low k dielectric material will be damaged during the process. If the thickness of the remained metal layer after CMP is too thick,

that means the electrochemical polishing removing thickness is thick, which causes the metal surface roughness after the electrochemical polishing is not good.

SUMMARY

[0005] The present invention provides a method for optimizing metal planarization process, comprising the following steps:

removing a bulk metal layer on a top surface of an interconnection structure by a stressed polishing process until the thickness of the remained metal layer reaches a predetermined value Y, the remained metal layer being a continuous layer covering the top surface of the interconnection structure, wherein the remained metal layer has a first surface mean roughness Ra1 induced by the stressed polishing process;

removing the remained metal layer on the top surface of the interconnection structure by a stress free polishing process, the top surface of the metal layer in recessed areas in the interconnection structure being lower than the top surface of the interconnection structure by a dishing value H2 after the stress free polishing process, wherein the metal layer in the recessed areas has a second surface mean roughness Ra2 induced by the stress free polishing process, dividing the removing thickness of the stress free polishing process by Ra2 for obtaining a ratio α ;

wherein when setting the dishing value H2, for obtaining the minimum metal surface roughness after the stress free polishing process, the thickness Y of the remained metal layer after the stressed polishing process satisfies the following equation: $Y = \alpha/6 * H2 - \alpha Ra1$.

[0006] As described above, for resisting the mechanical force of the stressed polishing process to avoid the underlying structures of the interconnection structure damaging, and improving the metal surface roughness after the stress free polishing process, the thickness of the remained metal layer after the stressed polishing process needs to meet the following requirements: the thickness of the remained metal layer is

as thin as possible; the remained metal layer is a continuous layer covering the top surface of the interconnection structure; when setting a target dishing value, the thickness of the remained metal layer satisfies the equation: $Y = \alpha/6 * H^2 - \alpha Ra1$.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The present invention will be apparent to those skilled in the art by reading the following description of embodiments thereof, with reference to the attached drawings, in which:

[0008] FIG. 1 is a cross-sectional view of an interconnection structure on which metal layer isn't removed.

[0009] FIG. 2 is a cross-sectional view showing the bulk metal layer on the top surface of the interconnection structure is removed by CMP.

[0010] FIG. 3 is a cross-sectional view showing the remained metal layer on the top surface of the interconnection structure is completely removed by electrochemical polishing.

[0011] FIG. 4 is a cross-sectional view showing a critical state of the remained metal layer on the top surface of the interconnection structure being removed by electrochemical polishing, and there are some residual metal on space areas of the interconnection structure.

[0012] FIG. 5 is a cross-sectional view showing the residual metal on space areas of the interconnection structure is completely removed by electrochemical polishing.

[0013] FIG. 6 is a graph showing the relationship between the electrochemical polishing removing thickness and the mean roughness after CMP and electrochemical polishing processes.

[0014] FIG. 7 is a graph showing the relationship between the electrochemical polishing removing thickness and the mean roughness induced by electrochemical polishing process.

[0015] FIG. 8 is a graph showing the corresponding relationship among the electrochemical polishing removing thickness and the mean roughness Ra1 induced by CMP process, the mean roughness Ra after CMP and electrochemical polishing processes, the mean roughness Ra2 induced by electrochemical polishing process, α which is got through dividing the electrochemical polishing removing thickness by the mean roughness Ra2 induced by electrochemical polishing process.

[0016] FIG. 9 is a cross-sectional view showing the bulk metal layer on the top surface of an interconnection structure with different line width and line density is removed by CMP.

DETAILED DESCRIPTION OF EMBODIMENTS

[0017] The present invention provides a method for optimizing metal planarization process, through controlling the thickness of remained metal layer on the top surface of an interconnection structure after CMP process, to improve the metal surface roughness after the remained metal layer is removed by electrochemical polishing process.

[0018] Referring to FIG. 1, an exemplary interconnection structure is illustrated. It is recognized that the formation of the interconnection structure is not limited to the exemplary interconnection structure shown in FIG. 1. According to different process requirement, the formation of the interconnection structure may be different. As shown in FIG. 1, the exemplary interconnection structure has a substrate 101, a first dielectric layer 102 formed on the substrate 101, a second dielectric layer 103 formed on the first dielectric layer 102, a hard mask layer 104 formed on the second dielectric layer 103, recessed areas 108, for example, trenches, vias, etc., formed on the hard mask layer 104, the second dielectric layer 103 and the first dielectric layer 102, a first barrier layer 105 formed on the hard mask layer 104, sidewall of the recessed areas 108 and bottom of the recessed areas 108, a second barrier layer 106 formed on the

first barrier layer 105, and a metal layer 107 formed on the second barrier layer 106 and filling the recessed areas 108.

[0019] After the metal layer 107 is formed on the second barrier layer 106 and fills the recessed areas 108, the subsequent process is to remove the metal layer 107 on the top surface of the interconnection structure. Firstly, use stressed polishing process, such as CMP to remove the bulk metal layer 107 and remain a certain thickness of the metal layer 107. For resisting the mechanical force of CMP to avoid the underlying structures of the interconnection structure damaging, and improving the metal surface roughness after electrochemical polishing, the thickness of the remained metal layer 107 after CMP is preferably as thin as possible and the remained metal layer 107 is a continuous layer covering the top surface of the interconnection structure, as shown in FIG. 2.

[0020] Then use stress free polishing process, such as electrochemical polishing to remove the remained metal layer 107 on the top surface of the interconnection structure, as shown in FIG. 3. After the remained metal layer 107 on the top surface of the interconnection structure is removed, the second barrier layer 106 is exposed. In consideration of the second barrier layer 106 and the first barrier layer 105 on the top surface of the interconnection structure and the hard mask layer 104 being removed in the next process, the surface of the metal layer 107 in the recessed areas 108 is flush with the top surface of the second dielectric layer 103 or slightly lower than the top surface of the second dielectric layer 103.

[0021] The present invention will introduce how to obtain the thickness of the remained metal layer 107 after CMP hereinafter.

[0022] In order to simplify calculation, as a hypothesis, the metal layer has the same thickness over the top surface of the interconnection structure. In other words, regardless of whether the line width and the line density of the interconnection structure are the same or not, before the metal layer on the top surface of the interconnection structure is removed by CMP, the thickness of the metal layer on the

top surface of the interconnection structure is the same. After CMP and electrochemical polishing processes are completed, the metal surface maximum roughness satisfies the following equation:

$$R_t = R_{t1} + R_{t2}$$

wherein R_t is the metal surface maximum roughness after CMP and electrochemical polishing processes are completed, R_{t1} is the metal surface roughness induced by CMP process, and R_{t2} is the metal surface roughness induced by electrochemical polishing process.

[0023] Based on statistics normal distribution, in 3 sigma condition, $R_t = 6Ra$, Ra is the metal surface mean roughness after CMP and electrochemical polishing processes are completed. The relation could be described as:

$$R_t = R_{t1} + R_{t2} = 6Ra_1 + 6Ra_2$$

wherein Ra_1 is the metal surface mean roughness induced by CMP process, and Ra_2 is the metal surface mean roughness induced by electrochemical polishing process.

[0024] Referring to FIG. 5, if not considering of the second barrier layer 106 and the first barrier layer 105 on the top surface of the interconnection structure and the hard mask layer 104 removed in the next process, dishing H_2 is equal to top surface height of the second barrier layer 106 minus top surface height of the metal layer 107 in the recessed area 108.

[0025] As shown in FIG. 4, in a critical state that the remained metal layer on the top surface of the interconnection structure is removed by electrochemical polishing, the top surface of the metal layer 107 in the recessed area 108 is flush with the top surface of the second barrier layer 106. There are some residual metal 107 on space areas of the interconnection structure, and normally the residual metal height H_1 is equal to R_t . It can be seen that the metal surface roughness after CMP and electrochemical polishing processes are completed, especially R_t , determines the

minimum dishing. The dishing H_2 must be not smaller than the R_t ($H_2 \geq R_t$). Only meeting the condition of $H_2 \geq R_t$, the residual metal can be completely removed. The relation between the thickness of the remained metal layer 107 after CMP and the minimum dishing satisfies the following equation:

$$Y = \alpha/6 (H_2 - R_t) = \alpha/6 * H_2 - \alpha R_t$$

[0026] wherein Y is the optimal thickness of the remained metal layer after CMP, H_2 is the minimum dishing which is a target value set according to process requirement, in this equation, H_2 is a known quantity, α is equal to dividing the electrochemical polishing removing thickness by R_a , α is an empirical equation got through experiments. The ratio α is determined by electrolyte type, viscosity, temperature, substrate spin speed, horizontal movement speed, current, voltage and so on.

[0027] As described above, for resisting the mechanical force of CMP to avoid the underlying structures of the interconnection structure damaging, and improving the metal surface roughness after electrochemical polishing, the thickness of the remained metal layer after CMP needs to meet the following requirements: the thickness of the remained metal layer is as thin as possible; the remained metal layer is a continuous layer covering the top surface of the interconnection structure; when setting a target dishing value, the thickness of the remained metal layer satisfies the equation: $Y = \alpha/6 (H_2 - R_t) = \alpha/6 * H_2 - \alpha R_t$

[0028] If considering of the second barrier layer 106 and the first barrier layer 105 on the top surface of the interconnection structure and the hard mask layer 104 being removed in the next process, the actual thickness of the remained metal layer after CMP satisfies the following equation:

$$Y' = Y - Y_b - Y_m$$

[0029] wherein Y' is the actual thickness of the remained metal layer after CMP, Y_b is the total thickness of the second barrier layer 106 and the first barrier layer 105, Y_m is the thickness of the hard mask layer 104.

[0030] Referring to FIG. 9, in another embodiment of the present invention, an interconnection structure has different line width and line density. In plating process, the line width and line density cause the step height difference between different line areas, which determines the metal layer height uniformity. The height of the metal layer covering a space area could be considered as 0 Angstrom and as a reference plane. Normally, the height of the metal layer covering on the wide line is lower than the reference plane. Conversely, the height of the metal layer covering on the narrow line is higher than the reference plane. In order to completely remove the metal layer on the top surface of the interconnection structure, the metal layer on the narrow line must be ensured to fully remove. On the other hand, because electrochemical polishing process is a conformal process, when the metal layer on the narrow line is fully removed, electrochemical polishing process will induce the dishing of the wide line. The depth of the dishing is determined by the step height difference after CMP process and the line's density. The dishing satisfies the following equation:

$$R_x = T_{\min}/D_x - T_x$$

wherein R_x is the dishing of line width x area, $T_{\min}$ is the step height of the minimum line width relative to the reference plane, D_x is the density of line width x area, T_x is the step height of the line width x area relative to the reference plane.

[0031] For instance, if the line width of the minimum narrow line is 28nm, the step height of the minimum narrow line relative to the reference plane is 200 Angstrom, and the line width of a wide line is 10um, the step height of the wide line relative to the reference plane is -100 Angstrom, and the density of the wide line is 50%, when the metal layer on the minimum narrow line is fully removed, the dishing of line width 10um area is equal to:

$$R_{10} = T_{\min}/D_{10} - T_{10} = 200/50\% - (-100) = 500 \text{ Angstrom}$$

[0032] Combined with the equation $Y' = Y - Y_b - Y_m$, if the interconnection structure has different line width and line density, the actual thickness of the remained metal layer after CMP satisfies the following equation:

$$Y'' = \alpha' / 6 (H_2 + T_{\min} - R_{t1}) = \alpha' / 6 * (H_2 + T_{\min}) - \alpha' R_{a1}$$

$$\alpha' = (Y' + T_{\min}) / R_{a2'}$$

wherein Y'' is the actual thickness of the remained metal layer after the stressed polishing process, $T_{\min}$ is the step height of the minimum line width relative to the reference plane.

$R_{a2'}$ is obtained according to the following two aspects:

1) the thickness $Y' + T_{\min}$ removed by electrochemical polishing (the stress free polishing process); and

2) the relationship between the electrochemical polishing removing thickness and the metal surface mean roughness induced by electrochemical polishing process, as shown in FIG. 7.

[0033] As described above, in order to completely remove the metal layer on the top surface of the interconnection structure and meanwhile obtain the target dishing and the minimum metal surface roughness, the thickness of the remained metal layer after CMP should satisfy the equation requirement, and the within die step height difference should be as low as possible, especially the narrow line step height should be optimized and trend to zero.

[0034] The foregoing description of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously many modifications and variations are possible in light of the above teaching. Such modifications and variations that may be apparent to those skilled in the art are intended to be included within the scope of this invention as defined by the accompanying claims.

CLAIMS

1. A method for optimizing metal planarization process, comprising:

removing a bulk metal layer on a top surface of an interconnection structure by a stressed polishing process until the thickness of the remained metal layer reaches a predetermined value Y, the remained metal layer being a continuous layer covering the top surface of the interconnection structure, wherein the remained metal layer has a first surface mean roughness Ra1 induced by the stressed polishing process;

removing the remained metal layer on the top surface of the interconnection structure by a stress free polishing process, the top surface of the metal layer in recessed areas in the interconnection structure being lower than the top surface of the interconnection structure by a dishing value H2 after the stress free polishing process, wherein the metal layer in the recessed areas has a second surface mean roughness Ra2 induced by the stress free polishing process, dividing the removing thickness of the stress free polishing process by Ra2 for obtaining a ratio α ;

wherein when setting the dishing value H2, for obtaining the minimum metal surface roughness after the stress free polishing process, the thickness Y of the remained metal layer after the stressed polishing process satisfies the following equation:

$$Y = \alpha/6 * H2 - \alpha Ra1$$

2. The method of claim 1, wherein before the metal layer on the top surface of the interconnection structure is removed by the stressed polishing process, the metal layer has the same thickness over the top surface of the interconnection structure.

3. The method of claim 1, wherein after the stressed polishing process and the stress free polishing process are completed, the metal surface maximum roughness satisfies the following equation:

$$R_t = R_{t1} + R_{t2}$$

wherein R_t is the metal surface maximum roughness after the stressed polishing process and the stress free polishing process are completed, R_{t1} is the metal surface roughness induced by the stressed polishing process, R_{t2} is the metal surface roughness induced by the stress free polishing process.

4. The method of claim 3, wherein based on statistics normal distribution, in 3 sigma condition, the R_t satisfies the following equation:

$$R_t = R_{t1} + R_{t2} = 6Ra_1 + 6Ra_2$$

5. The method of claim 3, wherein the dishing value $H_2 \geq R_t$.

6. The method of claim 1, wherein the interconnection structure includes at least one barrier layer and a hard mask layer, considering of the barrier layer on the top surface of the interconnection structure and the hard mask layer being removed, the actual thickness of the remained metal layer after the stressed polishing process satisfies the following equation:

$$Y' = Y - Y_b - Y_m$$

wherein Y' is the actual thickness of the remained metal layer after the stressed polishing process, Y_b is the thickness of the barrier layer, Y_m is the thickness of the hard mask layer.

7. The method of claim 6, wherein the interconnection structure has different line width, the height of the metal layer covering a space area is used as a reference plane, the actual thickness of the remained metal layer after the stressed polishing process satisfies the following equation:

$$Y'' = \alpha' / 6 * (H_2 + T_{min}) - \alpha' Ra_1$$

$$\alpha' = (Y' + T_{min}) / Ra_2'$$

wherein Y'' is the actual thickness of the remained metal layer after the stressed polishing process, T_{min} is the step height of the minimum line width relative to the reference plane, $Ra2'$ is obtained according to the followings:

the thickness $Y' + T_{min}$ removed by the stress free polishing process; and

the relationship between the thickness removed by the stress free polishing process and the metal surface mean roughness induced by the stress free polishing process.

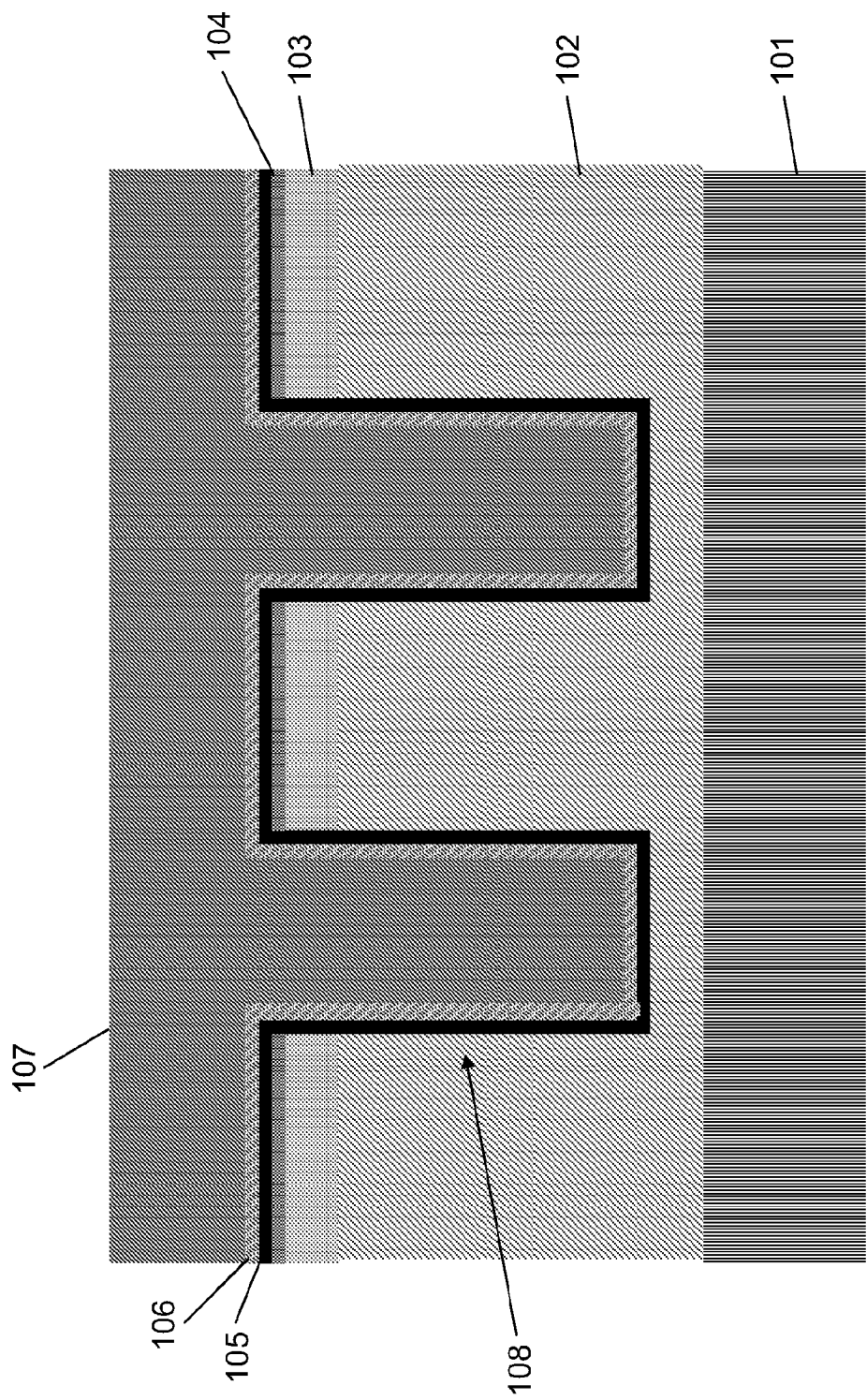


FIG 1

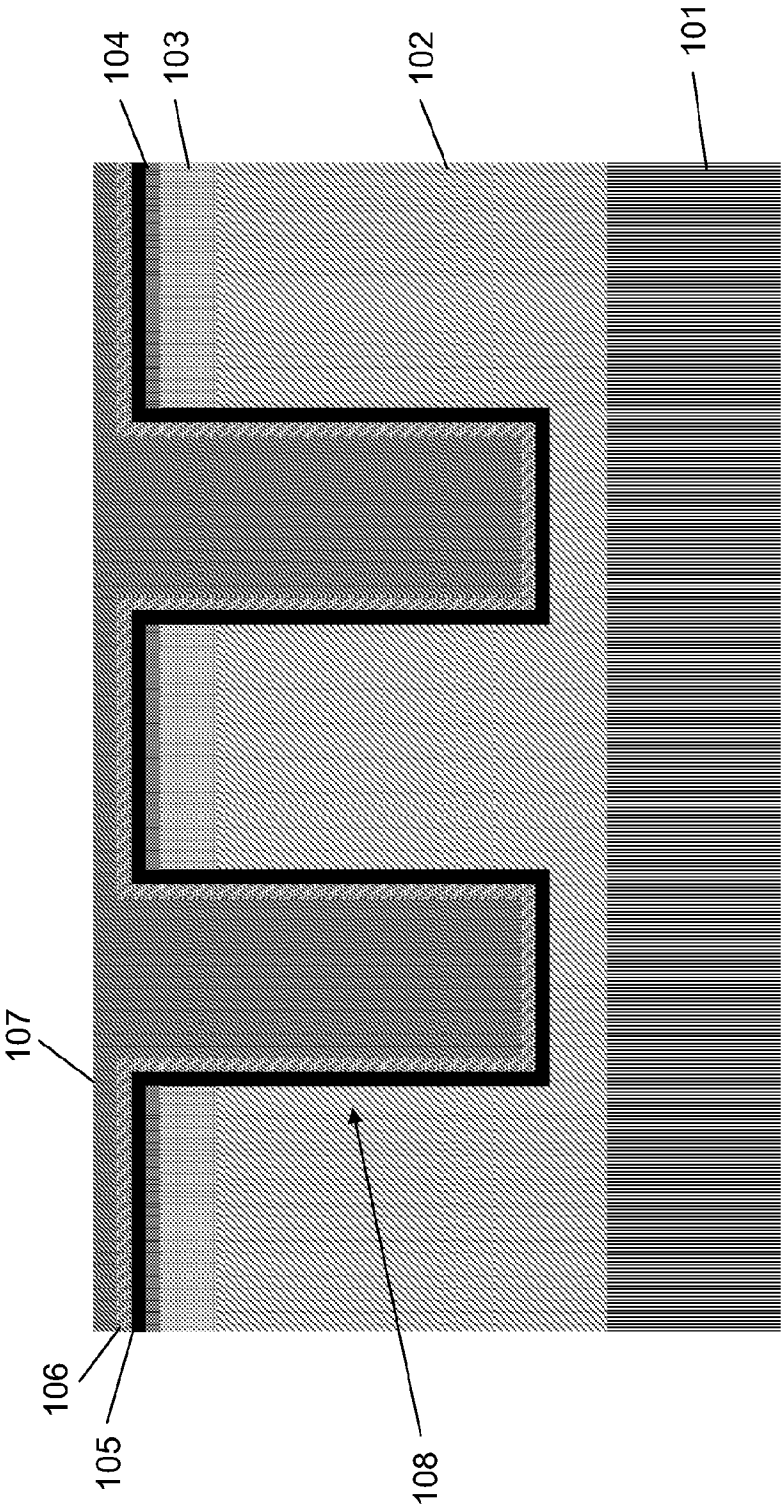


FIG 2

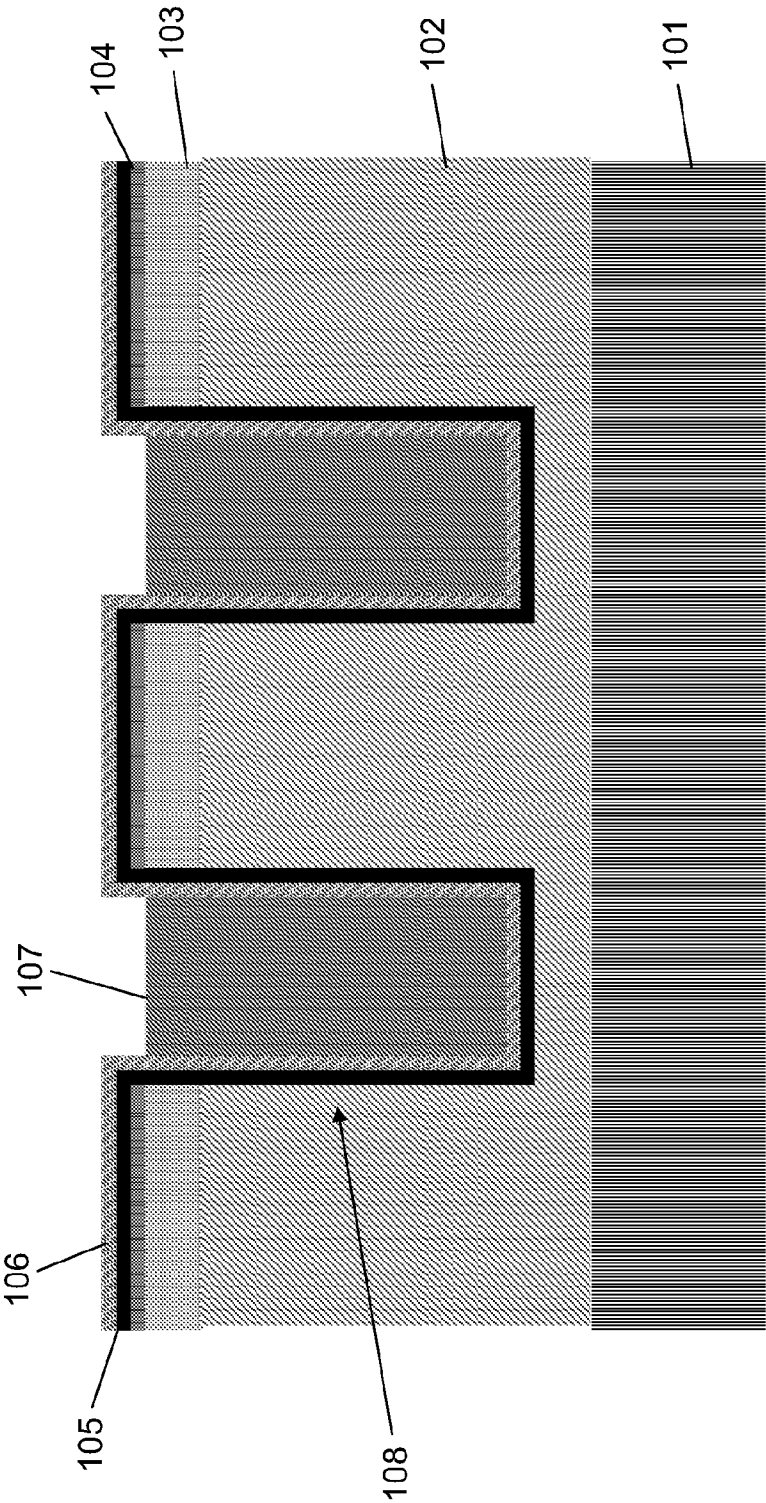


FIG 3

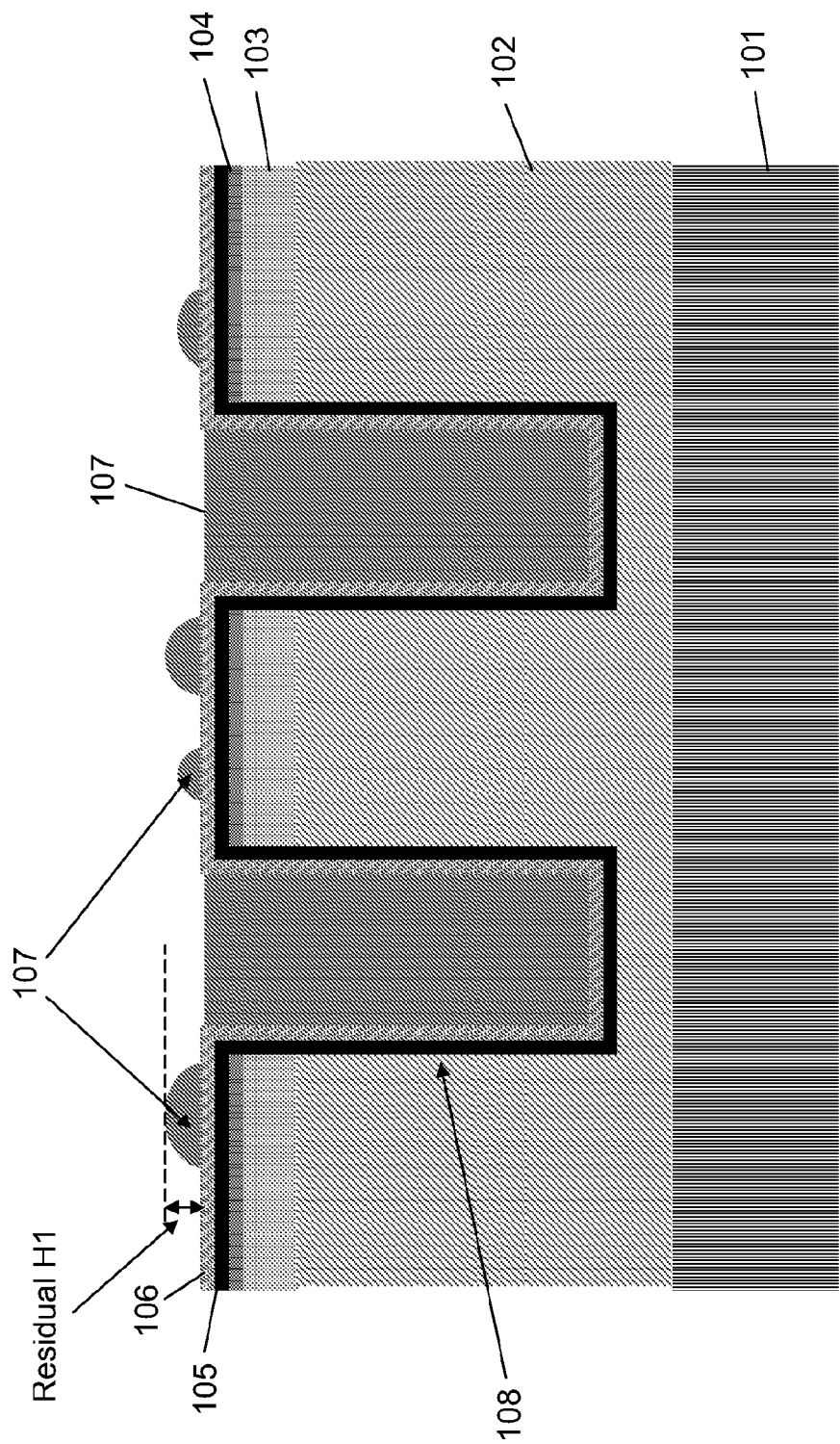


FIG 4

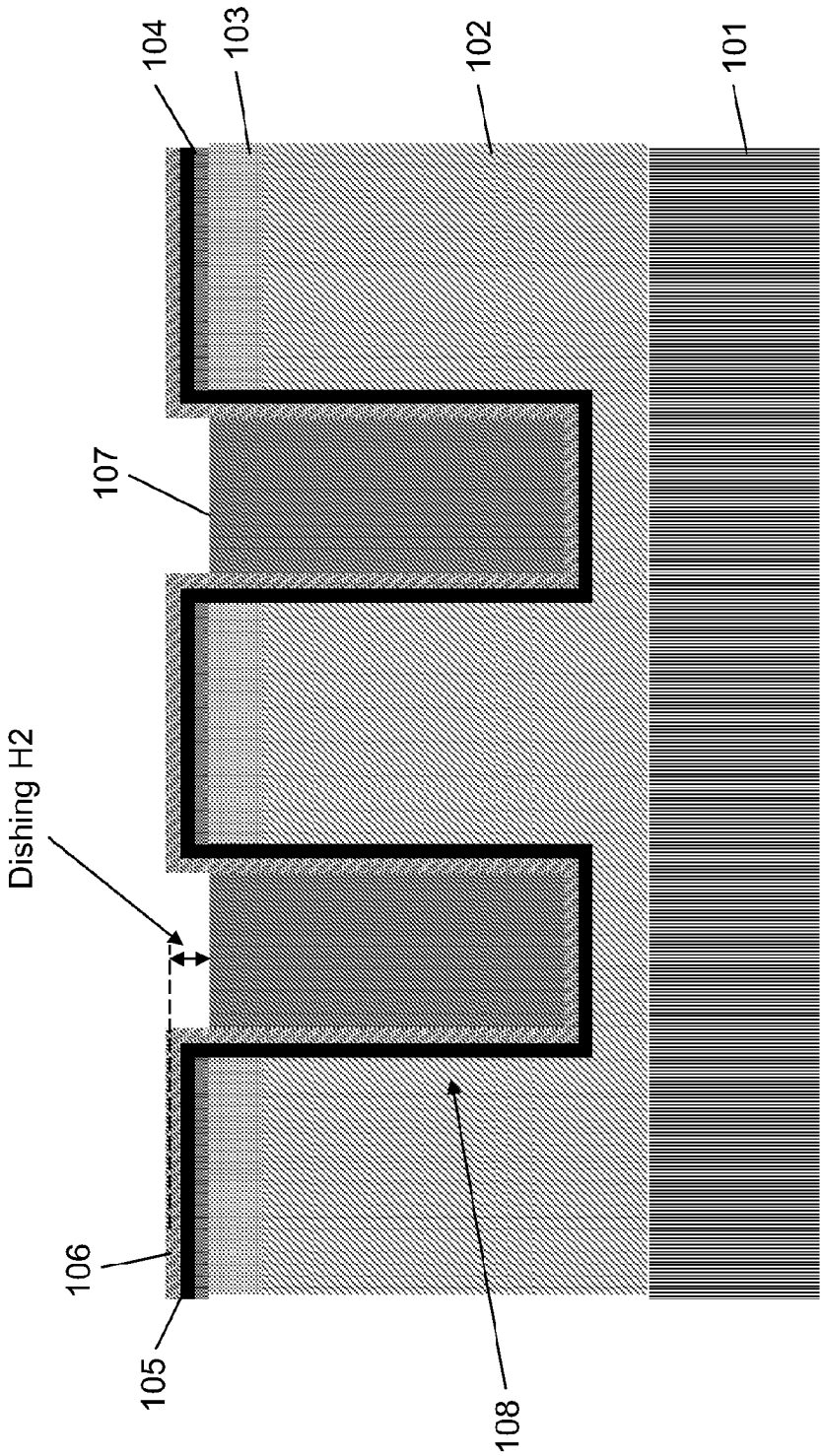
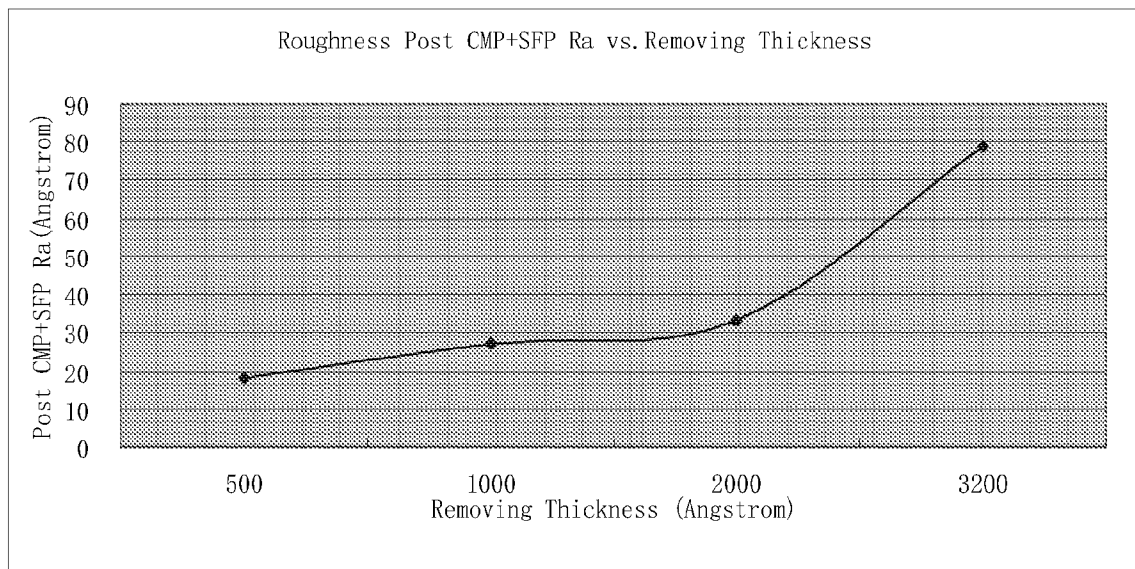
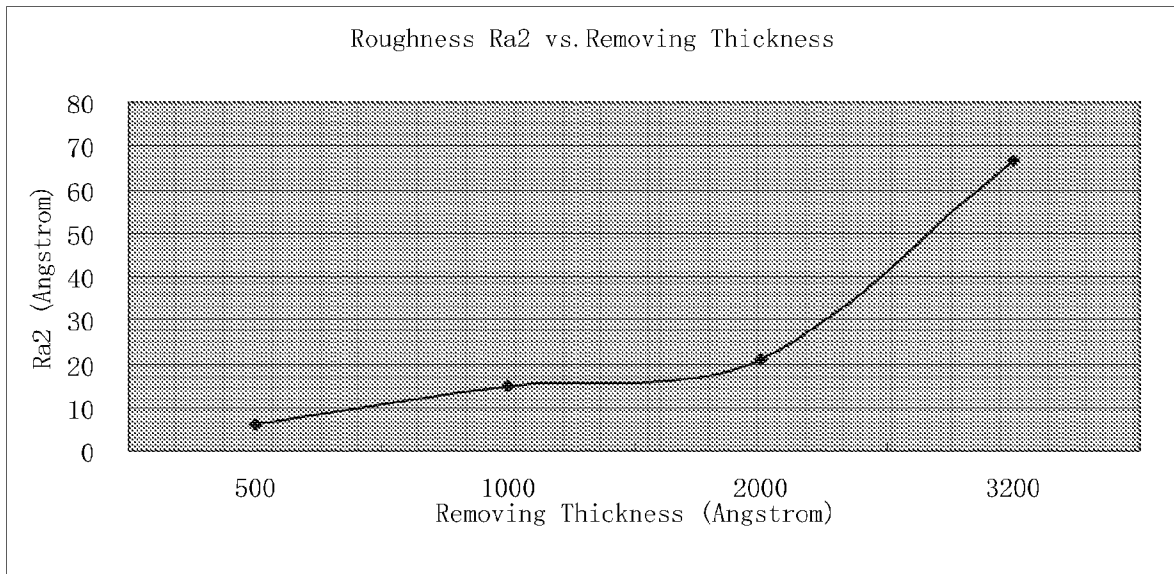


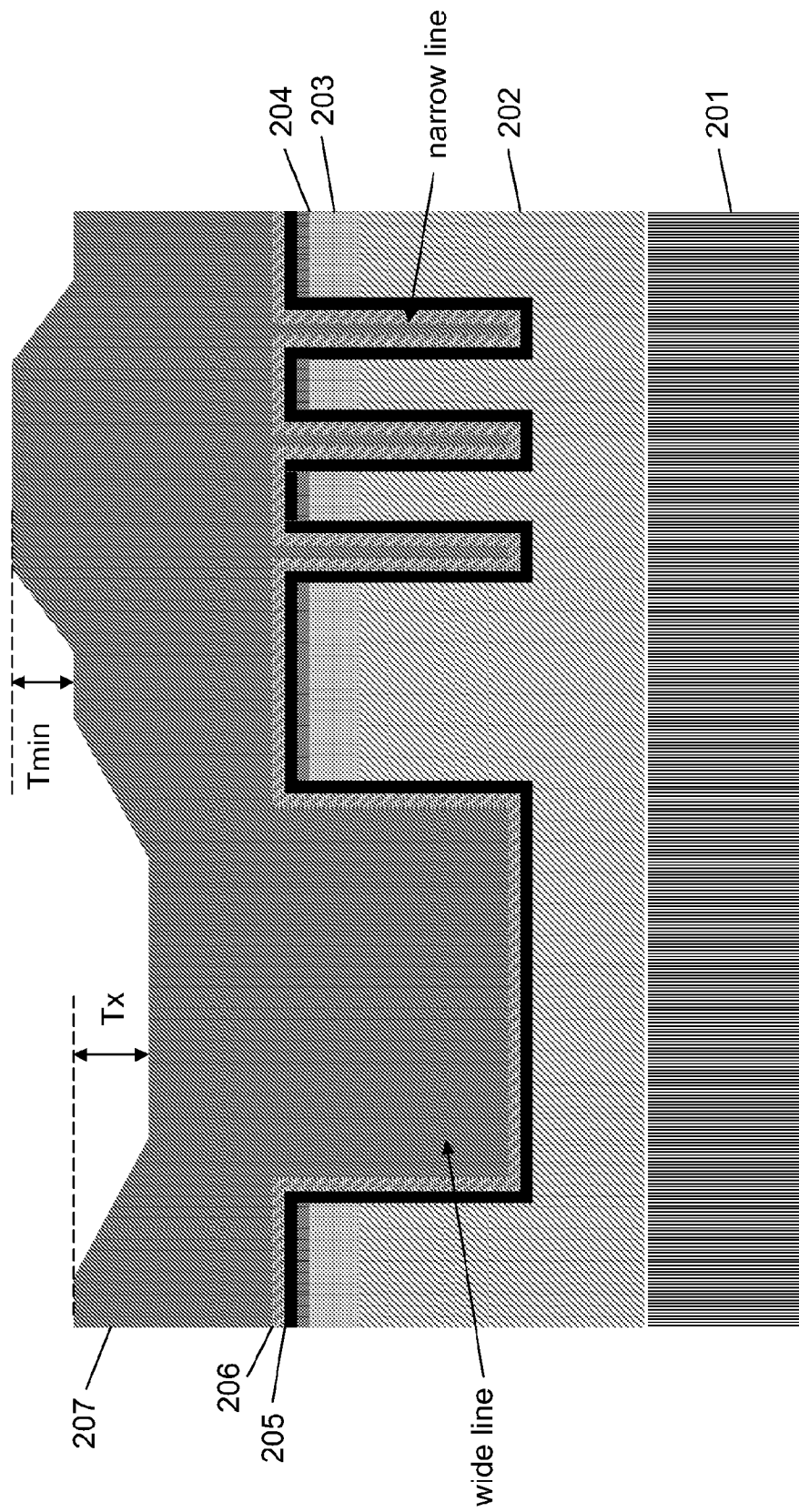
FIG 5

**FIG 6**

**FIG 7**

Removing Thickness (Å)				
	Ra1 (Å)	Ra (Å)	Ra2 (Å)	α
500	12	18	6	83
1000	12	27	15	67
2000	12	33	21	95
3200	12	79	67	48

FIG 8

**FIG 9**

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2015/073086

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/302(2006.01)i; H01L 21/304(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS;DWPI:metal, planarization, interconnection, roughness, polish

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 101992421 A (SEMICONDUCTOR MFG INT SHANGHAI CORP) 30 March 2011 (2011-03-30) description, paragraphs [0044] to [0076] and figures 7 to 11	1-7
A	CN 102689266 A (SEMICONDUCTOR MFG INT SHANGHAI CORP) 26 September 2012 (2012-09-26) the whole document	1-7
A	US 7229907 B2 (WU TOMET AL.) 12 June 2007 (2007-06-12) the whole document	1-7
A	US 6132292 A (NEC CORP) 17 October 2000 (2000-10-17) the whole document	1-7
A	JP 2005217360 A (HITACHI CHEMICAL CO LTD) 11 August 2005 (2005-08-11) the whole document	1-7



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

13 November 2015

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27 November 2015

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2015/073086

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