(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 465 212 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number : **91305984.6**

(22) Date of filing : **02.07.91**

(51) Int. Cl.[5] : **B41J 2/05,** B41J 2/005, B41J 2/16

(30) Priority : **02.07.90 US 547567**

(43) Date of publication of application : **08.01.92 Bulletin 92/02**

(84) Designated Contracting States : **DE FR GB**

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(54) Ink jet printheads.

(57) A thermal inkjet printhead is disclosed having improved reliability and thermal efficiency. The printhead includes heater resistors (14) and thin protective regions (46) positioned above the heating resistors for protecting the heating resistors from corrosion and cavitation damage from the ink. The heating resistors are positioned substantially within the geometric confines of the portion of the protective regions exposed to the ink. Positioned between the resistors and the underlying printhead structure are field oxide regions (60) that thermally insulate the heating resistors from the underlying printhead structure. Positioned between the resistors and the underlying printhead structure is a passivation layer consisting of a middle layer (62) of phosphorus glass, an underglaze (64) between the middle layer and the underlying printhead structure, and glass mesas (66) between the middle layer and the resistors. The underglaze helps prevent phosphorus from the middle layer from contaminating the underlying printhead structure. Similarly, the glass mesas prevent phosphorus from the middle layer from contaminating the resistors.

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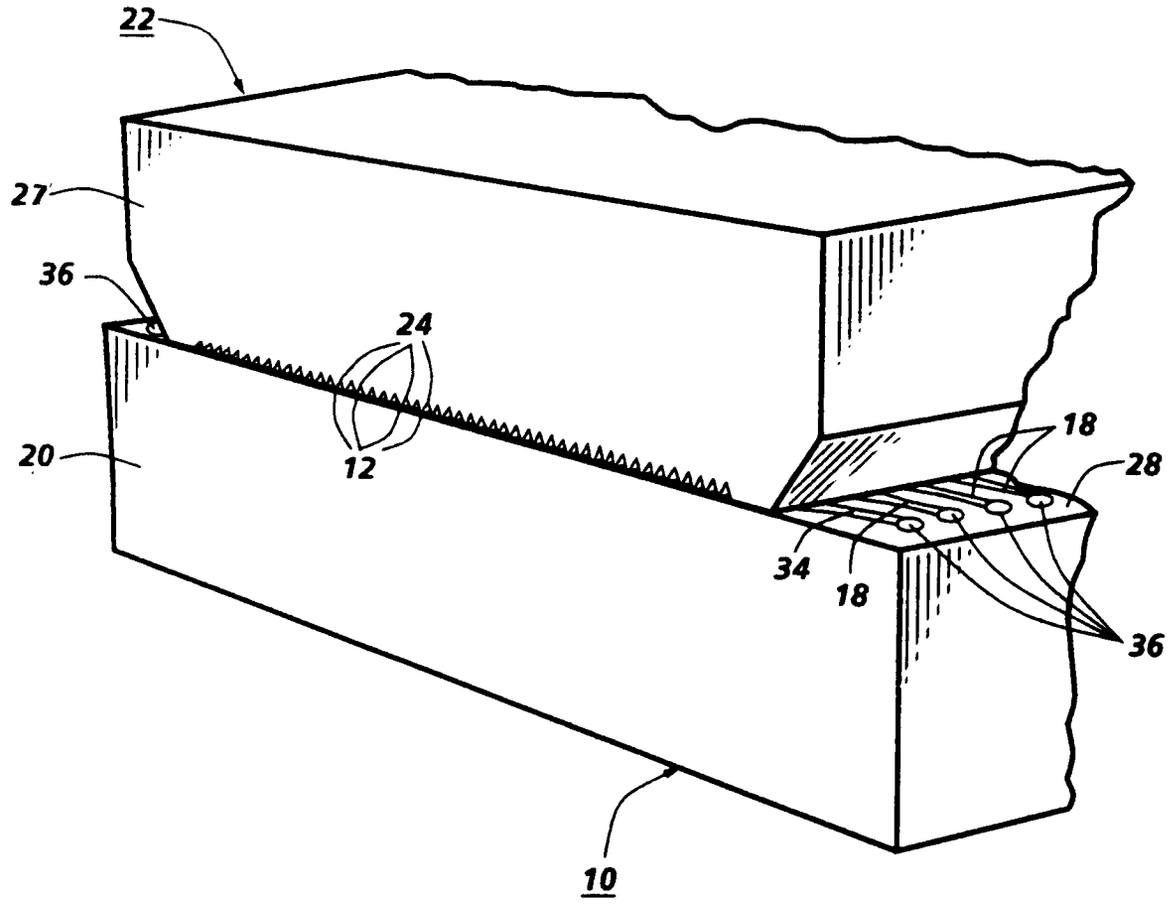

Fig. 1

This invention relates generally to thermal ink jet printing, and more particularly to a thermal ink jet printhead, and a process for fabricating it.

In thermal ink jet (TIJ) printing, the printhead comprises one or more ink-filled channels which communicate with an ink supply chamber at one end and an orifice at the opposite end, such as disclosed in US-A-Re. 32,572. A heating element, such as a resistor, is located in each channel near the orifice. The heating resistors are individually addressed with a current pulse to vaporize the ink momentarily and form a bubble which expels an ink droplet from the orifice. The current pulses originate in drive circuitry, which can be constructed in the printhead, and the current pulses are conveyed to the heating resistors by conductors, typically made of aluminum. The heating resistors consist of resistive material of substantially-uniform resistivity to help ensure uniform ink droplet size and speed.

So that most of the heat from the heater resistors heats the ink, some existing printheads separate the resistors from the underlying printhead structure with thermal insulation. For example, as disclosed in US-A-4,532,530 existing printheads constructed from silicon substrates use a passivation layer to isolate the heating resistors thermally from the underlying semiconductor substrate. The heating resistors are fabricated on top of the passivation layer. A typical passivation layer consists of silicon dioxide containing trace amounts of phosphorus to facilitate reflow at temperatures below the melting point of the aluminum interconnects. Reflowing the passivation layer ensures a smooth surface upon which the interconnects can be formed, thereby increasing the reliability of the interconnects.

Other existing printheads do not separate the heating resistors from the underlying printhead structure with a passivation layer. Instead, these existing printheads save steps in fabricating the heating resistors by fabricating the heating resistors from the same layer of polysilicon used in conventional MOS processes to construct the gate electrode of FETs, and for this reason such printheads are known as "single poly heating resistor" printheads. Consequently, the heating resistors in the single poly heating resistor printheads are separated from the underlying printhead structure only by the thin layer of gate silicon dioxide.

Generally, the existing printheads perform adequately. However, they transfer heat to the ink at a lower efficiency than is desirable. In addition, the reliability of the junctions between heating resistors and aluminum interconnects is lessened by excess temperatures at these junctions. In addition, heating resistors of non-uniform resistance result from phosphorus diffusing into the heating resistors from the underlying passivation layer.

Finally, in the course of fabricating the single poly heating resistor printheads, since the heating resistors are fabricated from the same polysilicon layer used to fabricate the gate electrodes, the heating resistors are covered by the passivation layer used to passivate the gate electrodes. This passivation layer is removed before a protective coating, such as tantalum, is applied into the resulting cavity above the heating resistors to protect the heating resistors from corrosion and cavitation damage from the ink. There are reliability problems, however, in depositing tantalum or other protective coatings into the cavity above the heating resistors, because of inadequate step coverage.

There is therefore a need for a thermal ink jet printhead with a higher heat transfer efficiency, more reliable junctions between heating resistors and aluminum interconnections, heating resistors with reduced phosphorus contamination, and an improved protective coating for heating resistors.

A thermal ink jet printhead is provided which includes ink channels and a heating resistor positioned within each ink channel. The heating resistors are fabricated on a major surface of a silicon substrate, along with drive circuitry that powers the heating resistors, channel stops that isolate drive circuitry, and aluminum interconnects that connect drive circuitry to respective heating resistors. More particularly, drive circuitry and channel stops are fabricated within the silicon substrate. The heating resistors and aluminum interconnects are fabricated on a passivation layer which covers the major surface of the substrate and electrically isolates the substrate from the heating resistors and aluminum interconnects, and thermally isolates the substrate from the heating resistors. Each heating resistor is covered by successive regions of silicon dioxide and silicon nitride, and a tantalum region which contacts the ink. These regions help prevent the ink from contaminating and cavitating the heating resistors. A second passivation layer covers most of the first passivation layer, including the aluminum interconnects, and overlaps the outer perimeter regions of the top surface of tantalum regions, leaving most of the top surface of the tantalum regions exposed so that the second passivation layer is not a thermal barrier between the heating resistors and the ink.

In accordance with one aspect of the invention, a double layer of polysilicon is employed, with the bottom layer of polysilicon being used to form gate electrodes of FETs, the top layer of polysilicon being used to form heating resistors, so that reliability problems associated with step coverage of the tantalum protective coating are minimized by placing the heating resistors above the passivation layer that covers the gate electrodes of the FETs.

In accordance with another aspect of the invention, there is a contact region at opposite ends of each heating resistor. The contact regions have a much lower sheet resistance than the heating resistors.

Therefore, the heating resistors will tend to be hotter than the contact regions during the flow of electricity therethrough. Efficient transfer of heat to the ink is aided by positioning respective heating resistors either substantially coextensive with the exposed portions of respective tantalum regions or substantially within the geometric confines of the exposed portions of respective tantalum regions. In addition, the contact regions space the junctions between contact regions and the aluminum interconnects from the hotter heating resistors, thereby contributing to lower junction temperatures, and thus greater junction reliability.

In accordance with another aspect of the invention, the printhead includes thick field oxide regions constructed in the silicon substrate between the first passivation layer and the major surface directly beneath each heating resistor. The field oxide regions supplement the thermal insulation provided by the first passivation layer to isolate the heating resistors thermally from the silicon substrate. One advantage of using the field oxide regions, rather than simply increasing the thickness of the first passivation layer, is that contact holes are etched through the first passivation layer to allow the interconnects to contact the drive circuitry, and a thicker passivation layer decreases the reliability of such contact. However, contact holes need not be etched through the field oxide regions, since the field oxide regions are positioned beneath the heating resistors and not above the drive circuitry.

In accordance with another aspect of the invention, the field oxide regions are constructed without additional fabrication steps by constructing them in the same steps used to construct the channel stops.

In accordance with a final aspect of the invention, the passivation layer between the heating resistors and the drive circuitry includes three separate layers of silicon dioxide, a middle layer doped with phosphorus, a non-doped underglaze, and non-doped overglaze mesas. The middle layer is doped with phosphorus to facilitate reflow of the middle layer. The underglaze is positioned below and contiguous with the middle layer, and above the drive circuitry and the field oxide regions. The underglaze prevents phosphorus from the middle doped layer from diffusing to the drive circuitry and altering its electrical characteristics, particularly the electrical characteristics in the drift regions. One of the overglaze mesas is positioned above the middle layer and directly beneath one of the heating resistors. The overglaze mesas prevent phosphorus from the middle layer from diffusing to the heating resistors and altering their electrical characteristics. In this manner, the heating resistors can more readily be made of uniform resistance.

The present invention will now be described by way of example with reference to the accompanying drawings, wherein:

Figure 1 is an enlarged isometric view of a first embodiment of a side shooter thermal ink jet printhead embodying the invention, showing the linear array of nozzles and ink channels;

Figure 2 is a partial sectional view of the heater board of the first preferred embodiment of the thermal ink jet printhead of Figure 1;

Figure 3 is a partial sectional view of a heater board of a second preferred embodiment of a thermal ink jet printhead;

Figure 4 is a view, similar to Figs 2 and 3, of another form of printhead of the invention, and

Figures 5a - 5d show process steps for making the third preferred embodiment of a thermal ink jet printhead.

Referring now to Figures 1 and 2, there is shown a first preferred embodiment of a thermal ink jet (TIJ) printhead 10 embodying the present invention. Housed in the printhead 10 are a linear array of ink jets. Each ink jet includes an ink channel 12 and a heating resistor 14 positioned in the channel 12. A droplet is expelled from the nozzle of ink channel 12 in response to a current pulse sent to the heating resistor 14 associated with that ink channel 12. The current pulse originates in drive circuitry 16 that is selectively addressed by a control signal along an addressing electrode 18 associated with its particular heating resistor 14.

Referring to Figure 1, printhead 10 comprises an electrically insulated substrate heater board 20 permanently attached to a structure board 22. Structure board 22 includes parallel triangular cross-sectional grooves 24 which extend in one direction and penetrate through front edge 26 of printhead 10. Heater board 20 is aligned and bonded to the surface of structure board 22 with grooves 24 so that ink channels 12 are formed by grooves 24 and the surface of the heater board 20, and so that ink channel 12 has positioned in it a heater resistor.

Referring to Figures 1 and 2, heater board 20 includes an electrically-insulated silicon substrate 27 with a major surface 28 on which there is patterned CMOS drive circuitry 16 and channel stops 30. Of course, drive circuitry 16 could be fabricated using other fabrication techniques. Major surface 28, drive circuitry 16, and channel stops 30 are covered by a passivation layer 32, which consists of a 1 μm thick layer of silicon dioxide. On the top surface of passivation layer 32 there are patterned heater resistors 14, addressing electrodes 18, a power bus 34 for supplying power to resistors 14, and terminals 36 connected to addressing electrodes 18 and power bus 34, and aluminum interconnects 38. Aluminum interconnects 38 connect heating resistors 14 to power bus 34, and connect drive circuitry 16 to respective addressing electrodes 18 and respective heating resistors 14.

Each heating resistor 14 is covered by successive regions of silicon dioxide 42, silicon nitride 44,

and tantalum 46, respectively, that separate resistor 14 from the ink (not shown) to stop the ink from contaminating or cavitating it. Moreover, each silicon dioxide region 42 and silicon nitride region 44 electrically insulates its respective resistor 14 from tantalum region 46, which is conductive. At and near junctions 40, tantalum regions 46 are spaced from aluminum interconnects 38 to prevent short-circuits.

A passivation layer 48 covers aluminum interconnects 38, power bus 34, and addressing electrodes 18. Passivation layer 48 consists of a 1 μm thick layer of silicon dioxide. Alternatively, passivation layer 48 consists of a 0.5 μm thick layer of silicon dioxide covered by a 1.0 μm thick layer of silicon nitride, with the silicon nitride layer providing increased protection against contaminants, while being separated from the tantalum region 46. Terminals 36 are not covered by passivation layer 48, to allow access to terminals 36. Passivation layer 48 also overlaps ends 50 of the top surface of tantalum regions 46, leaving exposed most of the top surface of tantalum regions 46 so that passivation layer 44 is not a thermal barrier between resistors 14 and the ink.

Referring now to Figure 2, in accordance with one aspect of the invention, each heater board 20 includes two contact regions 54 associated with each resistor 14. Resistors 14 have a substantially greater sheet resistance than contact regions 54. Contact regions 54 are positioned adjacent to, and on opposite sides of, resistors 14. Contact regions 54 have junctions 40 between and aluminum interconnects 38. Contact regions 54 help produce a lower temperature at junctions 40 by spacing junctions 40 from the resistors 14.

The efficient transfer of heat from resistors 14 to the ink is aided by positioning resistors 14 so that they lie aligned with, and either substantially coextensive with, the exposed portion of tantalum regions 46, or substantially within the geometric confines of the exposed portion of tantalum regions 46. More particularly, each resistor 14 has ends 56 that abut its respective contact regions 54, and ends 56 lie beneath and approximately coincident with edges 58 of the portion of the top surface of tantalum regions 46 not covered by passivation layer 48. In this manner, resistors 14 are separated from the ink only by silicon oxide regions 42, silicon nitride regions 44 and tantalum regions 46.

To fabricate resistors 14, a 0.4 μm thick layer of polysilicon is deposited on passivation layer 32, patterned and etched, then patterned and implanted with impurities to form contact regions 54, then patterned and implanted with impurities to form resistors 14. Subsequently, passivation layer 32 is reflowed to provide a smooth surface on which aluminum interconnects 38 can be deposited. Reflow of passivation layer 32 also drives impurities into resistors 14 and contact regions 54, and grows silicon dioxide region 42, which is 0.04 μm thick. Silicon dioxide region 42 could be removed, since protection of heating resistors 14 is mainly performed by tantalum regions 46, which are 0.5 μm thick, and silicon nitride regions 44, which are 0.5 microns thick, but preferably silicon dioxide regions 42 are not removed to save the steps required for their removal.

Referring now to Figure 3, there is shown a second preferred embodiment of a printhead 10 embodying the present invention. Heater board 20 includes 1 μm thick field oxide regions 60 that are constructed in silicon substrate 26 directly beneath resistors 14. Although passivation layer 32 provides some thermal insulation, a 1 μm thickness of silicon dioxide, between resistors 14 and substrate 26, field oxide regions 60 increase the thickness of the thermal insulation in the vicinity of the resistors 14, where thermal insulation is most needed. One advantage in using field oxide regions 60 to supplement the thermal insulation of passivation layer 32, rather than simply increasing the thickness of passivation layer 32, is that increasing the thickness of passivation layer 32 increases the difficulty of etching contact hole 76 in passivation layer 32 that allow interconnects 38 to reach drive circuitry 16.

Field oxide regions 60 are constructed in the same steps used to fabricate channel stops 30. In this manner, field oxide regions 60 are constructed without adding any steps to the conventional CMOS fabrication process, or other conventional fabrication process used to fabricate drive circuitry 16.

Although the second preferred embodiment shows the use of field oxide regions 60 in conjunction with resistors 14 and contact regions 54 to provide a more thermally-efficient printhead 10, field oxide regions 60 could be used by themselves to provide a thermally-efficient printhead 10.

Referring now to Figure 4, there is shown a third preferred embodiment of a printhead 10 embodying the present invention. Passivation layer 32 includes three separate layers, a middle layer 62 doped with phosphorus, a non-doped underglaze 64, and non-doped overglaze mesas 66. Middle layer 62 is doped with phosphorus to facilitate reflow of middle layer 62. Underglaze 64 is positioned below, in contact and coextensive with, middle layer 62, and above drive circuitry 16 and field oxide regions 60. Underglaze 64 prevents phosphorus from middle doped layer 62 from diffusing to drive circuitry 16 and altering the electrical characteristics, particularly the electrical characteristics in the drift regions (not shown). One overglaze mesa 66 is positioned between middle layer 62 and resistors 14. Overglaze mesas 66 prevent phosphorus from middle layer 62 from diffusing to resistors 14 and altering their electrical characteristics.

Referring now to Figures 4 and 5a, in fabricating printhead 10, underglaze 64 is deposited after drive circuitry 16, channel stops 30 and field oxide regions

60 have been constructed on major surface 28. Underglaze 64 is fabricated by depositing a 0.3 μm thick layer of chemical vapour deposited silicon dioxide on top of drive circuitry 16 and other portions of major surface 28. Next, middle layer 62 is formed by depositing on top of underglaze 64 a 0.7 μm thick layer of CVD silicon dioxide doped with 4% to 6% by weight of phosphorus.

Referring now to Figures 4 and 5b, glass mesas 66 are formed on top of middle layer 62 by depositing a 0.3 μm thick overglaze 68 of CVD silicon dioxide, then patterning and etching overglaze 68. Prior to the patterning and etching of overglaze 68, however, resistors 14 are formed on top of overglaze 68. On top of overglaze 68 there is deposited a 450nm thick layer 70 of CVD polysilicon. Referring now to Figures 4, 5b and 5c, polysilicon layer 70 is patterned and etched to form polysilicon regions 74 directly above field oxide regions 60. Next, referring to Figures 4, 5c and 5d, to facilitate reflow of middle layer 62, overglaze 68 is patterned and etched to remove it from the surface of middle layer 62, except where overglaze 66 is covered by polysilicon regions 74. The remaining portions of overglaze 68 form glass mesas 66. Polysilicon regions 74 are implanted with impurities to form resistors 14 and contact regions 54.

Next, referring to Figures 1 and 4, a reflow process is performed that reflows middle layer 62. As previously mentioned, the reflow process also grows silicon dioxide regions 42 on top of polysilicon regions 74, and implants the impurities within polysilicon regions 74 to give resistors 14 a sheet resistance from between 40 to 50 ohms per square. After thereflow process, silicon nitride and tantalum regions 44 and 46 are formed by depositing a 0.5 μm thick film of high-temperature silicon nitride, and a 0.5 μm thick film of tantalum, then patterning and etching the films. Contact holes 76 are opened in passivation layer 32, and a layer of aluminum is deposited, patterned and etched to form aluminum interconnects 38, terminals 36, power bus 34 and addressing electrodes 18. Passivation layer 48, a 1 μm thick layer of silicon dioxide, is deposited, and patterned and etched to expose terminals 36 and tantalum regions 46 above heating resistors 14. Alternatively, passivation layer 48 consists of a 0.5 μm thick layer of silicon dioxide covered by a 1.0 μm thick layer of silicon nitride.

Although the third preferred embodiment shows the use of a middle layer 62 doped with phosphorus, a non-doped underglaze 64, and non-doped overglaze mesas 66 in conjunction with field oxide regions 60, resistors 14 and contact regions 54 to provide a most reliable and thermally-efficient printhead 10, middle layer 62, underglaze 64 and mesas 66 could be used by themselves to provide a reliable printhead 10.

Although this has not been shown in the drawings, the major surface 28 of the substrate body 20 carrying the heaters for the bubble jet printer could also carry at least one transistor used to support heating current to the selected resistor. Each such transistor could have its source and drain regions formed on surface 28. An overlying layer of siliconoxide could have a polysilicon gate formed in it close to the source and drain regions. The transistor would be connected to its respective resistors by conductors 38 of aluminum and connects 76. The transistor and its conductors would be formed concurrently with the resistor 14 and its conductors and barriers against phosphorus migration.

Referring now to figures 2, 3 and 4, each drive circuitry 16 consists of an NMOS FET switch having a gate 17. Gates 17 are constructed from a 0.4 micrometer thick layer of polysilicon that is deposited adjacent major surface 28, then patterned and etched, then patterned and implanted with impurities in a concentration sufficient to make gate 17 conductive. Subsequently, passivation layer 32 is deposited, heating resistors 14 are constructed. Each heating resistor 14 is connected to its respective drive circuitry 16, including gate 17, by means of interconnects 38. Interconnects 38 contact drive circuitry 16 through passivation layer 32 by means of contact holes 76. In accordance with another aspect of the invention, gates 17 are constructed of a different layer of polysilicon than the layer of polysilicon used to construct heating resistors 14, so that heating resistors 14 are constructed above passivation layer 32 and gates 17 are constructed below passivation layer 32. Consequently, the step coverage of tantalum regions 46 is more reliable because tantalum regions 46 can be constructed without etching a cavity in passivation layer 32.

Claims

1. An ink jet printhead (10) having at least one ink channel (12), a heater element (14), and an interconnect (38), the ink channel having an open end that serves as a nozzle, the heater being positioned in the channel for ejecting ink droplets from the nozzle by selective application of current pulses along the interconnect to the heater, the heater comprising:

   a heater resistor,

   a protective layer (46) in thermal contact with the resistor and having a portion thereof exposed to the ink channel for protecting the resistor from the ink, the resistor being aligned with, and substantially within the geometric confines of, the exposed portion of the protective layer, and

   at least one contact region (54) electrically connecting the resistor and the interconnect, the and having lower resistance than the resistor.

2. The ink jet printhead of claim 1, including:
a silicon substrate (27) having a major surface (28), the resister and interconnect being located on the major surface;
a first layer (64) of silicon dioxide positioned on the major surface for passivation;
a second layer (62) of silicon dioxide with phosphorus positioned on the surface of the first layer, the first layer preventing phosphorus from the second layer from contaminating the substrate, and
a silicon dioxide mesa (66) positioned between, and in contact with, the second layer and the resistor and contact region, the mesa preventing phosphorus from the second layer from contaminating the resistor and contact region.

3. The ink jet printhead of claim 1 or 2, including:
a silicon substrate (26) having a major surface (28), the resistor and the interconnect being located on the major surface, and
a field oxide region (60) between the resistor and the major surface for thermally isolating the resistor from the substrate.

4. A thermal ink jet printhead (10) plurality of having a ink channels (12) each with a nozzle at one end in a structure (26) fixedly adjoined to an integrated circuit which contains driver logic and heater elements (14) formed on the major surface (28) of a common silicon substrate (27), the heater elements being positioned in the channels for ejecting ink droplets from the nozzles, the integrated circuit comprising:
at least one transistor switch formed on the major surface of the substrate and having a polysicon gate;
conductive vias (38) contacting the transistor switch to provide electrical connection between each transistor switch and its heater resistors;
a passivation layer (64) of silicon dioxide positioned on the major surface of the substrate ;
a layer of silicon dioxide containing phosphorus (62) positioned on the surface of the passivation layer, which prevents phosphorus from the second layer from contaminating the substrate, and
silicon dioxide mesas (66) positioned between, and in contact with the second layer and the resistors to prevent phosphorus from the second layer from contaminating the resistors.

5. The printhead of claim 4, wherein the integrated circuit further includes a first layer of polysilicon (62) deposited to form the gate layer, and a second layer of polysilicon deposited to form the resistors.

6. The printhead of claim 4 or 5, wherein the integrated circuit further includes:
field oxide regions (30), and
oxide regions (60) aligned with the resistors and located between the resistors and the major surface for thermally isolating the resistors from the substrate, wherein the field oxide regions and the oxide regions are formed by a single oxide growth.

7. The printhead of any of claims 4 to 6, wherein each heater element comprises:
a resistor;
a protective layer (46) positioned on the resistor and having a portion thereof exposed to the ink channel for protecting the resistor from ink, the resistor being aligned with, and substantially within the geometric confines, of the exposed portion of the protective layer, and
at least one contact region (54) electrically connecting the resistor and the interconnect (76), the and having lower resistance than the resistor.

8. A process for fabricating a thermal ink jet printhead, which includes the steps of:
a. providing a substrate (20);
b. forming a first layer (64) of silicon dioxide on a major surface (28) of the substrate;
c. forming a second layer (62) of silicon dioxide on the surface of the first layer, the second layer being doped with phosphorus to facilitate reflow;
d. forming a third layer (66) of silicon dioxide on the surface of the second layer;
e. forming a region (14) of electroresistive material on the surface of the third layer;
f. removing portions of the third layer not covered by the region of resistive material, and
g. reflowing the second layer.

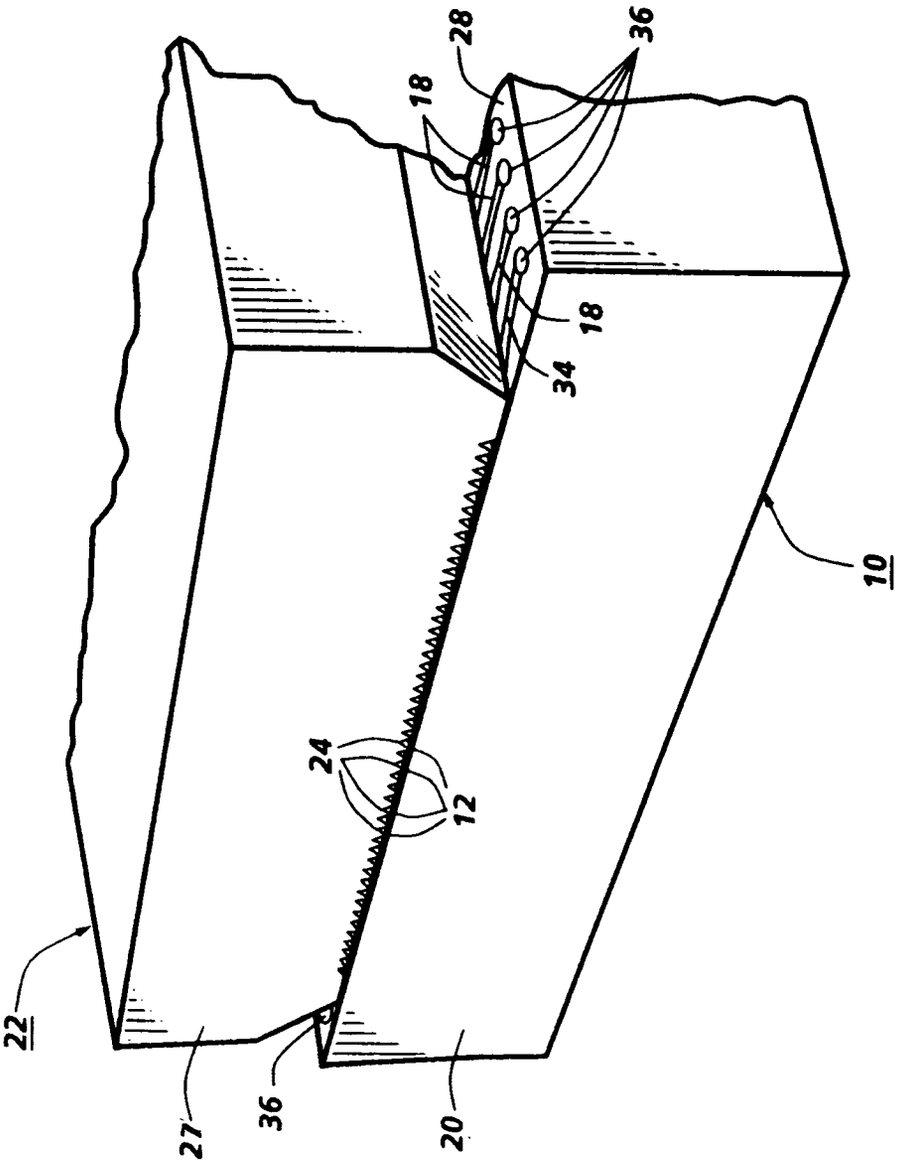

Fig. 1

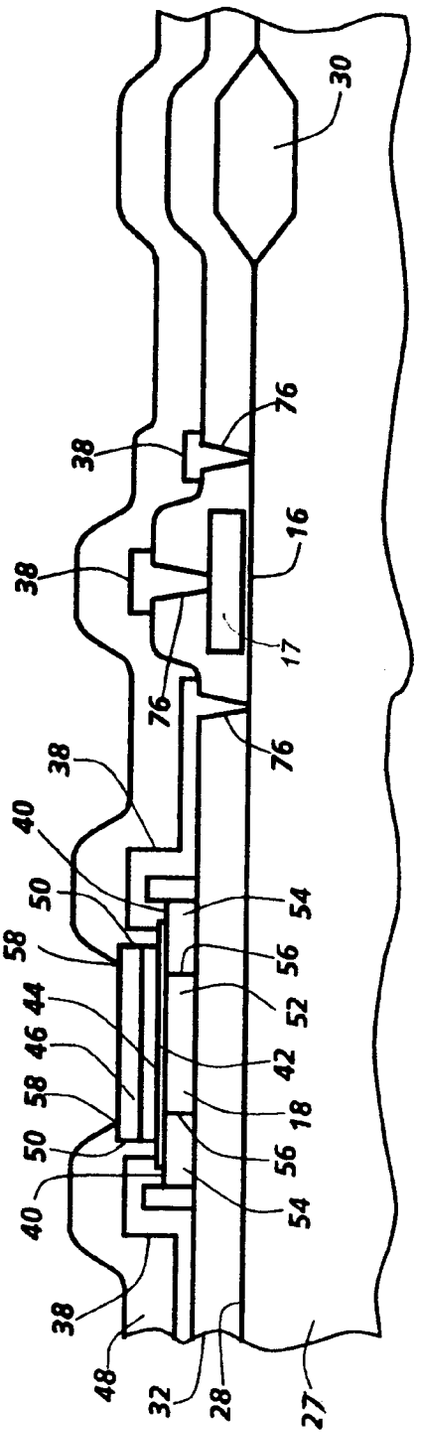
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Fig. 2

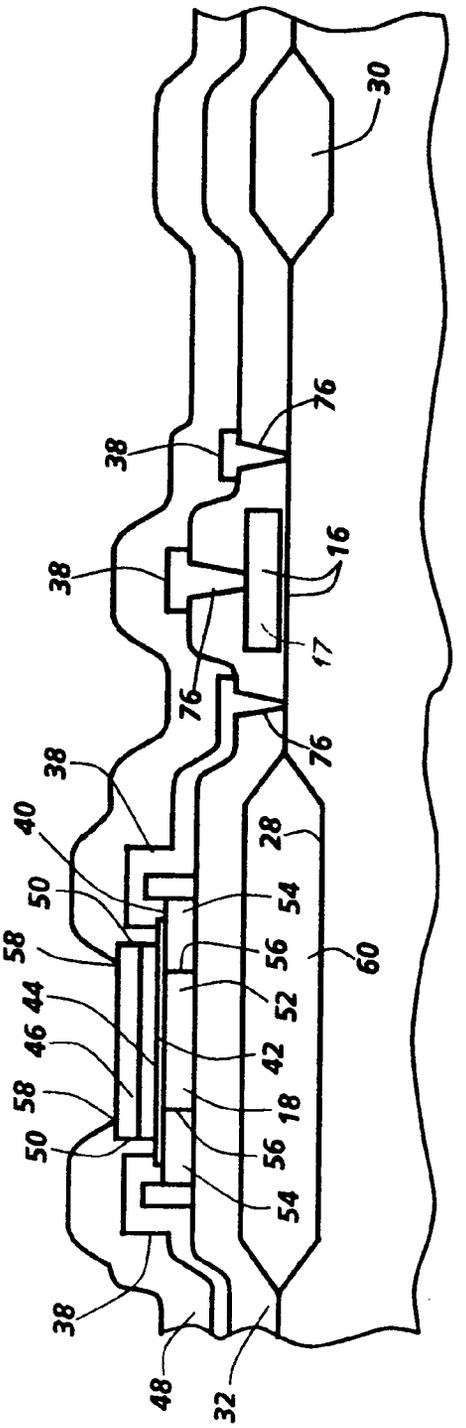
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Fig. 3

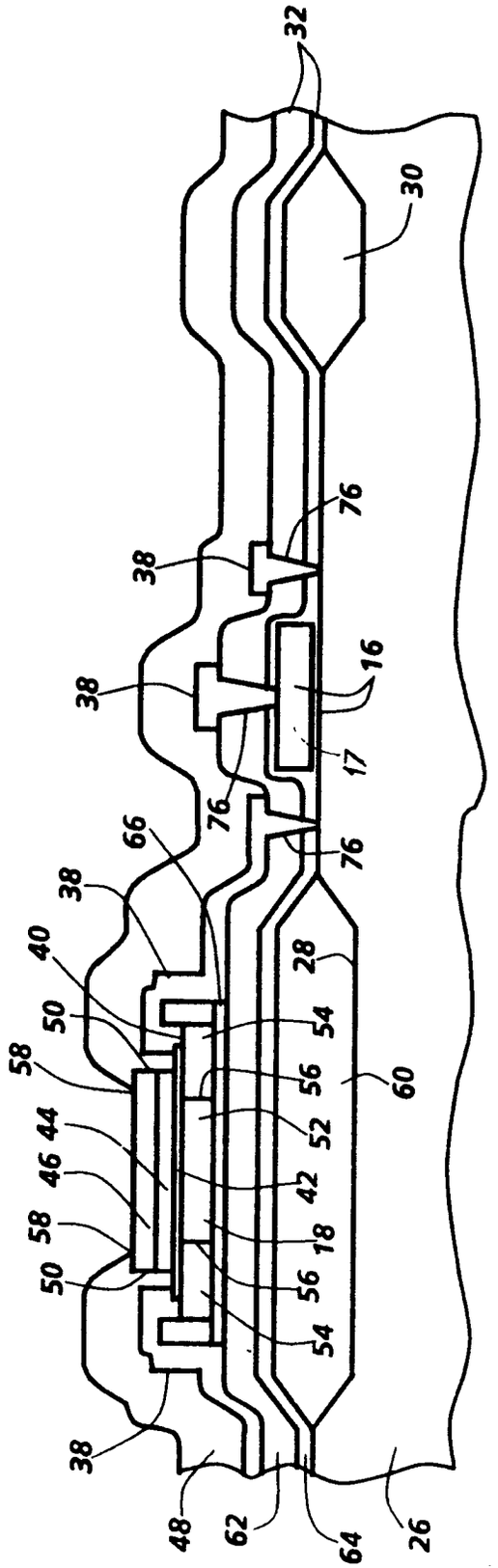

Fig. 4

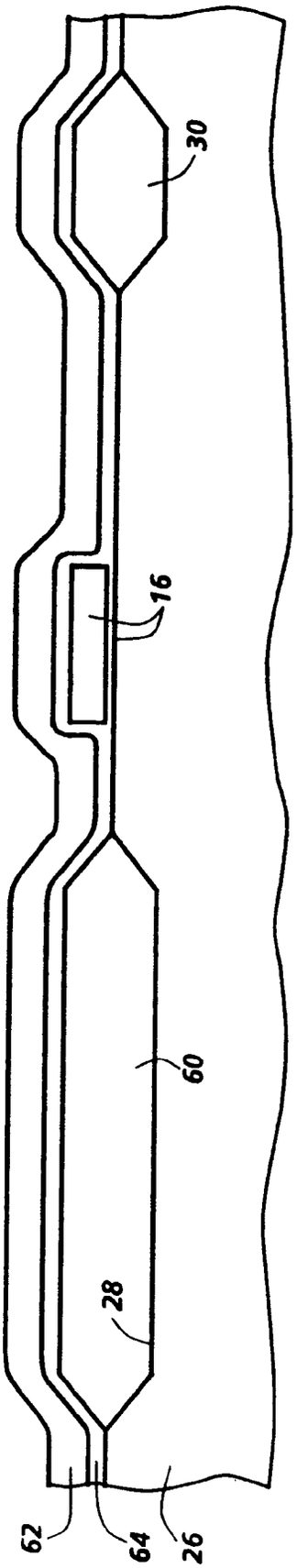

Fig. 5a

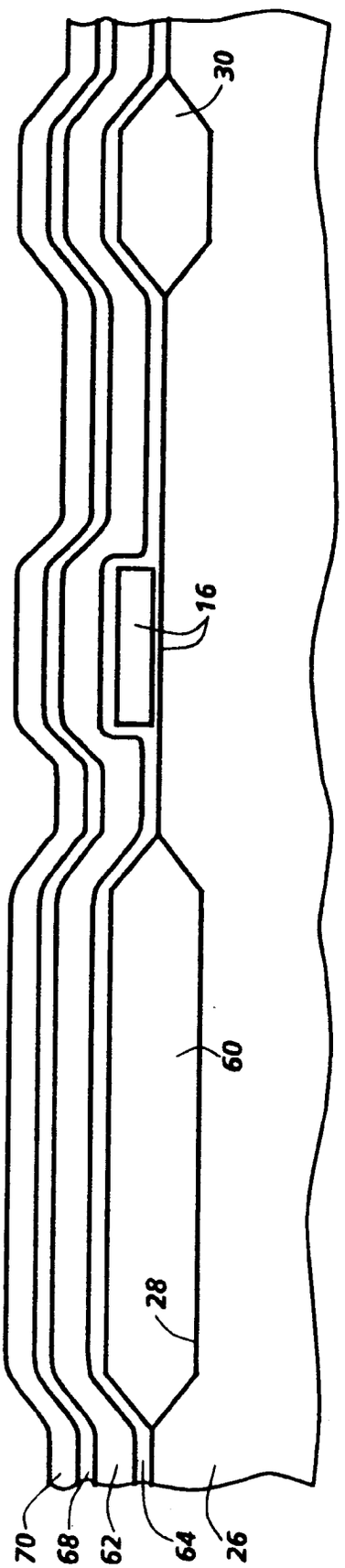

Fig. 5b

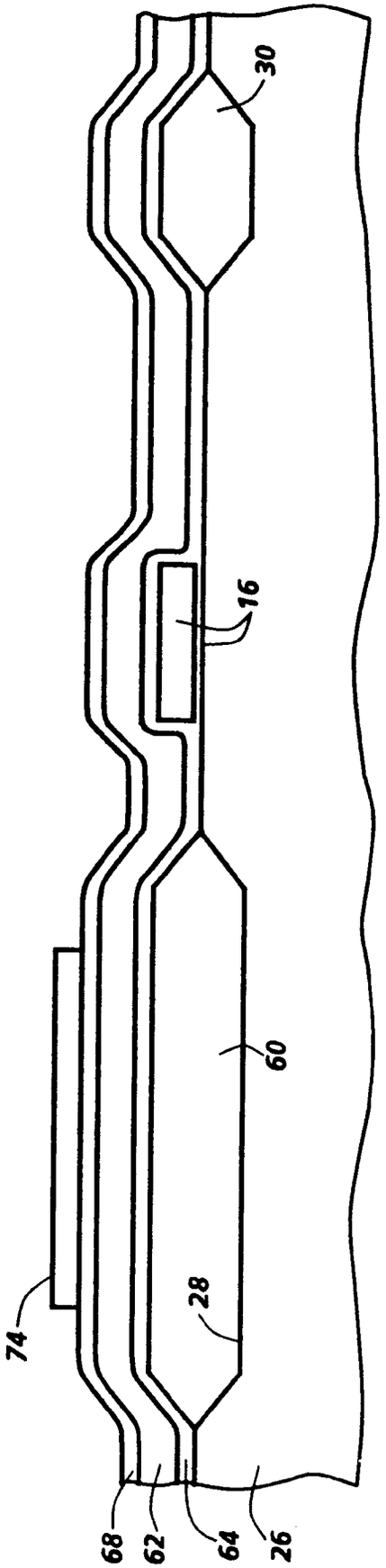

Fig. 5c

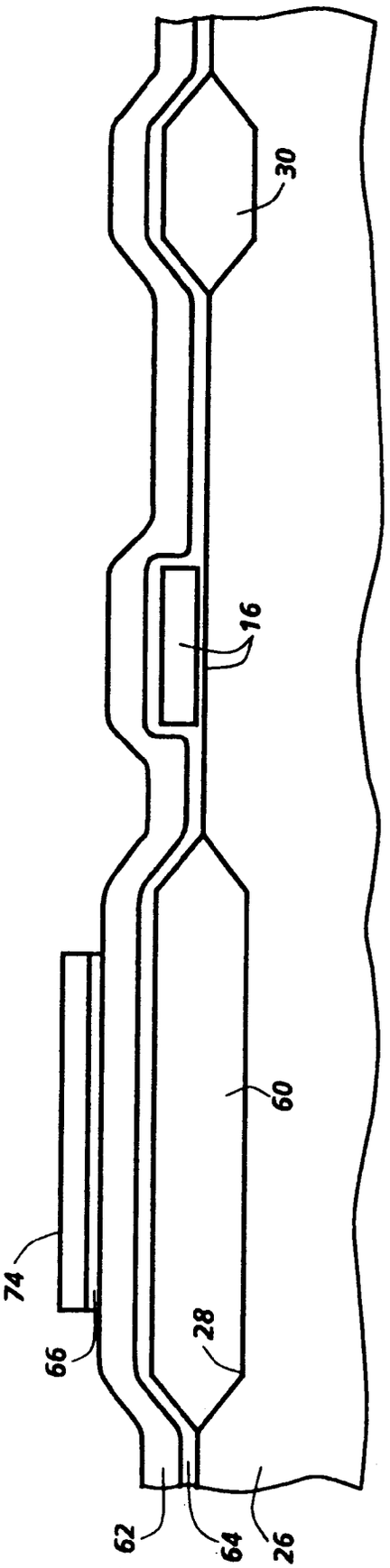

Fig. 5d