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(71) Applicants: INDIAN INSTITUTE OF TECHNOLOGY

MADRAS (IIT MADRAS) [IN/IN];

The Dean, Industrial Consultancy & Sponsored Research (IC&SR) Indian Institute of Technology Madras, IIT, Chennai, Tamil

Nadu 600036 (IN). **CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING, THIRUVANANTHAPURAM** [IN/IN]; Centre For Development of Advanced Computing, (CDAC-T), P.B.NO:6520, Vellayambalam, Thiruvananthapuram, Kerala 695033 (IN).

(72) **Inventors:** **HATUA, Kamalesh**; No. 6/1, Baisnabpara 1st Bye lane, Sibpur, Howrah, West Bengal 711101 (IN). **MIRYALA, Vamshi Krishna**; No.6-2-1252, Plot No:4, New Venkateshwara colony, Phase-III, Nalgonda, Telangana 508001 (IN). **DHANASEKARAN, Saravanan**; No.15, Rajarathinam Street, 3rd Cross, Ullagaram, Chennai, Tamil Nadu 600091 (IN). **PERUMAL, Ganesan**; Power Electronics Group, CDAC-T, P.B.NO:6520, Vellayambalam, Thiruvananthapuram, Kerala 695033 (IN).

(74) **Agent:** **SRIHARI, Saragur, Kasturirangan et al.**; K&S Partners Intellectual Property Attorneys, 515-B, Platinum

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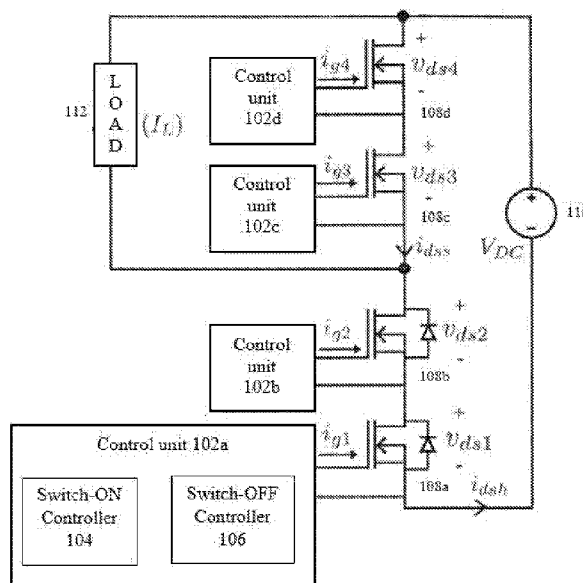


FIG. 1

(57) **Abstract:** A control unit for controlling voltage across a plurality of switching devices. The plurality of switching devices are operated by a plurality of switch-ON controllers and a plurality of switch-OFF controllers. The control unit is configured to enable each switch-ON controller to detect whether increase in drain to source voltage (V_{ds}) is greater than a first threshold voltage upon applying a switch-ON gate-pulse. Based on the detecting, a current with a first current magnitude is applied to switch ON the switching device. The control unit is further configured to enable each switch-OFF controller to detect whether the V_{ds} remains less than a second threshold voltage within a threshold time upon applying a switch-OFF gate pulse. Based on the detecting, the switch-OFF controller either applies a voltage to bias the gate or applies a current with a second current magnitude to the gate to turn OFF the switching device.



Tower, 5th Floor, Sohna Road, Sector 47, Gurgaon, National capital Region 122002 (IN).

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“SYSTEM AND METHOD FOR CONTROLLING VOLTAGE ACROSS SWITCHING DEVICES PRESENT IN CIRCUIT”

TECHNICAL FIELD

5 [0001] The present disclosure relates to a field of switching devices. More particularly, but not exclusively, the present disclosure describes a system and method for controlling voltage across a plurality of switching devices present in a circuit.

BACKGROUND

10 [0002] The following background information may present examples of specific aspects of the prior art (e.g., without limitation, approaches, facts, or common wisdom) that, while expected to be helpful to further educate the reader as to additional aspects of the prior art, is not to be construed as limiting the present invention, or any embodiments thereof,
15 to anything stated or implied therein or inferred thereupon.

[0003] Generally, series connecting several low voltage switching devices is one of the best possible ways to meet high voltage and high frequency requirements of the smart power transmission systems of the present day. Many techniques are present for realizing the
20 series connection of the switching devices. Master-slave based series connection of the switching devices is a one solution, where a single gate driver is used to switch multiple switching devices in series connection. However, the complexity of the master-slave technique increases with increase in number of the switching devices in the series connection. Thus, the master-slave configuration cannot be applied for series
25 connecting larger number of the switching devices.

[0004] Another technique is using individual gate driver for each switching device for series connecting multiple switching devices. In this technique, voltage balancing is achieved using snubber capacitors. But using the bulky and lossy snubber capacitors makes this
30 solution less attractive for series connection problem.

[0005] Yet another technique is employing an active gate control (AGC) to drive each switching device in the series connected string is a popular solution and this method can yield a compact solution with least switching losses. Several AGC solutions are

presented for series connecting the switching devices includes closed-loop driving of switching devices with a common voltage reference. Actively controlling the time durations of each subinterval in the switching transient to a set reference duration. Adjusting the gate pulse delay of the device by measuring the current flowing through the gate clamping diode. However, these methods cannot be directly applied to MOSFET's due to fast switching nature of the MOSFET.

[0006] Yet another conventional technique for series connection voltage information of the individual switching device is transmitted to a central controller, which in turn controls the delay of each gate driver of the each switching device in order to obtain the voltage balancing. This requires additional communication channels and a specialized delay line IC. In addition to this, the technique needs a specialized central controller that can control the voltage balancing of all the switching devices.

[0007] Thus, there is need of the techniques that provide the simpler gate control method which can actively balance device voltage without needing to send any additional communication to each gate controller. Therefore, there exists a need in the art for a technique that ensures proper voltage balancing among the series-connected devices.

SUMMARY

[0008] The present disclosure overcomes one or more shortcomings of the prior art and provides additional advantages discussed throughout the present disclosure. Additional features and advantages are realized through the techniques of the present disclosure. Other embodiments and aspects of the disclosure are described in detail herein and are considered a part of the claimed disclosure.

[0009] In one non-limiting embodiment of the present disclosure, a control unit is disclosed for controlling voltage across a plurality of switching devices present in a circuit, in which, each switching device having a gate, a source and a drain. The plurality of switching devices are operated by a plurality of switch-ON controllers and a plurality of switch-OFF controllers in such a manner that each switching device is operated by a corresponding switch-ON controller and a corresponding switch-OFF controller. The control unit enables each switch-ON controller to apply a switch-ON gate-pulse to the gate of corresponding switching device. Further, the switch-ON controller detects

whether increase in drain to source voltage (V_{ds}) of the switching device is greater than a first threshold voltage. Upon detecting the increase in the drain to source voltage (V_{ds}) of the switching device greater than the first threshold voltage, the switch-ON controller applies a current with a first current magnitude to switch ON the switching device.

5 Further, the control unit is further configured to enable each switch-OFF controller to apply a switch-OFF gate pulse to the gate of the switching device and detect whether the drain to source voltage (V_{ds}) of the switching device remains less than a second threshold voltage within a threshold time period. The switch-OFF controller, based upon the detecting, is configured to perform different functions. For example, the

10 switch-OFF controller may apply a voltage to bias the gate of the switching device to balance voltage of body diodes of the switching device when it is detected that the drain to source voltage (V_{ds}) of the switching device remains less than the second threshold voltage within the threshold time period. In another case, switch-OFF controller may apply a current with a second current magnitude to the gate to turn OFF the switching

15 device when it is detected that the drain to source voltage (V_{ds}) of the switching device exceeds the second threshold voltage within the threshold time period.

[0010] In yet another non-limiting embodiment of the present disclosure, a method to be performed by a control unit for controlling voltage across a plurality of switching

20 devices present in a circuit, wherein each switching device having a gate, a source and a drain. The plurality of switching devices are operated by a plurality of switch-ON controllers and a plurality of switch-OFF controllers in such a manner that each switching device is operated by a corresponding switch-ON controller and a corresponding switch-OFF controller. The method comprises enabling each switch-ON

25 controller, by the control unit, to apply a switch-ON gate-pulse to the gate of corresponding switching device. The method further comprises detecting whether increase in drain to source voltage (V_{ds}) of the switching device is greater than a first threshold voltage, and upon detecting the increase in the drain to source voltage (V_{ds}) of the switching device greater than the first threshold voltage, applying a current with

30 a first current magnitude to switch ON the switching device. The method comprises enabling each switch-OFF controller, by the control unit, to apply a switch-OFF gate-pulse to the gate of the switching device. The method further comprises detecting whether the drain to source voltage (V_{ds}) of the switching device remains less than a second threshold voltage within a threshold time period. Based upon the detecting, the

method further comprises steps of applying, by the switch-OFF controller, a voltage to bias the gate of the switching device to balance voltage of body diodes of the switching device when it is detected that the drain to source voltage (V_{ds}) of the switching device remains less than the second threshold voltage within the threshold time period, and
5 applying, by the switch-OFF controller, a current with a second current magnitude to the gate to turn OFF the switching device when it is detected that the drain to source voltage (V_{ds}) of the switching device exceeds the second threshold voltage within the threshold time period.

10 OBJECTS OF THE INVENTION

[0011] The primary object of the present invention is to provide a less complex and decentralized gate control techniques for enabling series connection of multiple switching devices while ensuring the fast switching.

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[0012] Another object of the present invention is to provide techniques in which each series-connected device is driven with a separate control unit by taking the gate pulse information alone.

20 [0013] Yet another object of the present invention is to provide less complex, lower switching loss solutions for series connecting multiple switching devices in series.

[0014] Yet another object of the present invention is to provide the voltage controlling techniques that can be directly employed for series connecting any number of switching
25 devices without needing to change the control in any way.

[0015] Further object of the present invention is to provide a generic gate driver that can be made for any voltage-source series-connection application.

30 BRIEF DESCRIPTION OF THE ACCOMPANYING DRAWINGS

[0016] The features, nature, and advantages of the present disclosure will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout.

Some embodiments of system and/or methods in accordance with embodiments of the present subject matter are now described, by way of example only, and with reference to the accompanying figures, in which:

5 **[0017]** Fig. 1 shows a block diagram illustrating a circuit illustrating a control circuit for controlling voltage across a plurality of switching devices in accordance with an embodiment of the present disclosure.

10 **[0018]** Fig. 2 shows a flow chart of a method for controlling voltage across a plurality of switching devices in accordance with an embodiment of the present disclosure.

[0019] Fig. 3 shows a test setup for explaining the method for controlling the voltage in accordance with an embodiment of the present disclosure.

15 **[0020]** Fig. 4 shows illustrates the switch-ON switching waveform of the switching devices in accordance with an embodiment of the present disclosure.

20 **[0021]** Fig. 5 shows an alternate implementation of a switch-ON controller of the control unit in accordance with an embodiment of the present disclosure.

[0022] Fig. 6 shows a circuit diagram of a voltage sensing unit and drive signal generation unit in accordance with an embodiment of the present disclosure.

25 **[0023]** Fig. 7 shows a circuit diagram of a voltage sensing unit in accordance with an embodiment of the present disclosure.

[0024] Fig. 8 shows a circuit diagram of alternate implementation of ON-stage-2 of the switch-ON in accordance with an embodiment of the present disclosure.

30 **[0025]** Fig. 9 shows illustrates the switch-OFF switching waveform of the switching devices in accordance with an embodiment of the present disclosure.

[0026] Fig. 10 shows an alternate implementation of a switch-OFF controller of the control unit in accordance with an embodiment of the present disclosure.

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[0027] Fig. 11 shows an alternate implementation of a switch-OFF controller of the control unit in accordance with an embodiment of the present disclosure.

[0028] Fig. 12 shows illustrates the switch-OFF switching waveform of the switching devices in accordance with an embodiment of the present disclosure.

[0029] Fig. 13 shows an alternate implementation of a switch-OFF controller of the control unit in accordance with an embodiment of the present disclosure.

[0030] Fig. 14 shows a block diagram of a control unit for controlling voltage across a plurality of switching devices in accordance with an embodiment of the present disclosure.

[0031] It should be appreciated by those skilled in the art that any block diagrams herein represent conceptual views of illustrative systems embodying the principles of the present subject matter. Similarly, it will be appreciated that any flow charts, flow diagrams, state transition diagrams, pseudo code, and the like represent various processes which may be substantially represented in computer readable medium and executed by a computer or processor, whether or not such computer or processor is explicitly shown.

DETAILED DESCRIPTION

[0032] In the present document, the word “exemplary” is used herein to mean “serving as an example, instance, or illustration”. Any embodiment or implementation of the present subject-matter described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other embodiments.

[0033] While the disclosure is susceptible to various modifications and alternative forms, specific embodiments thereof has been shown by way of example in the drawings and will be described in detail below. It should be understood, however that it is not intended to limit the disclosure to the particular forms disclosed, but on the contrary, the disclosure is to cover all modifications, equivalents, and alternatives falling within the scope of the disclosure.

[0034] The terms “comprises”, “comprising”, “include(s)”, or any other variations thereof, are intended to cover a non-exclusive inclusion, such that a setup, system or method that

comprises a list of components or steps does not include only those components or steps but may include other components or steps not expressly listed or inherent to such setup or system or method. In other words, one or more elements in a system or apparatus preceded by “comprises... a” does not, without more constraints, preclude the
5 existence of other elements or additional elements in the system or apparatus.

[0035] In the following detailed description of the embodiments of the disclosure, reference is made to the accompanying drawings that form a part hereof, and in which are shown by way of illustration specific embodiments in which the disclosure may be practiced.
10 These embodiments are described in sufficient detail to enable those skilled in the art to practice the disclosure, and it is to be understood that other embodiments may be utilized and that changes may be made without departing from the scope of the present disclosure. The following description is, therefore, not to be taken in a limiting sense.

[0036] The present disclosure will be described herein below with reference to the accompanying drawings. In the following description, well known functions or constructions are not described in detail since they would obscure the description with unnecessary detail.

[0037] The present disclosure relates to a control unit for controlling voltage across a plurality of switching devices connected in series connection in a circuit. The disclosure is related to the control unit that controls the switching of the switching devices in such a way that the voltage across the switching devices is distributed in a balanced manner. The control unit ensures that the voltage balancing across the switching devices is
25 achieved while providing the fast switching speed. Thus, the present disclosure provides the control unit which is less complex and also does not require any characteristic information and voltage information of individual switching device.

[0038] Referring to figure 1, an exemplary circuit 100 is disclosed illustrating a control unit
30 for controlling voltage across a plurality of switching devices in accordance with an embodiment of the present disclosure. The circuit 100 may include control units 102a...102d, a switch-ON controller 104, switch-OFF controller 106, switching devices 108a...108d, voltage source 110 and a load 112, which are interconnected in the circuit 100. The switching devices 108a...108d may be any semiconductor
35 switching device such as MOSFET and IGBT, but not limited thereto. The switching

device 108a...108d may have fast switching capability and low switching losses. The switching devices 108a...108d may have a gate, a source and a drain terminal, which are coupled to voltage and/or current sources to control the operation of the switching devices 108a...108d. In the circuit 100, only four switching devices 108a...108d are shown for ease of understanding but the number of switching devices is not limited thereto.

[0039] In an exemplary embodiment, the control unit 102 controls the operation such all the switching devices 108a...108d operate in a synchronous manner to ensure balanced distribution of voltage across all the switching devices 108a...108d present in the circuit 100. Each control unit 102 may be configured to enable the corresponding switch-ON controller 104 and the switch-OFF controller 106 to control the voltage across the respective switching devices 108a...108d. The switch-ON controller 104 may control the switching ON operation of the respective switching device 108 and the switch-OFF controller 106 may control the switching OFF operation of the respective switching device 108.

[0040] In an exemplary embodiment, the control unit 102 may include a processing unit (not shown in figure 1) such as processor, microcontroller, microprocessor, FPGA, etc., but not limited thereto, and a memory to enable the switch-ON controller 104 and the switch-OFF controller 106 for controlling the operations of the switching devices 108. In an exemplary embodiment, the switch-ON controller 104 and the switch-OFF controller 106 may be either elements of the control unit 102 or may be separate elements than the control unit 102 which may be coupled with the control unit 102.

[0041] In another exemplary embodiment, the switch-ON controller 104 and the switch-OFF controller 106 may comprise a processing unit and a memory (not shown in figure 1), and may be connected to voltage and current sources (not shown in figure) in order to provide the appropriate voltage and current signals to the switching devices 108 for controlling the operation of the switching devices 108.

[0042] Fig. 2 shows a flow chart illustrating an exemplary method 200 of controlling voltage across the plurality of switching devices 108 in the circuit 100. The plurality of switching devices 108 are operated by a plurality of switch-ON controllers 104 and a plurality of switch-OFF controllers 106 in such a manner that each switching device

108 is operated by a corresponding switch-ON controller 104 and a corresponding switch-OFF controller 106. In an exemplary embodiment, the plurality of switching devices may comprise a first group of switching devices and a second group of switching devices. The first and second groups of switching devices may comprises
5 almost equal number of the switching devices.

[0043] At step 202, the control unit 102 may enable each switch-ON controller 104 to apply a gate-pulse to the gate of corresponding switching device. By applying the gate-pulse to the gate of the switching device 108 is charged with a small gate current. In an
10 exemplary embodiment, upon the detection of the turn-on gate pulse, the switch-ON controller may immediately apply a current with small magnitude to the switching devices if the switching devices is one of the first group of switching devices.

[0044] At step 204, the switch-ON controller 104 may detect increase in drain to source voltage
15 (V_{ds}) of the switching devices 108 and may determine whether the increase in the drain to source voltage (V_{ds}) is greater than a threshold voltage or not.

[0045] At step 206, upon detecting the increase in the drain to source voltage (V_{ds}) of the switching device 108 greater than the threshold voltage, a current with a first current
20 magnitude may be applied to switch ON the switching device 108. The magnitude of the current is large such that the switching device 108 is switched ON very fast. Due to fast switching ON of the switching device 108 the drain to source voltage V_{ds} is reduced, which results in increase of drain to source voltage (V_{ds}) of other switching devices connected in the series to the switching device 108. The switch-ON controllers of the
25 other switching devices detect this increase in the drain to source voltage. Therefore, the corresponding switch-ON controller also applies the large current to the series connected switching devices to switch ON these devices. Thus, all the series connected switching devices 108 are switched ON with large and same current flows through the switching devices 108 leading to fast turn-on transient. In a non-limiting exemplary
30 embodiment, the switch-ON controller of the switching device applies a current with a third current magnitude before applying the current with the first current magnitude to switch ON the switching device. Also, the switch-ON controllers of the other switching devices apply the current with the third current magnitude along with the current with the first current magnitude to switch ON the other switching devices. In this manner,

all series connected switching devices are switched ON in a synchronous manner. This also ensures the fast switching of the switching devices without any loss in switching speed.

- 5 **[0046]** At step 208 of the method 200, the control unit 102 may enable each switch-OFF controller 106 to apply a current with a second current magnitude to the gate to turn OFF the switching device 108. In response to applying current, the drain to source voltage (V_{ds}) starts increasing.
- 10 **[0047]** At step 210, the method describes that switch-OFF controller detects whether the drain to source voltage of the switching device 108 remains less than a second threshold voltage within a threshold time period or exceeds the second threshold voltage. If the drain to source voltage (V_{ds}) remains less than the second threshold voltage, at step 212, the switch-OFF controller 108 may apply a voltage to bias the gate of the switching
- 15 device to balance voltage of body diodes of the switching device 108. If the drain to source voltage (V_{ds}) exceeds that of the second threshold voltage then at step 214, the switch-OFF controller 108 may apply a current with a second current magnitude to the gate to turn OFF the switching device 108.
- 20 **[0048]** For explaining the above defined embodiments, let us consider a circuit as shown in Fig. 3. The circuit may comprise four switching devices (MOSFETs) (M1-M4) and operation of each MOSFET may be controlled by a separate control unit 102. The series-connected switching devices may be grouped into two different sets with an equal number of switching devices (+1/-1 device is allowed). These groups may be
- 25 named as the first group and the second group. In the case of only two switching devices in series as shown in Fig. 3. M1 forms the first group and M2 forms the second group. The direction of the load current is chosen such that devices M1 and M2 experience positive drain current and device M3 and M4 experience negative drain current.
- 30 **[0049]** Figure 4 illustrates the switch-ON switching waveform of the switching devices in accordance with an exemplary embodiment of the present disclosure. The switching ON process of the switching devices may be divided into 4 different stages (ST1 to ST4).

[0050] Referring back to figure 3, initially a gate pulse may be applied to the gate of the switching devices. Upon application of the gate pulse, the gate of the switching devices may be charged close to the threshold voltage i.e. to V_{n1} level as shown in ST1 (t_{n0} to t_{n1}) duration of Fig. 4. This reduces the net switch-ON delay time. After a set time duration, the switching device of the first group (M1) is charged with a small gate current (I_{n2}). This starts the second stage (ST2) of operation (t_{n1} to t_{n2}), due to the gate current, the V_{ds} voltage of the first group devices (V_{ds1}) fall. As the second group devices are not yet switched ON, their drain to source voltage (V_{ds}) increases to satisfy the Kirchhoff's voltage law (KVL) as the switching devices M3 and M4 are short. The switch-ON controller of the control unit 102 senses the increase of V_{ds} in the second group of devices. The switch-ON controller may sense rise in the V_{ds} by a drain to source voltage (V_{ds}) sensing unit. Upon sensing the rise in the V_{ds} , the switch-ON controller starts increasing sensed output as a response (V_{rs2} output during t_{n1} - t_{n2} duration of Fig. 4). Once the voltage V_{rs} crosses a threshold limit ($V_{rs_{th}}$). The switch-ON controller connected to the second group of devices apply a very large gate current ($I_{n2}+I_{n3}$) to the switching device M3. This starts the stage 3 (STG-3) mode of operation (t_{n2} - t_{n3} duration).

[0051] The STG-3 results in a scenario where first group switching device is switch-ON with very small gate current, and the second group switching device is switch-ON with very large gate current ($I_{n2}+I_{n3}$). The fast switching ON of the second group device reduces their V_{ds} voltage (V_{ds2}) and increases the V_{ds} of the first group device (V_{ds1}). The V_{rs} sensors of the first group device (V_{rs1}) increases its output as a response to the increase in V_{ds} . Once the V_{rs} (V_{rs1}) of the first group device rises beyond the set threshold ($V_{rs_{th}}$), the switch-ON controller of the first group device injects the larger gate current. Thus, all the switching devices from instant t_{n3} onwards will be driven with the same gate current. The remaining duration of the switching transient may be marked as a stage-4 mode of operation (ST4), in which the switching devices (M1 and M2) complete their switch-ON transient with large gate current in a synchronous fashion ($t_{n3} - t_{n5}$). At the end of the switch-ON transient, the voltage sensing unit (V_{rs}) outputs are reset to zero and held at zero till the start of the next switch-ON transient. At the rising edge of reset instant (t_{n5}), a resistive stage is applied to hold the gate voltage at a positive level.

[0052] In this manner, the synchronizing stages (ST2 and ST3) do not cause additional switching loss as the drain current flowing through the devices is nearly zero. Moreover, the large gate current used to switch-ON the switching devices in stage-4 (ST4) reduces the switching loss in the switching devices significantly. In accordance with an exemplary embodiment, the switching devices used for the first group and for the second group may be swapped for every switch-on transient in order to eliminate any disparity in the switching losses of the first group and second group devices.

[0053] Figure 5 of the present disclosure elucidated a physical realization of a switch-ON controller in accordance with a non-limiting exemplary embodiment of the present disclosure. Four gate driving stages may be used for this realization, those are ON-stage-1, ON-stage-2, ON-stage-3, and ON-stage-4. The ON-stage-1 is a switched voltage stage with V_{n1} voltage and is used for switch-ON delay time compensation during the ST1 mode of operation. The ON-stage-4 is a switched resistor stage and is used to hold the gate voltage at a high level from the reset instant of V_{rs} (t_5 in fig. 4) till the end of the ON gate pulse. The ON-stage-2 and ON-stage-3 are the synchronizing stages that inject I_{n2} and I_{n3} gate currents respectively. The ON-stage-3 is turned off whenever the V_{rs} signal exceeds a threshold voltage V_{rs_th} .

[0054] According to an exemplary embodiment, a comparator may be used to generate the gating pulse for ON-stage-3 as illustrated in figure 6. The gating pulse for ON-stage-2 may be generated by performing logical OR operation on the comparator output (V_{rs_cmp}) and the control signal generated by complex programmable logic device (CPLD) (S_{n2}). A control signal S_{n2} may be driven with a rising edge delayed ON gate pulse and S_{n2} drives the On-stage-2. According to exemplary embodiment, the control signal S_{n2} may be set permanently LOW. In such a case, the comparator output (V_{rs_cmp}) drives the ON-stage-2.

[0055] According to an exemplary embodiment, the “ V_{ds} rise sense” (V_{rs}) may be generated by the “Drain voltage rise sensing stage” (voltage sensing unit) shown in Fig. 6. This stage passes the V_{ds} voltage through a differentiator circuit. The output of the differentiator is passed through a half-wave rectifier to extract the positive-slope-only information of the V_{ds} voltage. This slope information is then passed through an integrator circuit to generate the V_{rs} signal which proportionately increases with the

increase in V_{ds} but does not reduce when V_{ds} reduces. The reset input of the integrator is used to reset the V_{rs} sense output.

[0056] Figure 7 illustrates an alternate implementation of the voltage rise sensing unit in accordance with a non-limiting embodiment of the present disclosure. The voltage sensing unit may comprise a capacitor C_d , a capacitor C_i , a switch SW_i and diodes D_{r1} and D_{r2} . The capacitor C_d is used to generate a current which is derivative of the V_{ds} voltage. The diodes D_{r1} and D_{r2} are used to rectify this current. The rectified current is integrated using the capacitor C_i to generate the desired V_{rs} sense output. The switch SW_i connected across the capacitor C_i is used to reset the sensed output (V_{rs}). Section 1 in figure is a differentiator, section 2 is half wave rectifier and section 3 is an integrator being implemented by the capacitors, diodes, switch.

[0057] Figure 8 illustrates an alternative implementation of the ON-stage-2 of the figure 5 and Drive Signal Generation block shown in figure 6 in accordance with a non-limiting embodiment of the present disclosure. The disclosed alternate implementation avoids the use of high-speed comparator, and thereby reduces the net propagation delay. In this implementation, the voltage rise sense signal (V_{rs}) is fed to a transconductance stage. This transconductance stage converts the V_{rs} signal into current and drives the gate of the switching device. A saturation block is used at V_{rs} to limit the gate current to desired value, which comprises a voltage source and a diode. The transconductance stage may be realized by using a voltage to current converter block followed by a current mirror stage. The S_{n2} signal in the first half of the switching devices may be driven with gate pulse signal. But in the second half of the gate drivers, the S_{n2} signal may be driven with a rising edge delayed gate pulse. The remaining control signals S_{n1} , S_{n3} and S_{n4} may be driven as described in earlier embodiments of the present disclosure.

[0058] Referring back to Fig. 3, if a negative current is forced through a switching device, the switching device would conduct irrespective of its applied gate voltage. This is due to the presence of the body-diode in the switching device. Even if the gate pulse to the device is removed when the negative current is flowing, the switching device will not experience any switching transient as the current starts flowing through the body diode. The body diode of the device would continue to conduct till the other devices in the phase-leg experience a turn-on transient. This is called as soft-tun-off transient. But this

soft-turn-off of the switching device is not controlled by its gate voltage, thus the voltage balancing among the switching device entirely relies upon the characteristic mismatch in the body-diodes and other parasitic present in the layout. This may impact the reliability of the series-connected devices if this issue is not taken care.

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[0059] In accordance with a non-limiting exemplary embodiment of the present disclosure, it is important to apply a control method to switch-OFF the switching devices according to the phase of the switching devices i.e., soft-turn-off transient and hard-turn-off transient phase. Initially, it is assumed that switching devices are hard switched, which means that the gate discharged with a large gate current upon application of a switch-OFF gate pulse to switch-OFF the switching devices. In the duration of gate discharging, the switch-OFF controller waits for the V_{ds} voltage to rise. However, if the V_{ds} voltage stays low till the end of a time duration, then the switching device is declared to be in soft-turn-off transient phase. If the V_{ds} voltage stays exceeded a threshold voltage till the end of a time duration, then the switching device is declared to be in hard-turn-off transient phase.

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[0060] Fig. 9 discloses a switching-OFF methodology to switch-OFF the switching devices in the hard-turn-off transient phase with the help of device voltage and current waveforms in accordance with a nonlimiting exemplary embodiment of the present disclosure. The control unit 108 may use a three-stage gate driver for achieving both fast switching and voltage balancing in series-connected switching devices. The first stage may be termed as “Fast driving stage” which is a switched current stage with a larger current magnitude. The first stage may be used to drive the switching devices during delay time and in voltage rise time. The second driving stage may be termed as the “Droop control stage” which is a switched analog current stage and is responsible for voltage equalization. The second driving stage is applied at the end of the voltage rise period and remains ON until the end of switch-OFF transient. The third driving stage is optional and is termed as “Holding stage”. The third switching stage is a switched resistor stage that is used to for holding the gate voltage. The third driving stage holds the gate with strong gate clamping so that false turn-on due to miller currents can be avoided.

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[0061] As shown in figure 9, the switch-OFF process is divided into three regions of operation i.e. R₁, R₂, and R₃, but not limited thereto. The region R₁ is defined as the duration in which all the control units operate in the “fast driving stage”. In region R₂, some of the control units operate in the “Fast driving stage” and the remaining operate in the “Droop control stage”. In region R₃, all the control units 108 operate in the “Droop control stage”. In figure 9, I_g represents gate current, I_{dsh} represents drain to source current in hard-turn-off transient phase, t_f represents time period, and V_{ds} represents drain to source voltage of the switching device.

[0062] At the start of turn-off gate pulse (t_{f0} in Fig. 9), all the control units 108 synchronously start discharging the gate voltage using the “Fast driving stage”, this marks the start of Region R₁. In spite of the synchronized driving, the voltage rise instant of each device may be different (t_{f1} for V_{ds1} and t_{f2} for V_{ds2} as shown in Fig. 9) due to the mismatches present in individual control unit and switching devices. Due to this, the switching device M1 (V_{ds1}) reaches its nominal voltage quickly (V_{ds1} = V_{DC}/2 at t_{f3} instant), and it switches to the “Droop control stage”. In this stage, M1 is charged with a smaller gate current (Start of R₂ shown in figure). During R₂, as shown in fig. 9, the switching devices blocking higher than the nominal voltage (V_{ds1} in Fig.9) are discharged slowly with the “Droop control stage”, and the devices blocking lower than nominal voltage are driven with larger gate current using “Fast driving stage” (V_{ds2} in Fig.6). This causes the switching devices, blocking lower than nominal voltage to quickly rise and complete the voltage rise period (V_{ds} = V_{DC}/2). After some time, all the switching devices rise their V_{ds} beyond the nominal voltage (t_{f3} in Fig.9). In this region R₃, the gate current injected through each switching device may be expressed as

$$I_{gj} = I_{f2} + k*(V_{dsj} - V_{DC}/2) \text{ ----- (1)}$$

Where the suffix j denotes the switching device M_j. From equation 1, it can be observed that the gate current of j_{th} device contains a droop term of its V_{ds} voltage. This causes a balancing effect, as the switching device with larger voltage would be discharged with smaller gate current and vice-versa. Thus, the devices blocking larger V_{ds} (V_{ds1}) slowly decrease and the devices blocking lower V_{ds} (V_{ds2}) slowly increase till they reach equal values (t_{f3} to t_{f4} duration in Fig. 9). This voltage balancing happens as long as the ratio of transconductance to the input capacitance of individual devices match to a

sufficiently good extent. The droop controller stage of each gate driver can be optionally turned off and a resistive stage can be applied for stronger gate clamping after the completion of switching transient.

[0063] Figure 10 of the present disclosure elucidates an exemplary physical realization of a switch-OFF controller for switching OFF the devices in hard-turn-off transient phase in accordance with a non-limiting exemplary embodiment of the present disclosure. The switch-OFF control method may be realized using two switched current stages (OFF-Stage-1 and OFF-Stage-2), one switched resistive stage (OFF-stage-3) and a controlled current source (Controlled current stage) as shown in figure 10. The OFF-Stage-1 determines the duration of the “Fast driving stage”. OFF-Stage-2 and Controlled current stage combined inject the required gate current during the “Droop Control stage” operation (Eq. 1). The OFF-Stage-2 provides the I_{f2} current in Eq. 1 and the Controlled current stage generates the remaining part.

[0064] At the start of the switch-OFF gate pulse, OFF-stage-1, OFF-Stage-2 and controlled current stages are turned ON (S_{f1} is set to high). But as $V_{ds} < V_{DC}/2$, the controlled current source may not inject any gate current ($k*(V_{ds} - V_{DC}/2)$). So, a net gate current of $I_{f1} + I_{f2}$ may flow through the device during the fast driving stage. The OFF-Stage-1 may be turned off when the V_{ds} comes close to the nominal voltage ($V_{DC}/2$). A voltage (V_{ds}) sensing stage, a comparator and an SR flip-flop may be used for turning OFF the OFF-Stage-1. After the V_{ds} becomes greater than $V_{DC}/2$, the controlled current source starts injecting positive current ($k*(V_{ds} - V_{DC}/2)$). In response, the OFF-stage-2 and the controlled current stage together inject the gate current described in Eq. 1 in above paragraphs of the specification. After the completion of switching transient, control signal S_{f1} is made low and S_{f2} is made high. This switches OFF the OFF-Stage-2, Controlled current stage and switches ON the resistive stage OFF-Stage-3. This way the switch-off transient of switching device may be implemented.

[0065] In the same embodiment, figure 10 also illustrates an OFF-Stage-1 driver section and control signal generation section. The OFF-Stage-1 driver section comprises a comparator, a voltage sensing unit comprising resistor and capacitor, an OR gate and a flip flop to provide control signal to the OFF-stages of the switch-OFF controller. The

control signal generation generates control signals to operate the various stages of the controller to ensure the voltage balancing across the switching devices in the circuit.

[0066] Fig. 11 depicts a configuration of circuit elements for realizing the required high bandwidth Controlled current stage in accordance with a nonlimiting exemplary embodiment of the present disclosure. The gate of the transistor Q_1 is driven using a V_{ds} sensing section. The source terminal of Q_1 is connected to a voltage source (V_{ks}) through a resistor-diode circuit as shown in Fig. 11. Thus, the current flowing through the resistor R_p , can be expressed as $K_1 * V_{ds} - V_{ks}$. Where K_1 is the attenuation Factor of the V_{ds} sensing section. The voltage source (V_{ks}) value is set close to the $K * V_{DC} * R_p / 2$ and the value of K_1 is set close to $k * R_p$. By these settings, a current of $k * (V_{ds} - V_{DC} / 2)$ is realized in the resistor R_p . The current flowing through R_p is mirrored using a current mirror to drive the gate of the switching device. The transistor Q_2 is a matched pair of Q_1 and is used to compensate for the threshold voltage of the transistor Q_1 .

[0067] Fig. 12 discloses a switching-OFF methodology to switch-OFF the switching devices in the soft-turn-off transient phase with the help of device voltage and current waveforms in accordance with an exemplary embodiment of the present disclosure. In the proposed control, the voltage balancing in the devices is achieved by appropriately biasing gate voltage during the miller (dv/dt) region. However, it is important to apply this control method only during the soft-turn-off switching and not during the hard-turn-off switching. So, the operation of the proposed control may be divided into three different phases of operations. They are, Soft-turn-off detection phase, Gate voltage biasing phase. Miller (dv/dt) injection phase.

[0068] These phases of operations are explained by considering the soft-turn-off switching of devices M3 and M4 (Fig 1). The "Soft-turn-off detection" (PH1 in fig 12) phase starts at t_{d0} (Fig 12) instant where the turn off gate pulse is applied to M3 and M4. During PH1 the gate is driven assuming that it is hard switched, which means that the gate discharged with a large gate current of $(I_{f1} + I_{f2})$. In this duration of gate discharging (t_{d0} - t_{d1} of Fig. 12), the switch-OFF controller waits for the V_{ds} voltage to rise (V_{ds} signal to go high). The switching waveform depicted in Fig. 12 is divided into three different durations. If the V_{ds} continues to stay low till the end of the dead time duration (t_{d1} instant of Fig. 12), then the swicth-OFF controller declares the current switching

transient as soft-turn-off transient. This marks the end of the “soft-turn-off detection phase” and marks the beginning of the “gate voltage biasing phase” (PH2 ($t_{d1} - t_{d2}$)). In this duration, the respective controllers bias the gate voltages of devices M3 and M4 to an intermediate voltage level of V_{gb3} and V_{gb4} respectively.

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[0069] The gate voltage biasing is kept in effect until the completion of the turn-OFF of the body diodes. Wherein, the turn-OFF of the body diodes of M3 and M4 is caused by the turn ON of the M1 and M2 (Fig.1) and is initiated after the dead time (t_{d1} in Fig. 12). The turn-ON of M1 and M2 devices cause the I_{dss} to increase from a negative value to zero (t_{d2} of Fig. 12). This starts the reverse recovery of the body diodes of M3 and M4, and their voltage starts increasing. However, it is assumed that V_{ds3} rises faster than V_{ds4} due to mismatch in the body diodes. But the values of gate voltage biasing of M3 (V_{gb3}) and M4 (V_{gb4}) are adjusted such that both devices block equal voltage in the steady state. This is achieved by adjusting the level of (V_{gb3}) such that the V_{gs3} crosses the VTH at an appropriate instant such that voltage balancing happens (t_{d3} instant in Fig. 12). After the completion of the voltage rise (t_{d4} in Fig. 12), the gate biasing stage is turned off and the turn-off holding is applied to hold the gate voltage at the recommended negative level.

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[0070] Figure 13 illustrates an exemplary physical realization of switch-OFF controller for soft-turn-off the switching devices in accordance with a non-limiting exemplary embodiment of the present disclosure. As shown in Fig. 13, the switch-OFF controller may be realized into the gate-biasing section and V_{ds} sensing section. The gate biasing section is implemented by a switched voltage stage and a switched current source. The voltage level of the switched voltage stage can be digitally controlled (DAC_{out}) to exercise the precise adjustment of the V_{gb} level. The switched current source I_{f3} is set such that, the magnitude of miller injection into the gate of the device can be limited to a controllable level.

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[0071] To appropriately control the value of the V_{gb} , the voltage blocked during every soft-turn-off switching is sampled using an analog to digital convertor (ADC). The output of the ADC is sent to a central controller for implementing a closed-loop controller. The controller updates the V_{gb} value such that the device voltage in the next soft-turn-off switching can be regulated. The controller output is saturated between V_{gb_max} and

V_{gb_min} limits. The controller reference is set a little higher than the nominal voltage of the device, this is done to minimize the power loss incurred in the switching devices. In an exemplary embodiment, the switch-OFF controller may also be implemented in an alternative fashion, i.e., by fixing the V_{gb} value and varying the I_{f3} current.

5 [0072] In this manner, the control unit 102 may enable the switch-ON and the switch-OFF controllers to operate switching devices at fast switching speed with gate pulse information alone. Also, the described method may be directly employed for series connecting any number of switching devices without needing to change the control in
10 any way. The implemented method is very robust as each the control unit operates independently to each other with very little dependence on the control signals. The proposed voltage controlling method achieves voltage balancing during the hard switching transients as well as during the soft switching transients.

15 [0073] Figure 14 illustrates a control unit 302 for controlling voltage across a plurality of switching devices connected in series connection in a circuit in accordance with a non-limiting embodiment of present disclosure. The control unit 302 may comprise a switch-ON controller 304 and a switch-OFF controller 306, a processing unit 308, and a memory 310. The switch-ON controller 304, the switch-OFF controller 306, the
20 processing unit 308, and the memory 310 may communicate with each other over wired or wireless link. The processing unit 310 may comprise one or more processors. According to an exemplary embodiment of the present disclosure, the switch-ON controller 304 and the switch-OFF controller 306 may be individual entities different from the control unit 302. Each of the switch-ON controller 304 and the switch-OFF
25 controller 306 may comprise a voltage sensing unit, which may sense the voltage level between the terminals (the gate, source and drain) of the switching devices.

[0074] The control unit 302 may enable the switch-ON controller 304 and the switch-OFF controller 306 to control the voltage across the plurality of switching devices during
30 switch-ON and switch-OFF transient phase of the switching devices. In an exemplary embodiment, the plurality of switching devices may comprise at least a first group of switching devices and a second group of switching devices. Each switching device may be controlled by a separate control unit 302 and each switching device have a gate, a source and a drain.

[0075] According to a non-limiting exemplary embodiment, the control unit 302 may enable the switch-ON controller 304 to apply a switch-ON gate-pulse to the gate of the switching device. By applying the switch-ON gate-pulse, the gate is charged close to a voltage level, which reduces the net turn-on delay time. In an exemplary embodiment, upon the detection of the turn-on gate pulse, the switch-ON controller may immediately apply a current with small magnitude to the switching device if the switching device is one of the first group of switching devices.

[0076] In the same embodiment, the switch-ON controller 304 may detect whether increase in drain to source voltage (V_{ds}) of the switching device is greater than a first threshold voltage. Upon detecting the increase in the drain to source voltage (V_{ds}) of the switching device greater than the first threshold voltage, the switch-ON controller 304 may apply a current with a first current magnitude to switch ON the switching device. In an exemplary embodiment, the switch-ON controller may apply the current with the small current magnitude along with the current with the first current magnitude to switch ON the switching device if the switching device is one of the second group of the switching devices,

[0077] According to an exemplary embodiment, the switch-ON controller may comprise a first voltage sensing unit to detect the increase in the drain to source voltage (V_{ds}) upon applying the switch-ON gate-pulse. The first voltage sensing unit may comprise at least a differentiator, a positive half wave rectifier, and an integrator as shown in figures 6 and 7.

[0078] In the same embodiment, the control unit 302 may enable the switch-OFF controller 306 to apply a switch-OFF gate-pulse to the gate of the switching device. The switch-OFF controller 306 may detect whether the drain to source voltage (V_{ds}) of the switching device remains less than a second threshold voltage within a threshold time period. Based upon the detecting, the switch-OFF controller may determine whether the switching devices is in a hard-turn-off transient phase or in a soft-turn-off transient phase. It is important to determine the transient phase of switching device because the switching device in soft-turn-off transient phase cannot be not controlled by its gate voltage.

[0079] In the same embodiment, if a negative current is forced through a switching device, the switching device would conduct irrespective of its applied gate voltage. This is due to the presence of the body-diode in the switching device. Even if the gate pulse to the device is removed when the negative current is flowing, the switching device will not experience any switching transient as the current starts flowing through the body diode. The body diode of the device would continue to conduct till the other devices in the phase-leg experience a turn-on transient. This is called as soft-turn-off transient. But this soft-turn-off of the switching device is not controlled by its gate voltage, thus the voltage balancing among the switching device entirely relies upon the characteristic mismatch in the body-diodes and other parasitic present in the layout. This may impact the reliability of the series-connected devices if this issue is not taken care.

[0080] According to an exemplary embodiment, if the drain to source voltage (V_{ds}) of the switching device remains less than the second threshold voltage within the threshold time period, then the switching device may be considered to be in soft-turn-off transient phase. The threshold time period may be time period t_{d1} as defined in figure 12 and therefore, the switching device may not be controlled by its gate voltage and may only be controlled by controlling the operation of body-diodes of the switching device. Also, if the drain to source voltage (V_{ds}) of the switching device exceeds the second threshold voltage within the threshold time period, then the switching device may be considered to be in hard-turn-off transient phase.

[0081] Accordingly, based upon detecting that the drain to source voltage (V_{ds}) of the switching device remains less than the second threshold voltage within the threshold time period, the switch-OFF controller 306 may apply a voltage to bias the gate of the switching device to balance voltage of body diodes of the switching device. The voltage may be gate to body voltage (V_{gb}) being applied between the gate and source of the switching devices in order to tweak the turning-off of the body-diodes of the switching device.

[0082] According to another non-limiting exemplary embodiment, based upon detecting that the drain to source voltage (V_{ds}) of the switching device exceeds the second threshold voltage within the threshold time period, the switch-OFF controller 306 may apply a current with a second current magnitude to the gate to turn OFF the switching device.

In an exemplary embodiment, the switch-OFF controller 306 may comprise a second voltage sensing unit to detect increase in the drain to source voltage (V_{ds}) upon applying the switch-OFF gate-pulse. The second voltage sensing unit may comprise at least one resistor and capacitor in parallel connection as illustrated in detail in figure 13.

5 [0083] In an exemplary embodiment, the values of gate voltage biasing of the switching device may be adjusted such that the switching device block a voltage in the steady state which is equal to the voltage blocked by other switching devices in the circuit. This is achieved by adjusting the level of V_{gb} such that the V_{gs} crosses the V_{TH} (shown in figure 12) at
10 an appropriate instant such that voltage balancing happens i.e. t_{d3} instant as shown in Fig. 12. Thus, by applying the voltage to bias the gate of the switching device enables the switching device and remaining switching devices of the plurality of switching devices to remain in steady state with same voltage.

15 [0084] In this manner, the control unit 302 may enable the switch-ON controller 304 and the switch-OFF controller 306 to operate switching devices at fast switching speed with gate pulse information alone. Also, the control unit 302 may be directly employed for series connecting any number of switching devices without needing to change the control in any way. Also, each the control unit 302 operates independently to each other
20 with very little dependence control signals. Further, the control unit 302 may achieves voltage balancing during the transient phase as well and the voltage imbalance due the mismatch in the characteristics of the body diode as well as other parasitic effects can also be compensated.

25 [0085] The illustrated steps are set out to explain the exemplary embodiments shown, and it should be anticipated that ongoing technological development will change the manner in which particular functions are performed. These examples are presented herein for purposes of illustration, and not limitation. Further, the boundaries of the functional building blocks have been arbitrarily defined herein for the convenience of the
30 description. Alternative boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0086] Alternatives (including equivalents, extensions, variations, deviations, etc., of those described herein) will be apparent to persons skilled in the relevant art(s) based on the

teachings contained herein. Such alternatives fall within the scope and spirit of the disclosed embodiments.

[0087] Furthermore, one or more computer-readable storage media may be utilized in implementing embodiments consistent with the present disclosure. A computer-readable storage medium refers to any type of physical memory on which information or data readable by a processor may be stored. Thus, a computer-readable storage medium may store instructions for execution by one or more processors, including instructions for causing the processor(s) to perform steps or stages consistent with the embodiments described herein. The term “computer- readable medium” should be understood to include tangible items and exclude carrier waves and transient signals, i.e., are non-transitory. Examples include random access memory (RAM), read-only memory (ROM), volatile memory, non-volatile memory, hard drives, CD ROMs, DVDs, flash drives, disks, and any other known physical storage media.

[0088] Suitable processors include, by way of example, a general-purpose processor, a special purpose processor, a conventional processor, a digital signal processor (DSP), a plurality of microprocessors, one or more microprocessors in association with a DSP core, a controller, a microcontroller, Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs) circuits, any other type of integrated circuit (IC), and/or a state machine.

[0089] Exemplary embodiments discussed above may provide certain advantages. Though not required to practice aspects of the disclosure, these advantages may include those provided by the following features.

[0090] In an embodiment, the present disclosure describes the control unit that may achieve to operate the switching devices at the fast switching speed with gate pulse information alone.

[0091] In an embodiment, the controlling method can be directly employed for series connecting any number of switching devices without needing to change the control in any way. Thus, by employing the controlling method, a generic gate driver can be made for any voltage-source series-connection application.

[0092] In an embodiment, the described techniques may be realized at a low cost as its control implementation is simpler, and it does not require additional optical cables for its operation.

5 [0093] In an embodiment, unlike the low-frequency control of series-connected devices, the proposed method and control unit provide control at the switching transient time itself. Thus, the proposed method is more immune to gate pulse jitter, compared to other low-frequency control methods whose operation is heavily dependent on gate pulse jitter.

10 [0094] In an embodiment, implemented method is very robust as each control unit operates independently to each other with very little dependence control signals.

[0095] In an embodiment, methodology achieves voltage balancing during the soft-turn-off switching transient as well. The voltage imbalance due the mismatch in the
15 characteristics of the body diode as well as other parasitic effects can also be compensated.

[0096] In an embodiment, when properly adjusted, the turn-off controller has the capacity to clamp voltage overshoot in the switching device to a safe limit. Thus, the gate clamping
20 Zener-diodes are not mandatory for the proposed methodology.

[0097] In an embodiment, the present method and control unit improve the robustness and the reliability of the switching device.

The Claims:

1. A control unit for controlling voltage across a plurality of switching devices present in a circuit, wherein each switching device having a gate, a source and a drain, and wherein the plurality of switching devices are operated by a plurality of switch-ON controllers and a plurality of switch-OFF controllers in such a manner that each switching device is operated by a corresponding switch-ON controller and a corresponding switch-OFF controller,

and wherein the control unit is configured to enable each switch-ON controller to:

apply a switch-ON gate-pulse to the gate of corresponding switching device,

detect whether increase in drain to source voltage (V_{ds}) of the switching device is greater than a first threshold voltage, and

apply, upon detecting the increase in the drain to source voltage (V_{ds}) of the switching device greater than the first threshold voltage, a current with a first current magnitude to switch ON the switching device;

and wherein the control unit is further configured to enable each switch-OFF controller to:

apply a switch-OFF gate pulse to the gate of the switching device,

detect whether the drain to source voltage (V_{ds}) of the switching device remains less than a second threshold voltage within a threshold time period, wherein the switch-OFF controller, based upon the detecting, is configured to perform at least one of:

applying a voltage to bias the gate of the switching device to balance voltage of body diodes of the switching device, upon detecting that the drain to source voltage (V_{ds}) of the switching device remains less than the second threshold voltage within the threshold time period, and

applying a current with a second current magnitude to the gate to turn OFF the switching device, upon detecting that the drain to source voltage (V_{ds}) of the switching device exceeds the second threshold voltage within the threshold time period.

2. The control unit as claimed in claim 1, wherein the switch-ON gate-pulse charges the gate to a third threshold voltage to reduce turn-on delay time.

3. The control unit as claimed in claim 1, wherein the switch-ON controller further comprises a first voltage sensing unit to detect increase in the drain to source voltage

(V_{ds}) upon applying the switch-ON gate-pulse, wherein the first voltage sensing unit comprises at least a differentiator, a positive half wave rectifier, and an integrator.

4. The control unit as claimed in claim 1, wherein the switch-OFF controller further comprises a second voltage sensing unit to detect increase in the drain to source voltage (V_{ds}) upon applying the switch-OFF gate-pulse, and wherein the second voltage sensing unit comprises at least one resistor and capacitor in parallel connection.

5. The control unit as claimed in claim 1, wherein the applying, by the switch-OFF controller, of the voltage to bias the gate of the switching device enables the remaining switching devices, of the plurality of switching devices, to remain in steady state with same voltage.

6. The control unit as claimed in claim 1, wherein the plurality of switching devices comprises at least a first group of switching devices and a second group of switching devices, and

wherein the switch-ON controller is configured to perform at least one:

applying, if the switching device is one of the first group of the switching devices, a current with a third current magnitude before applying the current with the first current magnitude to switch ON the switching device, and

applying, if the switching device is one of the second group of the switching devices, the current with the third current magnitude along with the current with the first current magnitude to switch ON the switching device.

7. A method to be performed by a control unit for controlling voltage across a plurality of switching devices present in a circuit, wherein each switching device having a gate, a source and a drain, and wherein the plurality of switching devices are operated by a plurality of switch-ON controllers and a plurality of switch-OFF controllers in such a manner that each switching device is operated by a corresponding switch-ON controller and a corresponding switch-OFF controller, the method comprises:

enabling each switch-ON controller, by the control unit, to apply a switch-ON gate-pulse to the gate of corresponding switching device,

detecting, by the switch-ON controller, whether increase in the drain to source voltage (V_{ds}) of the switching device is greater than a first threshold voltage, and

applying, by the switch-ON controller, upon detecting the increase in the drain to source voltage (V_{ds}) of the switching device greater than the first threshold voltage, a current with a first current magnitude to switch ON the switching device; and

enabling each switch-OFF controller, by the control unit, to apply a switch-OFF gate-pulse to the gate of the switching device, and

detecting whether the drain to source voltage (V_{ds}) of the switching device remains less than a second threshold voltage within a threshold time period, wherein the method further comprises performing, based upon the detecting, at least one:

applying, by the switch-OFF controller, a voltage to bias the gate of the switching device to balance voltage of body diodes of the switching device, upon detecting that the drain to source voltage (V_{ds}) of the switching device remains less than the second threshold voltage within the threshold time period, and

applying, by the switch-OFF controller, a current with a second current magnitude to the gate to turn OFF the switching device, upon detecting that the drain to source voltage (V_{ds}) of the switching device exceeds the second threshold voltage within the threshold time period.

8. The method as claimed in claim 7, wherein the switch-ON gate-pulse charges the gate to a third threshold voltage to reduce turn-on delay time.

9. The method as claimed in claim 7, wherein the switch-ON controller further comprises a first voltage sensing unit to detect increases with increase in the drain to source voltage (V_{ds}) upon applying the switch-ON gate-pulse, wherein the first voltage sensing unit comprises at least a differentiator, a positive half wave rectifier, and an integrator.

10. The method as claimed in claim 7, wherein the switch-OFF controller further comprises a second voltage sensing unit to detect increase in the drain to source voltage (V_{ds}) upon applying the switch-OFF gate-pulse, and wherein the second voltage sensing unit comprises at least one resistor and capacitor in parallel.

11. The method as claimed in claim 7, wherein the applying, by the switch-OFF controller, of the voltage to bias the gate of the switching device enables the remaining

switching devices, of the plurality of switching devices, to remain in steady state with same voltage.

12. The method as claimed in claim 7, wherein the plurality of switching devices comprises at least a first group of switching devices and a second group of switching devices, and

wherein the method further comprises performing one of:

applying, by the switch-ON controller, if the switching device is one of the first group of the switching devices, a current with a third current magnitude before applying the current with the first current magnitude to switch ON the switching device, and

applying, by the switch-ON controller, if the switching device is one of the second group of the switching devices, the current with the third current magnitude along with the current with the first current magnitude to switch ON the switching device.

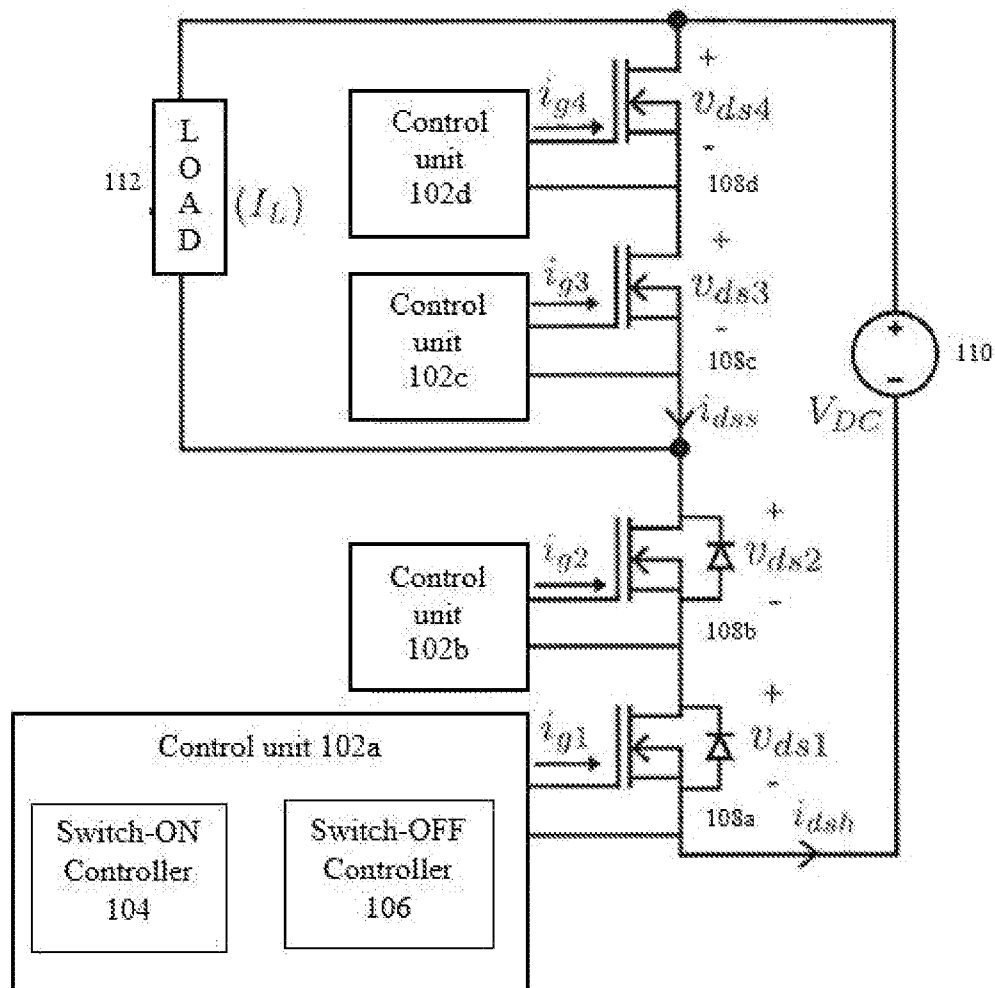
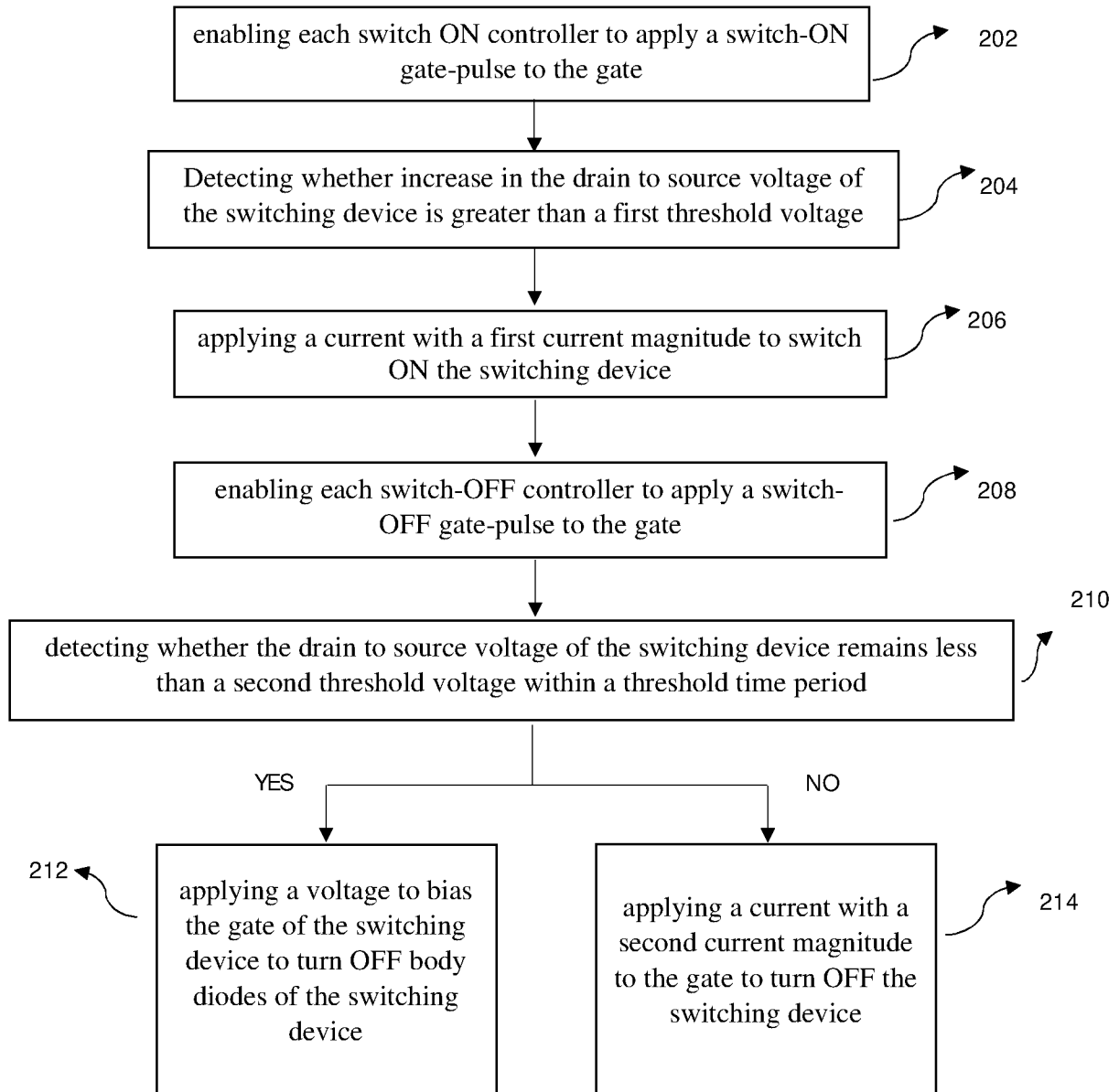


FIG. 1

200**FIG. 2**

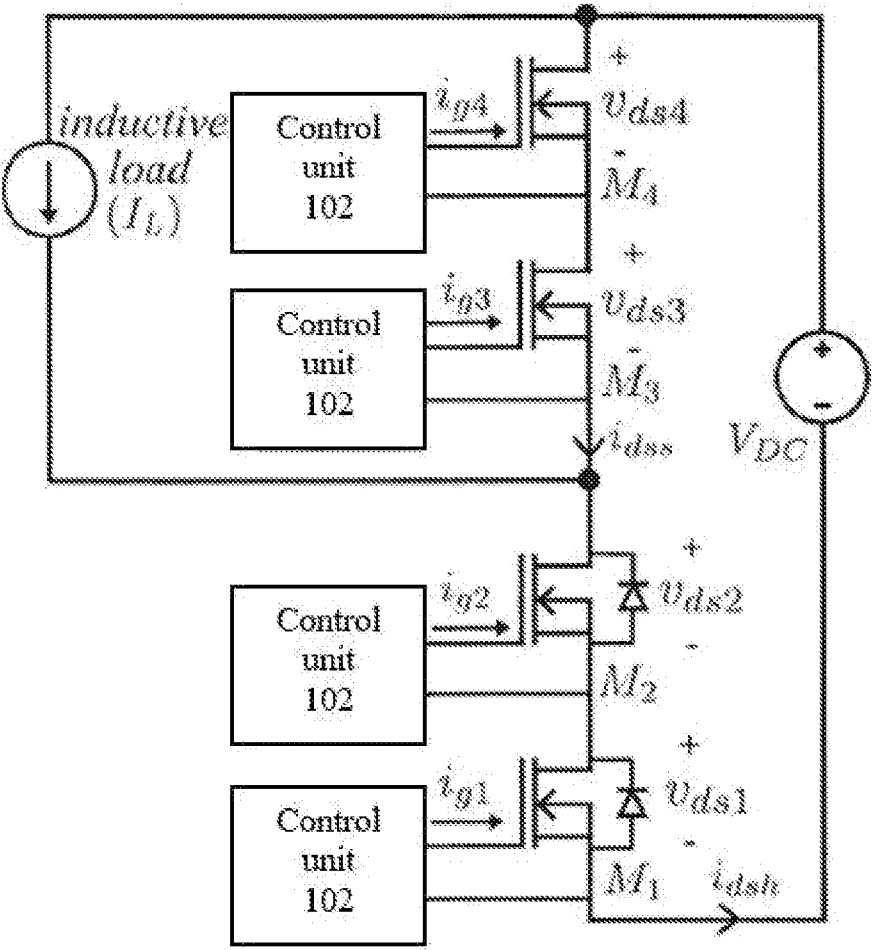


FIG. 3

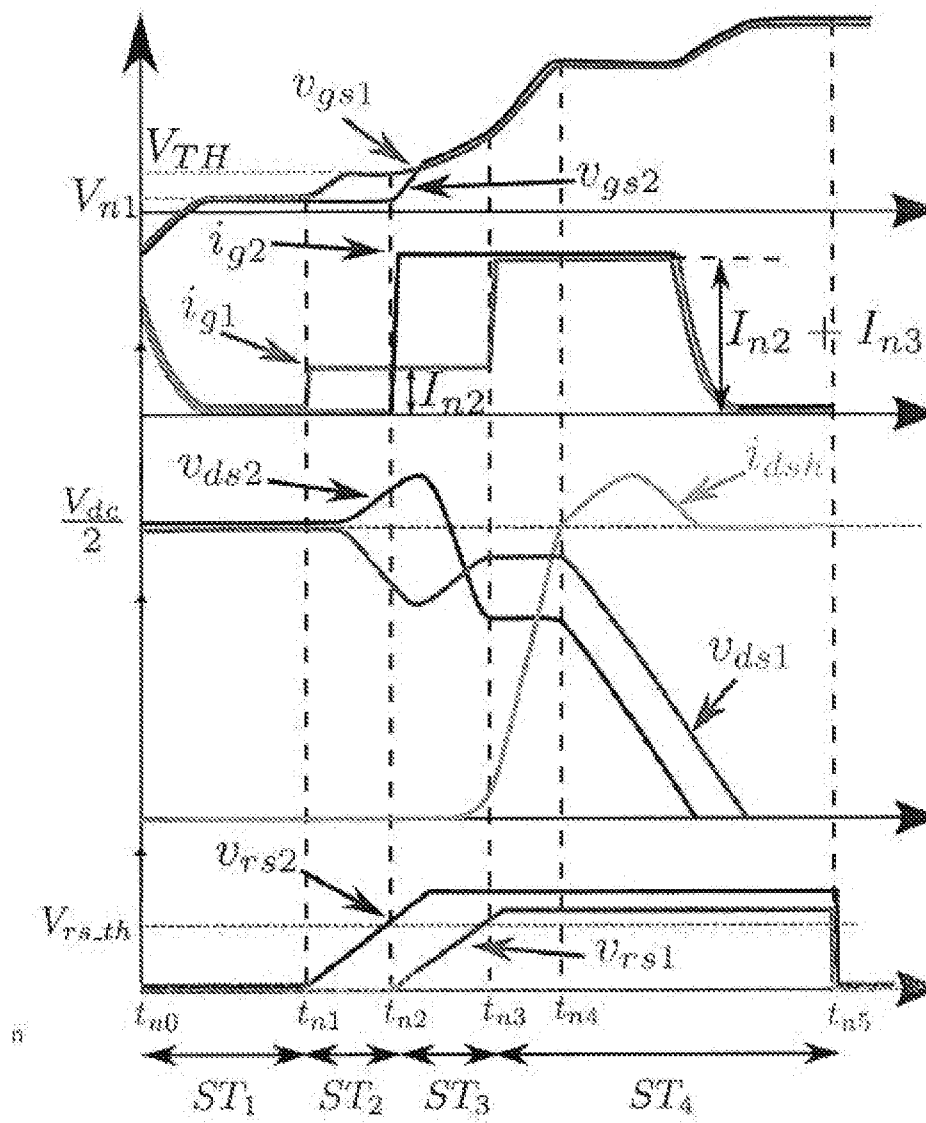


FIG. 4

Gate Driving Stages

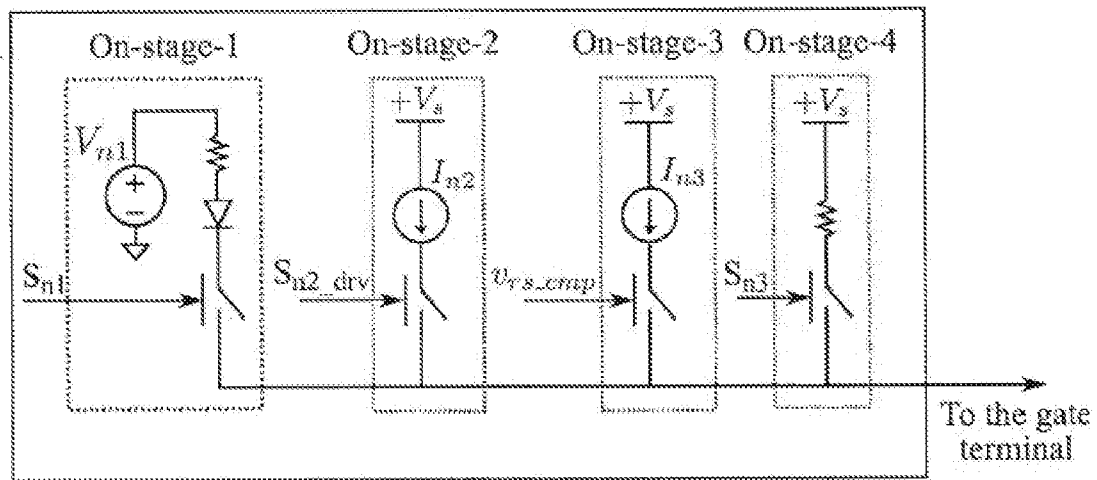


FIG. 5

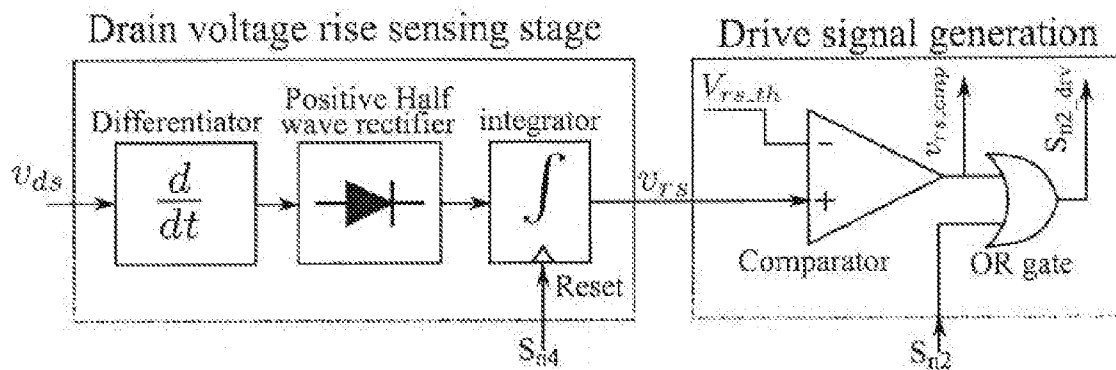


FIG. 6

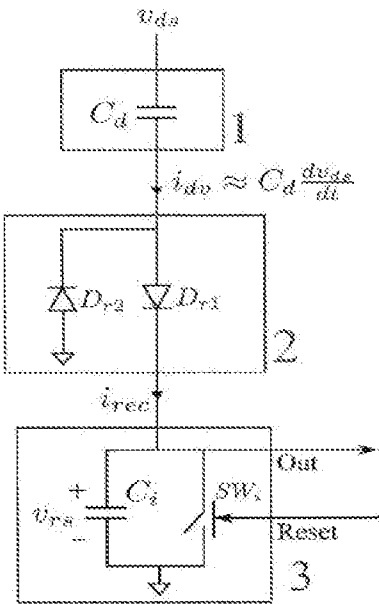


FIG.7

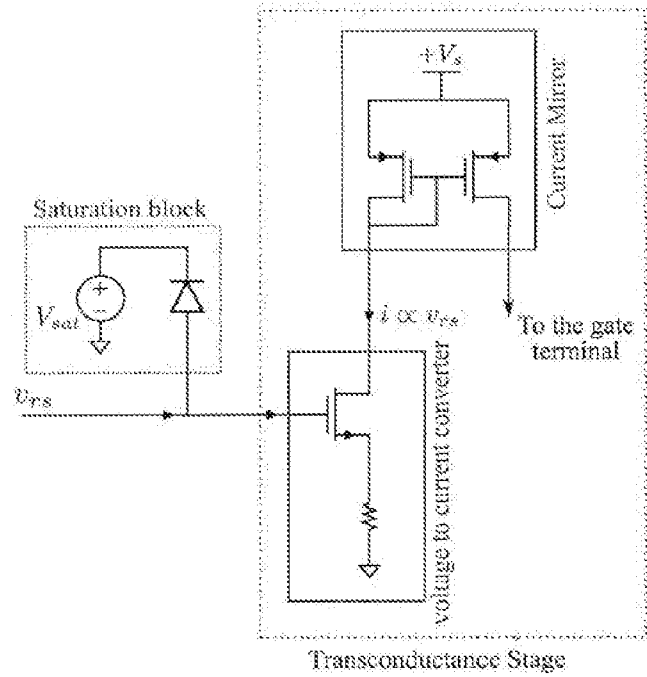
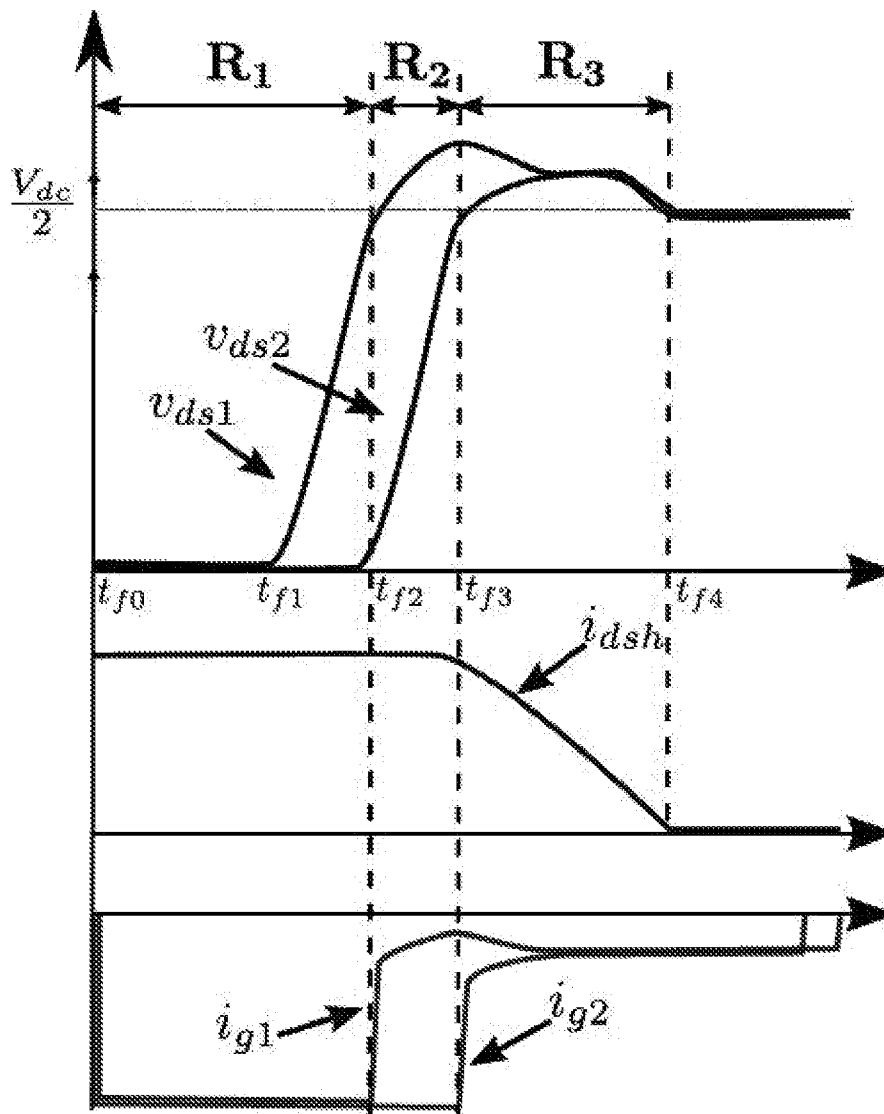


FIG.8

FIG. 9



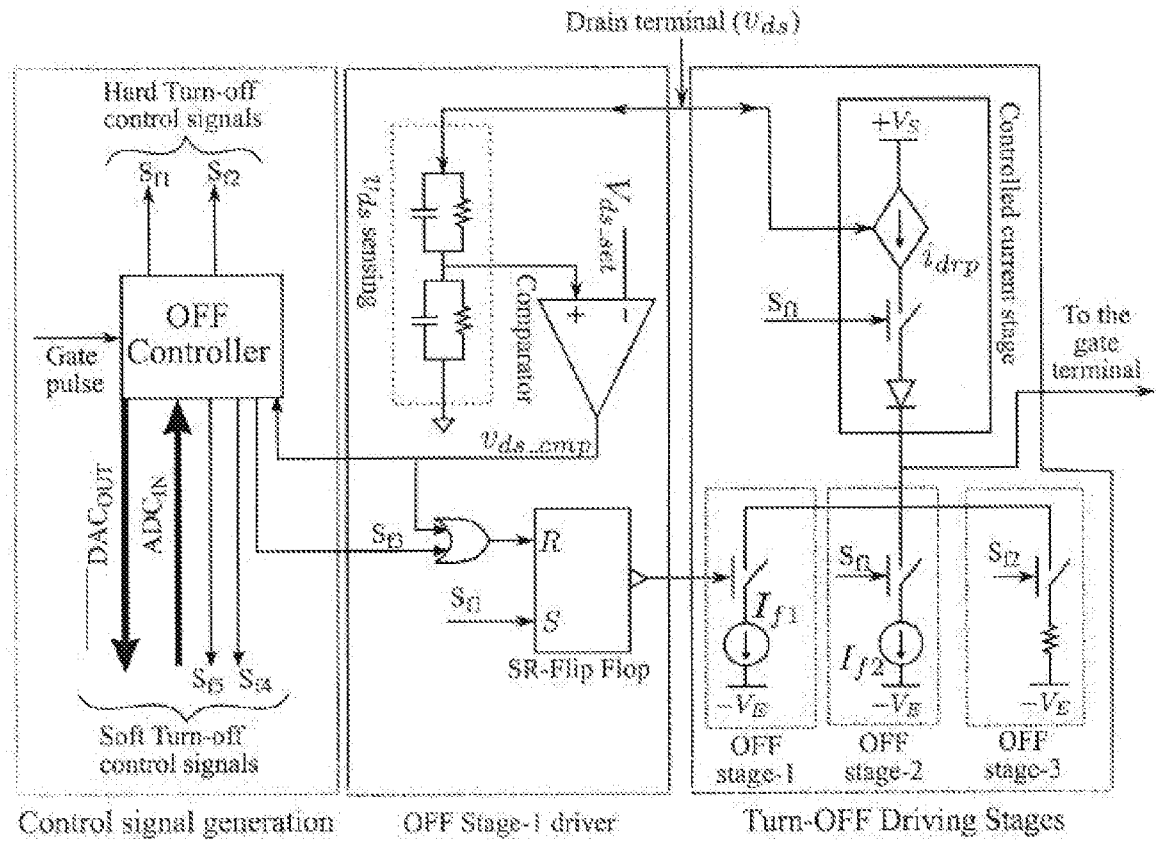


FIG.10

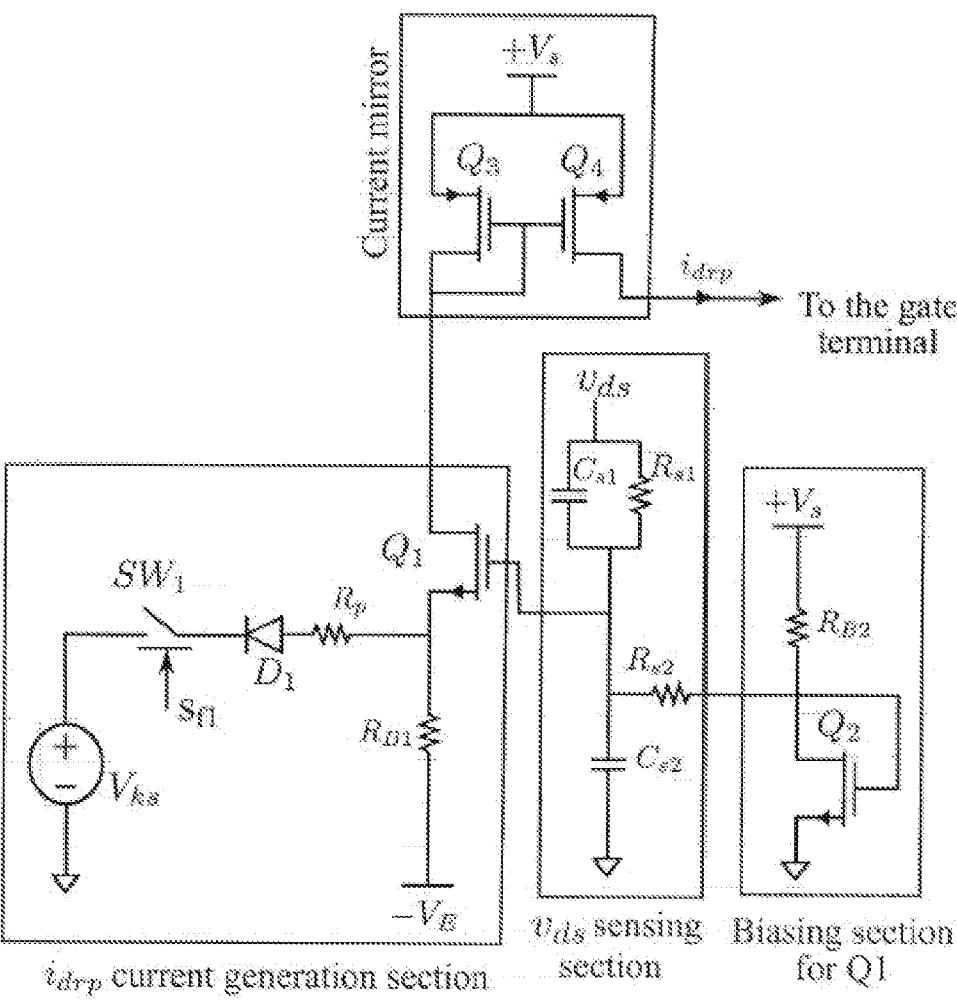


FIG. 11

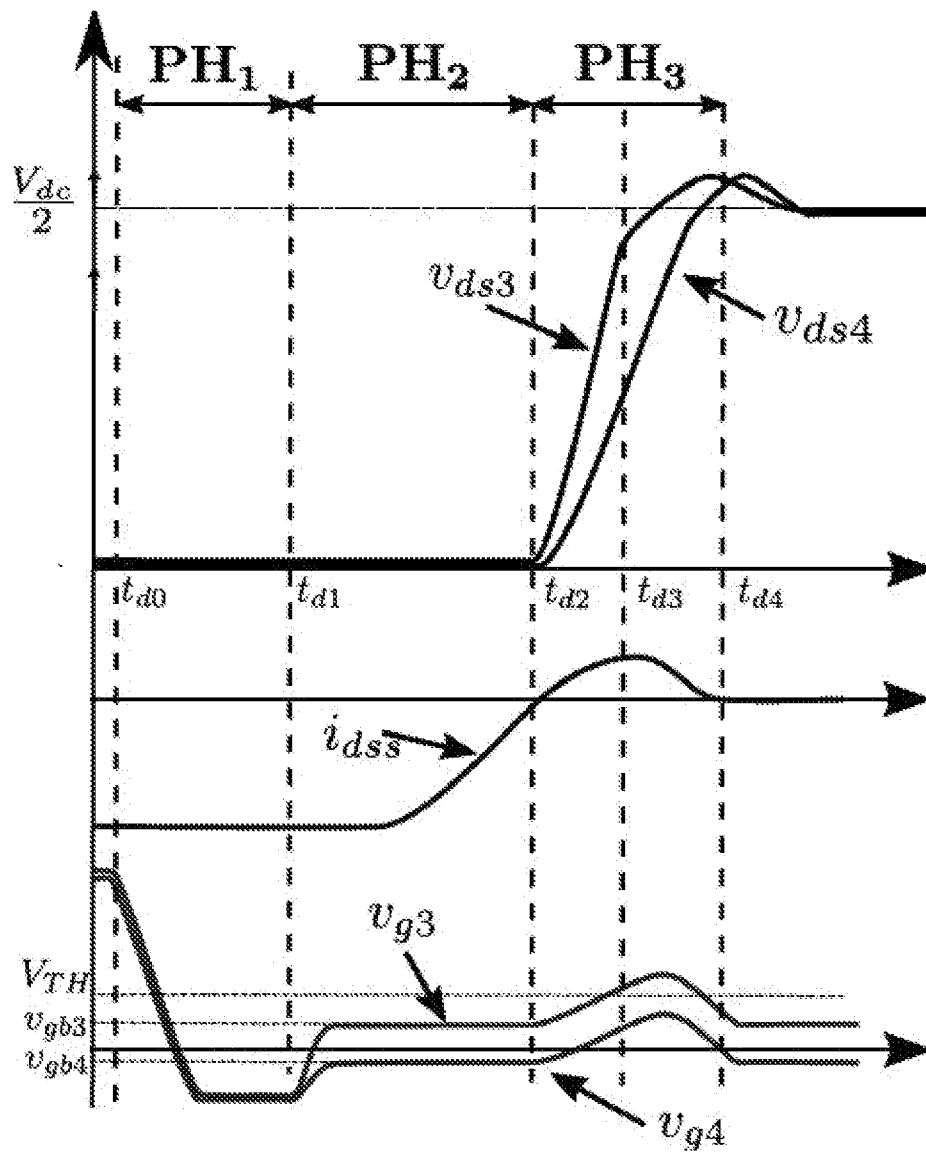


FIG. 12

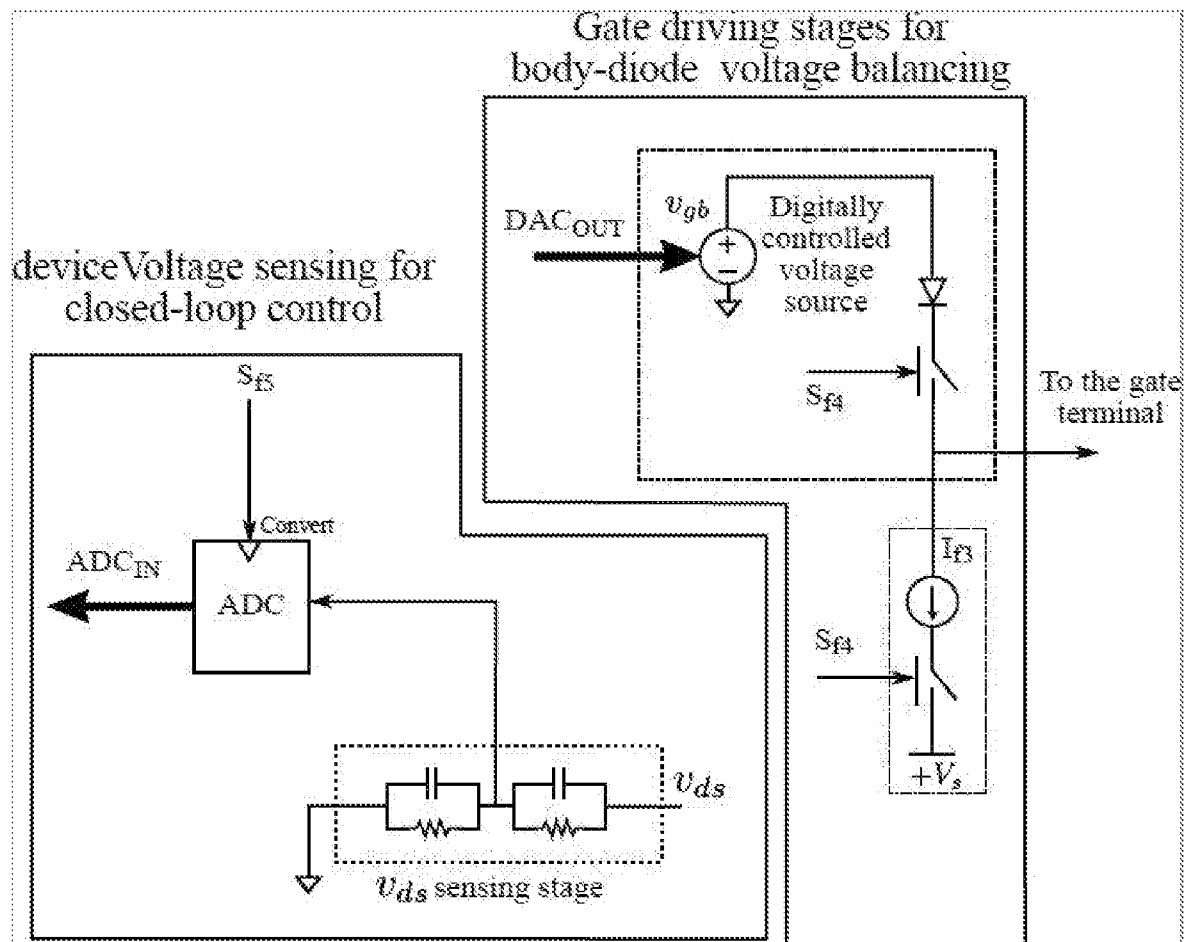


FIG. 13

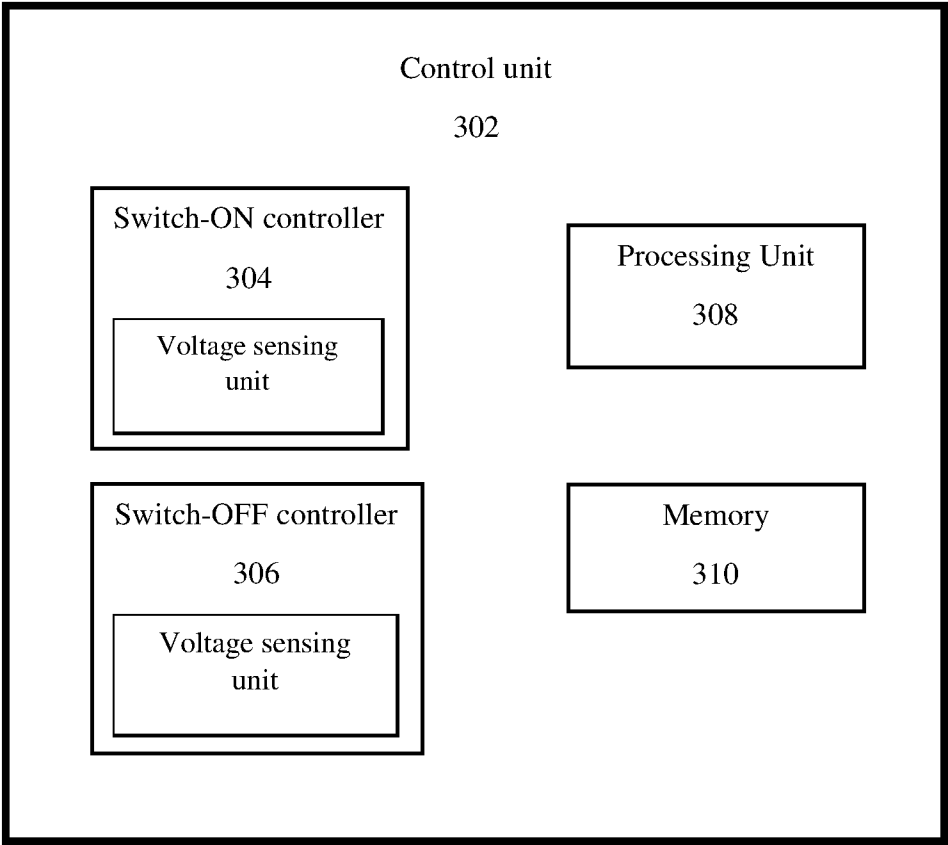


FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IN2021/050703

A. CLASSIFICATION OF SUBJECT MATTER
H02M1/08, H03K17/16 Version=2021.01

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M, H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases: PatSeer, IPO Internal Database,
Keywords: Switching device, Controller, Transistor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 20120176827 A1 (RENESAS ELECTRONIC CORP), 12 JULY 2012 (12-07-2012), Whole document	1-12
Y	US 20200036371 A1 (FURUKAWA CO GROUP), 30 JANUARY 2020 (30-01-2020), Whole document	1-12
Y	US 20180062633 A1 (FURUKAWA CO GROUP), 01 MARCH 2018 (01-03-2018), Abstract; Figs. 4, 15-17; Paragraphs [0009], [0040], [0042], [0046]-[0048], [0079]; Claims 1-7	1-12

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

22-11-2021

Date of mailing of the international search report

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Indian Patent Office
Plot No.32, Sector 14, Dwarka, New Delhi-110075
Facsimile No.

Authorized officer

Md. Tanveer Ur Rahman
Telephone No. +91-1125300200

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/IN2021/050703

Citation	Pub.Date	Family	Pub.Date
US 20120176827 A1	12-07-2012	US 8681514 B2	25-03-2014
		WO 2012096829 A2	19-07-2012
		WO 2012096829 A3	18-10-2012
US 20200036371 A1	30-01-2020	US 10547300 B1	28-01-2020
		JP 6451890 B1	16-01-2019
		CN 110098723 B	30-06-2020
		DE 102019114881 B4	11-02-2021
US 2018062633 A1	01-03-2018	US 10554202 B2	04-02-2020
		CN 107786075 B	14-09-2021
		JP 6870240 B2	12-05-2021
		DE 102017006230 A1	01-03-2018