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[Continued on next page]

(54) Title: LOW POWER ULTRA LOW DRIFT DC CURRENT SOURCE

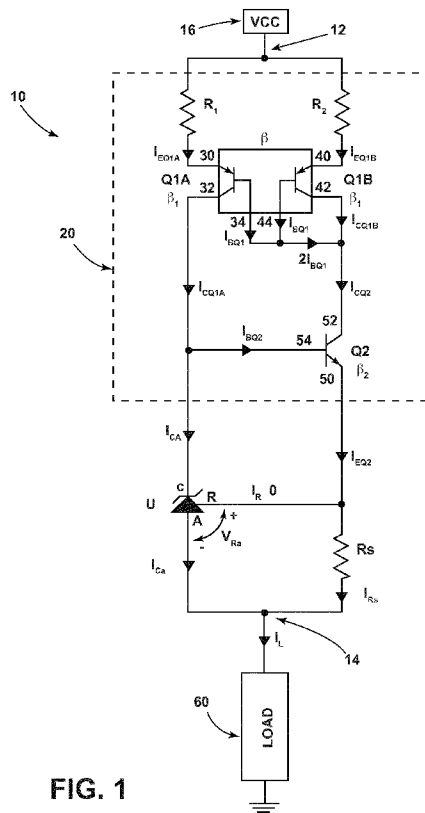


FIG. 1

(57) Abstract: An electrical current source includes an input terminal, an output terminal, a current mirror that may be connected to the input terminal, a shunt regulator that may be connected to the current mirror and the output terminal, and a setting resistor that may be connected to the current mirror, the shunt regulator, and the output terminal. The input terminal may be configured for connection with an input power source. The electrical current source may be configured to provide an output current according to a reference voltage of the shunt regulator and a resistance of the setting resistor.

**Declarations under Rule 4.17:**

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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LOW POWER ULTRA LOW DRIFT DC CURRENT SOURCE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of United States Provisional Application Serial No. 62/290,650, filed February 3, 2016, the disclosure of which is hereby incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present disclosure relates generally to electrical energy sources, including direct current (DC) sources.

BACKGROUND

[0003] Electrical energy sources are used in a wide variety of applications. Conventional DC current sources often include a drift current that may not be desirable. Among other things, embodiments of the present disclosure may address this challenge.

SUMMARY

[0004] In embodiments, an electrical current source may include an input terminal, an output terminal, a current mirror that may be connected to the input terminal, a shunt regulator that may be connected to the current mirror and the output terminal, and/or a setting resistor. The setting resistor may be connected to the current mirror, the shunt regulator, and/or the output terminal. The input terminal may be configured for connection with an input current source and the input current source may include a reference current. The electrical current source may be configured to provide an output current at the output terminal that is substantially constant.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present disclosure will now be described, by way of example, with reference to the accompanying drawings, wherein like reference numerals identify like components in the several figures, in which:

[0006] **FIG. 1** is a circuit diagram generally illustrating a current source in accordance with embodiments of the present disclosure.

[0007] **FIG. 2** is a circuit diagram generally illustrating a shunt regulator in accordance with embodiments of the present disclosure.

[0008] **FIG. 3** is a graphical view generally illustrating the performance of a current source in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

[0009] Reference will now be made in detail to embodiments of the present disclosure, examples of which are described herein and illustrated in the accompanying drawings. While the disclosed concepts will be described in conjunction with embodiments, it will be understood that they are not intended to limit the disclosure to these embodiments. On the contrary, the disclosure is intended to cover alternatives, modifications, and equivalents.

[0010] In embodiments, such as generally illustrated in **FIGS. 1 and 2**, a current source 10 (e.g., an electrical current source) may include an input terminal 12, an output terminal 14, current mirror 20, a shunt regulator U, and/or one or more resistors (e.g., resistors R_1 , R_2 , R_3). In embodiments, current source 10 may be configured to provide relatively constant electrical current at its output terminal 14 that may include relatively little drift.

[0011] In embodiments, input terminal 12 may be configured for connection with an input power source 16, such as, for example, an integrated circuit (IC) power supply. In embodiments, input terminal 12 may be connected to current mirror 20. In embodiments, current mirror 20 may be configured as a Wilson current mirror. In embodiments, current mirror 20 may include one or more resistors, such as first resistor R_1 and/or second resistor R_2 . In embodiments, first resistor R_1 and/or second resistor R_2 may be connected (e.g., in parallel) with input terminal 12.

[0012] In embodiments, current mirror 20 may include a first transistor Q1A, a second transistor Q1B, and/or a third transistor Q2. In embodiments, first transistor Q1A may include an emitter lead 30, a collector lead 32, and/or a base lead 34. In embodiments, second transistor Q1B may include an emitter lead 40, a collector lead 42, and/or a base lead 44. In embodiments, first resistor R_1 may be connected to first transistor Q1A (e.g., to emitter lead 30 of first transistor Q1A), and/or second resistor

R₂ may be connected to a second transistor Q1B (e.g., to emitter lead 40 of second transistor Q1B).

[0013] The Eber-Molls equation defines emitter current of a bipolar junction transistor (e.g., a PNP transistor) as:

$$[0014] \quad I_E = I_{ES} * (e^{\frac{V_{BE}}{V_T}} - 1) \quad \text{Eq. 1.}$$

[0015] where I_E corresponds to emitter current, I_{ES} corresponds to the reverse saturation current of a base-emitter diode (order of 10⁻¹⁵ to 10⁻¹² amps), V_{BE} corresponds to base-emitter voltage, and V_T corresponds to thermal voltage (e.g., about 26mV at room temperature).

[0016] In embodiments, first transistor Q1A and second transistor Q1B may include a matched pair of PNP transistors that may be disposed within a common housing/package. In embodiments, the reverse saturation current I_{ES} of the base-emitter diode, the thermal voltage, V_T, the common base current gain, α, and/or the common emitter current gain, β, may be identical for first transistor Q1A and second transistor Q1B.

[0017] In embodiments, first transistor Q1A and second transistor Q1B may be connected with a common base (e.g., such that base lead 34 of first transistor Q1A is connected with base lead 44 of second transistor Q1B). In embodiments, current I_{EQ1A} at emitter lead 30 of first transistor Q1A may equal the current I_{EQ1B} at emitter lead 40 of second transistor Q1B:

$$[0018] \quad I_{EQ1A} = I_{EQ1B} = I_{EQ1} \quad \text{Eq. 2.}$$

[0019] In embodiments, the current I_{CQ1A} at collector lead 32 of first transistor Q1A may equal the product of (i) the current I_{EQ1} at emitter leads 30, 40 and (ii) common base current gain α:

$$[0020] \quad I_{CQ1A} = \alpha I_{EQ1} \quad \text{Eq. 3.}$$

[0021] In embodiments, the current I_{CQ1A} at collector lead 32 of first transistor Q1A may equal the current I_{CQ1B} at collector lead 42 of second transistor Q1B. In embodiments, the current I_{CQ1A} at collector lead 32 of first transistor Q1A may equal the product of (i) the current I_{BQ1} at base leads 34, 44 of first and second transistors Q1A, Q1B and (ii) common emitter current gain β:

$$[0022] \quad I_{CQ1A} = I_{CQ1B} = I_{CQ1} = \beta I_{BQ1} \quad \text{Eq. 4.}$$

[0023] In embodiments, current mirror 20 may include a third transistor Q2, which may include a high gain transistor (e.g., an NPN transistor). In embodiments, third transistor Q2 may include an emitter lead 50, a collector lead 52, and/or a base lead 54. In embodiments, collector lead 52 of third transistor Q2 may be connected to base lead 34 of first transistor Q1A, base lead 44 of second transistor Q1B, and/or collector lead 42 of second transistor Q1B. In embodiments, the current I_{CQ2} at collector lead 52 of third transistor Q2 may (e.g., according to Kirchhoff's Current Law (KCL)) be generally represented by the following relationship:

$$[0024] \quad I_{CQ2} = \frac{I_{EQ1} * \beta_1}{1 + \beta_1} + \frac{2I_{EQ1}}{1 + \beta_1} \quad \text{Eq. 5.}$$

$$[0025] \quad I_{CQ2} = \frac{I_{EQ1} * (2 + \beta_1)}{1 + \beta_1} \quad \text{Eq. 6.}$$

[0026] In embodiments, common emitter current gain β_1 of first transistor Q1A may be relative high, such that:

$$[0027] \quad \frac{2 + \beta_1}{1 + \beta_1} \approx 1 \quad \text{Eq. 7.}$$

[0028] In embodiments, the current I_{CQ2} at collector lead 52 of third transistor Q2 may be generally equal to the current I_{EQ1} at emitter lead 30 of first transistor Q1A:

$$[0029] \quad I_{CQ2} = I_{EQ1} \quad \text{Eq. 8.}$$

[0030] In embodiments, the current I_{EQ2} at emitter lead 50 of third transistor Q2 may generally equal the sum of (i) the current I_{CQ2} at collector lead 52 of third transistor Q2 and (ii) the current at base lead 54 of third transistor Q2:

$$[0031] \quad I_{EQ2} = I_{CQ2} + I_{BQ2} \quad \text{Eq. 9.}$$

[0032] In embodiments, the current I_{BQ2} at base lead 54 of third transistor Q2 may generally equal the current I_{CQ2} at collector lead 52 of third transistor Q2 divided by the common emitter current gain β_2 of second transistor Q1B:

$$[0033] \quad I_{BQ2} = \frac{I_{CQ2}}{\beta_2} \quad \text{Eq. 10.}$$

[0034] If Equation 9 and Equation 10 are combined, the current I_{EQ2} at emitter lead 50 of third transistor Q2 may be generally represented by the following relationship:

$$[0035] \quad I_{EQ2} = I_{CQ2} * \frac{1 + \beta_2}{\beta_2} \quad \text{Eq. 11.}$$

[0036] In embodiments, common emitter current gain β_2 of second transistor Q1B may be relative high, such that:

$$[0037] \quad \frac{1+\beta_2}{\beta_2} \approx 1 \quad \text{Eq. 12.}$$

[0038] In embodiments, the current I_{EQ2} at emitter lead 50 of third transistor Q2 may substantially equal the current I_{CQ2} at collector lead 52 of third transistor Q2 and/or may substantially equal the current I_{EQ1} at the emitter leads 30, 40 of first and second transistors Q1A, Q1B:

$$[0039] \quad I_{EQ2} = I_{CQ2} = I_{EQ1} \quad \text{Eq. 13.}$$

[0040] In embodiments, current source 10 may include a third resistor R_s (e.g., a setting resistor). In embodiments, the current I_{R_s} at third resistor R_s may (e.g., via Kirchhoff's Current Law) generally equal the current I_{EQ2} at emitter lead 50 of third transistor Q2 less the current I_R at second input R of shunt regulator U:

$$[0041] \quad I_{R_s} = I_{EQ2} - I_R \quad \text{Eq. 14.}$$

[0042] In embodiments, shunt regulator U may include a tightly controlled closed loop system that may be configured to regulate the output current of current source (e.g., the current, I_L at load). In embodiments, shunt regulator U may include a three terminal adjustable shunt regulator and may include a first input terminal C, a second input terminal R, and/or an output terminal A. In embodiments, shunt regulator U may be connected to current mirror 20, third resistor R_s , and/or output terminal 14. For example, and without limitation, first input C may be connected to collector lead 32 of first transistor Q1A and/or to base lead 54 of third transistor Q2. Second input R may be connected to emitter lead 50 of third transistor Q2 and/or to third resistor R_s . Output A of shunt regulator U may be connected to output terminal 14 of current source 10. In embodiments, second input R of shunt regulator U may include a high impedance. For example, and without limitation, the impedance at second input R may be sufficiently high such that the current I_R at second input R may be effectively zero, and the current I_{R_s} at third resistor R_s may be substantially equal to the current I_{EQ2} at third transistor emitter lead 50 and/or the current I_{EQ1} at emitter leads 30, 40 of first and second transistors Q1A, Q1B:

$$[0043] \quad I_{R_s} = I_{EQ2} = I_{EQ1} \quad \text{Eq. 15.}$$

[0044] In embodiments, the current I_{CA} at shunt regulator first input C may, via Kirchhoff's Current Law, be generally represented by the following relationships:

$$[0045] \quad I_{CA} = \frac{I_{EQ1} * \beta_1}{1 + \beta_1} - I_{BQ2} \quad \text{Eq. 16.}$$

$$[0046] \quad I_{CA} = \frac{I_{EQ1} * \beta_1}{1 + \beta_1} - \frac{I_{EQ1}}{\beta_2} \quad \text{Eq. 17.}$$

$$[0047] \quad I_{CA} = I_{EQ1} \left(\frac{\beta_1}{1 + \beta_1} - \frac{1}{\beta_2} \right) \quad \text{Eq. 18.}$$

[0048] In embodiments, common emitter current gains β_1 and/or β_2 of first and second transistors Q1A, Q1B may be relative high, such that:

$$[0049] \quad \frac{\beta_1}{1 + \beta_1} \approx 1 \quad \text{Eq. 19.}$$

[0050] and

$$[0051] \quad \frac{1}{\beta_2} \approx 0 \quad \text{Eq. 20.}$$

[0052] In embodiments, the current I_{CA} at shunt regulator first input C may equal may substantially equal the current I_{EQ2} at third transistor emitter lead 50 and/or the current I_{EQ1} at emitter leads 30, 40 of first and second transistors Q1A, Q1B:

$$[0053] \quad I_{CA} = I_{EQ1A} = I_{EQ1B} \quad \text{Eq. 21.}$$

[0054] In embodiments, a load 60 may be connected to output terminal 14. In embodiments, the current I_L at load 60 may, via Kirchhoff's Current Law, be generally equal the sum of (i) the current I_{CA} at shunt regulator first input C and (ii) the current I_{RS} at third resistor R_S :

$$[0055] \quad I_L = I_{CA} + I_{RS} \quad \text{Eq. 22.}$$

[0056] If Equations 15 and 21 are combined, the current at input I_{CA} may be determined to generally equal the current at third resistor I_{RS} :

$$[0057] \quad I_{CA} = I_{RS} \quad \text{Eq. 23.}$$

[0058] If Equations 22 and 23 are combined, the current I_L at load 60 may be determined to generally equal two times the current I_{RS} at third resistor R_S :

$$[0059] \quad I_L = 2I_{RS} \quad \text{Eq. 24.}$$

[0060] In embodiments, shunt regulator U may be configured to regulate the current I_{CA} at first input C such that the voltage V_{RA} across second input R and output A substantially equals the internal reference voltage V_{ref} of shunt regulator U:

$$[0061] \quad V_{RA} = V_{ref} \quad \text{Eq. 25.}$$

[0062] In embodiments, the current I_{RS} at third resistor R_S may, via Ohm's law, be generally equal voltage V_{RA} divided by the resistance of third resistor R_S :

$$[0063] \quad I_{RS} = \frac{V_{RA}}{R_S} \quad \text{Eq. 26.}$$

[0064] If Equations 24, 25, and 26 are combined, the current I_L at load 60 may be determined to generally equal two times the reference voltage V_{ref} of shunt regulator U divided by the resistance of third resistor R_S :

$$[0065] \quad I_L = \frac{2V_{ref}}{R_S} \quad \text{Eq. 27.}$$

[0066] In embodiments, shunt regulator U may include, for example, and without limitation, a TL431 shunt regulator available from Texas Instruments®. In embodiments, a source voltage of about 5 volts may be provided at input terminal 12, and/or shunt regulator U may include a reference voltage, V_{ref} , of about 2.495 volts (e.g., $\pm 0.4\%$). In embodiments, third resistor R_S may include, for example, a resistance of about 25.2 thousand Ohms (e.g., $\pm 0.02\%$). Equation 27 may then solved for the load current I_L :

$$[0067] \quad I_L = \frac{2(2.495)}{25.2k}$$

$$[0068] \quad I_L = 198\mu A (\pm 0.4\%)$$

[0069] **FIG. 3** generally illustrates a chart 70 of sample load current I_L over time of an embodiment of current source 10 with such a configuration. In embodiments, load current tolerance may correspond to and/or depend on the tolerance of shunt regulator U.

[0070] In embodiments, current source 10 may be configured to provide current (e.g., current I_L) with ultra-low drift over a wide range of operating temperatures and/or voltages, such as to sensitive devices. Sensitive devices may include, for example, thermistors, MEMS (micro electromechanical systems), optocouplers, and/or others. In

embodiments, current source 10 may, for example, be disposed in and/or connected to a fuel pump, such as an aircraft fuel pump.

[0071] Various embodiments are described herein for various apparatuses, systems, and/or methods. Numerous specific details are set forth to provide a thorough understanding of the overall structure, function, manufacture, and use of the embodiments as described in the specification and illustrated in the accompanying drawings. It will be understood by those skilled in the art, however, that the embodiments may be practiced without such specific details. In other instances, well-known operations, components, and elements have not been described in detail so as not to obscure the embodiments described in the specification. Those of ordinary skill in the art will understand that the embodiments described and illustrated herein are non-limiting examples, and thus it can be appreciated that the specific structural and functional details disclosed herein may be representative and do not necessarily limit the scope of the embodiments.

[0072] Reference throughout the specification to “various embodiments,” “with embodiments,” “in embodiments,” or “an embodiment,” or the like, means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. Thus, appearances of the phrases “in various embodiments,” “with embodiments,” “in embodiments,” or “an embodiment,” or the like, in places throughout the specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments. Thus, the particular features, structures, or characteristics illustrated or described in connection with one embodiment may be combined, in whole or in part, with the features, structures, or characteristics of one or more other embodiments without limitation given that such combination is not illogical or non-functional.

[0073] It should be understood that references to a single element are not so limited and may include one or more of such element. All directional references (e.g., plus, minus, upper, lower, upward, downward, left, right, leftward, rightward, top, bottom, above, below, vertical, horizontal, clockwise, and counterclockwise) are only used for identification purposes to aid the reader’s understanding of the present disclosure, and

do not create limitations, particularly as to the position, orientation, or use of embodiments.

[0074] Joinder references (e.g., attached, coupled, connected, and the like) are to be construed broadly and may include intermediate members between a connection of elements and relative movement between elements. As such, joinder references do not necessarily imply that two elements are directly connected/coupled and in fixed relation to each other. The use of “e.g.” throughout the specification is to be construed broadly and is used to provide non-limiting examples of embodiments of the disclosure, and the disclosure is not limited to such examples. It is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative only and not limiting. Changes in detail or structure may be made without departing from the present disclosure.

[0075] Furthermore, the mixing and matching of features, elements and/or functions between various examples is expressly contemplated herein so that one of ordinary skill in the art would appreciate from this disclosure that features, elements, and/or functions of one example may be incorporated into another example as appropriate, unless described otherwise, above. Moreover, many modifications may be made to adapt a particular situation or material to the teachings of the present disclosure without departing from the essential scope thereof. Therefore, it is intended that the present teachings not be limited to the particular examples illustrated by the drawings and described in the specification.

CLAIMS

What is claimed:

1. An electrical current source comprising:
an input terminal;
an output terminal;
a current mirror connected to the input terminal;
a shunt regulator connected to the current mirror and the output terminal; and
a setting resistor connected to the current mirror, the shunt regulator, and the output terminal.
2. The electrical current source of claim 1, wherein the input terminal is configured for connection with an input power source.
3. The electrical current source of claim 1, wherein the electrical current source is configured to provide an output current according to a reference voltage of the shunt regulator and a resistance of the setting resistor.
4. The electrical current source of claim 3, wherein the output current generally equals two times the reference voltage divided by the setting resistor resistance.
5. The electrical current source of claim 1, wherein the current mirror is configured as a Wilson current mirror.
6. The electrical current source of claim 1, wherein the current mirror includes a first resistor and a second resistor connected in parallel with the input terminal.
7. The electrical current source of claim 1, wherein the current mirror includes a first transistor and a second transistor.
8. The electrical current source of claim 7, wherein the first transistor and the second transistor are a matched pair of PNP transistors.
9. The electrical current source of claim 7, wherein the first transistor and the second transistor are connected with a common base.
10. The electrical current source of claim 7, wherein the current mirror includes a third transistor, the third transistor is a NPN transistor, and a collector lead of the third

transistor is connected to (i) a base lead of the first transistor, (ii) a base lead of the second transistor, and (iii) a collector lead of the second transistor.

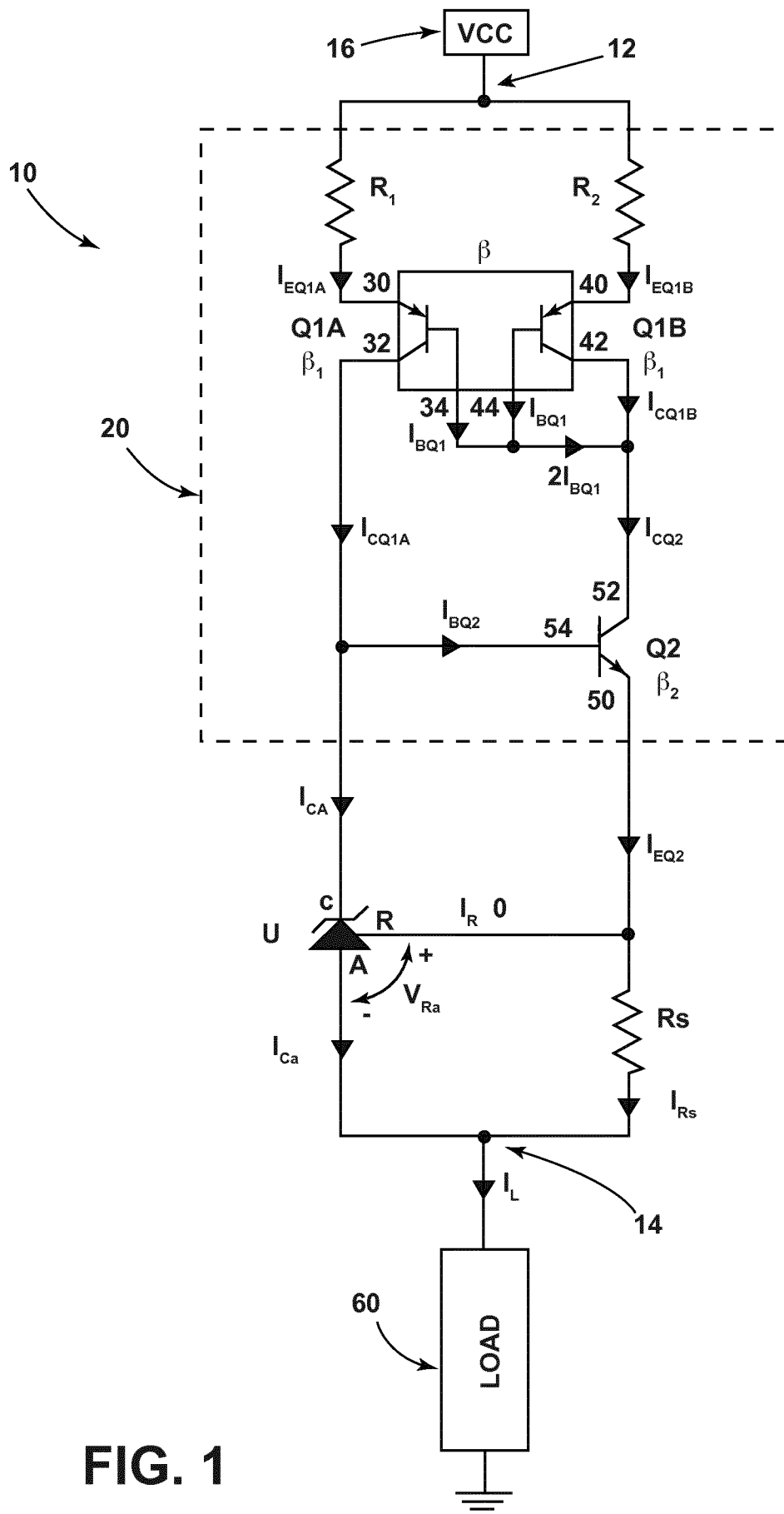
11. The electrical current source of claim 1, wherein the current mirror includes a first transistor, a second transistor, and a third transistor; a first input of the shunt regulator is connected with a collector lead of the first transistor; a second input of the shunt regulator is connected to an emitter lead of the third transistor, and an output of the shunt regulator is connected to the output terminal.

12. The electrical current source of claim 11, wherein an impedance of the second input of the shunt regulator is sufficiently high that an electrical current at the second input of the shunt regulator is substantially zero.

13. The electrical current source of claim 1, wherein the current mirror includes a first transistor and a second transistor, and gains of the first transistor and the second transistor are sufficiently high that an electrical current at the shunt regulator is substantially equal to an electrical current at an emitter lead of the first transistor and substantially equal to an electrical current at an emitter lead of the second transistor.

14. The electrical current source of claim 1, wherein an electrical current at the output terminal is substantially equal to twice an electrical current at the setting resistor.

15. The electrical current source of claim 1, wherein an electrical current at the output terminal includes minimal drift at a plurality of temperatures and voltages.



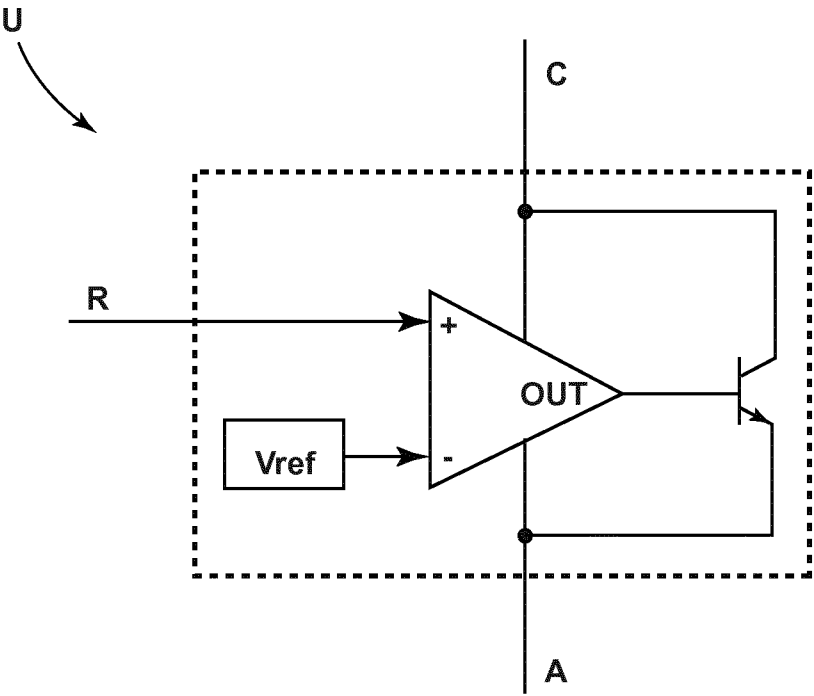
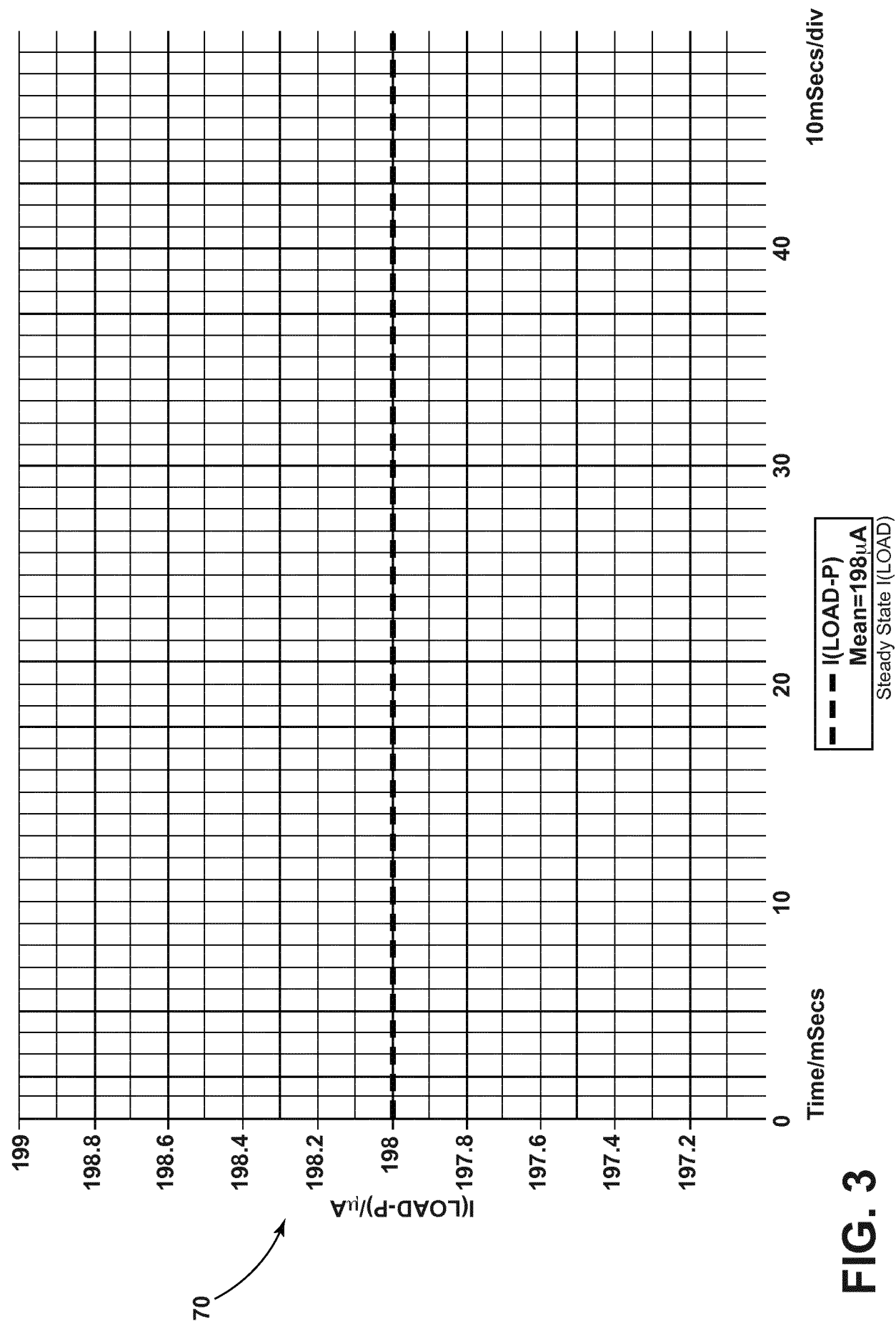


FIG. 2



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2017/052305

A. CLASSIFICATION OF SUBJECT MATTER
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ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 308 496 A (NAGANO KATSUMI) 29 December 1981 (1981-12-29) the whole document	1-15
X	----- TEXAS INSTRUMENTS: "TL431, TL431A, TL431B, TL432, TL432A, TL432B. ADJUSTABLE PRECISION SHUNT REGULATORS", INTERNET CITATION, 1 January 2005 (2005-01-01), pages 1-42, XP002637449, Retrieved from the Internet: URL:http://pdf1.alldatasheet.com/datasheet -pdf/view/28825/TI/TL431CDBZR.html [retrieved on 2011-05-18] the whole document	1-15
X	----- US 4 317 082 A (GROSS WILLIAM H) 23 February 1982 (1982-02-23) the whole document	1-15

☐

Further documents are listed in the continuation of Box C.

☒

See patent family annex.

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Date of the actual completion of the international search

29 March 2017

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Schobert, Daniel

INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 4308496	A	29-12-1981	DE 3027761 A1	12-02-1981
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