

Metz et al.

[15] **3,648,270**

[45] Mar. 7, 1972

[54] **GRAPHIC DISPLAY SYSTEM**

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[21] Appl. No.: 848,901

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[52] **U.S. Cl.****340/324 A, 340/154**

[51] **Int. Cl.**.....G06f 3/14

[58] **Field of Search**.....340/324 A, 172.5, 152, 154;
235/150.5, 198

[56] **References Cited**

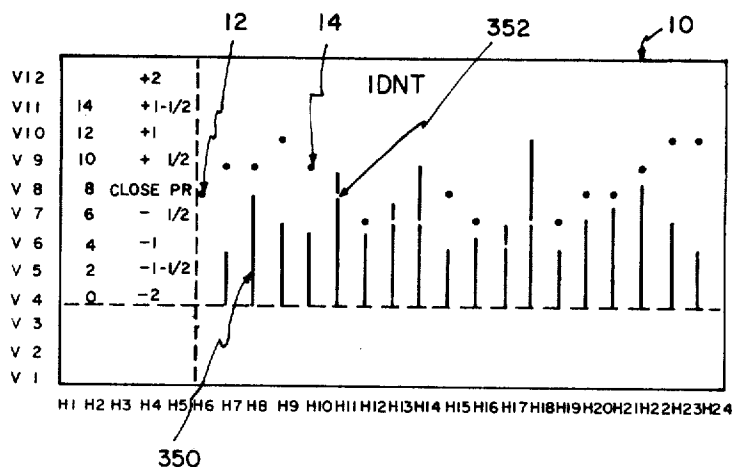
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[57] **ABSTRACT**

A graphic display system including separate means for storing a representation of a value to be graphically displayed and a reference value which is less than the value representation. The reference value is incremented in steps of predetermined amounts and compared with the stored representation. When a match is detected, a predetermined change is caused in the display on a display device. This change may be the generating of a dot on the display, the initiating of a line, the terminating of a line, or the like.

35 Claims, 11 Drawing Figures



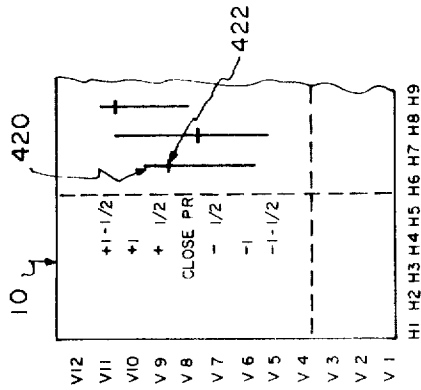


FIG. 3

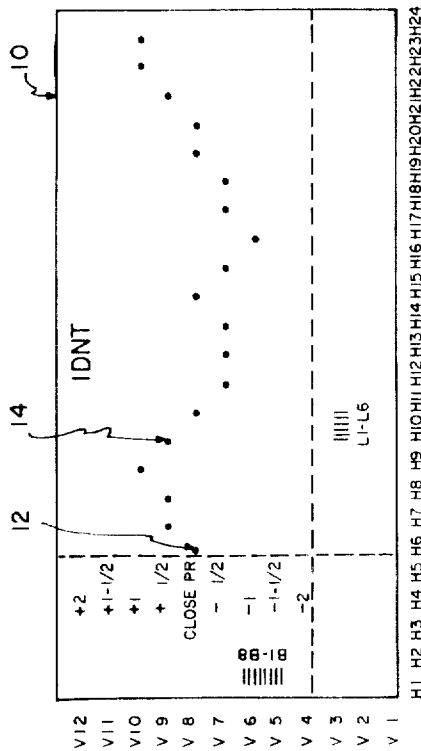


FIG. 1

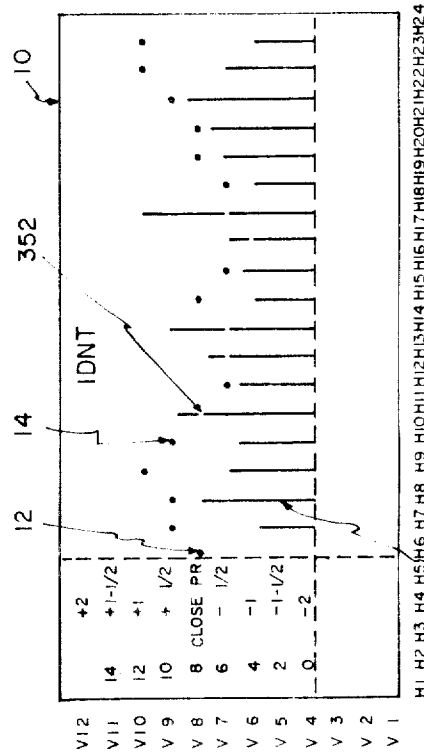


FIG. 2

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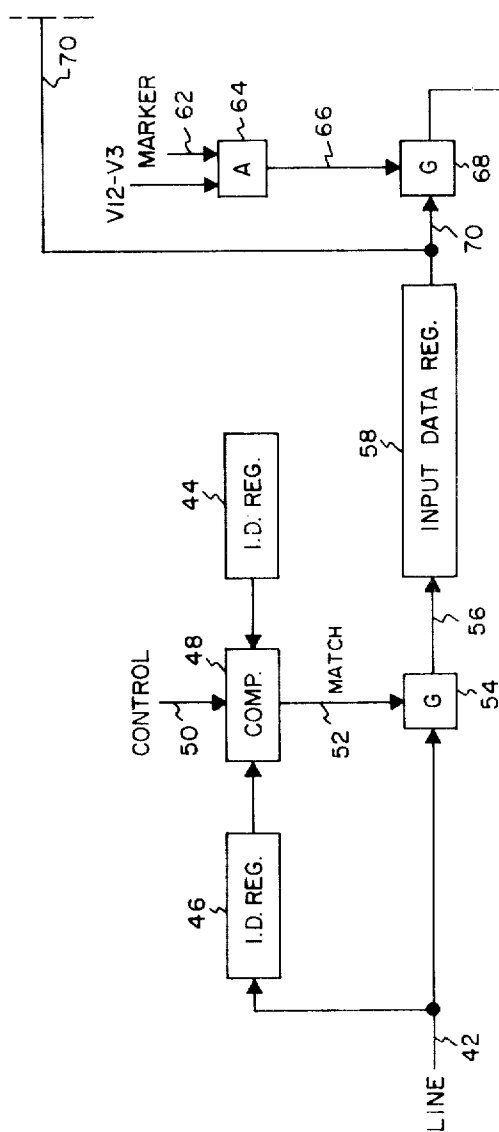


FIG. 4

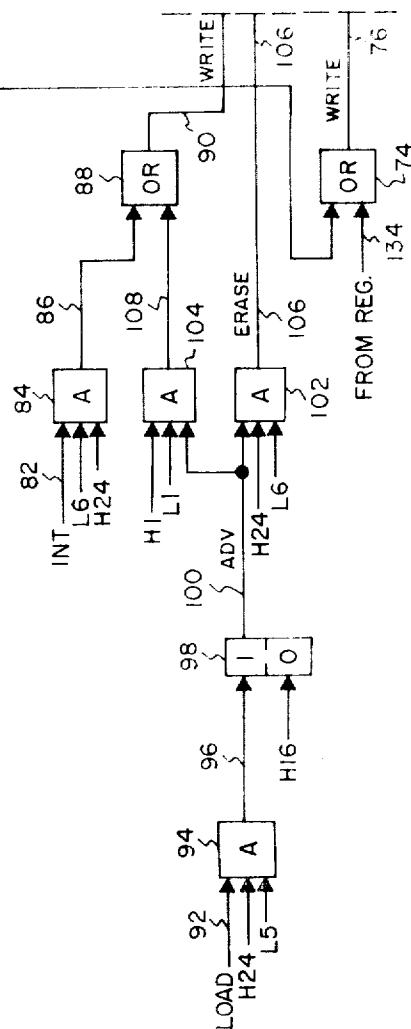
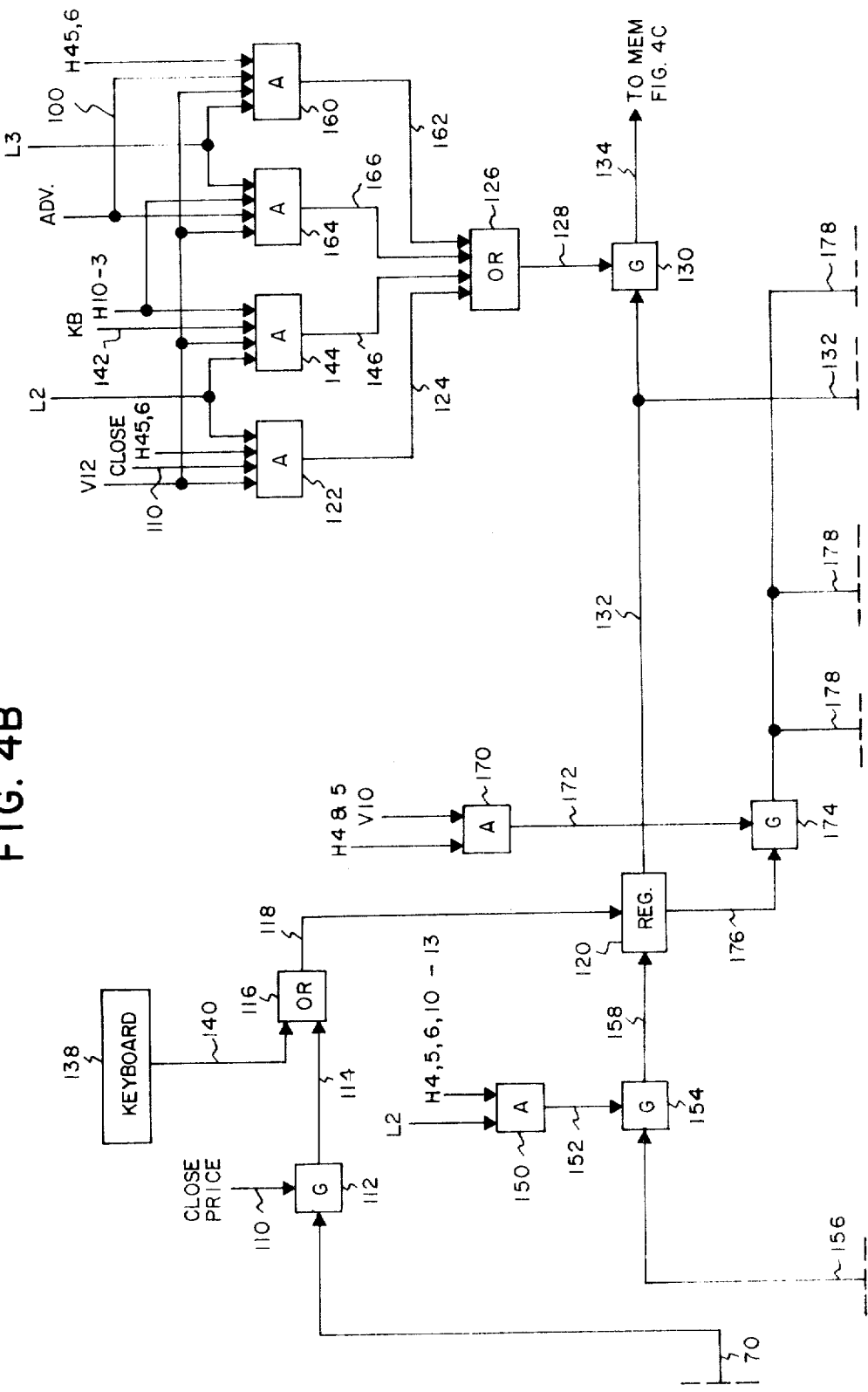


FIG. 4A

FIG. 4B



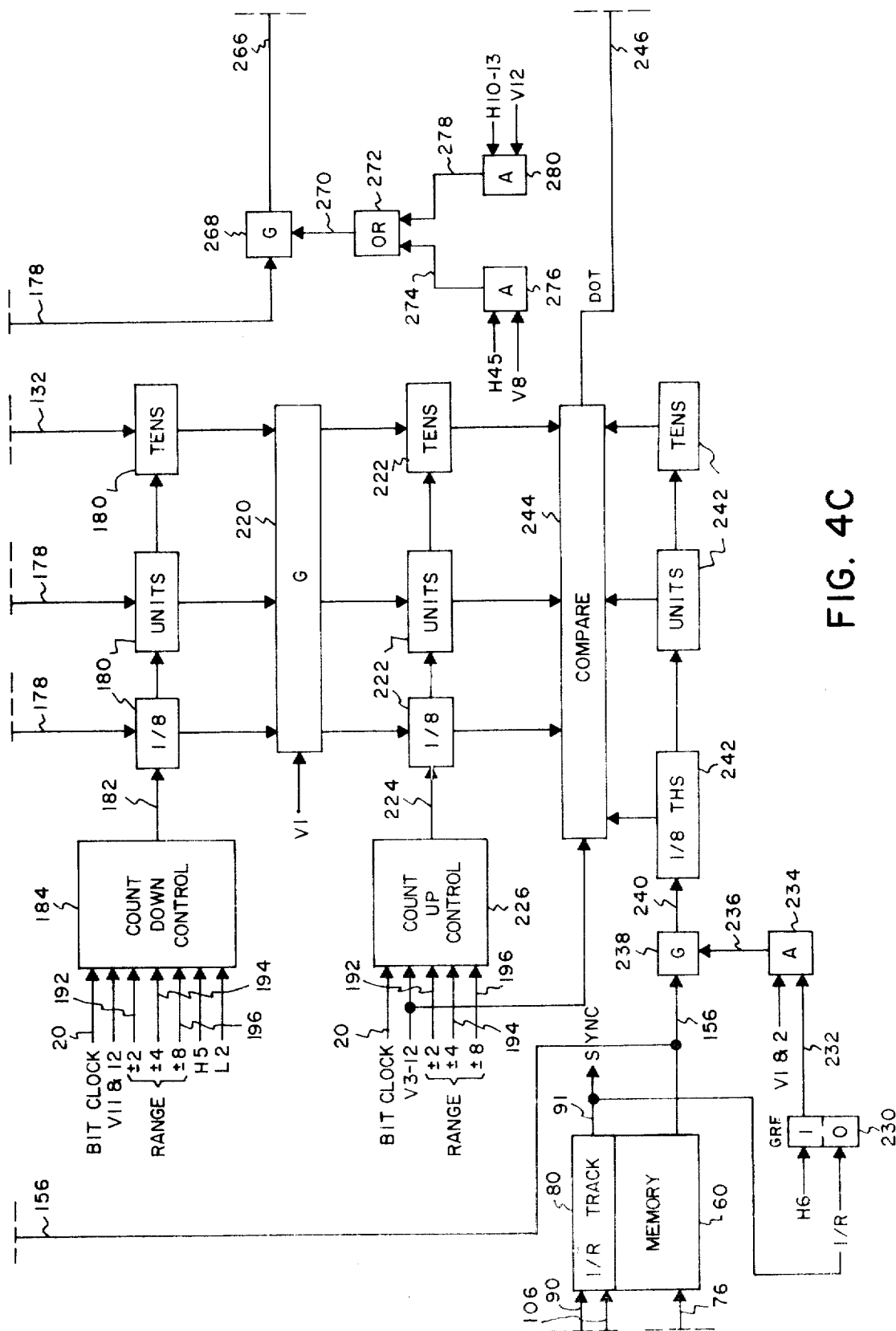
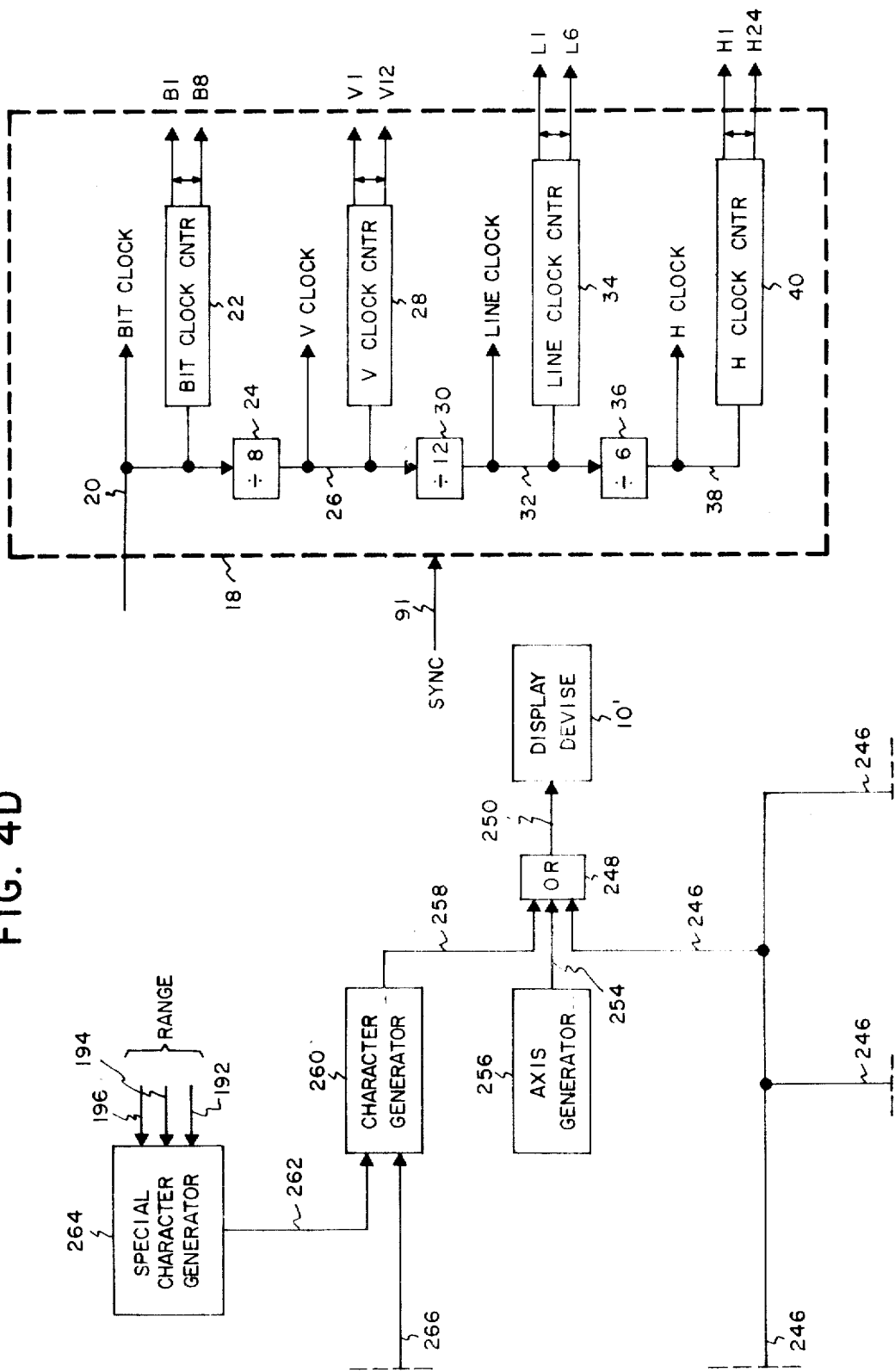


FIG. 4C

FIG. 4D



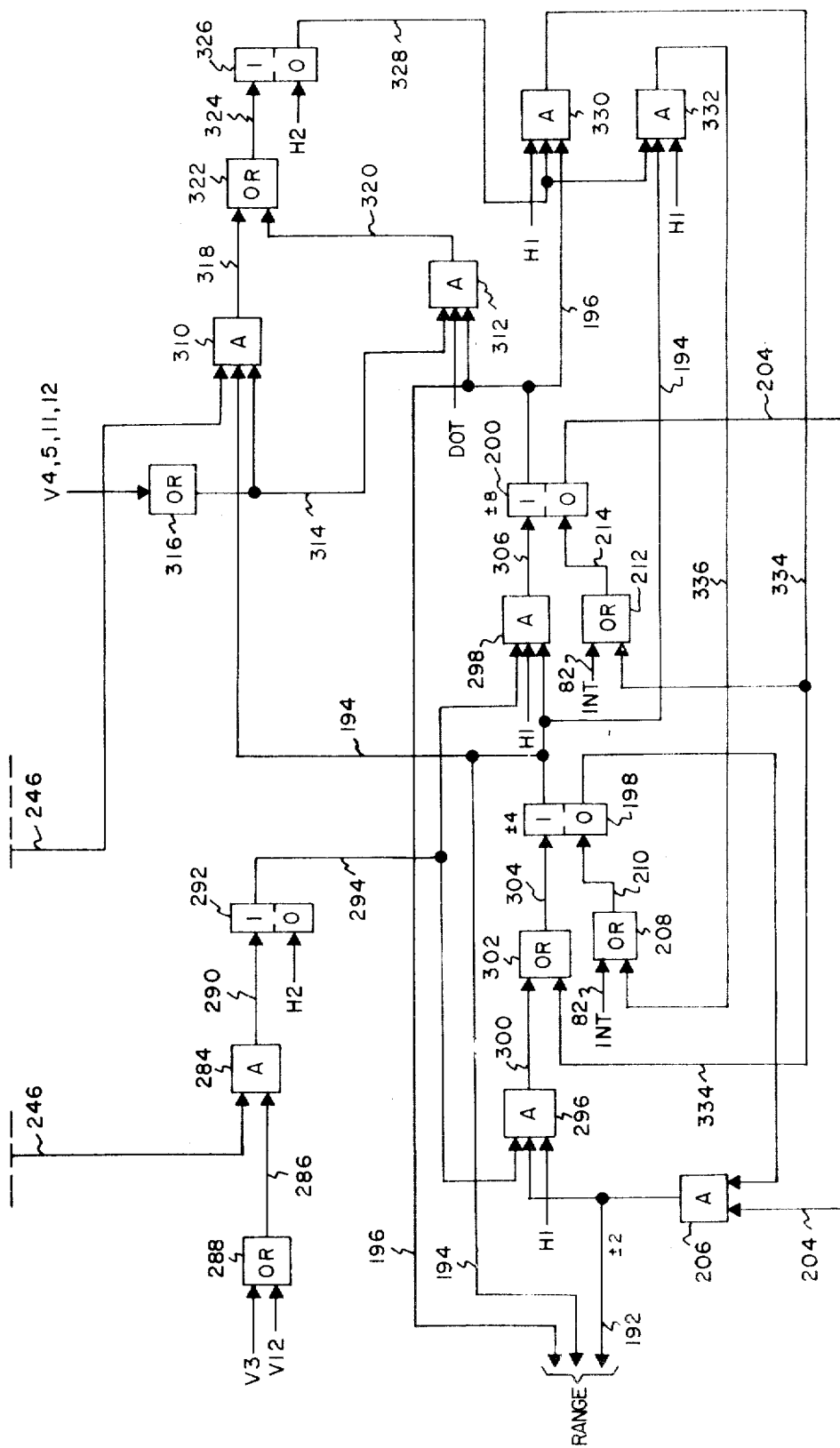


FIG. 4E

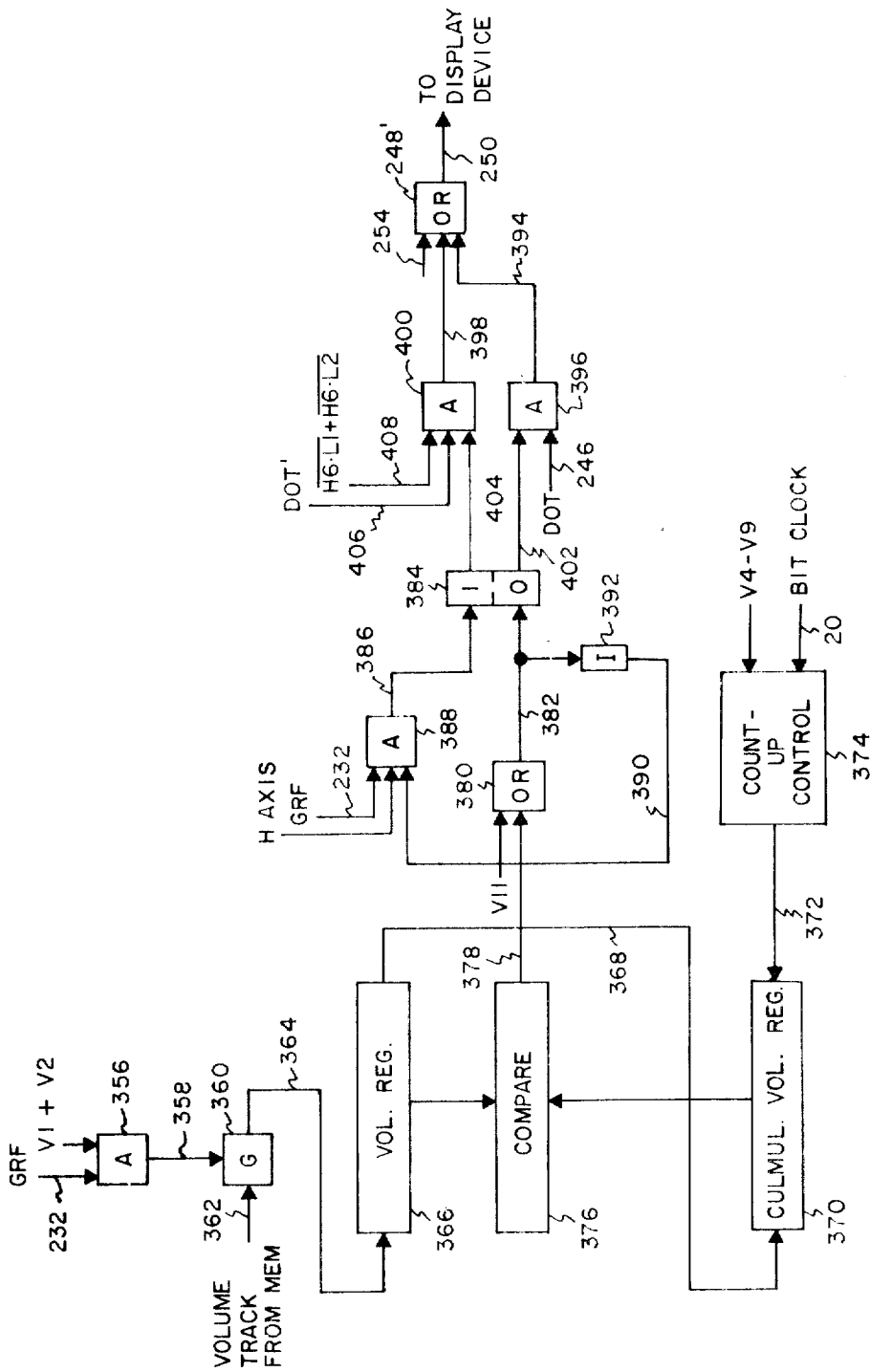


FIG. 5

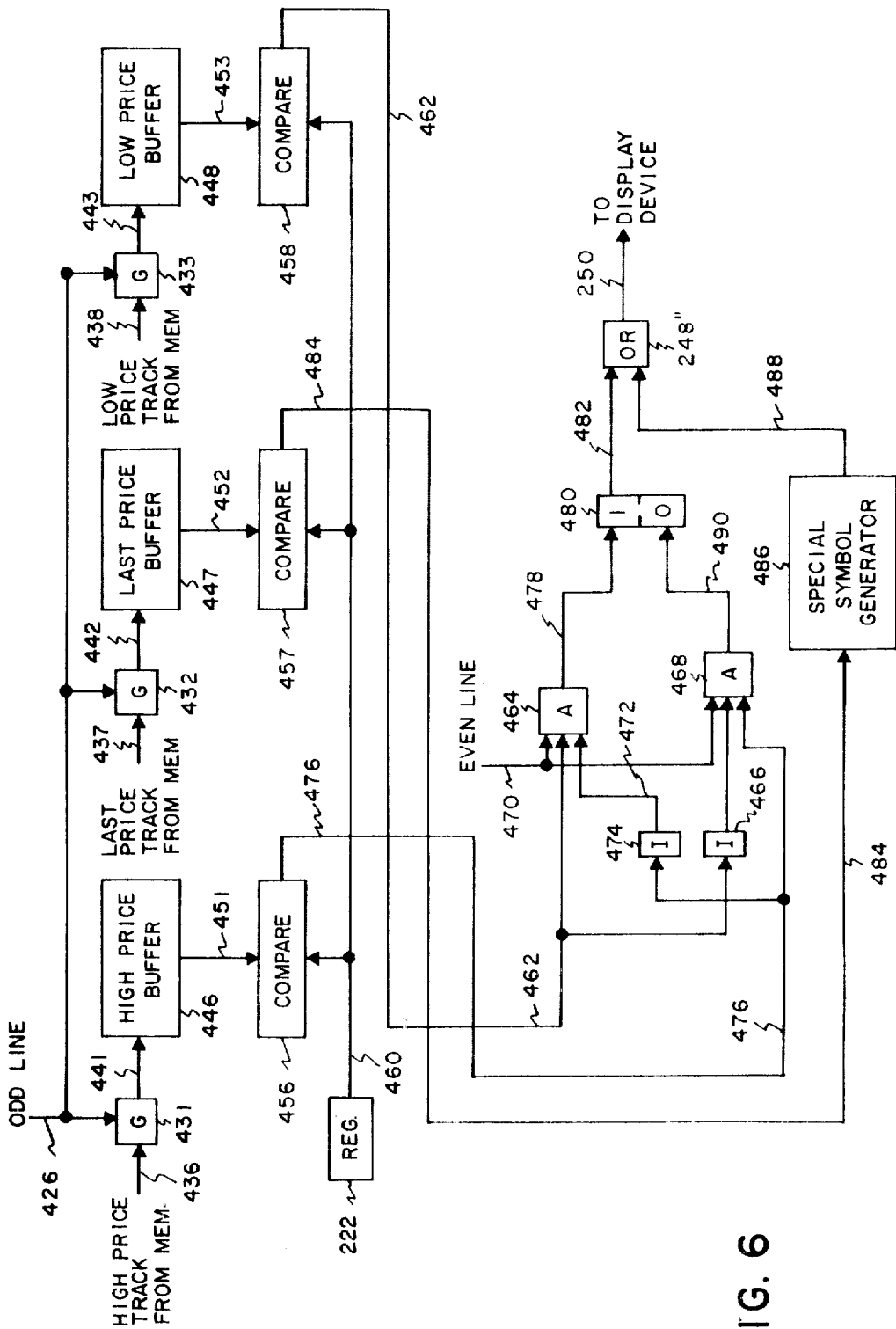


FIG. 6

GRAPHIC DISPLAY SYSTEM

This invention relates to a system for displaying a graphic representation of a value and more particularly to a cathode-ray tube (CRT) display system which is capable of displaying a graphic representation of a plurality of successively received values.

Display devices, such as CRTs, are becoming increasingly popular as output terminals for general and special purpose computers. These devices permit the user to either observe the results of various computer operations or to view selected information contained in the computer's memory. When used in conjunction with a keyboard, these devices permit the user to engage in a dialogue with the machine. While terminals of this type may be utilized at the computer site, they are frequently located at some distance from the computer and communicate with the computer over telephone or other lines.

Copending application, Ser. No. 703,052 entitled "Information Storage and Display System," filed Feb. 5, 1968, now U.S. Pat. No. 3,573,732 on behalf of C. Greenblum et al. and assigned to the assignee of the instant application shows a CRT display system of this type. In this system, alpha-numeric information is transmitted from a central station to a remote station, selectively stored at the remote station, and displayed in alpha-numeric form on request. One such display, for example, includes a listing of the price and volume for a number of preceding transactions on a selected stock. By viewing this information, the user can observe various trends on the particular stock. However, trends are more easily viewed from a graphic representation of the values.

Heretofore, graphic display on a CRT have generally been obtained by use of a TV raster. Such a display, however, requires the transmission of information for each individual dot on the screen. Thus, a display of this type, even if relatively coarse, requires a substantial transmission bandwidth.

It would be preferable if a graphic display could be generated from the same data base as is, for example, utilized to generate the alpha-numeric display in the before-mentioned Greenblum et al. application. In such a system, only the values which are to be graphically represented would be transmitted and stored, and these values would be utilized to locally generate the graphic display by causing selected changes in the intensification of a beam as it traces a predetermined raster pattern on the CRT screen. Such a system should be compatible with existing alpha-numeric displays and should also be flexible enough so as to permit the display of a variety of graphic representations such as a single line, various types of bar graphs, or combinations of multiples of the above. Since the graph is generated locally, it permits the user to select the particular information which he wishes to have plotted rather than limiting the display to a single plot being transmitted from a central source.

One problem with a system of the type indicated above is in the selecting of a proper scale factor. If too fine a scale is selected and relatively large fluctuations exist, some values will be off scale and an accurate picture of what is happening will not be provided. Similarly, if too coarse a scale is used where the fluctuations are not very great, the small differences between succeeding values will not be easily perceived. It is therefore desirable to provide the system with a scale adjustment, preferably automatic, which will at all times permit the system to be set for the finest scale adjustment which is compatible with the fluctuations in the received data.

It is therefore a primary object of this invention to provide a system for displaying a graphic representation of a stored value.

A more specific object of this invention is to provide a graphic representation of a plurality of successively received values so as to enable the viewer to easily observe developing trends.

A still more specific object of this invention is to provide a display system of the type indicated above which requires only the values, representations of which are to be displayed, to be transmitted and stored, with the graphic display being locally generated.

Another object of this invention is to provide a display system of the type indicated above which permits each individual user to select the particular items of information on which he desires a graphic display.

Still another object of this invention is to provide a display system of the type described above for providing graphic representations of stock market information.

A further object of this invention is to provide a display system of the type indicated above which includes a scale adjustment capability so as to provide the optimum scale in each instance for the range of data being displayed.

A still further object of this invention is to provide a display system of the type indicated above which is capable of operating with the same data base as that utilized for an alpha-numeric display of the same data and which is generally compatible with such an alpha-numeric display system.

In accordance with these objects this invention provides a system for displaying a graphic representation of a value on a display device which includes a means for storing a representation of the value. The system also includes a means of storing a reference value which is less than the stored representation and a means for incrementing the reference value in steps of predetermined amounts. The incremented reference value is compared with the stored representation in a comparing means. When a match is detected in the comparing means, a predetermined change is caused in the display on the display device. If the display device is a CRT, the raster of which is a plurality of parallel vertical strokes of a writing beam, the predetermined change indicated above may be the momentary intensifying of the beam to generate a dot on the CRT screen. If a bar graph is desired, the beam may be intensified on each stroke starting at the horizontal axis, with a successful comparison terminating the intensification. Other possible implementations will be discussed in the description to follow.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings.

In the drawings:

FIG. 1 is an illustrative representation of the display for a preferred embodiment of the invention.

FIG. 2 is an illustrative representation of the display for a first alternative embodiment of the invention.

FIG. 3 is an illustrative representation of a portion of the display for a second alternative embodiment of the invention.

FIGS. 4A-4E, when combined as shown in FIG. 4, form a schematic block diagram of a circuit for a preferred embodiment of the invention.

FIG. 5 is a schematic block diagram of additional circuitry required for a first alternative embodiment of the invention.

FIG. 6 is a schematic block diagram of additional circuitry required for a second alternative embodiment of the invention.

GENERAL DESCRIPTION OF PREFERRED EMBODIMENT

FIG. 1 is a representation of the face of a cathode-ray tube (CRT) 10. Information is displayed on this screen by tracing a plurality of parallel vertical strokes on the screen and selectively intensifying the tracing beam at selected index points along each stroke. The particular display shown is capable of displaying twelve rows of alpha-numeric characters, which rows are designated VI-VI2 respectively, with 24 characters, the positions of which are designated H1-H24, in each row. For each character there are six strokes, designated L1-L6, and for each row, there are eight index point or bit positions, designated B1-B8.

The illustrative display shown in FIG. 1 is a display of the price for succeeding transactions on a selected stock. This is the graphic equivalent of half of the stock list display shown in FIG. 5 of the before-mentioned Greenblum et al. application. In this display, four characters, VI2, H10-13, are designated to display an alphabetic indication of the given stock. A

horizontal axis is provided along the line V4, B1 and a vertical axis along the line H6, L1. A numeric indication of the close price of the given stock on the preceding trading day is provided at V8, H4 and H5, while scale values are provided at V4-V12, H4-H5. As will be seen shortly, these scale values may be changed to be compatible with the range of the values being displayed. At stroke H6, L2 there is a dot 12 which indicates the close price of the stock on the preceding day. The succeeding stroke position through H24, L6, each have a single dot 14 indicating the price of a particular transaction. Each time a new transaction occurs, the value of this transaction is displayed at H24, L6, with all other values except the close price being shifted left one position. The value which was previously displayed on stroke H6, L3 is lost. It should be noted that because of the difference in size between FIG. 1 and a normal CRT screen, it has only been possible to show the dots on the L1 strokes in the FIG. However, it should be understood that a dot will appear on each stroke providing a substantially continuous line on the display screen.

In general, the display of FIG. 1 is generated by initially taking the close price and reducing it by an amount such that the resulting value is less than the minimum value to be displayed with the scale factor being utilized. The values to be displayed are then transferred in succession into a first compare register with the reduced close price being at the same time transferred into a second compare register. The reduced close price is then incremented in steps which are compatible with the scale being utilized in synchronism with the movement of the writing beam on a stroke. When the quantities in the two compare registers are equal, the beam is momentarily intensified causing a dot to be generated on the stroke. If a dot appears in V3 or V12, the scale factor is increased.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

FIGS. 4A-4E, when combined as shown in FIG. 4, form a block diagram of a circuit for generating a display of the type shown in FIG. 1. Referring first to FIG. 4D it is seen that the system includes a clock circuit 18. One input to this circuit is bit clock line 20. This line is applied to a bit clock counter 22 and to a divide-by-eight circuit 24. The bit clock on line 20 occurs in synchronism with the scanning of the CRT beam past each bit (or index point) position (see FIG. 1). A means of controlling this synchronism will be described later. Bit counter 22 indicates the particular bit of a stroke which the beam is adjacent to at each instant. Since there are eight bits for each V position, output line 26 from divider 24 is the V clock line. Line 26 is applied as an input to V clock counter 28 and to divide-by-twelve circuit 30. V clock counter 28 provides an indication of the V position of the writing beam on each stroke. Since there are 12 V positions on each stroke, output line 32 from divide-by-twelve circuit 30 is the line or stroke clock. This line is connected as the step input to line clock counter 34 and as an input to divide-by-six circuit 36. Line clock counter 34 provides an indication of the stroke which is being performed by the writing beam at any given time. Since there are six strokes to each H or character position, output line 38 from divide-by-six circuit 36 is the H clock line. This line is connected as the step input to H clock counter line. This line is connected as the step input to H clock counter 40. Clock counter 40 provides an indication of the H position of the writing beam at any given time. In order to simplify the drawing, no attempt has been made to connect the various clock outputs described above to the points in the circuit of FIGS. 4A-4E at which they are utilized. Instead, at each of these points, a line appears with the appropriate letter and number designations for the clock or clocks which are utilized at that point in the circuit.

As in the circuit of the before-mentioned Greenblum et al. application, stock identification and price information is applied to the circuit over a line 42 (FIG. 4A). This line may, for example, be one of the ticker lines which is provided by the

various stock exchanges, or may be a special line which contains selected transaction information such as last price, volume, high price, low price, and the like. To simplify the present description it will be assumed that line 42 contains only an identification of a stock on which a transaction has occurred followed by a transaction price. The manner in which desired information may be obtained with a more sophisticated line is for example described in the before-mentioned Greenblum et al. application.

An I.D. for the stock on which information is to be displayed is stored in I.D. register 44. This register may, for example, be loaded from a keyboard 138 (FIG. 4B) in a standard manner. The data on line 42 is also applied to I.D. register 46. The contents of registers 44 and 46 are compared in compare circuit 48. A signal appears on control line 50 when a complete stock I.D. is in register 46. The signal on line 50 may, for example, be a line clock signal. When a match is detected in circuit 48 at a time when a signal appears on line 50, a signal appears on line 52 conditioning gate 54 to pass the following price information on line 42 through line 56 to be stored in input data register 58. When the data has passed, the signal on line 52 terminates.

The system also includes a memory 60 (FIG. 4C) which may, for example, be a rotating magnetic drum. The succeeding prices which are to be displayed on CRT 10 are stored on a single track memory 60. This track contains a write marker which indicates the memory position in which the next value is to be written. Each time a value is written into memory, this marker is advanced to the next succeeding memory position. This marker advance operation is performed in a standard manner which does not form part of the present invention. Memory 60 rotates at a speed such that information is read from the track of the memory in synchronism with the writing of the data on CRT 10. Therefore, the clocks from clock circuit 18 apply equally for the memory and the display. In fact, the bit clock on line 20 may be derived from a clock track on the memory drum.

Each time a write marker is detected on the track of memory 60, causing a signal to appear on marker line 62, and V clock counter 28 is generating an output on a line V12, V1, V2 or V3, AND-gate 64 (FIG. 4A) is fully conditioned to generate an output signal on line 66. This signal fully conditions gate 68 to pass any information in input data register 58 through line 70, gate 68, line 72, OR-gate 74, and write line 76 to be recorded in memory 60. New information is, in this manner, loaded into the memory. Memory 60 also has a separate one-per-revolution clock track 80. When the system is initialized, a signal appears on initialize line 82. This signal, in conjunction with L6 and H24 clock signals, fully conditions AND-gate 84 (FIG. 4A) to generate an output signal on line 86 which is applied through OR-gate 88 and write line 90 to initially write the one-per-revolution clock bit in the last stroke position. At the end of each drum revolution, the bit is read and applied through line 91 to resynchronize the clock counters of clock circuit 18.

When new information is loaded into memory 60, a signal appears on load line 92. This signal may, for example, be an output from a flip-flop which is set when new information is loaded into the memory. The signal on line 92, in conjunction with H24 and L5 clock signals, fully conditions AND-gate 94 (FIG. 4A) to generate an output on line 96 which is applied to set advance flip-flop 98 to its ONE state. The signal on ONE-side output line 100 from advance flip-flop 98 is applied as one input to AND-gates 102 and 104. During the next line time, L6, H24, AND-gate 102 is fully conditioned to generate an output signal on line 106 which is applied to erase the one-per-revolution clock bit on track 80. It should be noted, however, that before this bit is erased, it is read and utilized to resynchronize clock 18. Therefore, during the next revolution of drum 60, clock 18 will be operating in synchronism with the old one-per-revolution bit. During the next stroke time, H1, L1, AND-gate 104 is fully conditioned to generate an output signal on line 108 which is applied through OR gate 88 and

line 90 to write a new one-per-revolution clock on track 80. As will be seen shortly, the advancing of the one-per-revolution clock is effective to perform the required shift-left operation when a new value is stored in the memory.

Once a day, prior to the start of trading, line 42 contains the close price for the preceding trading day for the various stocks. When this close price is loaded into input data register 58, a signal also appears on close-price line 110. This line conditions gate 112 (FIG. 4B) to pass the close price on line 70 through line 114 OR-gate 116 and line 118 into register 120. The close signal on line 110 is also applied as one input to AND-gate 122. At clock times V12, L2, H4, H5 and H6 AND-gate 122 is fully conditioned to generate an output signal on line 124 which is applied through OR-gate 126 and line 128 to condition gate 130 to pass the contents of register 120 on line 132 through gate 130, line 134, OR-gate 74 and line 76, to be written in memory 60. The close price shown in FIG. 1 is in this manner obtained. It should be noted that the close price is written in memory twice. It is written at H4 and H5 to cause a numeric display of the close price, and at H6 to cause the generation of the close price dot 12.

It is apparent that, since close prices appear on line 42 only once a day, the stock on which a graphic display is being obtained cannot be changed during the course of a single day with the embodiment shown. However, the before-mentioned Greenblum et al. application teaches how several close prices may be stored on drum 60 for future use. A system could also be designed where the close price on a selected stock would be available on line 42 in response to an input request.

The final input to memory 60 is obtained from keyboard 138 (FIG. 4B). This keyboard is used to indicate the ID for the stock which is having its prices graphically displayed and, in addition to being used to load memory 60, may also be used to load ID register 44. As each character is generated from keyboard 138, coded signals appear on lines 140, which signals are applied through OR-gate 116 and line 118 to be stored in register 120. When a key is depressed on keyboard 138, a signal appears on keyboard line 142. This signal may, for example, be obtained by ORing the outputs on lines 140. This signal on line 142 is applied as one input to AND-gate 144. The other inputs to AND-gate 144 are clock lines V12, L2 and H10-13. Output line 146 from AND-gate 144 is applied through OR-gate 126 and line 128 to condition gate 130 to pass the stock ID in register 120 through line 134 to be stored in memory 60. From FIG. 1 it will be seen that the positions in which the IDs are loaded are the same as those in which the IDs are displayed. The manner in which these stored characters are utilized will be described shortly.

Before describing the manner in which the dots 12 and 14 are generated, one additional load operation should be described. As was indicated previously, the information stored in memory 60 is shifted left one position by advancing the one-per-revolution clock on track 80 which is used to synchronize clock 18. However, while it is desired to shift the value information in memory 60, it is not desired to shift the alpha-numeric information for the stock ID and the close price, nor is it desired to shift the dot 12. In order to prevent this from happening, these characters are effectively shifted right one stroke position during the first memory cycle after the rewriting of the one-per-revolution clock. It will be remembered from previous discussion that during this cycle the clock is still operating under control of the previous one-per-revolution marker.

During L2, H4, H5 and H6 time of this memory cycle, AND-gate 150 is fully conditioned to generate an output on line 152 which is applied to condition gate 154 to pass the close price then being read from memory 60 through line 156, conditioned gate 154, and line 158, into register 120. At this time, advance flip-flop 98 (FIG. 4A) is still in its ONE state causing a signal to appear on advance line 100 which signal is applied as one input to AND-gate 160 (FIG. 4B). The other inputs to this AND-gate are clock lines V12, L3, and H4, H5 and H6. Therefore, one stroke time after each character of the

close price is loaded into register 120, AND-gate 160 is fully conditioned to generate an output signal on line 162 which is applied through OR-gate 126 and line 128 to condition gate 130 to rewrite the character then in register 120 in memory 60. The desired one-stroke shift-right of the close price, including the close price dot 12, is in this manner effected. The writing of the close price value in H6, L3, effectively erases the oldest value previously being displayed, which value was stored in that position. Similarly, during L2, H10-H13, AND-gate 150 is conditioned to pass the ID characters then being read from memory 60 through gate 154 to be stored in register 120. The signal on line 100 is also applied as a conditioning input to AND-gate 164. One stroke time after each of the ID characters is loaded into register 120, AND-gate 164 is fully conditioned to generate an output signal on line 166 which is applied through OR-gate 126 to condition gate 130 to pass this character back into memory 60. The desired shift-right of the ID characters is in this manner effected.

During H4 and H5 time of each revolution of memory 60, the close price stored in memory is gated through gate 154 into register 120. At V10 time of H4 and H5, AND-gate 170 (FIG. 4B) is fully conditioned to generate an output on line 172 which is applied to condition gate 174 to pass the clock price in register 120 through line 176, gate 174 and line 178 to be stored in register 180. During V11 and V12 time of H5, L2, the close price in register 180 is counted down under control of signals on line 182 from count-down control circuit 184. In addition to the clocks indicated above, which indicate when the count-down is to be performed, count-down control circuit 184 also has as inputs bit clock line 20, which is the clock input for the count-down, and range control lines 192, 194, and 196.

As was indicated previously, the scale factor utilized on the display is automatically controlled to be the first scale commensurate with the range of received data. For the illustrative embodiment shown in FIGS. 4A-4E, three possible ranges are possible, ± 2 , ± 4 or ± 8 . The ± 4 range line 194 is the ONE-side output from ± 4 flip-flop 198 (FIG. 4E). The ± 8 range line 196 is the ONE-side output line from ± 8 flip-flop 200. ZERO-side output lines 202 and 204 from flip-flops 198 and 200 respectively are connected as the inputs to AND-gate 206. Thus, when the circuit is in neither ± 4 nor in ± 8 range, AND-gate 206 is fully conditioned to generate an output on ± 2 range line 192. Initialize line 82 is applied through OR-gate 208 and line 210 to the ZERO-side input of flip-flop 198, and through OR-gate 212 and line 214 to the ZERO-side input of flip-flop 200. Therefore, the circuit is initially set to operate in the ± 2 range with a signal on line 192. The manner in which the circuit adjusts to display information with different ranges will be described shortly.

Range inputs 192-196 thus determine how much the close price in register 180 will be counted down for each received bit clock. As was indicated previously, the total amount by which the register is counted down will be sufficient to bring the price well below the horizontal axis. For example, the price may be counted down sufficiently to bring it to the level represented by a dot V3, B1 for the range selected.

At V1 of each stroke, the counted down close price in register 180 (FIG. 4C) is transferred through conditioned gates 220 to a first compare register 222. During V3-V12 of each stroke, the reduced close price in this register is counted up under control of signals on output line 224 from count-up control circuit 226. Again, a count-up occurs for each bit clock on line 20 with the amount by which the count in register 222 is counted up for each clock being controlled by the range signals on lines 192-196. In each instance the amount by which the count in register 222 is counted up for each bit clock is equal to the increment in price represented by each bit. Thus, with a range of ± 2 , the count up operation would be by 16th's. With a range of ± 4 , the count-up would be by eights while with the range of ± 8 , the count-up would be by quarters.

Each time the one-per-revolution clock is detected on track 80, GRF flip-flop 230 (FIG. 4C) is reset to its ZERO state. At

the following H6 time, this flip-flop is set to its ONE state. The resulting GRF signal on ONE-side output line 232 from this flip-flop is applied as one input to AND-gate 234. At each succeeding V1 and V2 time, AND-gate 234 is fully conditioned to generate an output signal on line 236 which is applied to condition gate 238 to pass the output from memory 60 on line 156 through line 240 to be stored in a second compare register 242. It will be remembered that the close price, in addition to being stored at H4 and H5, is also stored at H6, L2. The first value read into register 242 is thus the close price. This price is compared against the incremented values in register 222 in compare circuit 244. When the quantities in registers 222 and 242 are equal, compare circuit 244 generates a signal which will be referred to as the DOT signal on line 246. The DOT signal is applied through OR-gate 248 (FIG. 4D) and line 250 to display device 10' to cause the dot 12 to be recorded on the face of CRT 10. Display device 10' includes CRT 10 and its related control circuitry.

The close price of stroke H6, L2 is followed during the next stroke time by the first price to be displayed by a dot 14. Since GRF flip-flop 230 (FIG. 4C) remains in its ONE state until the end of the drum revolution, during V1 and V2 time of this following stroke, gate 238 is conditioned to pass this price into register 242. During V1 time, gate 220 is conditioned to pass the counted-down close price in register 180 into register 222. Starting at V3 time, this price is again counted up and compared in compare circuit 244 with the price now stored in register 242. When compare circuit 244 detects a match between these quantities, a Dot signal again appears on line 246 resulting in a dot 14 being recorded on the face of CRT 10. During each succeeding stroke, a new value is transferred into register 242, the counted-down close price is transferred into register 222, and the quantity of register 222 is incremented in steps of predetermined length. When the quantity in register 222 is incremented to a value equal to that stored in register 242, a Dot signal appears on line 246, resulting in the desired dot 14 appearing on the CRT. The display shown in FIG. 1 is in this manner obtained.

It should be noted that in addition to line 246, output line 254 from axis generator 256 (FIG. 4D), and output line 258 from character generator 260 are also inputs to OR-gate 248. Axis generator 256 has as inputs thereto the clock signals for the axis selected. For example, for the axis shown in FIG. 1, the inputs to generator 256 would be V4, B1 and H6, L1. Character generator 260 is a device which converts characters coded in a transmission or storage code, such as ASCII, into the equivalent video coded character. One input to character generator 260 is output line 262 from special character generator 264. Generator 264 could, for example, be utilized to generate the scale reference shown in FIG. 1. In order to obtain the proper scale reference, range lines 192-196 are applied as inputs to this generator. In addition, clocks would be applied as inputs to this generator to assure that the range characters were displayed at proper display positions.

The other input to character generator 260 is output line 266 from gate 268 (FIG. 4C). The information input to gate 268 is output line 132 from register 120 (FIG. 4B). It will be remembered that gate 154 is conditioned by outputs from AND-gate 150 to store both the close price and the stock ID in register 120 during appropriate clock times. Gate 268 is conditioned by a signal on output line 270 from OR-gate 272. The inputs to OR-gate 272 are output line 274 from AND-gate 276 and output line 278 from AND-gate 280. The inputs to AND-gate 276 are V8 and H4-H5. From FIG. 1 it is seen that these are the coordinates at which the close price is displayed. Similarly, the inputs to AND-gate 280 are V12, H10-H13. From FIG. 1, it is seen that these are the positions at which the stock identification characters are displayed. Thus, at appropriate times in the display cycle, the close-price characters and the stock identification characters are applied to character generator 260. This results in the display of these characters on the CRT screen.

As was indicated previously, range flip-flops 198 (FIG. 4E) and 200 are originally reset, resulting in an output on ± 2 range line 192. If a dot is detected outside this range, for example in V3 or V12, then the range is too fine and must be expanded. This is accomplished by applying the Dot output on line 246 as one input to AND-gate 284, the other input to this AND-gate being output line 286 from OR-gate 288. The inputs to OR-gate 288 are the V3 and V12 clock line. Thus, AND-gate 284 is fully conditioned when a dot appears in either V3 or V12. Output line 290 from AND-gate 284 is connected to the ONE-side input of flip-flop 292. ONE-side output line 294 from flip-flop 292 is connected as one input to AND-gates 296 and 298. The H1 clock line is a second input to each of these AND gates. The final input to AND-gate 296 is ± 2 line 192, and the final input to AND-gate 298 is ± 4 line 194. Therefore, AND-gate 296 is fully conditioned at the first H1 time after flip-flop 292 is set if the circuit is operating in the ± 2 range. Output line 300 from AND-gate 296 is applied through OR-gate 302 and line 304 to set flip-flop 198 to its ONE state. The range is in this manner expanded from ± 2 to ± 4 . Similarly, if the circuit is in ± 4 range, at the first H1 time after flip-flop 292 is set to its ONE state, AND-gate 298 is fully conditioned to generate an output signal on line 306 which is applied to set flip-flop 200 to its ONE state. The range is in this manner expanded from ± 4 to ± 8 .

Since, after fluctuating widely for a period, the price may again stabilize, it is also desirable to have the capability to reduce the range. For example, if it is found that there is no dot in V4, V5, V11, or V12, then the range may be safely reduced without losing any of the dots. This reduction is accomplished by applying Dot line 246 as one input to AND-gates 310 and 312. A second input to each of these AND gates is output line 314 from OR-gate 316. The inputs to OR-gate 316 are the V4, V5, V11 and V12 clock lines. The final input to AND-gate 310 is ± 4 range line 194 and the final input to AND-gate 312 is ± 8 range line 196. Thus, AND-gate 310 is fully conditioned if the circuit is in ± 4 range and a dot is located in V4, B5, V11 or V12. Similarly, AND-gate 312 is fully conditioned if the circuit is in ± 8 range and a dot is located in one of the four positions indicated above. Under these conditions, no range change is desired. Therefore, output lines 318 and 320 from AND-gates 310 and 312 respectively are connected through OR-gate 322 and line 324 to set flip-flop 326 to its ONE state. Flip-flop 326 is reset to its ZERO state by an H2 clock. ZERO-side output line 328 from flip-flop 326 is connected as one input to AND-gates 330 and 332. A second input to each of these AND gates is the H1 clock line. The final input to AND-gate 330 is ± 8 range line 196, while the final input to AND-gate 332 is ± 4 range line 194. Therefore, AND-gate 330 is fully conditioned at H1 time if the circuit is in ± 8 range and a dot has not been detected in one of the four V positions indicated above. Output line 334 from AND-gate 330 is connected through OR-gate 212 to reset flip-flop 200 to its ZERO state and through OR-gate 302 to set flip-flop 198 to its ONE state. The range is, in this manner reduced from ± 8 to ± 4 . Similarly, AND-gate 332 is fully conditioned at H1 time if the circuit is in ± 4 range and a dot does not appear in one of the four positions indicated above. Output line 336 from AND-gate 332 is connected through OR-gate 208 to reset flip-flop 198 to its ZERO state. This effectively restores the circuit to ± 2 range.

A system has thus been described for generating a combined alpha-numeric and graphic display of a succession of related values. The circuit is capable of recording a single dot for each value and of shifting the display in order to accommodate new information. Finally, the circuit is capable of adjusting the range of the display both up and down in order to provide the optimum range for any set of values to be displayed.

GENERAL DESCRIPTION OF FIRST ALTERNATIVE EMBODIMENT

As was indicated previously, the display of FIG. 1 contains only half the information which was contained in the display of FIG. 5 of the before-mentioned Greenblum et al. application. FIG. 2 illustrates a display format which is adapted to provide information both as to the price and volume for each transaction. In this display, the dots 12 and 14 appear much as they did in the embodiment of FIG. 1. However, in addition, each stroke also includes a bar 350 the height of which indicates the volume of the transaction. The display of FIG. 2 also includes the axis, I.D., close price, and price range shown in FIG. 1. In addition, the embodiment of FIG. 2 also includes a volume range. While this range may be expanded or contracted by detecting bar height in much the same way that the price scale is expanded and contracted, specific circuitry for performing this function will not be shown. Referring still to FIG. 2, it is noted that at points 352 at which a dot 14 intersects a bar 350, a blank space appears. This is the method which has been selected in this embodiment of the invention for illustrating the combined occurrence of a dot and a line at the same bit position. Other means, such as a flashing dot or a horizontal bar, could also be utilized.

The dots 14 in FIG. 2 are generated in a manner substantially identical to that of the dots shown in FIG. 1. The only difference involves the blanking of a dot when it coincides with a bar 350. The generating of the bars is complicated slightly by the fact that volume is assumed to be cumulatively received. Thus, each time a new cumulative volume is received, it is stored in a first compare register, and the previously stored cumulative volume is transferred to a second compare register. The contents of the second compare register is then incremented in synchronism with the tracing of the bar 350 on the face of CRT 10. When a match is detected between the volumes stored in the two compare registers, the intensifying of the writing beam is terminated.

DETAILED DESCRIPTION OF FIRST ALTERNATIVE EMBODIMENT

In the same manner that the price for each stock transaction is recorded on a track of memory 60, volume may also be recorded. Each volume figure would appear in a corresponding clock position on an adjacent track to the price for the given transaction. As was indicated previously, at H6, L1, GRF flip-flop 230 (FIG. 4C) is set to its ONE state resulting in an output signal on GRF line 232. At each V1 and V2 time thereafter, AND-gate 356 (FIG. 5) is fully conditioned to generate an output signal on line 358 which signal is applied to condition gate 360. The volume output from a volume track of memory 60 is applied through line 362, conditioned gate 360, and line 364 to be stored in volume register 366. As was indicated previously, this is a cumulative volume for all transactions up through the indicated one for a given day. As a new volume is being shifted into register 366, the previous volume stored in this register is shifted out through line 368 into cumulative volume register 370.

During the following V4-V9 time, the count in register 370 is incremented under control of signals on line 372 from counter control circuit 374. Circuit 374 effectively gates the bit clocks on line 20 through to increment the count in counter 370 during V4-V9 time. It should be noted that no means is provided in this circuit for controlling the amount by which the count is incremented. However, such circuitry could be provided, if desired, in much the same manner as it is provided in FIGS. 4A-4E.

The counts in registers 366 and 370 are continuously compared in compare circuit 376. When these counts are equal, compare circuit 376 generates an output signal on line 378 which is applied through OR gate 380 and line 382 to reset flip-flop 384 to its ZERO state. As will be seen shortly, this effectively terminates the writing of a line 350.

Flip-flop 384 is set to its ONE state by a signal on output line 386 from AND-gate 388. The inputs to AND-gate 388 are GRF line 232, an H-axis clock line, and output line 390 from inverter 392. Thus, flip-flop 384 is set to its ONE state each time a stroke after H6, L1 crosses the H-axis, provided that a successful comparison is not occurring at that time at compare circuit 376.

Referring still to FIG. 5, it is seen that the OR-gate 248 of FIG. 4D has been replaced by an OR-gate 248', the inputs to which are the same as those in FIG. 4D except that the single Dot input line 246 has been replaced by two lines. These lines are output line 394 from AND-gate 396 and output line 398 from AND-gate 400. The inputs to AND-gate 396 are Dot line 246 and ZERO-side output line 402 from flip-flop 384. Thus, a dot 14 will be written on the display when there is a signal on Dot line 246 and flip-flop 384 is reset indicating that a line 350 is not to be drawn. The inputs to AND-gate 400 are output line 404 from the ONE-side of flip-flop 384, no Dot line 406 and a clock line 408 which has a signal on it where the circuit is not on stroke H6, L1 or stroke H6, L2. The reason for inhibiting the writing of a volume stroke during stroke H6, L1 is that this is the stroke on which the vertical axis is drawn and, therefore, no volume is stored or displayed during the stroke. During H6, L2, a volume corresponding to the price which was overwritten by the close price is written into in register 366, but there is no meaningful volume figure in register 370 against which to compare it. Therefore, the volume display is again inhibited. This inhibiting is also proper since the H6, L2 stroke is the stroke during which the close price dot 12 is recorded.

It is thus seen that the writing of a line 350 is started when a stroke after H6, L2 crosses the horizontal axis and continues until a successful comparison is had in compare circuit 376. It should be noted that if a successful comparison does not occur before then, the V11 clock is applied through OR-gate 380 to reset flip-flop 384. This prevents a line 350 from going off the screen. It should also be noted that if, during the writing of a line 350, a Dot signal appears on line 246, this terminates the signal on line 406 effectively inhibiting the writing of a dot on the display and resulting in a blank space 352.

GENERAL DESCRIPTION OF SECOND ALTERNATIVE EMBODIMENT

A third type of graph which is frequently employed in the financial community is one which shows the range of price for a particular stock over a unit of time such as a day, week, month, etc. Such a graph may also include, somewhere along the range line, an indication of the last price for the item during the indicated period.

FIG. 3 illustrates the first few lines of such a graph. Each line 420 starts at the low price for the stock on, for example, a given trading day, and ends at the high price of the stock during the same day. A horizontal line 422 appears at the point along line 420 at which the stock closed on the given day. The reference price for the display may be the close price of the stock on the last trading day preceding the period being displayed, or the reference may be some other selected value.

To generate a display of the type shown in FIG. 3, the axis, scales, I.D.'s and the like would be generated in the same manner as for the embodiment of the invention shown in FIG. 4. High price, low price, and last price for the selected period would be stored in corresponding clock positions on different tracks of memory drum 60. Each of these values would be read into a corresponding register and compared against an incremented value which starts lower than the lowest value which is to be displayed. When the incremented value matches the low price, the intensification of the writing beam begins. A special indication, such as a blinking dot, horizontal line, blank space, or the like is provided when the incremented value equals the last price, and the intensifying of the beam is terminated when the incremented value equals the high price.

DETAILED DESCRIPTION OF SECOND ALTERNATIVE EMBODIMENT

FIG. 6 is a schematic diagram of a circuit for generating a display of the type shown in FIG. 3. Unlike the displays previously described, this display appears only on every other line, in this instance the even numbered lines L2, L4, and L6. During the odd line times, L1, L3, and L5, a signal appears on line 426. These signals are applied to condition gates 431-433 to pass the high price, last price, and low price respectively on lines 436-438 from the appropriate tracks on memory 60 through lines 441-443 to be stored in buffers 446-448. The contents of buffers 446-448 are applied through lines 451-453 respectively as one set of inputs to compare circuits 456-458. The other set of inputs to each of these compare circuits are output lines 460 from register 222. Referring back to FIG. 4C, it will be seen that register 222 is the register in which the incrementing of the previously reduced close price is performed.

When the price in register 222 equals the low price in buffer 448, compare circuit 458 generates an output signal on line 462 which is applied as one input to AND-gate 464 and through inverter 466 as one input to AND-gate 468. The other inputs to AND-gate 464 are even clock line 470 and output line 472 from inverter 474. The input to inverter 474 is a match output line 476 from high-price compare circuit 456. Output line 478 from AND-gate 464 is applied to the ONE-side input of flip-flop 480. ONE-side output line 482 from flip-flop 480 is applied through OR-gate 248'' to line 250 leading to display device 10'. It is thus seen that the match in compare circuit 258 results in the intensifying of the beam then being traced on display screen 10.

When the value in register 222 equals that in last price buffer 447, compare circuit 457 generates an output signal on line 484 which is applied to trigger special symbol generator 486. Special symbol generator 486 may, for example, cause a high frequency horizontal waveform to be momentarily impressed on the raster generating circuitry, or may cause the blinking of the spot in a manner similar to that described in the before-mentioned Greenblum et al. application. In any event, it causes the appearance of this dot to be different from those on the remainder of the line 420. Output line 488 from generator 486 is applied through OR-gates 248'' to line 250.

Finally, when the value in register 222 equals the value in high-price buffer 446, compare circuit 456 generates an output on line 476 which, during an even line time, fully conditions AND-gate 468 to generate an output signal on line 490. This signal is applied to reset flip-flop 480 to its ZERO state, thus terminating the input to OR-gate 248''. The intensifying of the beam on display screen 10 is thus terminated.

A system has thus been described which is capable of graphically displaying various stored values in a variety of different configurations. The circuit is versatile in that the number of quantities, the nature of the quantity, the nature of the display, and the range of values to be displayed may be varied. Since a display is locally generated the operator may select the item on which he wishes a display, and another user, being served by the same data base, may obtain a display of a different item. The data to be transmitted need contain only the values without including graphic information and may be utilized for other purposes such as alpha-numeric display or the like.

In the above embodiments described above, a fixed reference value, namely the close price, has always been utilized. It is apparent that some other reference value, such as, for example, the open price or a computed average price for the values displayed might be utilized instead as a reference value. Also, in the description above, the ranges above and below the reference value have always been equal. With more sophisticated detection and control circuitry, the range variations above and below the reference value might be individually varied so as to further optimize the display range. Similarly, while specific elements have been described above

for performing the display, storage, logic and other functions, it is apparent that functionally equivalent hardware or software elements might be utilized to perform each of these functions. Thus, while the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A system for displaying a graphic representation of a value on a display device of the type having a moving raster comprising:

- means for storing a representation of said value;
- means for storing a reference value which is initially less than said representation;
- means for successively adding a predetermined quantity to said reference value in synchronism with the movement of said raster;
- means operative each time said reference value is added to for comparing the new reference value with said representation; and
- means responsive to a match in said comparing means for causing a predetermined change in the display on said display device.

2. A system of the type described in claim 1 wherein said display device is a cathode ray tube (CRT).

3. A system of the type described in claim 1 wherein there are a plurality of said values to be graphically represented and including means for applying representations of said values in succession to said value representation storing means.

4. A system of the type described in claim 1 including means for indicating a selected range for said value representations; means for detecting whether the values applied to said value representation storing means conform to such selected range; and

- means responsive to a detection that the range of values applied to said value representation storing means differs from said selected range for changing the selected range.

5. A system of the type described in claim 4 including means responsive to said range indicating means for controlling said predetermined quantity.

6. A system of the type described in claim 5 wherein said range detecting means includes means for detecting whether a value applied to said value representation storing means is greater than or less than the values of said selected range; and wherein said predetermined quantity controlling means includes means responsive to said detection for increasing said predetermined quantity.

7. A system of the type described in claim 5 wherein said range detection means includes means for detecting when the values applied to said value representation storing means during a predetermine time period do not exceed in range a selected amount which amount is less than the range indicated by said range indicating means; and

- wherein said predetermined quantity controlling means includes means responsive to said detecting means for decreasing said predetermined quantity.

8. A system of the type described in claim 3 wherein there are a fixed number of value representation display positions on said display device; and

- including means responsive to an attempt to display a new value when all are said display positions of being used for displaying the representation of said new value in the display position previously occupied by the most recently received of the displayed values, for shifting all of the displayed values one display position in the appropriate direction, and for eliminating the oldest displayed value from the display.

9. A system of the type described in claim 1 including means for varying said predetermined quantity.

10. A system of the type described in claim 1 wherein said predetermined change causing means includes means for displaying a point on said display device.

11. A system of the type described in claim 10 including means for storing a given value; and means for decrementing said given value by a predetermined amount to obtain said reference value.

12. A system of the type described in claim 11 including means for controlling the amount by which said given value is decremented.

13. A system of the type described in claim 11 wherein said value is a last price value for a selected stock; wherein said given value is the close price for said stock on the preceding trading day; and including means for applying succeeding last price values for said selected stock to said value representation storing means.

14. A system of the type described in claim 13 including means for controlling the range of last prices which may be displayed on said display device.

15. A system of the type described in claim 14 wherein said range controlling means includes means for controlling the amount by which said given value is decremented, and means for controlling the predetermined quantity successively added to the resulting reference value.

16. A system of the type described in claim 14 including means for displaying an alpha-numeric indication of the selected stock, the close price, and the range of values being displayed.

17. A system of the type described in claim 13 wherein there are a fixed number of display positions on said display device at which a last-price value may be displayed; and including

means responsive to the receipt of a new last price for said selected stock when all of said display positions are full for displaying the new value in the position previously occupied by the most recently received of the displayed values, for shifting all the displayed values one display position in the appropriate direction, and for eliminating the oldest displayed value from the display.

18. A system of the type described in claim 1 including means for displaying alpha-numeric information with said graphic representation.

19. A system of the type described in claim 1 wherein the normal display on said display device is the drawing of a line; and

wherein said predetermined change causing means includes means for terminating the drawing of said line in response to a match in said comparing means.

20. A system of the type described in claim 19 including means for defining a horizontal axis for said display; means for tracing a vertical line on said display device starting at said horizontal axis; and wherein said line drawing terminating means is operative to terminate the drawing of said line.

21. A system of the type described in claim 20 wherein there are a plurality of said values to be graphically represented and including means for applying representations of said values in succession to said value representations storing means;

said line drawing means being operative to draw a line starting at said horizontal axis for each of said values.

22. A system of the type described in claim 21 wherein two different sets of values are to be simultaneously displayed on said display device;

wherein one of said sets of values is displayed by drawing lines starting at said horizontal axis which are terminated in response to a match in a first comparing means; and wherein said second set of values is represented by displaying a point on said display device in response to a match in a second comparing means.

23. A system of the type described in claim 22 wherein said two sets of values are related with corresponding values in each of said sets being displayed on the same vertical line; and including means for uniquely identifying a point where the two values on a common vertical line intersect.

24. A system of the type described in claim 23 wherein said means for uniquely identifying includes means for inhibiting the display at a point where a point representing a value of said second set occurs on a line representing a line of said first set.

25. A system of the type described in claim 21, wherein the values to be displayed are applied to said system as a cumulative amount; and including

means responsive to the receipt of a new value for transferring the value in said value representation storing means to said reference value storing means.

26. A system of the type described in claim 22 wherein said first set of values are volume values for succeeding transactions on a selected stock; and

wherein said second set of values are last price values for said transactions.

27. A system of the type described in claim 1 wherein said graphic representation is of two related values; and

including separate means for storing a representation of each of said values;

means for comparing the added to reference value with each of said representations;

means responsive to a match between said added to reference value and a first of said stored representations for initiating the drawing of a line on said display device; and

means responsive to a match between said added-to reference value and the other of said stored representations for terminating the drawing of the line on said display device.

28. A system of the type described in claim 27 wherein said graphic representation is of three related values;

wherein there is a separate one of said storing means and a separate one of said comparing means for each of the three values; and including

means responsive to a match between said added-to reference value and the third of said values for causing a unique mark to appear on said line.

29. A system of the type described in claim 28 wherein said line is a vertical line; and

wherein said unique mark is a short horizontal line intersecting said vertical line.

30. A system of the type described in claim 28 wherein said three values are the low price, high price, and last price respectively for a selected stock during a predetermined period of time.

31. A system of the type described in claim 27 wherein said display is of at least two sets of related values; and including means for applying succeeding corresponding values from each of said sets in succession to the appropriate value representation storing means.

32. In a CRT of the type having a raster scan with a plurality of index point containing strokes for each row displayed on the CRT screen, a system for displaying a graphic representation of a value comprising:

means for storing a representation of said value;

means for storing a reference value which is initially less than said representation;

means for successively increasing said reference value in steps of predetermined quantity in synchronism with said raster moving past the index points of a stroke;

means for comparing the increased reference value with said representation; and

means responsive to a match in said comparing means for causing a predetermined indication to appear on said CRT at the index point being scanned at the time of said match.

33. A system of the type described in claim 32 including means operative between the displayed portion of successive strokes for restoring the initial reference value in said reference value storing means.

34. A method of displaying a graphic representation of a value on a CRT of the type having a raster scan with a plurality

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of index point containing strokes for each row displayed on the CRT screen comprising the steps of:
storing a reference value which is initially less than said representation;
successively increasing said reference value in steps of 5
predetermined quantity in synchronism with said raster moving past index points of a stroke;
comparing the increased reference value with said represen-

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tation; and
generating a predetermined indication on said CRT at the index point being scanned when a match is detected during said comparing step.
35. A method of the type described in claim 34 including the step of restoring the initial reference value during the time interval between the displayed portion of successive strokes.

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