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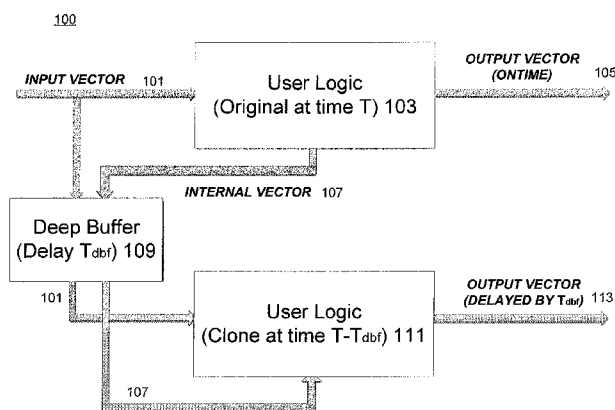


Fig. 1

(57) Abstract: A method and system for compiling a representation of a source circuit including one or more source subchannels associated with portions of source logic driven by a plurality of clock domains are described. Each source subchannel may generate packets carrying signal data from one of the portions of the source logic. A representation of a destination circuit may be compiled to include one or more destination subchannels associated with portions of destination logic replicating the source logic. Each destination subchannel may forward the signal data via the packets to one of the portions of the destination logic. A switching logic may be configured to map the source subchannels to the destination subchannels as virtual channels to forward the packets from the source subchannels to the destination subchannels. A single queue may be configured to couple with the switching logic to record packets from the source subchannels into a packet stream for a delay period to distribute to the destination subchannels. The destination logic may emulate the source logic synchronized with the plurality of clock domains delayed by the delay period.



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B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: packet, channel, mapping, debug, source

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006-0125517 A1 (DARREN VAN WAGENINGEN et al.) 15 June 2006 See abstract; paragraph 24 - paragraph 51 and figures 1,2	1-40
A	US 2008-0301601 A1 (CHUN KIT NG et al.) 04 December 2008 See abstract; paragraph 79 - paragraph 87	1-40
A	US 2006-0248377 A1 (BERTAN TEZCAN et al.) 02 November 2006 See abstract; paragraph 7 - paragraph 12, paragraph 58 - paragraph 73	1-40
A	US 2008-0191736 A1 (REDGRAVE JASON et al.) 14 August 2008 See abstract; paragraph 45 - paragraph 58	1-40

 Further documents are listed in the continuation of Box C. See patent family annex.

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