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Wojcik

[11] **3,786,485**

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[54] **BAKER CLAMPED SUSTAINER VOLTAGE GENERATOR FOR PULSING DISCHARGE DISPLAY PANEL**

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[52] **U.S. Cl.** ..... **340/324 M,** 307/327, 313/108 B, 315/169 R, 340/166 EL

[51] **Int. Cl.** **G08b 5/36**

[58] **Field of Search** ..... 340/324 R, 324 M, 340/166 R, 166 EL, 173 PL; 315/169 R, 169 TV; 313/108 B; 178/7.3 D; 307/327

[56] **References Cited**

UNITED STATES PATENTS

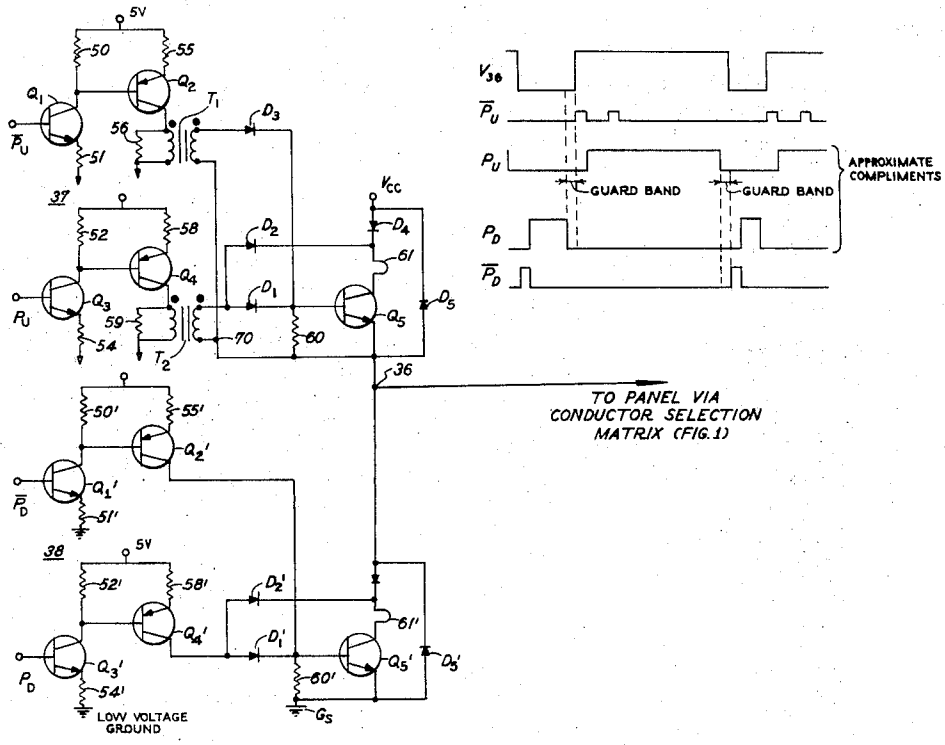
3,654,388	4/1972	Slottow et al.	178/7.3 D
3,225,217	12/1965	Corney	307/237
3,534,281	10/1970	Hillhouse	307/237 X

Primary Examiner—David L. Trafton
Attorney—Donald Keith Wedding et al.

[57] **ABSTRACT**

There is disclosed an improved sustaining voltage supply system for driving a gas discharge display panel having row-column conductor arrays, the matrix cross points of which are non-conductively coupled to a gaseous discharge medium in the panel. A pair of Baker clamped switching transistor amplifier circuits are series connected and have the intermediate point therebetween connected to supply square wave sustainer output voltages to the panel. Each amplifier circuit is provided with a Baker clamp diode circuit to avoid deep conduction or saturation operation of the switching transistors. The rise and fall times of the high power square wave output voltages are thereby much sharper and faster response to control signals by the circuit is achieved.

6 Claims, 3 Drawing Figures



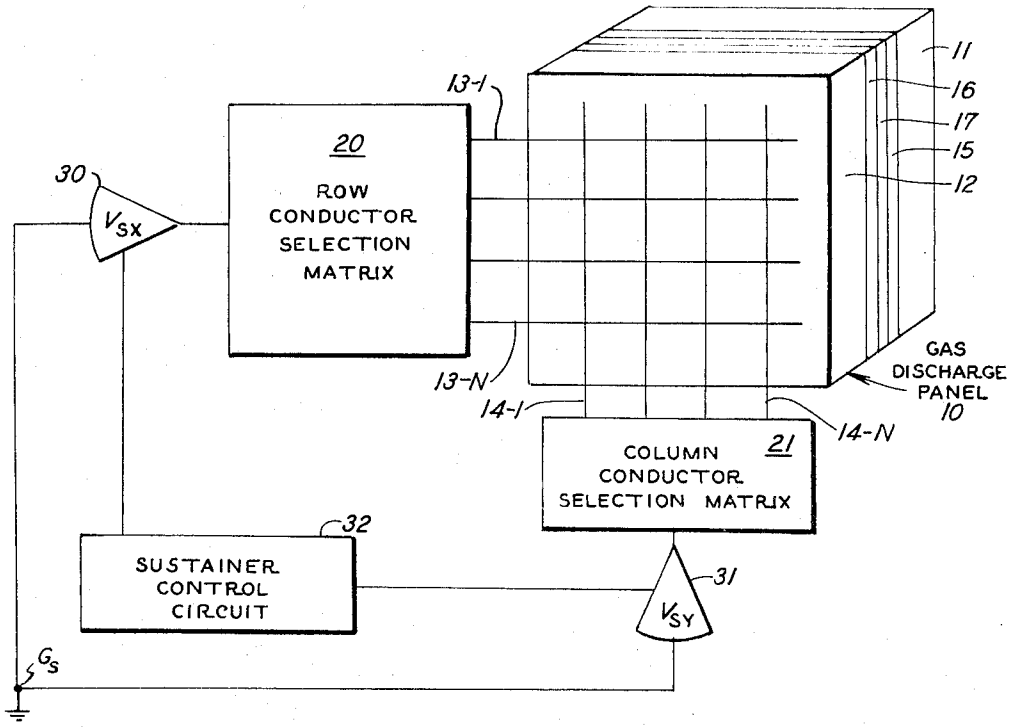

11
16
17
15
12
13-1
20
ROW CONDUCTOR SELECTION MATRIX
30
V_{SX}
13-N
14-1
14-N
GAS DISCHARGE PANEL 10
COLUMN CONDUCTOR SELECTION MATRIX 21
32
SUSTAINER CONTROL CIRCUIT
31
V_{SY}
G_S

Fig. 1

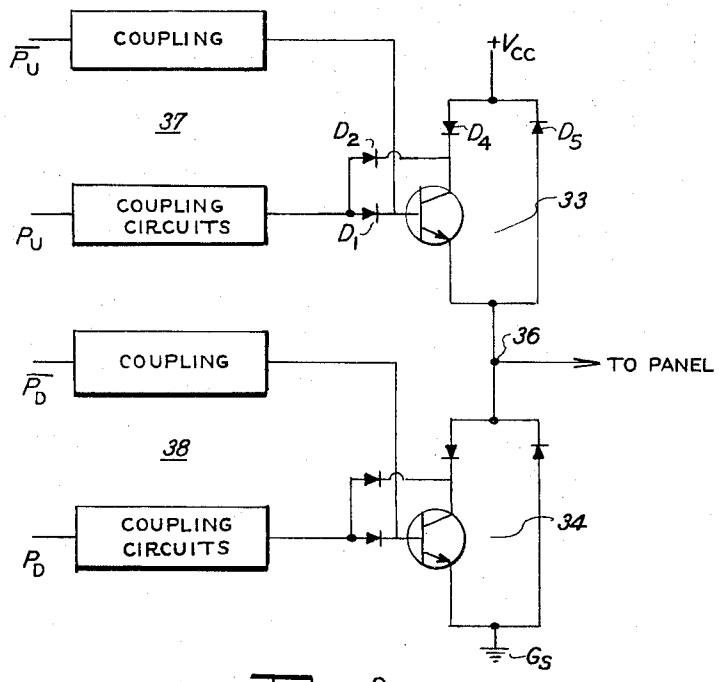

COUPLING
$\overline{P_U}$
37
COUPLING CIRCUITS
P_U
$+V_{CC}$
D_2
D_4
D_5
D_1
33
36
TO PANEL
COUPLING
$\overline{P_D}$
38
COUPLING CIRCUITS
P_D
34
G_S

Fig. 2

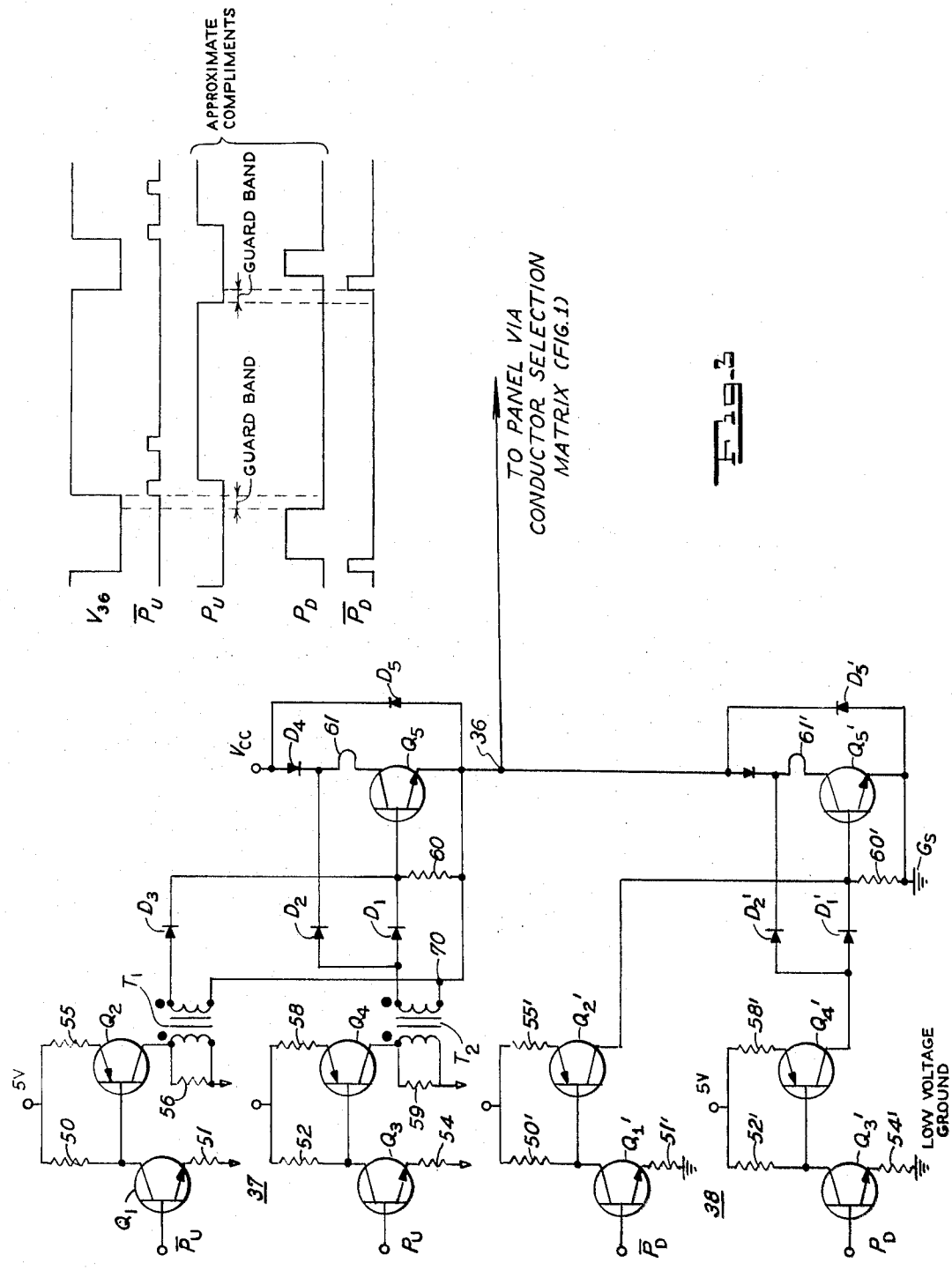

APPROXIMATE COMPLIMENTS
GUARD BAND
GUARD BAND
V_{36}
$\overline{P_U}$
P_U
P_D
$\overline{P_D}$
TO PANEL VIA CONDUCTOR SELECTION MATRIX (FIG.1)
V_{CC}
5V
LOW VOLTAGE GROUND
37
38

Fig. 3

BAKER CLAMPED SUSTAINER VOLTAGE GENERATOR FOR PULSING DISCHARGE DISPLAY PANEL

The present invention is directed to a sustaining voltage generator and supply system for gaseous discharge display panels having inherent memory sustaining voltage generators supply operating power to such gaseous discharge devices (as disclosed in Baker et al. U.S. Pat. No. 3,499,167 and/or Bitzer et al. U.S. Pat. No. 3,559,190 wherein the cross conductor arrays, e.g., the row and column conductors, are dielectrically isolated from the discharge medium so as to not be in conductive contact therewith and the load on the generator is essentially capacitive in nature. Because of the non-linearity of the impedance presented by the panel to the generator, and the pulsing nature of the discharges in the panel (e.g., the load current is pulsing in nature), distortion in the sustaining voltage waveform can effect the operating characteristics of the device to such an extent as to distort and disturb the memory function thereof.

The present invention is directed to a high power, square wave sustaining voltage generators for gas discharge display panels having lower distortion in the waveform of the sustainer voltage as applied to the panel. According to the invention, a pair of Baker clamped switching transistor amplifiers are connected in series across a supply voltage source with the intermediate point between the two transistor amplifiers being connected to the conductor arrays of the panel via any addressing and/or multiplexing circuit. Each such amplifier is provided with Baker clamp diode circuits, to avoid deep conduction or saturation operation of the transistors. Thus, the output is able to track the input over a very wide range of pulse widths and frequencies. Power dissipation in the output transistors is minimized and a large number of discharge sites may be driven by the generator.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, advantages and features of the invention will become more apparent in light of the following specification taken in conjunction with the accompanying drawings wherein:

FIG. 1 is a diagrammatic illustration of the gaseous discharge display panel to which the invention has been applied.

FIG. 2 is a simplified block diagram for illustrating the principles of the invention,

FIG. 3 is a circuit diagram illustrating details of a sustaining voltage generator incorporating the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. 1, the gaseous discharge display panel **10** is generally of the type disclosed in Baker et al. U.S. Pat. No. 3,499,167 and is constituted by a pair of support plates **11** and **12** on which are placed row conductor arrays **13** and column conductor array **14**, the conductor arrays having dielectric or insulating coatings **15** and **16** applied thereto so that there is no conductive current passing from the conductors via the dielectric coating to the gaseous medium, that is, the matrix cross points defined by the cross conductor arrays are non-conductively coupled to the gaseous discharge medium in the panel. The respective plates are joined in spaced apart relation by a spacer sealant means **17** to form a thin gaseous discharge chamber which may be placed a neon-argon gas mixture (99.9% neon and 0.1% argon is preferred) as is disclosed in Nolan application Ser. No. 764,577 filed Oct. 2, 1968. Other gaseous discharge mediums may likewise be incorporated in the panel but the improvement achieved by the use of the gas mixture recited above permits the panels to be operated in the 30– 50 kHz range without being damaged by thermal shock and at the same time with good light output and good memory margins. The dielectric or insulative layers **15** and **16** may be treated with a lead oxide coating (not shown) to lower the operating voltage level.

The individual conductors in row conductor matrix **13** are preferably driven by row conductor selection matrix **20** and the column conductors are preferably driven by column conductor selection matrix **21**, such selection matrices not forming a part of the present invention but may be constituted by diode-resistor selection matrices, multiplexed or non-multiplexed as may be desired. However, instead of a selection matrix operating on multiplex principles, individual pulsing circuits may be used for selecting individual ones of the row and column conductors respectively. The selection matrices **20** and **21** receive input signals from a signal source, not shown, but which may be a computer, keyset, tape reader or other data source.

A pair of sustaining generator voltage sources **30** and **31** are provided for supplying opposite phase or opposite polarity sustaining potentials to the row conductor array **13** and the column conductor array **14** in the panel **10.**

Since voltage on the gas at each one-half of the sustainer potential as applied to the panel (a) is applied to row conductors and the other one-half of the sustainer potential is applied to the column conductors, it being noted that the sustaining generators **30** and **31** have a common point or terminal Gs (which is not necessarily electrical ground) so that in the arrangement shown, the potentials generated in or produced by row conductor selection matrix **20** floats or is referenced to the potential from the sustainer generator source **30.** Similarly, the firing and discharge condition manipulating potentials generated in the column conductor selection matrix **21** are in series with and have as a reference point the instantaneous voltage from sustaining generator **31.** Moreover, both sustaining generators **30** and **31** receive controlling logic input signals from a source **32** which if desired, may be a computer, or other signal source. Thus, it may be desired at times to erase the panel in which case one of the signals applied to one of the sustainer generators **30** and **31** may simply be removed for a certain time interval to thereby permit bulk erasing of all information on the panel or it may be desirable to vary the sustaining rate by varying the sustaining rate from control circuit **32.**

Referring now to the block diagram shown in FIG. **2,** a sustaining voltage generator in accordance with the present invention is essentially constituted by a pair of Baker clamped transistor amplifier circuits **33** and **34,** respectively, which have an intermediate point **36** connected to the panel row or column conductor selection matrix for supplying sustaining potentials to the corresponding row or column conductor on the panel **10.** Each transistor circuit **33** and **34** is provided with its as-

sociated control signal coupling means **37** and **38**, respectively, which isolate control circuit **32** from the high voltage circuits, and, at the same time assure positive control over the alternate switching of the transistors.

Referring to FIG. **3**, one sustaining generator for one of the conductor arrays is shown in detail, it being appreciated that the conductors in the array may be sectioned or grouped with a sustainer generator for each section or group of conductors on the display panel shown in FIG. **1**. The control signal input to control circuit **37** is constituted by a pair of pull up signal voltage pulses, with timing relationship to the pair of pull up voltage pulses as shown in the wave form diagrams. NPN transistor Q1 has its collector connected through a collector resistor **50** to a low voltage control source and its emitter connected through resistor **51** to a low voltage ground (which is not the same as group Gs). A separate signal is applied to the base of NPN transistor Q3 which, in a similar fashion has its collector connected through a resistor **52** to the low voltage power supply and its emitter connected through an emitter resistor **54** to the low voltage ground. The collector of transistor Q1 is connected directly to the base of PNP transistor Q2 which has its emitter connected through resistor **55** to the low voltage supply and its collector connected through the primary winding of transformer T1 to the low voltage ground. Resistor **56** is connected in parallel with the primary winding of transformer T1 so as to provide a controlled recovery therefor.

In a similar manner, an output is taken from the collector of transistor Q3 and applied to the base of PNP transistor Q4 which has its emitter connected through resistor **58** to the low voltage supply and its collector connected through the primary winding of transformer T2 to the low voltage ground. Resistor **59** is connected in parallel with the primary winding of transformer T2 to provide a control recovery therefore. The polarity relationship between the primary and secondary of the transformers T1 and T2 is as indicated by the dots.

The lower end of the secondary winding of transformer T1 is connected to a common point **70** at the lower end of the transformer secondary of transformer T2 both of which are connected to the emitter electrode of transistor Q5 which is the switching and load carrying transistor. However, the upper end of the secondary winding of transformer T2 is connected through a diode D1 to the base electrode of transistor Q5 and, by way of a Baker clamp diode D2 to the collector electrode of transistor Q5. The upper end of the secondary winding of transformer T1 is connected through diode D3 to the base electrode of transistor Q5. A low value resistor **60** is connected between the base and emitter electrode of transistor Q5 and a current loop **61** is connected to provide a measuring point for current flow to the collector of transistor Q5 along with a heat sink (not shown). The collector of transistor Q5 is then connected to the high voltage supply Vcc (of about 150 volts) through diode D4, which diode prevents transistor Q5 from turning on in an inverted mode. The bypass diode D5 is for the purpose of providing a return pass for charging currents to the panel when the generator on the opposite sides of the panel is reversed. If these diodes D5, D4 were not present, the charging of the panel or load could spike the transistor Q5 on if this blocking and bypassing were not provided.

Diodes D1 and D2 clamp transistor Q5 on and constitute, in effect, a modified Baker clamp circuit. Thus, these diode circuits render the switching transistor Q5 in a conductive state to avoid deep conduction or full saturation operation of this transistor. The rise and fall times of the square wave voltage generated at the output is thereby much sharper and a fast response to control signals is achieved thereby. Transistors Q1 and Q2, via transformer T1, supply the high base current pulses to transistor Q5 which causes this transistor to saturate for the period in which the discharge takes place. Transistor Q3 and Q4, via transformer T2, presents a drive to base of transistor Q5, via diode D1 that goes through the collectors if the device is saturated and tends to turn the transistor Q5 off. Once this tends to happen, current is drawn through diode D2 and D1 to supply only the base drive needed to keep transistor Q5 just out of saturation but always capable of handling the current that might be called for by the collector thereof.

Diode D3 is provided so as to present a high impedance to the secondary of transformer T2 and thereby prevent the secondary of transformer T1 from shorting the signal from transformer secondary T2. That is, diode D3 isolates the base drive so that the pulse on the transformer secondary T2 is effective at the base of transistor Q5.

By avoiding the deep saturation condition in transistor Q5 by the use of the modified Baker diode clamping circuits described above, the effect of charge storage time in transistors Q5 which is detrimental to the wave form supplied to the panel, is reduced. Moreover, the sensitivity or responsiveness to inputs signals on the bases of transistors Q1 and Q3 is greatly improved.

The lower half of the circuit, e.g., the pull down half, constituted by transistors Q1', Q2' and Q3', Q4' is essentially identical to the operation of the control circuit **37**. In this case, since transformers T1 and T2 are not necessary, diode D3 is not necessary. That is, transistor Q2 in itself presents a high impedance to the output from transistor Q4 so that the output of transistor Q4 is applied directly to the base of transistor Q5'. It will be noted that both transistor Q2' and transistor Q4' utilize in effect, the same collector resistor which corresponds to resistor **60** in the pull up circuitry.

The circuit as described provides the flexibility of the output signal so as to make it closely track the input, provides a reduced power dissipation and approaches the ideal square wave form to a much better approximation than heretofore. In addition, the circuit permits the driving of more discharge sites from a single generator. The output square wave from this sustainer generator closely tracks the combined input voltages applied to the bases of transistors Q1, Q3 and Q1', Q3' over a very wide range of pulse widths and frequencies. The modified Baker clamp as disclosed is such that the output transistors are saturated for a portion of the period only and are not saturated for the remaining time. This pulling out of saturation is accomplished by the resistor **R60** draining the charge out of the base of Q5 while all of the secondary current of T2 is flowing through D2. Thus, the basic feature of this invention is in the use of the modified clamp circuit so as to avoid deep saturation of the output transistors of a sustainer generator for applying square wave output voltages to a high power capacitative load as constituted by a gaseous dis-

charge display panel of the type disclosed in the aforementioned Baker et al. patent.

It will be apparent that many modifications and adaptations of the invention will become apparent to those skilled in the art and it is intended to encompass such obvious modifications and changes in the scope of the claims appended hereto.

What is claimed is:

1. In a system for supplying square wave sustaining potentials to transversely related conductor arrays in a capacitive load type gas discharge display panel wherein the crossing points of said conductor arrays locates a discharge site in the panel, a high voltage direct current voltage source having a pair of output terminals, a first pair of alternatively conductive transistor means connected in series across said high voltage source and having a point intermediate said pair of transistor means connected to one of said conductor arrays, a second pair of alternatively conductive transistor means connected in series across said high voltage source and a point intermediate said second pair of transistor means being connected to the other one of said conductor arrays, a control means for controlling the alternative conduction and non-conduction conditions of said transistor means at selected times such that square wave sustaining potentials are connected to said conductor arrays respectively, to supply charging current thereto and secondly to said point of reference potential common to said sources to discharge said conductor arrays, said control means including a separate control circuit for each transistor to control the time duration of each square wave potential respectively, and means connecting each said control circuit to receive a low level logic voltage from a source thereof, the improvement comprising:

each of said alternately conductive transistor means being constituted by at least one modified Baker clamped transistor circuit including diode clamp means between the collector and base electrodes to provide a base current drive to the transistor to maintain same out of deep saturation at times other than peak currents to supply displacement currents to said capacitive load type gas discharge panel and discharge currents to said panel when a plurality of sites in said panel are discharging.

2. A square wave sustainer voltage supply system for a gas discharge display panel having row-column conductor arrays, the matrix cross-points of which are non-conductively coupled to a gas discharge medium in the panel comprising a pair of square wave sustainer voltage generator means, one for the row conductor array and one for the column conductive array, respectively, each said sustainer generator means including

a pair of series connected, alternately conductive and non-conductive, respectively, transistor amplifiers,

means connecting an intermediate point between said transistor amplifiers to the conductors in an array,

diode circuit means, one for each said transistor amplifier and connected between the base and collector circuits of said transistor amplifiers to provide base current device to keep said transistor amplifiers out of deep saturation, unless required for peak or displacement and discharging currents, and

control means connected to the input circuits of said transistor amplifier for alternately controlling the conduction conditions thereof.

3. The invention defined in claim 2, each said diode circuit includes a diode means in circuit between the collector and base of the transistor amplifiers for carrying peak displacement or discharging current to said panel.

4. The invention in claim 3 wherein said diode means is constituted by a pair of back connected diodes having an intermediate point therebetween with the base of said transistor amplifier being connected to one end of one of said diodes and to receive one of said control signals and other end of said one diode is connected to receive the other control signal.

5. The invention defined in claim 1 wherein the control means for one of the transistor of a pair includes a pair of input transistors for receiving logic pulses,

a pair of transformers having primary windings connected to said input transistors, respectively, and secondary windings, and a common output for supplying a control signal to said transistor amplifier, and diode means in circuit with said secondary windings to constitute a blocking impedance to one of said secondary windings.

6. In a system for supplying square wave sustaining potentials to transversely related conductor arrays in a capacitive load type gas discharge panel wherein the crossing points of said conductor arrays locates a plurality of discharge sites in the panel, a high voltage direct current voltage source having a pair of output terminals, a first pair of alternately controllable impedance means connected in series across said high voltage source and having a point intermediate said first controllable impedance means connected to one of said conductor arrays, a second pair of controllable impedance means connected in series across said high voltage source in a polarity direction opposite said first pair of controllable impedance means and a point intermediate said second pair of controllable impedance means being connected to the other one of said conductor arrays, an impedance control means for alternately controlling rapid impedance lowering and rapid impedance raising of said controllable impedance means at selected times such that said high voltage source is first connected to said conductor arrays respectively, to supply charging current thereto and secondly to said point of reference potential common to said sources to discharge said conductor arrays, each of said controllable impedances being constituted by at least one transistor amplifier circuit, said impedance control means including a separate control circuit for each transistor amplifier to control the time duration of each square wave potential, means connecting each said control circuit to receive a low level logic voltage from a source thereof; the improvement comprising a diode clamp circuit between the collector and base of each transistor amplifier to provide base current drive to each said transistor and maintain same out of deep saturation at times other than peak currents and supply displacement currents to said capacitive load gas discharge panel and discharge currents to said panel when a plurality of sites in said panel are in the ON state.

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