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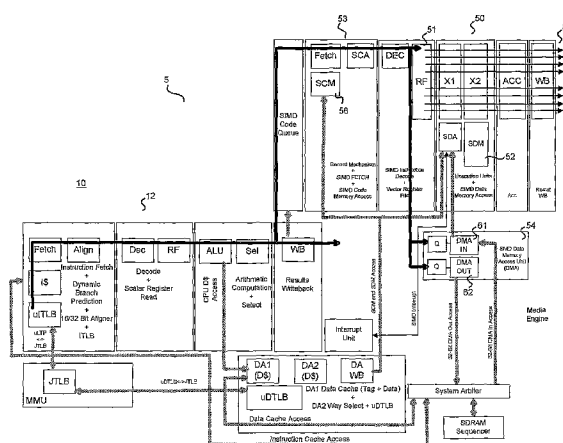
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[Continued on next page]

(54) Title: ARCHITECTURE FOR MICROPROCESSOR-BASED SYSTEMS INCLUDING SIMD PROCESSING UNIT AND ASSOCIATED SYSTEMS AND METHODS



(57) Abstract: An architecture for microprocessor-based systems is provided. The architecture includes a SIMD processing unit and associated systems and methods for optimizing the performance of such a system. In one embodiment systems and methods for performing systolic array-based block matching are provided. In another embodiment, a parameterizable clip instruction is provided. In an additional embodiment, two pair of deblocking instruction for use with the H.264 and VCI codecs provided. In a further embodiment, an instruction and datapath for accelerating sub-pixel interpolation are provided. In another embodiment, systems and methods for selectively decoupling processor extension logic are provided. In yet another embodiment, systems and methods for recording instruction sequences in a microprocessor having dynamically decoupleable extension logic is provided, hi yet one other embodiment, systems and methods for synchronizing multiple processing engines of a SIMD engine are provided.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2006/003358

A. CLASSIFICATION OF SUBJECT MATTER

INV. G06F9/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 93/08526 A (INTEL CORP [US]) 29 April 1993 (1993-04-29) page 5, line 1 - line 10 figures 4a, 5a page 9, line 1 - line 20	1
A	US 5 884 057 A (BLOMGREN JAMES S [US] ET AL) 16 March 1999 (1999-03-16) column 2, line 27 - line 58 column 4, line 24 - line 33	1
A	GB 2 365 583 B (HEWLETT PACKARD CO [US]) 4 August 2004 (2004-08-04) page 1, line 28 - page 2, line 14	1
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Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

- *A* document defining the general state of the art which is not considered to be of particular relevance
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X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

* & * document member of the same patent family

Date of the actual completion of the international search

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>SMITH J E ET AL: "THE ASTRONAUTICS ZS-1 PROCESSOR" PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON COMPUTER DESIGN : VLSI IN COMPUTERS AND PROCESSORS. (ICCD). NEW YORK, OCT. 3 - 5, 1988, WASHINGTON, IEEE COMP. SOC. PRESS, US, 3 October 1988 (1988-10-03), pages 307-310, XP000093793 ISBN: 0-8186-0872-2 the whole document</p> <p>-----</p>	1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2006/003358

Box II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claim: 1

An instruction queue coupling two instruction pipelines between their respective front end and rear portions.

2. claim: 2

Issuing a begin record instruction to an extended instruction pipeline, causing the extended instruction pipeline to begin recording a sequence of instructions issued by a main instruction pipeline.

3. claim: 3

Coupling direct memory access (DMA) engines to an extended instruction pipeline; and blocking the extended instruction pipeline from further execution when a DMA engine instruction queue is full and a new DMA instruction arrives at the queue, until a current DMA operation is complete.

4. claim: 4

A method of performing block matching with a systolic array.

5. claim: 5

A method of causing a microprocessor to perform a clip operation.

6. claim: 6

A method of causing a microprocessor to perform a CODEC deblocking operation.

7. claim: 7

Performing heterogeneous arithmetic interpolation operations in a SIMD processor.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/IB2006/003358

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
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