(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
23 December 2015 (23.12.2015)

WIPO | PCT

(10) International Publication Number
WO 2015/193769 A1

(51) International Patent Classification:
H01L 29/786 (2006.01) *H01L 27/108* (2006.01)
H01L 21/336 (2006.01) *H01L 27/115* (2006.01)
H01L 21/8234 (2006.01) *H01L 29/78* (2006.01)
H01L 21/8242 (2006.01) *H01L 29/788* (2006.01)
H01L 21/8247 (2006.01) *H01L 29/792* (2006.01)
H01L 27/088 (2006.01)

(21) International Application Number:
PCT/IB2015/054367

(22) International Filing Date:
10 June 2015 (10.06.2015)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2014-125221 18 June 2014 (18.06.2014) JP

(71) Applicant: **SEMICONDUCTOR ENERGY LABORATORY CO., LTD.** [JP/JP]; 398, Hase, Atsugi-shi, Kanagawa 2430036 (JP).

(72) Inventor: **YAMAZAKI, Shunpei**; c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD., 398, Hase, Atsugi-shi, Kanagawa 2430036 (JP).

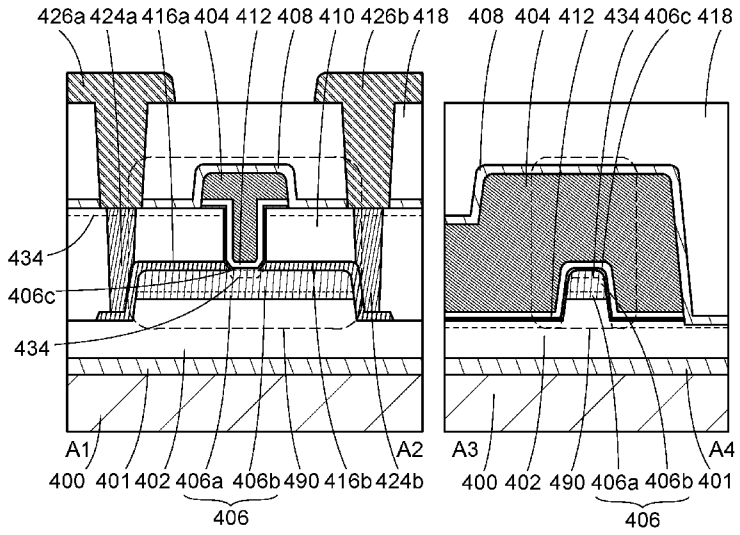
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) Title: TRANSISTOR AND SEMICONDUCTOR DEVICE

FIG. 1B



(57) Abstract: A transistor with small parasitic capacitance is provided. The transistor includes an oxide semiconductor, a first conductor, a second conductor, a third conductor, a first insulator, and a second insulator. The first conductor includes a first region, a second region, and a third region. The oxide semiconductor includes a fourth region, a fifth region, and a sixth region. The first region has a region where the first region and the sixth region overlap each other with the first insulator positioned therebetween. The second region has a region where the second region and the second conductor overlap each other with the first insulator and the second insulator positioned therebetween. The third region has a region where the third region and the third conductor overlap each other with the first insulator and the second insulator positioned therebetween. The fourth region has a region in contact with the second conductor.

WO 2015/193769 A1

DESCRIPTION

TRANSISTOR AND SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001]

The present invention relates to a transistor and a semiconductor device, and a manufacturing method thereof, for example. The present invention relates to a display device, a light-emitting device, a lighting device, a power storage device, a memory device, a processor, or an electronic device, for example. The present invention relates to a method for manufacturing a display device, a liquid crystal display device, a light-emitting device, a memory device, or an electronic device. The present invention relates to a driving method of a semiconductor device, a display device, a liquid crystal display device, a light-emitting device, a memory device, or an electronic device.

[0002]

Note that one embodiment of the present invention is not limited to the above technical field. The technical field of one embodiment of the invention disclosed in this specification and the like relates to an object, a method, or a manufacturing method. In addition, one embodiment of the present invention relates to a process, a machine, manufacture, or a composition of matter.

[0003]

In this specification and the like, a semiconductor device generally means a device that can function by utilizing semiconductor characteristics. A display device, a light-emitting device, a lighting device, an electro-optical device, a semiconductor circuit, and an electronic device include a semiconductor device in some cases.

BACKGROUND ART

[0004]

In recent years, a transistor including an oxide semiconductor has attracted attention. An oxide semiconductor can be formed by a sputtering method or the like, and thus can be used for a semiconductor of a transistor in a large display device. In addition, there is an advantage in a transistor including an oxide semiconductor that capital investment can be reduced because part of production equipment for a transistor including amorphous silicon can be retrofitted and utilized.

[0005]

It is known that a transistor including an oxide semiconductor has an extremely low leakage current in an off state. For example, a low-power CPU and the like utilizing the characteristics that a leakage current of the transistor including an oxide semiconductor is low is disclosed (see Patent Document 1).

[Reference]

[Patent Document]

[0006]

[Patent Document 1] Japanese Published Patent Application No. 2012-257187

DISCLOSURE OF INVENTION

[0007]

An object is to provide a transistor with low parasitic capacitance. Another object is to provide a transistor with high frequency characteristics. Another object is to provide a transistor with favorable electrical characteristics. Another object is to provide a transistor with stable electrical characteristics. Another object is to provide a transistor with low off-state current. Another object is to provide a novel transistor. Another object is to provide a semiconductor device including the transistor. Another object is to provide a semiconductor device which can operate at high speed. Another object is to provide a novel semiconductor device. Another object is to provide a module including the semiconductor device. Another object is to provide an electronic device including the semiconductor device or the module.

[0008]

Note that the descriptions of these objects do not disturb the existence of other objects. In one embodiment of the present invention, there is no need to achieve all the objects. Other objects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

[0009]

(1) One embodiment of the present invention is a transistor including an oxide semiconductor, a first conductor, a second conductor, a third conductor, a first insulator, and a second insulator. The first conductor includes a first region, a second region, and a third region. The oxide semiconductor includes a fourth region, a fifth region, and a sixth region. The first region has a region where the first region and the sixth region overlap each other with the first insulator positioned therebetween, the second region has a region where the second region and the second conductor overlap each other with the first insulator and the second insulator positioned therebetween, and the third region has a region where the third region and the third conductor overlap each other with the first insulator and the second insulator positioned

therebetween. The fourth region has a region in contact with the second conductor, and the fifth region has a region in contact with the third conductor. The sixth region has a region with a lower carrier density than a carrier density of the fourth region or the fifth region.

[0010]

(2) Another embodiment of the present invention is a transistor including an oxide semiconductor, a first conductor, a second conductor, a third conductor, a first insulator, and a second insulator. The first conductor includes a first region, a second region, and a third region. The oxide semiconductor includes a fourth region, a fifth region, and a sixth region. The first region has a region where the first region and the sixth region overlap each other with the first insulator positioned therebetween, the second region has a region where the second region and the second conductor overlap each other with the first insulator and the second insulator positioned therebetween, and the third region has a region where the third region and the third conductor overlap each other with the first insulator and the second insulator positioned therebetween. The fourth region has a region in contact with the second conductor, and the fifth region has a region in contact with the third conductor. The sixth region has a region with lower conductivity than conductivity of the fourth region or the fifth region.

[0011]

(3) Another embodiment of the present invention is a transistor including an oxide semiconductor, a first conductor, a second conductor, a third conductor, a first insulator, and a second insulator. The first conductor includes a first region, a second region, and a third region. The oxide semiconductor includes a fourth region, a fifth region, and a sixth region. The first region has a region where the first region and the sixth region overlap each other with the first insulator positioned therebetween, the second region has a region where the second region and the second conductor overlap each other with the first insulator and the second insulator positioned therebetween, and the third region has a region where the third region and the third conductor overlap each other with the first insulator and the second insulator positioned therebetween. The fourth region has a region in contact with the second conductor, and the fifth region has a region in contact with the third conductor. The sixth region has a region with a lower hydrogen concentration than a hydrogen concentration of the fourth region or the fifth region.

[0012]

(4) Another embodiment of the present invention is a semiconductor device including a p-channel transistor and an n-channel transistor. A source or a drain of the p-channel transistor is electrically connected to a source or a drain of the n-channel transistor, and a gate of the p-channel transistor is electrically connected to a gate of the n-channel transistor. The

p-channel transistor includes silicon in a channel formation region, and the n-channel transistor is the transistor described in any one of (1) to (3).

[0013]

(5) Another embodiment of the present invention is the semiconductor device described in (4) where the p-channel transistor is formed using a silicon substrate whose crystal plane in the top surface includes a region of a (110) plane.

[0014]

(6) Another embodiment of the present invention is the semiconductor device described in (4) or (5) where a channel formation region of the p-channel transistor has a concentration gradient where a concentration of an impurity imparting an n-type conductivity gets higher toward a vicinity of a surface of the channel formation region.

[0015]

(7) Another embodiment of the present invention is the semiconductor device described in any one of (4) to (6) where the gate of the p-channel transistor includes a conductor with a work function of 4.5 eV or higher.

[0016]

(8) Another embodiment of the present invention is the semiconductor device described in any one of (4) to (7) where the oxide semiconductor contains indium.

[0017]

(9) Another embodiment of the present invention is the semiconductor device described in any one of (4) to (8) where the oxide semiconductor includes a first oxide semiconductor, a second oxide semiconductor, and a third oxide semiconductor, and has a region where the first oxide semiconductor, the second oxide semiconductor, and the third oxide semiconductor overlap each other.

[0018]

Note that in the semiconductor device of one embodiment of the present invention, the oxide semiconductor may be replaced with another semiconductor.

[0019]

A transistor with low parasitic capacitance can be provided. A transistor with high frequency characteristics can be provided. A transistor with favorable electrical characteristics can be provided. A transistor with stable electrical characteristics can be provided. A transistor with low off-state current can be provided. A novel transistor can be provided. A semiconductor device including the transistor can be provided. A semiconductor device which can operate at high speed can be provided. A novel semiconductor device can be provided. A

module including the semiconductor device can be provided. Furthermore, an electronic device including the semiconductor device or the module can be provided.

[0020]

Note that the description of these effects does not disturb the existence of other effects. One embodiment of the present invention does not necessarily achieve all the effects listed above. Other effects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

BRIEF DESCRIPTION OF DRAWINGS

[0021]

In the accompanying drawings:

FIGS. 1A and 1B are a top view and a cross-sectional view illustrating a transistor of one embodiment of the present invention;

FIGS. 2A to 2D are cross-sectional views each illustrating part of a transistor of one embodiment of the present invention;

FIGS. 3A and 3B are a cross-sectional view and a band diagram of part of a transistor of one embodiment of the present invention;

FIGS. 4A and 4B are cross-sectional views each illustrating a transistor of one embodiment of the present invention;

FIGS. 5A and 5B are cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 6A and 6B are cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 7A and 7B are cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 8A and 8B are cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 9A and 9B are a top view and a cross-sectional view illustrating a transistor of one embodiment of the present invention;

FIGS. 10A and 10B are cross-sectional views each illustrating a transistor of one embodiment of the present invention;

FIGS. 11A and 11B are cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 12A and 12B are cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 13A and 13B are cross-sectional views illustrating a method for manufacturing a transistor of one embodiment of the present invention;

FIGS. 14A and 14B are each a circuit diagram of a semiconductor device of one embodiment of the present invention;

FIG. 15 is a cross-sectional view illustrating a semiconductor device of one embodiment of the present invention;

FIG. 16 is a cross-sectional view illustrating a semiconductor device of one embodiment of the present invention;

FIG. 17 is a cross-sectional view illustrating a semiconductor device of one embodiment of the present invention;

FIGS. 18A and 18B are each a circuit diagram of a memory device of one embodiment of the present invention;

FIG. 19 is a block diagram illustrating a CPU of one embodiment of the present invention;

FIG. 20 is a circuit diagram of a memory element of one embodiment of the present invention;

FIGS. 21A to 21C are a top view and circuit diagrams of display devices of one embodiment of the present invention;

FIGS. 22A to 22F each illustrate an electronic device of one embodiment of the present invention; and

FIGS. 23A and 23B are a perspective diagram illustrating an ashing apparatus and a conceptual diagram illustrating oxygen plasma in the ashing apparatus during oxygen addition treatment.

BEST MODE FOR CARRYING OUT THE INVENTION

[0022]

Hereinafter, embodiments of the present invention will be described in detail with the reference to the drawings. However, the present invention is not limited to the description below, and it is easily understood by those skilled in the art that embodiments and details disclosed herein can be modified in various ways. Further, the present invention is not construed as being limited to description of the embodiments and the examples. In describing structures of the present invention with reference to the drawings, common reference numerals are used for the same portions in different drawings. Note that the same hatched pattern is applied to similar parts, and the similar parts are not especially denoted by reference numerals in some cases.

[0023]

Note that the size, the thickness of films (layers), or regions in drawings is sometimes exaggerated for simplicity.

[0024]

In this specification, the terms “film” and “layer” can be interchanged with each other.

[0025]

In this specification, for example, for describing the shape of an object, the length of one side of a minimal cube where the object fits, or an equivalent circle diameter of a cross section of the object can be interpreted as the “diameter”, “grain size (diameter)”, “dimension”, “size”, or “width” of the object. The term “equivalent circle diameter of a cross section of the object” refers to the diameter of a perfect circle having the same area as the cross section of the object.

[0026]

A voltage usually refers to a potential difference between a certain potential and a reference potential (e.g., a ground potential (GND) or a source potential). A voltage can be referred to as a potential and vice versa.

[0027]

Note that the ordinal numbers such as “first” and “second” in this specification are used for convenience and do not denote the order of steps or the stacking order of layers. Therefore, for example, the term "first" can be replaced with the term "second", "third", or the like as appropriate. In addition, the ordinal numbers in this specification and the like are not necessarily the same as those which specify one embodiment of the present invention.

[0028]

Note that a “semiconductor” includes characteristics of an “insulator” in some cases when the conductivity is sufficiently low, for example. Further, a “semiconductor” and an “insulator” cannot be strictly distinguished from each other in some cases because a border between the “semiconductor” and the “insulator” is not clear. Accordingly, a “semiconductor” in this specification can be called an “insulator” in some cases. Similarly, an “insulator” in this specification can be called a “semiconductor” in some cases.

[0029]

Further, a “semiconductor” includes characteristics of a “conductor” in some cases when the conductivity is sufficiently high, for example. Further, a “semiconductor” and a “conductor” cannot be strictly distinguished from each other in some cases because a border between the “semiconductor” and the “conductor” is not clear. Accordingly, a “semiconductor”

in this specification can be called a "conductor" in some cases. Similarly, a "conductor" in this specification can be called a "semiconductor" in some cases.

[0030]

Note that an impurity in a semiconductor refers to, for example, elements other than the main components of the semiconductor. For example, an element with a concentration of lower than 0.1 atomic% is an impurity. When an impurity is contained, the density of states (DOS) may be formed in a semiconductor, the carrier mobility may be decreased, or the crystallinity may be decreased, for example. In the case where the semiconductor is an oxide semiconductor, examples of an impurity which changes characteristics of the semiconductor include Group 1 elements, Group 2 elements, Group 14 elements, Group 15 elements, and transition metals other than the main components; specifically, there are hydrogen (included in water), lithium, sodium, silicon, boron, phosphorus, carbon, and nitrogen, for example. In the case of an oxide semiconductor, oxygen vacancy may be formed by entry of impurities such as hydrogen. Further, in the case where the semiconductor is silicon, examples of an impurity which changes characteristics of the semiconductor include oxygen, Group 1 elements except hydrogen, Group 2 elements, Group 13 elements, and Group 15 elements.

[0031]

In this specification, the phrase "A has a region with a concentration B" includes, for example, "the concentration of the entire region in a region of A in the depth direction is B", "the average concentration in a region of A in the depth direction is B", "the median value of a concentration in a region of A in the depth direction is B", "the maximum value of a concentration in a region of A in the depth direction is B", "the minimum value of a concentration in a region of A in the depth direction is B", "a convergence value of a concentration in a region of A in the depth direction is B", and "a concentration in a region of A in which a probable value is obtained in measurement is B".

[0032]

In this specification, the phrase "A has a region with a size B, a length B, a thickness B, a width B, or a distance B" includes, for example, "the size, the length, the thickness, the width, or the distance of the entire region in a region of A is B", "the average value of the size, the length, the thickness, the width, or the distance of a region of A is B", "the median value of the size, the length, the thickness, the width, or the distance of a region of A is B", "the maximum value of the size, the length, the thickness, the width, or the distance of a region of A is B", "the minimum value of the size, the length, the thickness, the width, or the distance of a region of A is B", "a convergence value of the size, the length, the thickness, the width, or the distance of a

region of A is B", and "the size, the length, the thickness, the width, or the distance of a region of A in which a probable value is obtained in measurement is B".

[0033]

Note that a channel length refers to, for example, a distance between a source (a source region or a source electrode) and a drain (a drain region or a drain electrode) in a region where a semiconductor (or a portion where a current flows in a semiconductor when a transistor is on) and a gate electrode overlap with each other or a region where a channel is formed in a top view of the transistor. In one transistor, channel lengths in all regions are not necessarily the same. In other words, the channel length of one transistor is not limited to one value in some cases. Therefore, in this specification, the channel length is any one of values, the maximum value, the minimum value, or the average value in a region where a channel is formed.

[0034]

A channel width refers to, for example, the length of a portion where a source and a drain face each other in a region where a semiconductor (or a portion where a current flows in a semiconductor when a transistor is on) and a gate electrode overlap with each other, or a region where a channel is formed. In one transistor, channel widths in all regions do not necessarily have the same value. In other words, a channel width of one transistor is not fixed to one value in some cases. Therefore, in this specification, a channel width is any one of values, the maximum value, the minimum value, or the average value in a region where a channel is formed.

[0035]

Note that depending on transistor structures, a channel width in a region where a channel is formed actually (hereinafter referred to as an effective channel width) is different from a channel width shown in a top view of a transistor (hereinafter referred to as an apparent channel width) in some cases. For example, in a transistor having a three-dimensional structure, an effective channel width is greater than an apparent channel width shown in a top view of the transistor, and its influence cannot be ignored in some cases. For example, in a miniaturized transistor having a three-dimensional structure, the proportion of a channel region formed in a side surface of a semiconductor is higher than the proportion of a channel region formed in a top surface of a semiconductor in some cases. In that case, an effective channel width obtained when a channel is actually formed is greater than an apparent channel width shown in the top view.

[0036]

In a transistor having a three-dimensional structure, an effective channel width is difficult to measure in some cases. For example, to estimate an effective channel width from a design value, it is necessary to assume that the shape of a semiconductor is known as an

assumption condition. Therefore, in the case where the shape of a semiconductor is not known accurately, it is difficult to measure an effective channel width accurately.

[0037]

Therefore, in this specification, in a top view of a transistor, an apparent channel width that is the length of a portion where a source and a drain face each other in a region where a semiconductor and a gate electrode overlap with each other is referred to as a surrounded channel width (SCW) in some cases. Further, in this specification, in the case where the term "channel width" is simply used, it may denote a surrounded channel width and an apparent channel width. Alternatively, in this specification, in the case where the term "channel width" is simply used, it may denote an effective channel width in some cases. Note that the values of a channel length, a channel width, an effective channel width, an apparent channel width, a surrounded channel width, and the like can be determined by obtaining and analyzing a cross-sectional TEM image and the like.

[0038]

Note that in the case where electric field mobility, a current value per channel width, and the like of a transistor are obtained by calculation, a surrounded channel width may be used for the calculation. In that case, a value different from one in the case where an effective channel width is used for the calculation is obtained in some cases.

[0039]

Note that in this specification, the description "A has a shape jutting out from B" may indicate, for example, the case where at least one of end portions of A is positioned on an outer side than at least one of end portions of B in a top view or a cross-sectional view. Thus, the description "A has a shape jutting out from B" can be alternately referred to as the description "one of end portions of A is positioned on an outer side than one of end portions of B," for example in a top view.

[0040]

In this specification, the term "parallel" indicates that the angle formed between two straight lines is greater than or equal to −10° and less than or equal to 10°, and accordingly also includes the case where the angle is greater than or equal to −5° and less than or equal to 5°. A term "substantially parallel" indicates that the angle formed between two straight lines is greater than or equal to −30° and less than or equal to 30°. The term "perpendicular" indicates that the angle formed between two straight lines is greater than or equal to 80° and less than or equal to 100°, and accordingly includes the case where the angle is greater than or equal to 85° and less than or equal to 95°. A term "substantially perpendicular" indicates that the angle formed between two straight lines is greater than or equal to 60° and less than or equal to 120°.

[0041]

In this specification, the trigonal and rhombohedral crystal systems are included in the hexagonal crystal system.

[0042]

<Structure of Transistor>

The structures of transistors of embodiments of the present invention will be described below.

[0043]

<Transistor Structure 1>

FIGS. 1A and 1B are a top view and a cross-sectional view of a transistor 490 of one embodiment of the present invention. FIG. 1A is the top view. FIG. 1B is the cross-sectional view taken along dashed-dotted line A1-A2 and dashed-dotted line A3-A4 in FIG. 1A. Note that for simplification of the drawing, some components are not illustrated in the top view in FIG. 1A.

[0044]

In FIG. 1B, the transistor 490 includes an insulator 401 over a substrate 400; an insulator 402 over the insulator 401; a semiconductor 406a over the insulator 402; a semiconductor 406b over the semiconductor 406a; conductors 416a and 416b each including a region in contact with top and side surfaces of the semiconductor 406b and a side surface of the semiconductor 406a; an insulator 410 that is in contact with top surfaces of the conductors 416a and 416b and has an opening reaching the conductor 416a and an opening reaching the conductor 416b; a conductor 424a and a conductor 424b in contact with the conductor 416a and the conductor 416b, respectively, through the openings in the insulator 410; a semiconductor 406c in contact with the top surface of the semiconductor 406b; an insulator 412 over the semiconductor 406c; a conductor 404 over the semiconductor 406b with the insulator 412 provided therebetween; and an insulator 408 over the insulator 410 and the conductor 404. Note that the semiconductors 406a and 406b are collectively referred to as a semiconductor 406 in some cases.

[0045]

Note that the transistor 490 does not necessarily include the insulator 401. Note that the transistor 490 does not necessarily include the insulator 402. Note that the transistor 490 does not necessarily include the insulator 408. Note that the transistor 490 does not necessarily include the conductor 424a. Note that the transistor 490 does not necessarily include the conductor 424b. Note that the transistor 490 does not necessarily include the semiconductor 406a. Note that the transistor 490 does not necessarily include the semiconductor 406c.

[0046]

In FIG. 1B, an insulator 418 including an opening reaching the conductor 424a and another opening reaching the conductor 424b, a conductor 426a and a conductor 426b in contact with the conductor 424a and the conductor 424b, respectively, through the openings in the insulator 418 are over the insulator 408 of the transistor 490.

[0047]

In the transistor 490, the conductor 404 serves as a gate electrode. The insulator 412 serves as a gate insulator. The conductor 416a and the conductor 416b serve as a source electrode and a drain electrode. Therefore, resistance of the semiconductor 406b and the like can be controlled by a potential applied to the conductor 404. That is, conduction or non-conduction between the conductors 416a and 416b can be controlled by the potential applied to the conductor 404.

[0048]

In the transistor 490, the conductor 404 includes a region overlapping with the conductor 416a with the insulator 410 provided therebetween, and a region overlapping with the conductor 416b with the insulator 410 provided therebetween. The transistor 490 includes the insulator 410 between the conductor 404 and the conductor 416a, and between the conductor 404 and the conductor 416b, whereby parasitic capacitance can be reduced. Thus, the transistor 490 has high frequency characteristics.

[0049]

A case where the semiconductors 406a, 406b, and 406c are oxide semiconductors is described below.

[0050]

In the transistor 490, a region 434 with excess oxygen is included in the semiconductors 406b and 406c, the insulator 410, and the like. Note that a portion shown by a dashed line as the region 434 in FIG. 1B indicates a portion with the highest concentration of excess oxygen in the thickness direction. In addition to the region 434, a region with the high concentration of excess oxygen is present near the region 434. There may be a concentration gradient where the concentration of excess oxygen gets higher toward the region 434, for example. It is preferred that the region 434 be present in a channel formation region of the transistor 490 while hardly present in a source region or a drain region. Note that there may be the region with the highest concentration of excess oxygen at or in the vicinity of an interface between the semiconductor 406b and the semiconductor 406c.

[0051]

Excess oxygen is oxygen which can move in an oxide semiconductor through heat treatment or the like. Excess oxygen has a function of filling an oxygen vacancy. In addition, a portion from which excess oxygen is released does not form an oxygen vacancy. Therefore, when the oxide semiconductor includes excess oxygen, oxygen vacancies in the oxide semiconductor can be reduced in some cases. Excess oxygen reacts with hydrogen in the oxide semiconductor to form water in some cases. Therefore, in some cases, the hydrogen concentration can be reduced at or near the region with the high concentration of excess oxygen when hydrogen in the oxide semiconductor is diffused outward as water. Note that excess oxygen is included in an oxide insulator as well as the oxide semiconductor in some cases.

[0052]

Because the region 434 and the vicinity thereof contain excess oxygen, oxygen vacancies and/or hydrogen are/is reduced in the channel formation region. That is, carrier generation or the like caused by oxygen vacancies and/or hydrogen is not likely to occur in the channel formation region. Therefore, a shift of the threshold voltage of the transistor 490 in the negative direction, which occurs when a carrier density is high, can be suppressed. Meanwhile, because the influence of the region 434 is small and oxygen vacancies are not reduced in the source and drain regions, the source and drain regions can have lower resistance than the channel formation region. Therefore, the transistor 490 can have a high on-state current and a low off-state current.

[0053]

As illustrated in FIG. 1B, the side surfaces of the semiconductors 406a and 406b are in contact with the conductor 416a and the conductor 416b. In addition, the semiconductor 406b and the like can be electrically surrounded by an electric field of the conductor 404 serving as the gate electrode. A structure in which a semiconductor is electrically surrounded by an electric field of a gate electrode is referred to as a surrounded channel (s-channel) structure. Therefore, a channel is formed in the whole of the semiconductor 406b and the like (bulk) in some cases. In the s-channel structure, a large amount of current can flow between a source and a drain of the transistor, so that an on-state current can be increased. In addition, since the semiconductor 406b and the like are surrounded by the electric field of the conductor 404, an off-state current can be decreased.

[0054]

Note that electrical characteristics of the transistor 490 can be stabilized when the transistor 490 is surrounded by an insulator with a function of blocking oxygen and impurities such as hydrogen. For example, an insulator with a function of blocking oxygen and impurities such as hydrogen may be used as the insulator 401 and the insulator 408.

[0055]

An insulator with a function of blocking oxygen and impurities such as hydrogen may have a single-layer structure or a stacked-layer structure including an insulator containing, for example, boron, carbon, nitrogen, oxygen, fluorine, magnesium, aluminum, silicon, phosphorus, chlorine, argon, gallium, germanium, yttrium, zirconium, lanthanum, neodymium, hafnium, or tantalum may be used.

[0056]

For example, the insulator 401 may be formed of aluminum oxide, magnesium oxide, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, or tantalum oxide. Note that the insulator 401 preferably includes aluminum oxide or silicon nitride. The insulator 401 including aluminum oxide or silicon nitride can suppress entry of impurities such as hydrogen into the semiconductor 406b and the like, and can reduce outward diffusion of oxygen, for example.

[0057]

Furthermore, for example, the insulator 408 may be formed of aluminum oxide, magnesium oxide, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, or tantalum oxide. Note that the insulator 408 preferably includes aluminum oxide or silicon nitride. The insulator 408 including aluminum oxide or silicon nitride can suppress entry of impurities such as hydrogen into the semiconductor 406b and the like, and can reduce outward diffusion of oxygen, for example.

[0058]

The insulator 402 may have a single-layer structure or a stacked-layer structure including an insulator containing, for example, boron, carbon, nitrogen, oxygen, fluorine, magnesium, aluminum, silicon, phosphorus, chlorine, argon, gallium, germanium, yttrium, zirconium, lanthanum, neodymium, hafnium, or tantalum. The insulator 402 may be formed of, for example, aluminum oxide, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, or tantalum oxide.

[0059]

The insulator 402 may have a function of preventing diffusion of impurities from the substrate 400. In the case where the semiconductor 406b and the like are oxide semiconductors, the insulator 402 can have a function of supplying oxygen to the semiconductor 406b and the like.

[0060]

Each of the conductor 416a and the conductor 416b may have a single-layer structure or a stacked-layer structure including a conductor containing, for example, one or more kinds of boron, nitrogen, oxygen, fluorine, silicon, phosphorus, aluminum, titanium, chromium, manganese, cobalt, nickel, copper, zinc, gallium, yttrium, zirconium, molybdenum, ruthenium, silver, indium, tin, tantalum, and tungsten. An alloy or a compound may be used, for example, and a conductor containing aluminum, a conductor containing copper and titanium, a conductor containing copper and manganese, a conductor containing indium, tin, and oxygen, a conductor containing titanium and nitrogen, or the like may be used.

[0061]

An offset region or an overlap region can be formed depending on the shape of the end portion of the conductor 416a or 416b.

[0062]

In cross-sectional views in FIGS. 2A and 2B, θa is an angle between the top surface of the semiconductor 406 and a side surface of the conductor 416a at the end portion of the conductor 416a, and θb is an angle between the top surface of the semiconductor 406 and a side surface of the conductor 416b at the end portion of the conductor 416b. Note that when there is a range in angle at the end portion of the conductor 416a or at the end portion of the conductor 416b, the average value, the median value, the minimum value, or the maximum value of the angles is regarded as θa or θb. For easy understanding, the semiconductors 406a, 406b, and 406c are not individually illustrated in FIGS. 2A to 2D.

[0063]

In FIG. 2A, θa is large and the jutting amount of the conductor 416a is smaller than the thickness of the insulator 412, whereby an offset region Loffa is formed. Similarly, θb in FIG. 2A is large and the jutting amount of the conductor 416b is smaller than the thickness of the insulator 412, whereby an offset region Loffb is formed. For example, θa and θb may be each larger than or equal to 60° and smaller than 90°. Note that the size of Loffa and that of Loffb may be the same or different from each other. When the size of Loffa and that of Loffb are the same, for example, variation in electrical characteristics or shapes of a plurality of transistors 490 in a semiconductor device can be reduced. In contrast, when the size of Loffa and that of Loffb are different from each other, deterioration of the transistor 490 due to concentration of an electric field in a certain region can be reduced in some cases.

[0064]

In FIG. 2B, θa is small and the jutting amount of the conductor 416a is larger than the thickness of the insulator 412, whereby an overlap region Lova is formed. Similarly, θb in FIG. 2B is small and the jutting amount of the conductor 416b is larger than the thickness of the insulator 412, whereby an overlap region Lovb is formed. For example, θa and θb may be each larger than or equal to 15° and smaller than 60°, or larger than or equal to 20° and smaller than 50°. Note that the size of Lova and that of Lovb may be the same or different from each other. When the size of Lova and that of Lovb are the same, for example, variation in electrical characteristics or shapes of a plurality of transistors 490 in a semiconductor device can be reduced. In contrast, when the size of Lova and that of Lovb are different from each other, deterioration of the transistor 490 due to concentration of an electric field in a certain region can be reduced in some cases.

[0065]

Note that the transistor 490 may include both the overlap region and the offset region. For example, with Lova and Loffb, the on-state current can be increased, while the deterioration of the transistor 490 due to concentration of an electric field in a certain region can be reduced.

[0066]

In a cross-sectional view in FIG. 2C, the angle between the top surface of the semiconductor 406 and the side surface of the conductor 416a is approximately 90° at the end portion of the conductor 416a, and the angle between the top surface of the semiconductor 406 and the side surface of the conductor 416b is approximately 90° at the end portion of the conductor 416b. In that case, the thickness of the insulator 412 corresponds to the length of the offset region (denoted by Loffa or Loffb in FIG. 2C).

[0067]

In a cross-sectional view in FIG. 2D, the end portions of the conductors 416a and 416b have curved surfaces. With the curved surfaces of the end portions of the conductors 416a and 416b, concentration of an electric field in the end portions may be reduced. Therefore, the deterioration of the transistor 490 due to the concentration of the electric field may be reduced.

[0068]

The insulator 410 may have a single-layer structure or a stacked-layer structure including an insulator containing, for example, boron, carbon, nitrogen, oxygen, fluorine, magnesium, aluminum, silicon, phosphorus, chlorine, argon, gallium, germanium, yttrium, zirconium, lanthanum, neodymium, hafnium, or tantalum. For example, the insulator 410 can be formed of aluminum oxide, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, or tantalum oxide.

[0069]

Note that the insulator 410 preferably includes an insulator with low relative permittivity. For example, the insulator 410 preferably includes silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, resin, or the like. Alternatively, the insulator 410 preferably has a stacked-layer structure of silicon oxide or silicon oxynitride and resin. When silicon oxide or silicon oxynitride, which is thermally stable, is combined with resin, the stacked-layer structure can have thermal stability and low relative permittivity. Examples of the resin include polyester, polyolefin, polyamide (e.g., nylon or aramid), polyimide, polycarbonate, and acrylic.

[0070]

The insulator 412 may have a single-layer structure or a stacked-layer structure including an insulator containing, for example, boron, carbon, nitrogen, oxygen, fluorine, magnesium, aluminum, silicon, phosphorus, chlorine, argon, gallium, germanium, yttrium, zirconium, lanthanum, neodymium, hafnium, or tantalum. The insulator 412 may be formed of, for example, aluminum oxide, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, or tantalum oxide.

[0071]

Note that the insulator 412 preferably contains an insulator with a high dielectric constant. For example, the insulator 412 preferably includes gallium oxide, hafnium oxide, oxide including aluminum and hafnium, oxynitride including aluminum and hafnium, oxide including silicon and hafnium, oxynitride including silicon and hafnium, or the like. The insulator 412 preferably has a stacked-layer structure including silicon oxide or silicon oxynitride and an insulator with a high dielectric constant. Because silicon oxide and silicon oxynitride have thermal stability, combination of silicon oxide or silicon oxynitride with an insulator with a high dielectric constant allows the stacked-layer structure to be thermally stable and have a high dielectric constant. For example, when aluminum oxide, gallium oxide, or hafnium oxide of the insulator 412 is present on the semiconductor 406b side, entry of silicon included in the silicon oxide or the silicon oxynitride into the semiconductor 406b and the like can be suppressed. When silicon oxide or silicon oxynitride is contained on the semiconductor 406b side, for example, trap centers might be formed at the interface between aluminum oxide, gallium oxide, or hafnium oxide and silicon oxide or silicon oxynitride. The trap centers can shift the threshold voltage of the transistor in the positive direction by trapping electrons in some cases.

[0072]

The conductor 404 may have a single-layer structure or a stacked-layer structure including a conductor containing, for example, one or more kinds of boron, nitrogen, oxygen, fluorine, silicon, phosphorus, aluminum, titanium, chromium, manganese, cobalt, nickel, copper, zinc, gallium, yttrium, zirconium, molybdenum, ruthenium, silver, indium, tin, tantalum, and tungsten. An alloy or a compound may be used, for example, and a conductor containing aluminum, a conductor containing copper and titanium, a conductor containing copper and manganese, a conductor containing indium, tin, and oxygen, a conductor containing titanium and nitrogen, or the like may be used.

[0073]

Each of the conductor 424a and the conductor 424b may have a single-layer structure or a stacked-layer structure including a conductor containing, for example, one or more kinds of boron, nitrogen, oxygen, fluorine, silicon, phosphorus, aluminum, titanium, chromium, manganese, cobalt, nickel, copper, zinc, gallium, yttrium, zirconium, molybdenum, ruthenium, silver, indium, tin, tantalum, and tungsten. An alloy or a compound may be used, for example, and a conductor containing aluminum, a conductor containing copper and titanium, a conductor containing copper and manganese, a conductor containing indium, tin, and oxygen, a conductor containing titanium and nitrogen, or the like may be used.

[0074]

Each of the conductor 426a and the conductor 426b may have a single-layer structure or a stacked-layer structure including a conductor containing, for example, one or more kinds of boron, nitrogen, oxygen, fluorine, silicon, phosphorus, aluminum, titanium, chromium, manganese, cobalt, nickel, copper, zinc, gallium, yttrium, zirconium, molybdenum, ruthenium, silver, indium, tin, tantalum, and tungsten. An alloy or a compound may be used, for example, and a conductor containing aluminum, a conductor containing copper and titanium, a conductor containing copper and manganese, a conductor containing indium, tin, and oxygen, a conductor containing titanium and nitrogen, or the like may be used.

[0075]

The insulator 418 may have a single-layer structure or a stacked-layer structure including an insulator containing, for example, boron, carbon, nitrogen, oxygen, fluorine, magnesium, aluminum, silicon, phosphorus, chlorine, argon, gallium, germanium, yttrium, zirconium, lanthanum, neodymium, hafnium, or tantalum. The insulator 418 may be formed with, for example, aluminum oxide, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, or tantalum oxide.

[0076]

Note that the insulator 418 preferably includes an insulator with low relative permittivity. For example, the insulator 418 preferably includes silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, resin, or the like. Alternatively, the insulator 418 preferably has a stacked-layer structure of silicon oxide or silicon oxynitride and resin. When silicon oxide or silicon oxynitride, which is thermally stable, is combined with resin, the stacked-layer structure can have thermal stability and low relative permittivity. Examples of the resin include polyester, polyolefin, polyamide (e.g., nylon or aramid), polyimide, polycarbonate, and acrylic.

[0077]

An oxide semiconductor is preferably used for the semiconductors 406a, 406b, and 406c. However, silicon (including strained silicon), germanium, silicon germanium, silicon carbide, gallium arsenide, aluminum gallium arsenide, indium phosphide, gallium nitride, an organic semiconductor, or the like can be used in some cases.

[0078]

A structure of an oxide semiconductor is described below.

[0079]

Oxide semiconductors are classified roughly into a single-crystal oxide semiconductor and a non-single-crystal oxide semiconductor. The non-single-crystal oxide semiconductor includes any of a c-axis aligned crystalline oxide semiconductor (CAAC-OS), a polycrystalline oxide semiconductor, a microcrystalline oxide semiconductor, an amorphous oxide semiconductor, and the like.

[0080]

First, a CAAC-OS is described.

[0081]

A CAAC-OS is an oxide semiconductor having a plurality of c-axis aligned crystal parts.

[0082]

With a transmission electron microscope (TEM), a combined analysis image (high-resolution TEM image) of a bright-field image and a diffraction pattern of the CAAC-OS is observed, and a plurality of crystal parts can be found. However, in the high-resolution TEM image, a boundary between crystal parts, that is, a grain boundary is not clearly observed. Thus, in the CAAC-OS, a reduction in electron mobility due to the grain boundary is less likely to occur.

[0083]

In the high-resolution cross-sectional TEM image of the CAAC-OS observed in a direction substantially parallel to the sample surface, metal atoms arranged in a layered manner are seen in the crystal parts. Each metal atom layer has a configuration reflecting unevenness of a surface over which the CAAC-OS is formed (hereinafter, the surface is referred to as a formation surface) or a top surface of the CAAC-OS, and is arranged parallel to the formation surface or the top surface of the CAAC-OS.

[0084]

In the high-resolution planar TEM image of the CAAC-OS observed in a direction substantially perpendicular to the sample surface, metal atoms arranged in a triangular or hexagonal configuration are seen in the crystal parts. However, there is no regularity of arrangement of metal atoms between different crystal parts.

[0085]

A CAAC-OS is subjected to structural analysis with an X-ray diffraction (XRD) apparatus. For example, when the CAAC-OS including an $InGaZnO_4$ crystal is analyzed by an out-of-plane method, a peak appears frequently when the diffraction angle (2θ) is around 31°. This peak is derived from the (009) plane of the $InGaZnO_4$ crystal, which indicates that crystals in the CAAC-OS have c-axis alignment, and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS.

[0086]

Note that when the CAAC-OS with an $InGaZnO_4$ crystal is analyzed by an out-of-plane method, a peak of 2θ may also be observed at around 36°, in addition to the peak of 2θ at around 31°. The peak of 2θ at around 36° indicates that a crystal having no c-axis alignment is included in part of the CAAC-OS. It is preferable that in the CAAC-OS, a peak of 2θ appear at around 31° and a peak of 2θ not appear at around 36°.

[0087]

The CAAC-OS is an oxide semiconductor with a low impurity concentration. The impurity means here an element other than the main components of the oxide semiconductor, such as hydrogen, carbon, silicon, or a transition metal element. An element (specifically, silicon or the like) having higher strength of bonding to oxygen than a metal element included in an oxide semiconductor extracts oxygen from the oxide semiconductor, which results in disorder of the atomic arrangement and reduced crystallinity of the oxide semiconductor. A heavy metal such as iron or nickel, argon, carbon dioxide, or the like has a large atomic radius (or molecular radius), and thus disturbs the atomic arrangement of the oxide semiconductor and decreases crystallinity when included in the oxide semiconductor. Note that the impurity contained in the oxide semiconductor might serve as a carrier trap or a carrier generation source.

[0088]

Moreover, the CAAC-OS is an oxide semiconductor having a low density of defect states. For example, oxygen vacancies in the oxide semiconductor serve as carrier traps or serve as carrier generation sources when hydrogen is captured therein.

[0089]

The state in which impurity concentration is low and density of defect states is low (the number of oxygen vacancies is small) is referred to as a "highly purified intrinsic" or "substantially highly purified intrinsic" state. A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor has few carrier generation sources, and thus has a low carrier density in some cases. Thus, a transistor including the oxide semiconductor rarely has a negative threshold voltage (is rarely normally on). The highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor has few carrier traps. Accordingly, the transistor including the oxide semiconductor has little variation in electrical characteristics and high reliability. An electric charge trapped by the carrier traps in the oxide semiconductor takes a long time to be released. The trapped electric charge may behave like a fixed electric charge. Thus, the transistor which includes the oxide semiconductor having a high impurity concentration and a high density of defect states might have unstable electrical characteristics.

[0090]

In a transistor using the CAAC-OS, change in electrical characteristics due to irradiation with visible light or ultraviolet light is small.

[0091]

Next, a microcrystalline oxide semiconductor is described.

[0092]

A microcrystalline oxide semiconductor has a region in which a crystal part is observed and a region in which a crystal part is not observed clearly in a high-resolution TEM image. In most cases, the size of a crystal part included in the microcrystalline oxide semiconductor is greater than or equal to 1 nm and less than or equal to 100 nm, or greater than or equal to 1 nm and less than or equal to 10 nm. A microcrystal with a size greater than or equal to 1 nm and less than or equal to 10 nm, or a size greater than or equal to 1 nm and less than or equal to 3 nm is specifically referred to as nanocrystal (nc). An oxide semiconductor including nanocrystal is referred to as an nc-OS (nanocrystalline oxide semiconductor). In a high-resolution TEM image of the nc-OS, for example, a grain boundary is not clearly observed in some cases.

[0093]

In the nc-OS, a microscopic region (for example, a region with a size greater than or equal to 1 nm and less than or equal to 10 nm, in particular, a region with a size greater than or

equal to 1 nm and less than or equal to 3 nm) has a periodic atomic arrangement. There is no regularity of crystal orientation between different crystal parts in the nc-OS. Thus, the orientation of the whole film is not observed. Accordingly, in some cases, the nc-OS cannot be distinguished from an amorphous oxide semiconductor, depending on an analysis method. For example, when the nc-OS is subjected to structural analysis by an out-of-plane method with an XRD apparatus using an X-ray having a diameter larger than the diameter of a crystal part, a peak which shows a crystal plane does not appear. Furthermore, a diffraction pattern like a halo pattern is observed when the nc-OS is subjected to electron diffraction using an electron beam with a probe diameter (e.g., 50 nm or larger) that is larger than the diameter of a crystal part (the electron diffraction is also referred to as selected-area electron diffraction). Meanwhile, spots are shown in a nanobeam electron diffraction pattern of the nc-OS obtained by using an electron beam having a probe diameter close to, or smaller than the diameter of a crystal part. Moreover, in a nanobeam electron diffraction pattern of the nc-OS, regions with high luminance in a circular (ring) pattern are shown in some cases. Also in a nanobeam electron diffraction pattern of the nc-OS, a plurality of spots is shown in a ring-like region in some cases.

[0094]

The nc-OS is an oxide semiconductor that has high regularity as compared with an amorphous oxide semiconductor. Therefore, the nc-OS is likely to have a lower density of defect states than an amorphous oxide semiconductor. However, there is no regularity of crystal orientation between different crystal parts in the nc-OS. Therefore, the nc-OS has a higher density of defect states than the CAAC-OS.

[0095]

Next, an amorphous oxide semiconductor is described.

[0096]

The amorphous oxide semiconductor is such an oxide semiconductor having disordered atomic arrangement and no crystal part. For example, the amorphous oxide semiconductor does not have a specific state as in quartz.

[0097]

In a high-resolution TEM image of the amorphous oxide semiconductor, crystal parts cannot be found.

[0098]

When the amorphous oxide semiconductor is subjected to structural analysis by an out-of-plane method with an XRD apparatus, a peak which shows a crystal plane does not appear. A halo pattern is observed when the amorphous oxide semiconductor is subjected to electron

diffraction. Furthermore, a spot is not observed and a halo pattern appears when the amorphous oxide semiconductor is subjected to nanobeam electron diffraction.

[0099]

Note that an oxide semiconductor may have a structure having physical properties intermediate between the nc-OS and the amorphous oxide semiconductor. The oxide semiconductor having such a structure is specifically referred to as an amorphous-like oxide semiconductor (a-like OS).

[0100]

In a high-resolution TEM image of the a-like OS, a void may be observed. Furthermore, in the high-resolution TEM image, there are a region where a crystal part is clearly observed and a region where a crystal part is not observed. In the a-like OS, crystallization by a slight amount of electron beam used for TEM observation occurs and growth of the crystal part is found sometimes. In contrast, crystallization by a slight amount of electron beam used for TEM observation is less observed in the nc-OS having good quality.

[0101]

Note that the crystal part size in the a-like OS and the nc-OS can be measured using high-resolution TEM images. For example, an $InGaZnO_4$ crystal has a layered structure in which two Ga-Zn-O layers are included between In-O layers. A unit lattice of the $InGaZnO_4$ crystal has a structure in which nine layers of three In-O layers and six Ga-Zn-O layers are layered in the c-axis direction. Accordingly, the spacing between these adjacent layers is equivalent to the lattice spacing on the (009) plane (also referred to as d value). The value is calculated to be 0.29 nm from crystal structural analysis. Thus, with a focus on lattice fringes in the high-resolution TEM image, lattice fringes in which the lattice spacing therebetween is greater than or equal to 0.28 nm and less than or equal to 0.30 nm each correspond to the a-b plane of the $InGaZnO_4$ crystal.

[0102]

Furthermore, the density of an oxide semiconductor varies depending on the structure in some cases. For example, when the composition of an oxide semiconductor is determined, the structure of the oxide semiconductor can be estimated by comparing the density of the oxide semiconductor with the density of a single crystal oxide semiconductor having the same composition as the oxide semiconductor. For example, the density of the a-like OS is higher than or equal to 78.6% and lower than 92.3% of the density of the single crystal oxide semiconductor having the same composition. For example, the density of each of the nc-OS and the CAAC-OS is higher than or equal to 92.3% and lower than 100% of the density of the single crystal oxide semiconductor having the same composition. Note that it is difficult to

form an oxide semiconductor having a density of lower than 78% of the density of the single crystal oxide semiconductor.

[0103]

Specific examples of the above description are given. For example, in the case of an oxide semiconductor having an atomic ratio of In:Ga:Zn = 1:1:1, the density of single crystal $InGaZnO_4$ with a rhombohedral crystal structure is 6.357 g/cm^3. Accordingly, in the case of the oxide semiconductor having an atomic ratio of In:Ga:Zn = 1:1:1, the density of the a-like OS is higher than or equal to 5.0 g/cm^3 and lower than 5.9 g/cm^3. In addition, for example, in the case of the oxide semiconductor having an atomic ratio of In: Ga: Zn = 1:1:1, the density of each of the nc-OS film and the CAAC-OS film is higher than or equal to 5.9 g/cm^3 and lower than 6.3 g/cm^3.

[0104]

Note that single crystal oxide semiconductor with the same composition do not exist in some cases. In such a case, by combining single crystal oxide semiconductor with different compositions at a given proportion, it is possible to calculate density that corresponds to the density of a single crystal oxide semiconductor with a desired composition. The density of the single crystal oxide semiconductor with a desired composition may be calculated using weighted average with respect to the combination ratio of the single crystal oxide semiconductor with different compositions. Note that it is preferable to combine as few kinds of single crystal oxide semiconductor as possible for density calculation.

[0105]

Note that an oxide semiconductor may be a stacked film including two or more films of an amorphous oxide semiconductor, an a-like OS, a microcrystalline oxide semiconductor, and a CAAC-OS, for example.

[0106]

FIG. 3A is an enlarged cross-sectional view of a part of the transistor 490.

[0107]

Next, a semiconductor which can be used as the semiconductor 406a, the semiconductor 406b, the semiconductor 406c, or the like is described below.

[0108]

The semiconductor 406b is an oxide semiconductor containing indium, for example. An oxide semiconductor can have high carrier mobility (electron mobility) by containing indium, for example. The semiconductor 406b preferably contains an element *M*. The element *M* is preferably aluminum, gallium, yttrium, tin, or the like. Other elements which can be used as the element *M* are boron, silicon, titanium, iron, nickel, germanium, yttrium, zirconium,

molybdenum, lanthanum, cerium, neodymium, hafnium, tantalum, tungsten, and the like. Note that two or more of the above elements may be used in combination as the element *M*. The element *M* is an element having a high bonding energy with oxygen, for example. The element *M* is an element whose bonding energy with oxygen is higher than that of indium, for example. The element *M* is an element that can increase the energy gap of the oxide semiconductor, for example. Furthermore, the semiconductor 406b preferably contains zinc. When the oxide semiconductor contains zinc, the oxide semiconductor is easily to be crystallized in some cases.

[0109]

Note that the semiconductor 406b is not limited to the oxide semiconductor containing indium. The semiconductor 406b may be, for example, an oxide semiconductor which does not contain indium and contains zinc, an oxide semiconductor which does not contain indium and contains gallium, or an oxide semiconductor which does not contain indium and contains tin, e.g., a zinc tin oxide, a gallium tin oxide, or gallium oxide.

[0110]

For the semiconductor 406b, an oxide with a wide energy gap may be used. For example, the energy gap of the semiconductor 406b is greater than or equal to 2.5 eV and less than or equal to 4.2 eV, preferably greater than or equal to 2.8 eV and less than or equal to 3.8 eV, more preferably greater than or equal to 3 eV and less than or equal to 3.5 eV.

[0111]

For example, the semiconductor 406a and the semiconductor 406c include one or more, or two or more elements other than oxygen included in the semiconductor 406b. Since the semiconductor 406a and the semiconductor 406c each include one or more, or two or more elements other than oxygen included in the semiconductor 406b, an interface state is less likely to be formed at the interface between the semiconductor 406a and the semiconductor 406b and the interface between the semiconductor 406b and the semiconductor 406c.

[0112]

The case where the semiconductor 406a, the semiconductor 406b, and the semiconductor 406c contain indium is described. In the case of using an In-*M*-Zn oxide as the semiconductor 406a, when the summation of In and *M* is assumed to be 100 atomic%, the proportions of In and *M* are preferably set to be less than 50 atomic% and greater than 50 atomic%, respectively, more preferably less than 25 atomic% and greater than 75 atomic%, respectively. In the case of using an In-*M*-Zn oxide as the semiconductor 406b, when the summation of In and *M* is assumed to be 100 atomic%, the proportions of In and *M* are preferably set to be greater than 25 atomic% and less than 75 atomic%, respectively, more preferably greater than 34 atomic% and less than 66 atomic%, respectively. In the case of using

an In-*M*-Zn oxide as the semiconductor 406c, when the summation of In and *M* is assumed to be 100 atomic%, the proportions of In and *M* are preferably set to be less than 50 atomic% and greater than 50 atomic%, respectively, more preferably less than 25 atomic% and greater than 75 atomic%, respectively. Note that the semiconductor 406c may be an oxide that is a type the same as that of the semiconductor 406a.

[0113]

As the semiconductor 406b, an oxide having an electron affinity higher than those of the semiconductors 406a and 406c is used. For example, as the semiconductor 406b, an oxide having an electron affinity higher than those of the semiconductors 406a and 406c by 0.07 eV or higher and 1.3 eV or lower, preferably 0.1 eV or higher and 0.7 eV or lower, more preferably 0.15 eV or higher and 0.4 eV or lower is used. Note that the electron affinity refers to an energy gap between the vacuum level and the bottom of the conduction band.

[0114]

An indium gallium oxide has a small electron affinity and a high oxygen-blocking property. Therefore, the semiconductor 406c preferably includes indium gallium oxide. The gallium atomic ratio [Ga/(In+Ga)] is, for example, higher than or equal to 70%, preferably higher than or equal to 80%, more preferably higher than or equal to 90%.

[0115]

Note that the semiconductor 406a and/or the semiconductor 406c may be gallium oxide. For example, when gallium oxide is used for the semiconductor 406c, a leakage current generated between the conductor 404 and the conductor 416a or 416b can be reduced. In other words, the off-state current of the transistor 490 can be reduced.

[0116]

At this time, when a gate voltage is applied, a channel is formed in the semiconductor 406b having the highest electron affinity in the semiconductor 406a, the semiconductor 406b, and the semiconductor 406c.

[0117]

FIG. 3B is a band diagram taken along dashed-dotted line E1-E2 in FIG. 3A. FIG. 3B shows a vacuum level (denoted by vacuum level), and an energy of the bottom of the conduction band (denoted by Ec) and an energy of the top of the valence band (denoted by Ev) of each of the layers.

[0118]

Here, in some cases, there is a mixed region of the semiconductor 406a and the semiconductor 406b between the semiconductor 406a and the semiconductor 406b. Furthermore, in some cases, there is a mixed region of the semiconductor 406b and the

semiconductor 406c between the semiconductor 406b and the semiconductor 406c. The mixed region has a low density of interface states. For that reason, the stack of the semiconductor 406a, the semiconductor 406b, and the semiconductor 406c has a band structure where energy at each interface and in the vicinity of the interface is changed continuously (continuous junction).

[0119]

At this time, electrons move mainly in the semiconductor 406b, not in the semiconductor 406a and the semiconductor 406c. Thus, when the interface state density at the interface between the semiconductor 406a and the semiconductor 406b and the interface state density at the interface between the semiconductor 406b and the semiconductor 406c are decreased, electron movement in the semiconductor 406b is less likely to be inhibited and the on-sate current of the transistor 490 can be increased.

[0120]

In the case where the transistor 490 has an s-channel structure, a channel is formed in the whole of the semiconductor 406b. Therefore, as the semiconductor 406b has a larger thickness, a channel region becomes larger. In other words, the thicker the semiconductor 406b is, the larger the on-state current of the transistor 490 is. For example, the semiconductor 406b has a region with a thickness of greater than or equal to 20 nm, preferably greater than or equal to 40 nm, more preferably greater than or equal to 60 nm, still more preferably greater than or equal to 100 nm. Note that the semiconductor 406b has a region with a thickness of, for example, less than or equal to 300 nm, preferably less than or equal to 200 nm, or more preferably less than or equal to 150 nm because the productivity of the semiconductor device including the transistor 490 might be decreased.

[0121]

Moreover, the thickness of the semiconductor 406c is preferably as small as possible to increase the on-state current of the transistor 490. The semiconductor 406c has a region with a thickness of less than 10 nm, preferably less than or equal to 5 nm, more preferably less than or equal to 3 nm, for example. Meanwhile, the semiconductor 406c has a function of blocking elements other than oxygen (such as hydrogen and silicon) included in the adjacent insulator from entering the semiconductor 406b where a channel is formed. For this reason, it is preferable that the oxide semiconductor 406c have a certain thickness. The semiconductor 406c has a region with a thickness of greater than or equal to 0.3 nm, preferably greater than or equal to 1 nm, more preferably greater than or equal to 2 nm, for example. The semiconductor 406c preferably has an oxygen blocking property to suppress outward diffusion of oxygen released from the insulator 402 and the like.

[0122]

To improve reliability, preferably, the thickness of the semiconductor 406a is large and the thickness of the semiconductor 406c is small. For example, the semiconductor 406a has a region with a thickness of, for example, greater than or equal to 10 nm, preferably greater than or equal to 20 nm, more preferably greater than or equal to 40 nm, still more preferably greater than or equal to 60 nm. When the thickness of the semiconductor 406a is made large, a distance from an interface between the adjacent insulator and the semiconductor 406a to the semiconductor 406b in which a channel is formed can be large. However, the productivity of the semiconductor device including the transistor 490 might be decreased; therefore, the semiconductor 406a has a region with a thickness, for example, less than or equal to 200 nm, preferably less than or equal to 120 nm, or further preferably less than or equal to 80 nm.

[0123]

Silicon in the oxide semiconductor might serve as a carrier trap or a carrier generation source, for example. Therefore, the silicon concentration in the semiconductor 406b is preferably as low as possible. For example, a region in which the silicon concentration which is measured by secondary ion mass spectrometry (SIMS) is lower than 1×10^{19} atoms/cm^3, preferably lower than 5×10^{18} atoms/cm^3, or further preferably lower than 2×10^{18} atoms/cm^3 is provided between the semiconductor 406b and the semiconductor 406a. A region with a silicon concentration of lower than 1×10^{19} atoms/cm^3, preferably lower than 5×10^{18} atoms/cm^3, more preferably lower than 2×10^{18} atoms/cm^3 which is measured by SIMS is provided between the semiconductor 406b and the semiconductor 406c.

[0124]

The semiconductor 406b has a region in which the hydrogen concentration measured by SIMS is greater than or equal to 1×10^{16} atoms/cm^3 and less than or equal to 2×10^{20} atoms/cm^3, preferably greater than or equal to 1×10^{16} atoms/cm^3 and less than or equal to 5×10^{19} atoms/cm^3, more preferably greater than or equal to 1×10^{16} atoms/cm^3 and less than or equal to 1×10^{19} atoms/cm^3, or still more preferably greater than or equal to 1×10^{16} atoms/cm^3 and less than or equal to 5×10^{18} atoms/cm^3. It is preferable to reduce the hydrogen concentration in the semiconductor 406a and the semiconductor 406c in order to reduce the hydrogen concentration in the semiconductor 406b. The semiconductor 406a and the semiconductor 406c each have a region in which the hydrogen concentration measured by SIMS is lower than or equal to 2×10^{20} atoms/cm^3, preferably lower than or equal to 5×10^{19} atoms/cm^3, more preferably lower than or equal to 1×10^{19} atoms/cm^3, still more preferably lower than or equal to 5×10^{18} atoms/cm^3. The semiconductor 406b has a region in which the nitrogen concentration measured by SIMS is greater than or equal to 1×10^{15} atoms/cm^3 and less than or equal to 5×10^{19} atoms/cm^3,

preferably greater than or equal to 1×10^{15} atoms/cm^3 and less than or equal to 5×10^{18} atoms/cm^3, more preferably greater than or equal to 1×10^{15} atoms/cm^3 and less than or equal to 1×10^{18} atoms/cm^3, or still more preferably greater than or equal to 1×10^{15} atoms/cm^3 and less than or equal to 5×10^{17} atoms/cm^3. It is preferable to reduce the nitrogen concentration in the semiconductor 406a and the semiconductor 406c in order to reduce the nitrogen concentration in the semiconductor 406b. The semiconductor 406a and the semiconductor 406c each have a region in which the nitrogen concentration measured by SIMS is lower than 5×10^{19} atoms/cm^3, preferably lower than or equal to 5×10^{18} atoms/cm^3, more preferably lower than or equal to 1×10^{18} atoms/cm^3, still more preferably lower than or equal to 5×10^{17} atoms/cm^3.

[0125]

Note that when copper enters the oxide semiconductor, an electron trap might be generated. The electron trap might shift the threshold voltage of the transistor in the positive direction. Therefore, the copper concentration on the surface of or in the semiconductor 406b is preferably as low as possible. For example, the semiconductor 406b preferably has a region in which the copper concentration is lower than or equal to 1×10^{19} atoms/cm^3, lower than or equal to 5×10^{18} atoms/cm^3, or lower than or equal to 1×10^{18} atoms/cm^3.

[0126]

The above three-layer structure is an example. For example, a two-layer structure without the semiconductor 406a or the semiconductor 406c may be employed. A four-layer structure in which any one of the semiconductors described as examples of the semiconductor 406a, the semiconductor 406b, and the semiconductor 406c is provided below or over the semiconductor 406a or below or over the semiconductor 406c may be employed. An *n*-layer structure (*n* is an integer of 5 or more) in which any one of the semiconductors described as examples of the semiconductor 406a, the semiconductor 406b, and the semiconductor 406c is provided at two or more of the following positions: over the semiconductor 406a, below the semiconductor 406a, over the semiconductor 406c, and below the semiconductor 406c.

[0127]

As the substrate 400, an insulator substrate, a semiconductor substrate, or a conductor substrate may be used, for example. As the insulator substrate, a glass substrate, a quartz substrate, a sapphire substrate, a stabilized zirconia substrate (e.g., an yttria-stabilized zirconia substrate), or a resin substrate is used, for example. As the semiconductor substrate, a single material semiconductor substrate of silicon, germanium, or the like or a compound semiconductor substrate of silicon carbide, silicon germanium, gallium arsenide, indium phosphide, zinc oxide, gallium oxide, or the like is used, for example. A semiconductor

substrate in which an insulator region is provided in the above semiconductor substrate, e.g., a silicon on insulator (SOI) substrate or the like is used. As the conductor substrate, a graphite substrate, a metal substrate, an alloy substrate, a conductive resin substrate, or the like is used. A substrate including a metal nitride, a substrate including a metal oxide, or the like is used. An insulator substrate provided with a conductor or a semiconductor, a semiconductor substrate provided with a conductor or an insulator, a conductor substrate provided with a semiconductor or an insulator, or the like is used. Alternatively, any of these substrates over which an element is provided may be used. As the element provided over the substrate, a capacitor, a resistor, a switching element, a light-emitting element, a memory element, or the like is used.

[0128]

Alternatively, a flexible substrate may be used as the substrate 400. As a method for providing the transistor over a flexible substrate, there is a method in which the transistor is formed over a non-flexible substrate and then the transistor is separated and transferred to the substrate 400 which is a flexible substrate. In that case, a separation layer is preferably provided between the non-flexible substrate and the transistor. As the substrate 400, a sheet, a film, or a foil containing a fiber may be used. The substrate 400 may have elasticity. The substrate 400 may have a property of returning to its original shape when bending or pulling is stopped. Alternatively, the substrate 400 may have a property of not returning to its original shape. The substrate 400 has a region with a thickness of, for example, greater than or equal to 5 μm and less than or equal to 700 μm, preferably greater than or equal to 10 μm and less than or equal to 500 μm, more preferably greater than or equal to 15 μm and less than or equal to 300 μm. When the substrate 400 has a small thickness, the weight of the semiconductor device including the transistor 490 can be reduced. When the substrate 400 has a small thickness, even in the case of using glass or the like, the substrate 400 may have elasticity or a property of returning to its original shape when bending or pulling is stopped. Therefore, an impact applied to the semiconductor device over the substrate 400, which is caused by dropping or the like, can be reduced. That is, a durable semiconductor device can be provided.

[0129]

For the substrate 400 which is a flexible substrate, metal, an alloy, resin, glass, or fiber thereof can be used, for example. The flexible substrate 400 preferably has a lower coefficient of linear expansion because deformation due to an environment is suppressed. The flexible substrate 400 is formed using, for example, a material whose coefficient of linear expansion is lower than or equal to 1×10^{-3}/K, lower than or equal to 5×10^{-5}/K, or lower than or equal to 1×10^{-5}/K. Examples of the resin include polyester, polyolefin, polyamide (e.g., nylon or aramid),

polyimide, polycarbonate, and acrylic. In particular, aramid is preferably used for the flexible substrate 400 because of its low coefficient of linear expansion.

[0130]

Note that the transistor 490 may have a cross-sectional structure shown in FIG. 4A or 4B. The structure in FIG. 4A is different from that in FIG. 1B in that a conductor 413 is provided under the insulator 402. The structure in FIG. 4B is different from that in FIG. 4A in that the conductor 413 is electrically connected to the conductor 404.

[0131]

The conductor 413 serves as a second gate electrode (also referred to as a back gate electrode) of the transistor 490. For example, by applying a lower voltage or a higher voltage than a source electrode to the conductor 413, the threshold voltage of the transistor 490 may be shifted in the positive direction or the negative direction. For example, by shifting the threshold voltage of the transistor 490 in the positive direction, a normally-off transistor in which the transistor 490 is in a non-conduction state (off state) even when the gate voltage is 0 V can be achieved in some cases. The voltage applied to the conductor 413 may be variable or fixed.

[0132]

The conductor 413 may have a single-layer structure or a stacked-layer structure using a conductor containing one or more kinds of boron, nitrogen, oxygen, fluorine, silicon, phosphorus, aluminum, titanium, chromium, manganese, cobalt, nickel, copper, zinc, gallium, yttrium, zirconium, molybdenum, ruthenium, silver, indium, tin, tantalum, and tungsten, for example. An alloy or a compound may be used, for example, and a conductor containing aluminum, a conductor containing copper and titanium, a conductor containing copper and manganese, a conductor containing indium, tin, and oxygen, a conductor containing titanium and nitrogen, or the like may be used.

[0133]

<Manufacturing Method of Transistor Structure 1>

A method for manufacturing the transistor 490 illustrated in FIGS. 1A and 1B is described below.

[0134]

First, the substrate 400 is prepared.

[0135]

Next, the insulator 401 is formed. The insulator 401 may be formed by a sputtering method, a chemical vapor deposition (CVD) method, a molecular beam epitaxy (MBE) method, a pulsed laser deposition (PLD) method, an atomic layer deposition (ALD) method, or the like.

[0136]

CVD methods can be classified into a plasma enhanced CVD (PECVD) method using plasma, a thermal CVD (TCVD) method using heat, a photo CVD method using light, and the like. Moreover, the CVD methods can be classified into a metal CVD (MCVD) method and a metal organic CVD (MOCVD) method depending on a source gas.

[0137]

By using a PECVD method, a high-quality film can be obtained at a relatively low temperature. Furthermore, a thermal CVD method does not use plasma and thus causes less plasma damage to an object. For example, a wiring, an electrode, an element (e.g., transistor or capacitor), or the like included in a semiconductor device might be charged up by receiving charges from plasma. In that case, accumulated charges might break the wiring, electrode, element, or the like included in the semiconductor device. By contrast, when a thermal CVD method not using plasma is employed, such plasma damage is small and the yield of the semiconductor device can be increased. A thermal CVD method causes small plasma damage during film formation, so that a film with few defects can be obtained.

[0138]

An ALD method also causes less plasma damage to an object. An ALD method causes small plasma damage during film formation, so that a film with few defects can be obtained.

[0139]

Different from a film formation method whereby particles released from a target are deposited, a CVD method and an ALD method are film formation methods whereby a film is formed by a reaction at a surface of an object of the treatment. Therefore, they are film formation methods whereby a film with favorable coverage is formed without being greatly affected by the shape of the object. In particular, a film formed by an ALD method has favorable coverage and excellent uniformity in thickness. Therefore, an ALD method is preferred for forming a film covering a surface of an opening with a high aspect ratio. However, film formation speed of an ALD method is relatively slow, and thus it may be preferable to use an ALD method in combination with another film formation method with high film formation speed such as a CVD method in some cases.

[0140]

In the case of a CVD method or an ALD method, the composition of a film to be obtained can be controlled by adjusting the flow ratio of a source gas. For example, by a CVD method or an ALD method, a film with a desired composition can be formed by adjusting the flow ratio of a source gas. Moreover, with a CVD method or an ALD method, by changing the flow ratio of the source gases while forming the film, a film whose composition is continuously changed can be formed. In the case where the film is formed while changing the flow ratio of

the source gases, as compared with the case where the film is formed using a plurality of film formation chambers, time taken for the film formation can be reduced because time taken for transfer and pressure adjustment is omitted. Thus, semiconductor devices can be manufactured with improved productivity.

[0141]

Next, the insulator 402 is formed (FIG. 5A). The insulator 402 can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like.

[0142]

Next, treatment to add oxygen to the insulator 402 may be performed. An ion implantation method, a plasma treatment method, or the like can be used for the treatment to add oxygen. Note that oxygen added to the insulator 402 is excess oxygen.

[0143]

Next, a semiconductor to be the semiconductor 406a is formed. The semiconductor can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like.

[0144]

Next, a semiconductor to be the semiconductor 406b is formed. The semiconductor can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like.

[0145]

Next, treatment to add oxygen to the semiconductor to be the semiconductor 406a and/or to the semiconductor to be the semiconductor 406b may be performed. An ion implantation method, a plasma treatment method, or the like can be used for the treatment to add oxygen. Note that oxygen added to the semiconductor to be the semiconductor 406a and/or the semiconductor to be the semiconductor 406b becomes excess oxygen. Oxygen is preferably added to a layer corresponding to the semiconductor to be the semiconductor 406a.

[0146]

Next, first heat treatment is preferably performed. The first heat treatment can be performed at a temperature higher than or equal to 250 °C and lower than or equal to 650 °C, preferably higher than or equal to 450 °C and lower than or equal to 600 °C, further preferably higher than or equal to 520 °C and lower than or equal to 570 °C. The first heat treatment is performed in an inert gas atmosphere or an atmosphere containing an oxidizing gas at 10 ppm or more, 1% or more, or 10% or more. The first heat treatment may be performed under a reduced pressure. Alternatively, the first heat treatment may be performed in such a manner that heat

treatment is performed in an inert gas atmosphere, and then another heat treatment is performed in an atmosphere containing an oxidizing gas at 10 ppm or more, 1% or more, or 10% or more in order to compensate desorbed oxygen. By the first heat treatment, crystallinity of the semiconductor can be increased and impurities such as hydrogen and moisture can be removed, for example.

[0147]

Next, the semiconductors are processed by a photolithography method or the like, so that the semiconductor 406 including the semiconductors 406a and 406b is formed (FIG. 5B). Note that when the semiconductor 406 is formed, part of the insulator 402 may be etched and thinned in some cases. That is, the insulator 402 may have a protruding portion in a region in contact with the semiconductor 406.

[0148]

Next, a conductor to be the conductor 416a and the conductor 416b is formed. The conductor can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like.

[0149]

Next, the conductor is processed by a photolithography method or the like, so that a conductor 416 is formed (FIG. 6A). Note that the conductor 416 covers the semiconductor 406.

[0150]

In a photolithography method, first, a resist is exposed to light through a photomask. Next, a region exposed to light is removed or left using a developing solution, so that a resist mask is formed. Then, etching through the resist mask is conducted. As a result, a conductor, a semiconductor, an insulator, or the like can be processed into a desired shape. The resist mask is formed by, for example, exposure of the resist to light using KrF excimer laser light, ArF excimer laser light, extreme ultraviolet (EUV) light, or the like. Alternatively, a liquid immersion technique may be employed in which a portion between a substrate and a projection lens is filled with liquid (e.g., water) to perform light exposure. An electron beam or an ion beam may be used instead of the above-mentioned light. Note that a photomask is not necessary in the case of using an electron beam or an ion beam. Note that dry etching treatment such as ashing and/or wet etching treatment can be used for removal of the resist mask.

[0151]

Next, an insulator 438 is formed (FIG. 6B). The insulator 438 can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. Alternatively, the insulator 438 can be formed by a spin coating method, a dipping method, a droplet discharging method (such as an ink-jet method), a printing method (such as screen

printing or offset printing), a doctor knife method, a roll coater method, a curtain coater method, or the like.

[0152]

The insulator 438 is formed to have a flat top surface. For example, the top surface of the insulator 438 may have planarity immediately after the film formation. Alternatively, after the film formation, an upper portion of the insulator 438 may be removed so that the top surface of the insulator 438 becomes parallel to a reference surface such as a rear surface of the substrate. Such treatment is referred to as planarization treatment. As the planarization treatment, for example, chemical mechanical polishing (CMP) treatment, dry etching treatment, or the like can be performed. However, the top surface of the insulator 438 is not necessarily flat.

[0153]

Next, the insulator 438 is processed by a photolithography method or the like, so that an insulator 439 with an opening reaching a portion to be the conductor 416a and an opening reaching a portion to be the conductor 416b is formed.

[0154]

Next, a conductor is formed. The conductor can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. The conductor is formed so as to fill the openings in the insulator 439. Therefore, a CVD method (an MCVD method, in particular) is preferred. A stacked-layer film of a conductor formed by an ALD method or the like and a conductor formed by a CVD method is preferred in some cases to increase adhesion of the conductor formed by a CVD method. For example, a stacked-layer film where titanium nitride and tungsten are formed in this order may be used.

[0155]

Next, planarizing parallel to the reference surface such as the rear surface of the substrate, the treatment for removing an upper portion of the conductor is performed until only the conductors in the openings in the insulator 439 are left. As a result, only top surfaces of the conductors in the openings in the insulator 439 are exposed. At this time, the conductors in the openings in the insulator 439 are referred to as the conductors 424a and 424b (FIG. 7A).

[0156]

Next, the insulator 439 is processed by a photolithography method or the like, so that the insulator 410 is formed.

[0157]

Next, the conductor 416 is processed by a photolithography method or the like, so that the conductors 416a and 416b are formed (FIG. 7B). Note that the insulator 439 and the conductor 416 may be processed in the same photolithography process. Processing in the same

photolithography process can reduce the number of manufacturing steps. Thus, productivity of a semiconductor device including the transistor 490 can be increased. Alternatively, the insulator 439 and the conductor 416 may be processed in different photolithography processes. Processing in different photolithography processes may facilitate formation of films with different shapes.

[0158]

Here, the semiconductor 406 is exposed.

[0159]

Next, a semiconductor 436 to be the semiconductor 406c is formed. The semiconductor 436 can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like.

[0160]

Next, treatment to add oxygen to the semiconductor 406 is performed. As the treatment to add oxygen, ions 430 including oxygen are added by an ion implantation method, for example. The ions 430 are implanted at an angle (incident angle) within a range of 0° to 20°, preferably 0° to 10°, or still preferably 0° to 5° with respect to a normal vector of the top or bottom surface of the substrate 400. When the incident angle of the ions 430 is within the above-described range, oxygen can be efficiently added to the semiconductor 406. Note that oxygen added to the semiconductor 406 becomes excess oxygen. Then, the region 434 most including oxygen in the depth direction of the semiconductor 406 is formed (FIG. 8A). Oxygen is added to the semiconductor 406 at a concentration of greater than or equal to 1×10^{15} ions/cm^2 and less than or equal to 2×10^{17} ions/cm^2, for example.

[0161]

Alternatively, oxygen may be added by plasma treatment. Here, an ashing apparatus which adds oxygen to the semiconductor 406 through the semiconductor 436 will be described. In addition, an example of a concept of oxygen plasma in the ashing apparatus will be described.

[0162]

FIG. 23A is a perspective diagram illustrating an ashing apparatus capable of performing oxygen addition treatment. FIG. 23B is a conceptual diagram illustrating the state of oxygen plasma in the ashing apparatus.

[0163]

As shown in FIG. 23A, inductively-coupled plasma (ICP) can be used in an ashing apparatus 200, for example.

[0164]

The ashing apparatus 200 includes an upper electrode 201 provided above a reaction space, a high-frequency power source 205 electrically connected to the upper electrode 201 with a matching box 203 provided therebetween, a dielectric 207 provided between the upper electrode 201 and the reaction space, a lower electrode 202 provided below the reaction space, a high-frequency power source 206 electrically connected to the lower electrode 202 with a matching box 204 provided therebetween, and a substrate stage 208 provided between the lower electrode 202 and the reaction space. Note that a substrate 400 to be treated is provided over the substrate stage 208 of the ashing apparatus 200. In addition, the upper electrode 201 is provided with an antenna coil 209.

[0165]

As the high-frequency power source 205, a high-frequency power source of 1 MHz or more and 50 MHz or less, typically 13.56 MHz, can be used, for example. As the high-frequency power source 206, a high-frequency power source of 100 kHz or more and 60 MHz or less, typically 3.2 MHz, can be used, for example. As the dielectric 207, quartz, ceramic, or the like can be used.

[0166]

As illustrated in FIGS. 23A and 23B, when high-frequency power is applied to the upper electrode 201, a high-frequency current flows in a direction θ of the antenna coil 209 provided over the upper electrode 201, so that a magnetic field is produced in a direction Z. Then, an induction field is produced in the direction θ in accordance with the Faraday's law of electromagnetic induction. Electrons e are trapped in the induction field and accelerated in the direction θ, and collide with molecules of the gas (e.g., oxygen molecules), so that high-density plasma 210 is produced in the reaction space through the dielectric 207. An influence of the magnetic field is small in a region apart from the upper electrode 201; therefore, the high-density plasma 210 is expanded flatly near the dielectric 207 on the upper electrode 201. Here, by adjusting the high-frequency power applied to the lower electrode 202, a region where the high-density plasma 210 is produced can be closer to a region on the substrate 400 side. As illustrated in FIGS. 23A and 23B, the upper electrode 201 and the lower electrode 202 each individually have a high-frequency power source, whereby the bias voltage applied to each electrode can be controlled separately.

[0167]

Furthermore, as illustrated in FIG. 23B, for example, oxygen molecules (O_2) and/or oxygen radicals (O^*) can be efficiently added to the substrate 400 by controlling the bias voltage applied to the substrate 400, specifically increasing high-frequency power applied to the lower electrode 202. Note that at this time, when the outermost surface of the substrate 400 has an

insulating property, the oxygen cannot be added efficiently in some cases. However, in one embodiment of the present invention, the outermost surface of the substrate 400 is the semiconductor 436; therefore, the oxygen can be efficiently added to the semiconductor 406 positioned below the semiconductor 436. The temperature of the substrate 400 during the oxygen addition treatment is higher than or equal to room temperature (for example, 25 °C) and lower than or equal to 300 °C, preferably higher than or equal to 100 °C and lower than or equal to 250 °C, whereby the oxygen can be added efficiently to the substrate 400. Note that a heater may be provided in the substrate stage 208 to raise the temperature of the substrate 400. As a structure of the heater, heating performed using a resistance heater, or heat conduction or heat radiation from a medium such as a heated gas (e.g., a He gas), may be used.

[0168]

Note that although the ashing apparatus using ICP is described as an example in FIGS. 23A and 23B, the present invention is not limited thereto, and a plasma etching apparatus using capacitively coupled plasma (CCP) may be used, for example. Alternatively, plasma etching apparatus using reactive ion etching (RIE) instead of ICP may be used.

[0169]

When the semiconductor 436 is provided over the semiconductor 406 and oxygen addition is performed, the semiconductor 436 may serve as a protection film suppressing desorption of oxygen from the semiconductor 406. Thus, a larger amount of oxygen can be added to the semiconductor 406. By addition of oxygen, oxygen vacancies of the semiconductor 406 may be reduced and the resistance of the semiconductor 406 may be increased.

[0170]

In the case where oxygen is introduced by plasma treatment, by making oxygen excited by a microwave to generate high-density oxygen plasma, the amount of oxygen added to the semiconductor 406 can be increased in some cases.

[0171]

After addition of oxygen into the semiconductor 406 by the above-described method or the like, second heat treatment is preferably performed. The second heat treatment can be performed at a temperature higher than or equal to 250 °C and lower than or equal to 650 °C, preferably higher than or equal to 400 °C and lower than or equal to 650 °C, further preferably higher than or equal to 520 °C and lower than or equal to 570 °C. The second heat treatment is performed in an inert gas atmosphere or an atmosphere containing an oxidizing gas at 10 ppm or more, 1% or more, or 10% or more. The second heat treatment may be performed under a reduced pressure. Alternatively, the second heat treatment may be performed in such a manner

that heat treatment is performed in an inert gas atmosphere, and then another heat treatment is performed in an atmosphere containing an oxidizing gas at 10 ppm or more, 1% or more, or 10% or more in order to compensate desorbed oxygen.

[0172]

By the second heat treatment, oxygen vacancies in the semiconductor 406 can be reduced with excess oxygen. In addition, moisture generated by reaction between hydrogen in the semiconductor 406 and excess oxygen can diffuse outward. Thus, in the semiconductor 406 including excess oxygen, the hydrogen concentration can be effectively reduced by the second heat treatment. In this way, oxygen vacancies and/or hydrogen in the semiconductor 406 can be reduced. Thus, since oxygen vacancies in the channel formation region are reduced, the transistor 490 has a small off-state current.

[0173]

For the second heat treatment, a heating mechanism which performs heating with a resistance heater or the like may be used, for example. Alternatively, heat conduction or heat radiation from a medium such as a heated gas may be used as the heating mechanism. For example, rapid thermal annealing (RTA) such as gas rapid thermal annealing (GRTA) or lamp rapid thermal annealing (LRTA) can be used. The LRTA is a method for heating an object by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high-pressure sodium lamp, or a high-pressure mercury lamp. In the GRTA, heat treatment is performed using a high-temperature gas. An inert gas is used as a gas.

[0174]

The region 434 is formed also in the insulator 410 and the like. Because of the presence of the insulator 410, oxygen is not added to the conductors 416a and 416b. In other words, the amount of oxygen added to the conductors 416a and 416b can be extremely small. Thus, increase in resistance of the conductors 416a and 416b due to addition of oxygen is not easily caused. That is, the transistor 490 formed through such steps has a large on-state current.

[0175]

Next, an insulator to be the insulator 412 is formed. The insulator can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. The insulator is preferably formed to have the uniform thickness along bottom and side surfaces of an opening formed by the insulator 410 and the conductors 416a and 416b. Therefore, an ALD method is preferably used.

[0176]

Next, a conductor to be the conductor 404 is formed. The conductor can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. The conductor is formed so as to fill the opening formed by the insulator 410 and others. Therefore, a CVD method (an MCVD method, in particular) is preferred. A stacked-layer film of a conductor formed by an ALD method or the like and a conductor formed by a CVD method is preferred in some cases to increase adhesion of the conductor formed by a CVD method. For example, a stacked-layer film where titanium nitride and tungsten are formed in this order may be used.

[0177]

Next, the conductor is processed by a photolithography method or the like, so that the conductor 404 is formed.

[0178]

Next, the insulator to be the insulator 412 is processed by a photolithography method or the like, so that the insulator 412 is formed. Note that the conductor and the insulator may be processed in the same photolithography step. Processing in the same photolithography process can reduce the number of manufacturing steps. Thus, productivity of a semiconductor device including the transistor 490 can be increased. Alternatively, the conductor to be the conductor 404 and the insulator to be the insulator 412 may be processed in different photolithography processes. Processing in different photolithography processes may facilitate formation of films with different shapes. Though an example where the insulator is processed into the insulator 412 is shown here, the transistor of one embodiment of the present invention is not limited thereto. For example, the insulator without being processed may be used as the insulator 412 in some cases.

[0179]

Next, the semiconductor 436 to be the semiconductor 406c is processed by a photolithography method or the like, so that the semiconductor 406c is formed. Note that the conductor and the insulator may be processed in the same photolithography step. Processing in the same photolithography process can reduce the number of manufacturing steps. Thus, productivity of a semiconductor device including the transistor 490 can be increased. Alternatively, the conductor to be the conductor 404, the insulator to be the insulator 412, and the semiconductor 436 may be processed in different photolithography processes. Processing in different photolithography processes may facilitate formation of films with different shapes. Though an example where the semiconductor 436 is processed into the semiconductor 406c is shown here, the transistor of one embodiment of the present invention is not limited thereto.

For example, the semiconductor 436 may be used without being processed into the semiconductor 406c.

[0180]

Next, an insulator to be the insulator 408 is formed. The insulator to be the insulator 408 can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like.

[0181]

Third heat treatment may be performed at any time after the formation of the insulator to be the insulator 408. By the third heat treatment, defects (oxygen vacancies) in the semiconductor 406 can be reduced with excess oxygen included in the insulator 402, the semiconductor 406, and/or the like. Note that the third heat treatment may be performed at a temperature such that excess oxygen (oxygen) in the insulator 402 is diffused to the semiconductor 406, for example. The description of the first or second heat treatment may be referred to, for example. The third heat treatment is preferably performed at a temperature lower than that of the first or second heat treatment. The temperature difference between the third heat treatment and the first or second heat treatment is higher than or equal to 20 °C and lower than or equal to 150 °C, or preferably higher than or equal to 40 °C and lower than or equal to 100 °C. Such a temperature will suppress release of excess oxygen (oxygen) from the insulator 402 and/or the semiconductor 406 too much. Note that in the case where heating at the time of formation of the layers doubles as the third heat treatment, the third heat treatment is not necessarily performed.

[0182]

Next, an insulator to be the insulator 418 is formed. The insulator to be the insulator 418 can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like.

[0183]

Next, the insulator to be the insulator 418 is processed by a photolithography method or the like, so that the insulator 418 is formed.

[0184]

Next, the insulator to be the insulator 408 is processed by a photolithography method or the like, so that the insulator 408 is formed. Note that the insulators to be the insulators 418 and 408 may be processed in the same photolithography process. Processing in the same photolithography process can reduce the number of manufacturing steps. Thus, productivity of a semiconductor device including the transistor 490 can be increased. Alternatively, the insulator to be the insulator 418 and the insulator to be the insulator 408 may be processed in

different photolithography processes. Processing in different photolithography processes may facilitate formation of films with different shapes.

[0185]

At this time, the conductors 424a and 424b are exposed.

[0186]

Next, a conductor to be the conductor 426a and the conductor 426b is formed. The conductor can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like.

[0187]

Next, the conductor is processed by a photolithography method or the like, so that the conductors 426a and 426b are formed (FIG. 8B).

[0188]

Through the above steps, the transistor 490 illustrated in FIGS. 1A and 1B can be manufactured.

[0189]

In the transistor 490, the size or the like of the offset region or the overlap region can be controlled by the thicknesses, shapes, or the like of the films. Therefore, the size or the like of the offset region or the overlap region can be smaller than a minimum feature size formed by a photolithography method; thus, the transistor can be easily miniaturized. In addition, since the parasitic capacitance is small, the transistor can have high frequency characteristics. Moreover, since there are a few oxygen vacancies in the channel formation region, the transistor can have normally-off electric characteristics. In addition, the transistor can have a small off-state current. Furthermore, since the source electrode and the drain electrode are not easily oxidized, the transistor can have a large on-state current.

[0190]

<Transistor Structure 2>

A transistor 590, which has a different structure from the transistor 490 in FIGS. 1A and 1B and the like, is described below. FIGS. 9A and 9B are a top view and a cross-sectional view of the transistor 590 of one embodiment of the present invention. FIG. 9A is a top view. FIG. 9B is a cross-sectional view taken along dashed-dotted line B1-B2 and dashed-dotted line B3-B4 in FIG. 9A. Note that for simplification of the drawing, some components are not illustrated in the top view in FIG. 9A.

[0191]

In FIG. 9B, the transistor 590 includes an insulator 501 over a substrate 500; an insulator 502 over the insulator 501; a semiconductor 506 over the insulator 502; conductors

516a and 516b each include a region in contact with a top surface of the semiconductor 506; an insulator 510 that is in contact with top surfaces of the conductors 516a and 516b; an insulator 512 in contact with the top surface of the semiconductor 506; a conductor 504 over the semiconductor 506 with the insulator 512 provided therebetween; and an insulator 508 over the insulator 510 and the conductor 504.

[0192]

Note that the transistor 590 does not necessarily include the insulator 501 in some cases. Note that the transistor 590 does not necessarily include the insulator 502 in some cases. Note that the transistor 590 does not necessarily include the insulator 508 in some cases.

[0193]

In FIG. 9B, an insulator 518 is over the insulator 508 of the transistor 590. The insulators 518, 508, and 510 have an opening reaching the conductor 516a and an opening reaching the conductor 516b. Additionally formed are a conductor 524a and a conductor 524b in contact with the conductor 516a and the conductor 516b, respectively, through the openings in the insulators 518, 508, and 510; a conductor 526a in contact with the conductor 524a; and a conductor 526b in contact with the conductor 524b.

[0194]

In the transistor 590, the conductor 504 serves as a gate electrode. The insulator 512 serves as a gate insulator. The conductor 516a and the conductor 516b serve as a source electrode and a drain electrode. Therefore, resistance of the semiconductor 506 can be controlled by a potential applied to the conductor 504. That is, conduction or non-conduction between the conductors 516a and 516b can be controlled by the potential applied to the conductor 504.

[0195]

In the transistor 590, the conductor 504 includes a region overlapping with the conductor 516a with the insulator 510 provided therebetween, and a region overlapping with the conductor 516b with the insulator 510 provided therebetween. The transistor 590 includes the insulator 510 between the conductor 504 and the conductor 516a, and between the conductor 504 and the conductor 516b, whereby parasitic capacitance can be reduced. Thus, the transistor 590 has high frequency characteristics.

[0196]

In the transistor 590, a region 534 with excess oxygen is included in the semiconductor 506, the insulator 510, and the like. Note that a portion shown by a dashed line as the region 534 in FIG. 9B indicates a portion with the highest concentration of excess oxygen in the thickness direction. In addition to the region 534, a region with the high concentration of

excess oxygen is present near the region 534. There may be a concentration gradient where the concentration of excess oxygen gets higher toward the region 534, for example. It is preferred that the region 534 be present in a channel formation region of the transistor 590 while hardly present in a source region or a drain region. Note that there may be the region with the highest concentration of excess oxygen at or in the vicinity of an interface between the semiconductor 506 and the insulator 512.

[0197]

Because the region 534 and the vicinity thereof contain excess oxygen, oxygen vacancies and/or hydrogen are/is reduced in the channel formation region. That is, carrier generation or the like caused by oxygen vacancies and/or hydrogen is not likely to occur in the channel formation region. Therefore, a shift of the threshold voltage of the transistor 590 in the negative direction, which occurs when a carrier density is high, can be suppressed. Meanwhile, because the influence of the region 534 is small and oxygen vacancies are not reduced in the source and drain regions, the source and drain regions can have lower resistance than the channel formation region. Therefore, the transistor 590 can have a high on-state current and a low off-state current.

[0198]

As shown in FIG. 9B, the semiconductor 506 is electrically surrounded by an electric field of the conductor 504. That is, the transistor 590 has an s-channel structure. Therefore, the on-state current of the transistor can be increased. In addition, the off-state current of the transistor can be reduced. Furthermore, because the conductors 516a and 516b are not in contact with side surfaces of the semiconductor 506, the effect caused by surrounding the semiconductor 506 with the electric field of the conductor 504 is strengthened. Thus, the transistor 590 can gain more benefits of the s-channel structure than the transistor 490.

[0199]

Note that electrical characteristics of the transistor 590 can be stabilized when the transistor 590 is surrounded by an insulator with a function of blocking oxygen and impurities such as hydrogen. For example, an insulator with a function of blocking oxygen and impurities such as hydrogen may be used as the insulator 501 and the insulator 508.

[0200]

For the substrate 500, the description of the substrate 400 is referred to. For the insulator 501, the description of the insulator 401 is referred to. For the insulator 502, the description of the insulator 402 is referred to. For the semiconductor 506, the description of the semiconductor 406 is referred to. For the conductor 516a, the description of the conductor 416a is referred to. For the conductor 516b, the description of the conductor 416b is referred to.

For the insulator 512, the description of the insulator 412 is referred to. For the conductor 504, the description of the conductor 404 is referred to. For the insulator 508, the description of the insulator 408 is referred to. For the insulator 518, the description of the insulator 418 is referred to. For the conductor 524a, the description of the conductor 424a is referred to. For the conductor 524b, the description of the conductor 424b is referred to. For the conductor 526a, the description of the conductor 426a is referred to. For the conductor 526b, the description of the conductor 426b is referred to. Note that, although not illustrated, a semiconductor corresponding to the semiconductor 406c of the transistor 490 may be provided under the insulator 512.

[0201]

Note that the transistor 590 may have a cross-sectional structure shown in FIG. 10A or 10B. The structure in FIG. 10A is different from that in FIG. 9B in that a conductor 513 is provided under the insulator 502. The structure in FIG. 10B is different from that in FIG. 10A in that the conductor 513 is electrically connected to the conductor 504.

[0202]

The conductor 513 serves as a second gate electrode (also referred to as a back gate electrode) of the transistor 590. For example, by applying a lower voltage or a higher voltage than a source electrode to the conductor 513, the threshold voltage of the transistor 590 may be shifted in the positive direction or the negative direction. For example, by shifting the threshold voltage of the transistor 590 in the positive direction, a normally-off transistor in which the transistor 590 is in a non-conduction state (off state) even when the gate voltage is 0 V can be achieved in some cases. The voltage applied to the conductor 513 may be variable or fixed.

[0203]

For the conductor 513, the description of the conductor 413 is referred to.

[0204]

<Manufacturing Method of Transistor Structure 2>

A method for manufacturing the transistor 590 illustrated in FIGS. 9A and 9B is described below.

[0205]

First, the substrate 500 is prepared.

[0206]

Next, the insulator 501 is formed. The insulator 501 can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like.

[0207]

Next, the insulator 502 is formed (FIG. 11A). The insulator 502 can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like.

[0208]

Next, treatment to add oxygen to the insulator 502 may be performed. An ion implantation method, a plasma treatment method, or the like can be used for the treatment to add oxygen. Note that oxygen added to the insulator 502 is excess oxygen.

[0209]

Next, a semiconductor to be the semiconductor 506 is formed. The semiconductor can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like.

[0210]

Next, treatment to add oxygen to the semiconductor may be performed. An ion implantation method, a plasma treatment method, or the like can be used for the treatment to add oxygen. Note that oxygen added to the semiconductor becomes excess oxygen. When the semiconductor is a stacked-layer film, oxygen is preferably added to a layer corresponding to the semiconductor to be the semiconductor 406a of the transistor 490.

[0211]

Next, first heat treatment is preferably performed. The first heat treatment can be performed at a temperature higher than or equal to 250 °C and lower than or equal to 650 °C, preferably higher than or equal to 450 °C and lower than or equal to 600 °C, further preferably higher than or equal to 520 °C and lower than or equal to 570 °C. The first heat treatment is performed in an inert gas atmosphere or an atmosphere containing an oxidizing gas at 10 ppm or more, 1% or more, or 10% or more. The first heat treatment may be performed under a reduced pressure. Alternatively, the first heat treatment may be performed in such a manner that heat treatment is performed in an inert gas atmosphere, and then another heat treatment is performed in an atmosphere containing an oxidizing gas at 10 ppm or more, 1% or more, or 10% or more in order to compensate desorbed oxygen. By the first heat treatment, crystallinity of the semiconductor can be increased and impurities such as hydrogen and moisture can be removed, for example.

[0212]

Next, a conductor to be the conductor 516a and the conductor 516b is formed. The conductor can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like.

[0213]

Next, the conductor is processed by a photolithography method or the like, so that a conductor 516 is formed.

[0214]

Next, the semiconductor is etched through the conductor 516, so that the semiconductor 506 is formed (FIG. 11B). Note that when the semiconductor 506 is formed, part of the insulator 502 may be etched and thinned in some cases. That is, the insulator 502 may have a protruding portion in a region in contact with the semiconductor 506.

[0215]

Next, an insulator 538 is formed (FIG. 12A). The insulator 538 can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. Alternatively, the insulator 538 can be formed by a spin coating method, a dipping method, a droplet discharging method (such as an ink-jet method), a printing method (such as screen printing or offset printing), a doctor knife method, a roll coater method, a curtain coater method, or the like.

[0216]

A top surface of the insulator 538 may have planarity.

[0217]

Next, the insulator 538 is processed by a photolithography method or the like, so that the insulator 539 is formed.

[0218]

Next, the conductor 516 is processed by a photolithography method or the like, so that the conductors 516a and 516b are formed. Note that the insulator 538 and the conductor 516 may be processed in the same photolithography process. Processing in the same photolithography process can reduce the number of manufacturing steps. Thus, productivity of a semiconductor device including the transistor 590 can be increased. Alternatively, the insulator 538 and the conductor 516 may be processed in different photolithography processes. Processing in different photolithography processes may facilitate formation of films with different shapes.

[0219]

Here, the semiconductor 506 is exposed.

[0220]

Next, a semiconductor corresponding to the semiconductor 436 may be formed and subjected to treatment to add oxygen. In that case, the description for the method for forming the transistor 490 is referred to.

[0221]

Here, treatment to add oxygen to the semiconductor 506 is performed next. As the treatment to add oxygen, ions 530 including oxygen are added by an ion implantation method, for example. For example, the ions 530 are implanted at an angle (incident angle) within a range of 0° to 20°, preferably 0° to 10°, or still preferably 0° to 5° with respect to a normal vector of the top or bottom surface of the substrate 500. When the incident angle of the ions 530 is within the above-described range, oxygen can be efficiently added to the semiconductor 506. Note that oxygen added to the semiconductor 506 becomes excess oxygen. Then, the region 534 most including oxygen in the depth direction of the semiconductor 506 is formed (FIG. 12B). Oxygen is added to the semiconductor 506 at a concentration of greater than or equal to 1×10^{15} ions/cm^2 and less than or equal to 2×10^{17} ions/cm^2, for example.

[0222]

Alternatively, oxygen may be added by plasma treatment. As to the plasma treatment, the description for the method for forming the transistor 490 is referred to.

[0223]

After addition of oxygen into the semiconductor 506 by the above-described method or the like, second heat treatment is preferably performed. The second heat treatment can be performed at a temperature higher than or equal to 250 °C and lower than or equal to 650 °C, preferably higher than or equal to 400 °C and lower than or equal to 650 °C, further preferably higher than or equal to 520 °C and lower than or equal to 570 °C. The second heat treatment is performed in an inert gas atmosphere or an atmosphere containing an oxidizing gas at 10 ppm or more, 1% or more, or 10% or more. The second heat treatment may be performed under a reduced pressure. Alternatively, the second heat treatment may be performed in such a manner that heat treatment is performed in an inert gas atmosphere, and then another heat treatment is performed in an atmosphere containing an oxidizing gas at 10 ppm or more, 1% or more, or 10% or more in order to compensate desorbed oxygen.

[0224]

By the second heat treatment, oxygen vacancies in the semiconductor 506 can be reduced with excess oxygen. In addition, moisture generated by reaction between hydrogen in the semiconductor 506 and excess oxygen can diffuse outward. Thus, in the semiconductor 506 including excess oxygen, the hydrogen concentration can be effectively reduced by the second heat treatment. In this way, oxygen vacancies and/or hydrogen in the semiconductor 506 can be reduced. Thus, since oxygen vacancies in the channel formation region are reduced, the transistor 590 has a small off-state current.

[0225]

For the second heat treatment, a heating mechanism which performs heating with a resistance heater or the like may be used, for example. Alternatively, heat conduction or heat radiation from a medium such as a heated gas may be used as the heating mechanism. For example, RTA such as GRTA or LRTA can be used.

[0226]

The region 534 is formed also in the insulator 539 and the like. Because of the presence of the insulator 539, oxygen is not added to the conductors 516a and 516b. In other words, the amount of oxygen added to the conductors 516a and 516b can be extremely small. Thus, increase in resistance of the conductors 516a and 516b due to addition of oxygen is not easily caused. That is, the transistor 590 formed through such steps has a large on-state current.

[0227]

Next, an insulator to be the insulator 512 is formed. The insulator can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. The insulator is preferably formed to have the uniform thickness along bottom and side surfaces of an opening formed by the insulator 539 and the conductors 516a and 516b. Therefore, an ALD method is preferably used.

[0228]

Next, a conductor to be the conductor 504 is formed. The conductor can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. The conductor is formed so as to fill the opening formed by the insulator 539 and others. Therefore, a CVD method (an MCVD method, in particular) is preferred. A stacked-layer film of a conductor formed by an ALD method or the like and a conductor formed by a CVD method is preferred in some cases to increase adhesion of the conductor formed by a CVD method. For example, a stacked-layer film where titanium nitride and tungsten are formed in this order may be used.

[0229]

Next, the conductor is processed by a photolithography method or the like, so that the conductor 504 is formed.

[0230]

Next, the insulator to be the insulator 512 is processed by a photolithography method or the like, so that the insulator 512 is formed (FIG. 13A). Note that the conductor to be the conductor 504 and the insulator to be the insulator 512 may be processed in the same photolithography process. Processing in the same photolithography process can reduce the number of manufacturing steps. Thus, productivity of a semiconductor device including the transistor 590 can be increased. Alternatively, the conductor and the insulator may be

processed in different photolithography processes. Processing in different photolithography processes may facilitate formation of films with different shapes. Though an example where the insulator is processed into the insulator 512 is shown here, the transistor of one embodiment of the present invention is not limited thereto. For example, the insulator without being processed may be used as the insulator 512 in some cases.

[0231]

Next, an insulator to be the insulator 508 is formed. The insulator to be the insulator 508 can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like.

[0232]

Third heat treatment may be performed at any time after the formation of the insulator to be the insulator 508. Excess oxygen included in the insulator 502 and the like moves into the semiconductor 506 by performing the third heat treatment, whereby defects (oxygen vacancies) in the semiconductor 506 can be reduced. Note that the third heat treatment may be performed at a temperature such that excess oxygen (oxygen) in the insulator 502 is diffused to the semiconductor 506. For example, the description of the first and/or second heat treatment may be referred to. The third heat treatment is preferably performed at a temperature lower than that of the first and/or second heat treatment. The temperature difference between the third heat treatment and the first and/or second heat treatment is higher than or equal to 20 °C and lower than or equal to 150 °C, or preferably higher than or equal to 40 °C and lower than or equal to 100 °C. Such a temperature will suppress release of excess oxygen (oxygen) from the insulator 502 too much. Note that in the case where heating at the time of formation of the layers doubles as the third heat treatment, the second heat treatment is not necessarily performed.

[0233]

Next, an insulator to be the insulator 518 is formed. The insulator to be the insulator 518 can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like.

[0234]

Next, the insulator to be the insulator 518 is processed by a photolithography method or the like, so that the insulator 518 is formed.

[0235]

Next, the insulator to be the insulator 508 is processed by a photolithography method or the like, so that the insulator 508 is formed. Note that the insulators to be the insulators 518 and 508 may be processed in the same photolithography process. Processing in the same photolithography process can reduce the number of manufacturing steps. Thus, productivity of

a semiconductor device including the transistor 590 can be increased. Alternatively, the insulator to be the insulator 518 and the insulator to be the insulator 508 may be processed in different photolithography processes. Processing in different photolithography processes may facilitate formation of films with different shapes.

[0236]

Next, the insulator 539 is processed by a photolithography method or the like, so that the insulator 510 is formed. Note that the insulator to be the insulator 518, the insulator to be the insulator 508, and the insulator 539 may be processed in the same photolithography process. Processing in the same photolithography process can reduce the number of manufacturing steps. Thus, productivity of a semiconductor device including the transistor 590 can be increased. Alternatively, the insulator to be the insulator 518, the insulator to be the insulator 508, and the insulator 539 may be processed in different photolithography processes. Processing in different photolithography processes may facilitate formation of films with different shapes.

[0237]

At this time, the conductors 516a and 516b are exposed.

[0238]

Next, a conductor to be the conductors 524a and 524b is formed. The conductor can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. The conductor is formed so as to fill the openings in the insulators 518, 508, and 510. Therefore, a CVD method (an MCVD method, in particular) is preferred. A stacked-layer film of a conductor formed by an ALD method or the like and a conductor formed by a CVD method is preferred in some cases to increase adhesion of the conductor formed by a CVD method. For example, a stacked-layer film where titanium nitride and tungsten are formed in this order may be used.

[0239]

Next, planarizing parallel to the reference surface such as the rear surface of the substrate, the treatment for removing an upper portion of the conductor is performed until only the conductors in the openings in the insulators 518, 508, and 510 are left. As a result, only top surfaces of the conductors in the openings in the insulators 518, 508, and 510 are exposed. At this time, the conductors in the openings in the insulators 518, 508 and 510 are referred to as the conductors 524a and 524b.

[0240]

Next, a conductor is formed. The conductor can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like.

[0241]

Next, the conductor is processed by a photolithography method or the like, so that the conductors 526a and 526b are formed (FIG. 13B).

[0242]

Through the above steps, the transistor 590 illustrated in FIGS. 9A and 9B can be manufactured.

[0243]

In the transistor 590, the size or the like of the offset region or the overlap region can be controlled by the thicknesses, shapes, or the like of the films. Therefore, the size or the like of the offset region or the overlap region can be smaller than a minimum feature size formed by a photolithography method; thus, the transistor can be easily miniaturized. In addition, since the parasitic capacitance is small, the transistor can have high frequency characteristics. Moreover, since there are a few oxygen vacancies in the channel formation region, the transistor can have normally-off electric characteristics. In addition, the transistor can have a small off-state current. Furthermore, since the source electrode and the drain electrode are not easily oxidized, the transistor can have a large on-state current.

[0244]

<Semiconductor Device>

An example of a semiconductor device of one embodiment of the present invention is shown below.

[0245]

<Circuit>

An example of a circuit including a transistor of one embodiment of the present invention is shown below.

[0246]

[CMOS inverter]

A circuit diagram in FIG. 14A shows a configuration of a so-called CMOS inverter in which a p-channel transistor 2200 and an n-channel transistor 2100 are connected to each other in series and in which gates of them are connected to each other.

[0247]

<Structure of Semiconductor Device>

FIG. 15 is a cross-sectional view of the semiconductor device of FIG. 14A. The semiconductor device shown in FIG. 15 includes the transistor 2200 and the transistor 2100 above the transistor 2200. Although an example where the transistor 490 shown in FIGS. 1A and 1B is used as the transistor 2100 is shown, a semiconductor device of one embodiment of the present invention is not limited thereto. For example, the transistor 490 shown in FIG. 4A or

4B, the transistor 590 shown in FIGS. 9A and 9B, the transistor 590 shown in FIG. 10A or 10B can be used as the transistor 2100. Therefore, the description regarding the above-mentioned transistors is referred to for the transistor 2100 as appropriate.

[0248]

The transistor 2200 shown in FIG. 15 is a transistor using a semiconductor substrate 450. The transistor 2200 includes a region 474a in the semiconductor substrate 450, a region 474b in the semiconductor substrate 450, a region 470 in the semiconductor substrate 450, an insulator 462, and a conductor 454. Note that the transistor 2200 does not necessarily include the region 470 in some cases.

[0249]

In the transistor 2200, the regions 474a and 474b have a function as a source region and a drain region. In addition, the region 470 has a function of controlling a threshold voltage. The insulator 462 has a function as a gate insulator. The conductor 454 has a function as a gate electrode. Therefore, resistance of a channel formation region can be controlled by a potential applied to the conductor 454. In other words, conduction or non-conduction between the region 474a and the region 474b can be controlled by the potential applied to the conductor 454.

[0250]

For the semiconductor substrate 450, a single-material semiconductor substrate of silicon, germanium, or the like or a compound semiconductor substrate of silicon carbide, silicon germanium, gallium arsenide, indium phosphide, zinc oxide, gallium oxide, or the like may be used, for example. A single crystal silicon substrate is preferably used as the semiconductor substrate 450.

[0251]

For the semiconductor substrate 450, a semiconductor substrate including impurities imparting n-type conductivity is used. However, a semiconductor substrate including impurities imparting p-type conductivity may be used as the semiconductor substrate 450. In that case, a well including impurities imparting the n-type conductivity is provided in a region where the transistor 2200 is formed. Alternatively, the semiconductor substrate 450 may be an i-type semiconductor substrate.

[0252]

A top surface of the semiconductor substrate 450 preferably has a (110) plane. Then, on-state characteristics of the transistor 2200 can be improved.

[0253]

The regions 474a and 474b are regions including impurities imparting the p-type conductivity. Accordingly, the transistor 2200 has a structure of a p-channel transistor.

[0254]

The region 470 is a region where the concentration of impurities imparting n-type conductivity is higher than that in the semiconductor substrate 450 or the well. With the region 470, the threshold voltage of the transistor 2200 can be shifted in the negative direction. Accordingly, normally-off electrical characteristics can be easily obtained even when a conductor with a high work function is used as the conductor 454. The conductor with the high work function has higher heat resistance than a conductor with a low work function in many cases, and thus may facilitate a degree of freedom of later steps and increase performance of the semiconductor device.

[0255]

Note that the transistor 2200 is separated from an adjacent transistor by a region 460 and the like. The region 460 is an insulating region.

[0256]

The semiconductor device shown in FIG. 15 includes an insulator 464, an insulator 466, an insulator 468, a conductor 480a, a conductor 480b, a conductor 480c, a conductor 478a, a conductor 478b, a conductor 478c, a conductor 476a, a conductor 476b, a conductor 416c, a conductor 424c, and a conductor 426c.

[0257]

The insulator 464 is over the transistor 2200. The insulator 466 is over the insulator 464. The insulator 468 is over the insulator 466. The transistor 2100 and the conductor 416c are over the insulator 468.

[0258]

The insulator 464 includes an opening reaching the region 474a, an opening reaching the region 474b, and an opening reaching the conductor 454, in which the conductor 480a, the conductor 480b, and the conductor 480c are embedded, respectively.

[0259]

In addition, the insulator 466 includes an opening reaching the conductor 480a, an opening reaching the conductor 480b, and an opening reaching the conductor 480c, in which the conductor 478a, the conductor 478b, and the conductor 478c are embedded, respectively.

[0260]

In addition, the insulator 468 includes an opening reaching the conductor 478b and an opening reaching the conductor 478c, in which the conductor 476a and the conductor 476b are embedded, respectively.

[0261]

The conductor 476a is in contact with the conductor 416b of the transistor 2100. The conductor 476b is in contact with the conductor 416c.

[0262]

The insulator 410 includes an opening reaching the conductor 416c. In addition, the conductor 424c is embedded in the opening.

[0263]

The insulators 418 and 408 include an opening reaching the conductor 424c and an opening reaching the conductor 404. In addition, the conductor 424c and the conductor 404 are electrically connected to each other by the conductor 426c through the openings.

[0264]

Note that a semiconductor device in FIG. 16 is the same as the semiconductor device in FIG. 15 except a structure of the transistor 2200. Therefore, the description of the semiconductor device in FIG. 15 is referred to for the semiconductor device in FIG. 16. In the semiconductor device in FIG. 16, the transistor 2200 is a FIN-type transistor. The effective channel width is increased in the FIN-type transistor 2200, whereby the on-state characteristics of the transistor 2200 can be improved. In addition, since contribution of the electric field of the gate electrode can be increased, the off-state characteristics of the transistor 2200 can be improved.

[0265]

Note that a semiconductor device in FIG. 17 is the same as the semiconductor device in FIG. 15 except a structure of the transistor 2200. Therefore, the description of the semiconductor device in FIG. 15 is referred to for the semiconductor device in FIG. 17. In the semiconductor device in FIG. 17, the transistor 2200 is formed using an SOI substrate. In the structure in FIG. 17, a region 456 is separated from the semiconductor substrate 450 with an insulator 452 provided therebetween. Since the SOI substrate is used, a punch-through current can be reduced; and thus the off-state characteristics of the transistor 2200 can be improved. Note that the insulator 452 can be formed by turning part of the semiconductor substrate 450 into an insulator. For example, silicon oxide can be used as the insulator 452.

[0266]

In each of the semiconductor devices shown in FIG. 15, FIG. 16, and FIG. 17, a p-channel transistor is formed utilizing a semiconductor substrate, and an n-channel transistor is formed above that; therefore, an occupation area of the element can be reduced. That is, the integration degree of the semiconductor device can be improved. In addition, the manufacturing process can be simplified compared to the case where an n-channel transistor and a p-channel transistor are formed utilizing the same semiconductor substrate; therefore, the

productivity of the semiconductor device can be increased. Moreover, the yield of the semiconductor device can be improved. For the p-channel transistor, some complicated steps such as formation of lightly doped drain (LDD) regions, formation of a shallow trench structure, or distortion design can be omitted in some cases. Therefore, the productivity and yield of the semiconductor device in FIG. 15, FIG. 16, or FIG. 17 can be increased in some cases, compared to a semiconductor device where an n-channel transistor is formed utilizing the semiconductor substrate.

[0267]

[CMOS analog switch]

A circuit diagram in FIG. 14B shows a configuration in which sources of the transistors 2100 and 2200 are connected to each other and drains of the transistors 2100 and 2200 are connected to each other. With such a configuration, the transistors can function as a so-called CMOS analog switch.

[0268]

[Memory device example]

An example of a semiconductor device (memory device) which includes the transistor of one embodiment of the present invention, which can retain stored data even when not powered, and which has an unlimited number of write cycles is shown in FIGS. 18A and 18B.

[0269]

The semiconductor device illustrated in FIG. 18A includes a transistor 3200 using a first semiconductor, a transistor 3300 using a second semiconductor, and a capacitor 3400. Note that any of the above-described transistors can be used as the transistor 3300.

[0270]

The transistor 3300 is a transistor using an oxide semiconductor. Since the off-state current of the transistor 3300 is low, stored data can be retained for a long period at a predetermined node of the semiconductor device. In other words, power consumption of the semiconductor device can be reduced because refresh operation becomes unnecessary or the frequency of refresh operation can be extremely low.

[0271]

In FIG. 18A, a first wiring 3001 is electrically connected to a source of the transistor 3200. A second wiring 3002 is electrically connected to a drain of the transistor 3200. A third wiring 3003 is electrically connected to one of the source and the drain of the transistor 3300. A fourth wiring 3004 is electrically connected to the gate of the transistor 3300. The gate of the transistor 3200 and the other of the source and the drain of the transistor 3300 are electrically

connected to one electrode of the capacitor 3400. A fifth wiring 3005 is electrically connected to the other electrode of the capacitor 3400.

[0272]

The semiconductor device in FIG. 18A has a feature that the potential of the gate of the transistor 3200 can be retained, and thus enables writing, retaining, and reading of data as follows.

[0273]

Writing and holding of data will be described. First, the potential of the fourth wiring 3004 is set to a potential at which the transistor 3300 is turned on, so that the transistor 3300 is turned on. Accordingly, the potential of the third wiring 3003 is supplied to a node FG where the gate of the transistor 3200 and the one electrode of the capacitor 3400 are electrically connected to each other. That is, a predetermined charge is supplied to the gate of the transistor 3200 (writing). Here, one of two kinds of charges providing different potential levels (hereinafter referred to as a low-level charge and a high-level charge) is supplied. After that, the potential of the fourth wiring 3004 is set to a potential at which the transistor 3300 is turned off, so that the transistor 3300 is turned off. Thus, the charge is held at the node FG (retaining).

[0274]

Since the off-state current of the transistor 3300 is extremely low, the charge of the node FG is retained for a long time.

[0275]

Next, reading of data will be described. An appropriate potential (a reading potential) is supplied to the fifth wiring 3005 while a predetermined potential (a constant potential) is supplied to the first wiring 3001, whereby the potential of the second wiring 3002 varies depending on the amount of charge retained in the node FG. This is because in the case of using an n-channel transistor as the transistor 3200, an apparent threshold voltage V_{th_H} at the time when the high-level charge is given to the gate of the transistor 3200 is lower than an apparent threshold voltage V_{th_L} at the time when the low-level charge is given to the gate of the transistor 3200. Here, an apparent threshold voltage refers to the potential of the fifth wiring 3005 which is needed to turn on the transistor 3200. Thus, the potential of the fifth wiring 3005 is set to a potential V_0 which is between V_{th_H} and V_{th_L}, whereby charge supplied to the node FG can be determined. For example, in the case where the high-level charge is supplied to the node FG in writing and the potential of the fifth wiring 3005 is V_0 ($> V_{th_H}$), the transistor 3200 is turned on. On the other hand, in the case where the low-level charge is supplied to the node FG in writing, even when the potential of the fifth wiring 3005 is V_0 ($< V_{th_L}$), the transistor 3200

remains off. Thus, the data retained in the node FG can be read by determining the potential of the second wiring 3002.

[0276]

Note that in the case where memory cells are arrayed, it is necessary that data of a desired memory cell is read in read operation. In the case where data of the other memory cells is not read, the fifth wiring 3005 may be supplied with a potential at which the transistor 3200 is turned off regardless of the charge supplied to the node FG, that is, a potential lower than V_{th_H}. Alternatively, the fifth wiring 3005 may be supplied with a potential at which the transistor 3200 is turned on regardless of the charge supplied to the node FG, that is, a potential higher than V_{th_L}.

[0277]

The semiconductor device in FIG. 18B is different from the semiconductor device in FIG. 18A in that the transistor 3200 is not provided. Also in this case, writing and retaining operation of data can be performed in a manner similar to the semiconductor device in FIG. 18A.

[0278]

Reading of data in the semiconductor device in FIG. 18B is described. When the transistor 3300 is turned on, the third wiring 3003 which is in a floating state and the capacitor 3400 become in the conduction state, and the charge is redistributed between the third wiring 3003 and the capacitor 3400. As a result, the potential of the third wiring 3003 is changed. The amount of change in potential of the third wiring 3003 varies depending on the potential of the one electrode of the capacitor 3400 (or the charge accumulated in the capacitor 3400).

[0279]

For example, the potential of the third wiring 3003 after the charge redistribution is $(C_B \times V_{B0} + C \times V)/(C_B + C)$, where V is the potential of the one electrode of the capacitor 3400, C is the capacitance of the capacitor 3400, C_B is the capacitance component of the third wiring 3003, and V_{B0} is the potential of the third wiring 3003 before the charge redistribution. Thus, it can be found that, assuming that the memory cell is in either of two states in which the potential of the one electrode of the capacitor 3400 is V_1 and V_0 ($V_1 > V_0$), the potential of the third wiring 3003 in the case of the one electrode of the capacitor 3400 retaining the potential V_1 ($= (C_B \times V_{B0} + C \times V_1)/(C_B + C)$) is higher than the potential of the third wiring 3003 in the case of the one electrode of the capacitor 3400 retaining the potential V_0 ($= (C_B \times V_{B0} + C \times V_0)/(C_B + C)$).

[0280]

Then, by comparing the potential of the third wiring 3003 with a predetermined potential, data can be read.

[0281]

In this case, a transistor including the first semiconductor may be used for a driver circuit for driving a memory cell, and a transistor including the second semiconductor may be stacked over the driver circuit as the transistor 3300.

[0282]

When including a transistor using an oxide semiconductor and having an extremely low off-state current, the semiconductor device described above can retain stored data for a long time. In other words, refresh operation becomes unnecessary or the frequency of the refresh operation can be extremely low, which leads to a sufficient reduction in power consumption of a semiconductor device. Moreover, stored data can be retained for a long time even when power is not supplied (note that a potential is preferably fixed).

[0283]

Further, in the semiconductor device, high voltage is not needed for writing data and deterioration of elements is less likely to occur. Unlike in a conventional nonvolatile memory, for example, it is not necessary to inject and extract electrons into and from a floating gate; thus, a problem such as deterioration of an insulator is not caused. That is, the semiconductor device of one embodiment of the present invention does not have a limit on the number of times of rewriting data, which is a problem of a conventional nonvolatile memory, and the reliability thereof is drastically improved. Furthermore, data is written depending on the state of the transistor (on or off), whereby high-speed operation can be easily achieved.

[0284]

<CPU>

A CPU including a semiconductor device such as any of the above-described transistors or the above-described memory device is described below.

[0285]

FIG. 19 is a block diagram illustrating a configuration example of a CPU including any of the above-described transistors as a component.

[0286]

The CPU illustrated in FIG. 19 includes, over a substrate 1190, an arithmetic logic unit (ALU) 1191, an ALU controller 1192, an instruction decoder 1193, an interrupt controller 1194, a timing controller 1195, a register 1196, a register controller 1197, a bus interface 1198, a rewritable ROM 1199, and an ROM interface 1189. A semiconductor substrate, an SOI substrate, a glass substrate, or the like is used as the substrate 1190. The ROM 1199 and the ROM interface 1189 may be provided over a separate chip. Obviously, the CPU shown in FIG. 19 is just an example in which the configuration has been simplified, and an actual CPU may have various configurations depending on the application. For example, the CPU may have the

following configuration: a structure including the CPU illustrated in FIG. 19 or an arithmetic circuit is considered as one core; a plurality of the cores are included; and the cores operate in parallel. The number of bits that the CPU can process in an internal arithmetic circuit or in a data bus can be 8, 16, 32, or 64, for example.

[0287]

An instruction that is input to the CPU through the bus interface 1198 is input to the instruction decoder 1193 and decoded therein, and then, input to the ALU controller 1192, the interrupt controller 1194, the register controller 1197, and the timing controller 1195.

[0288]

The ALU controller 1192, the interrupt controller 1194, the register controller 1197, and the timing controller 1195 conduct various controls in accordance with the decoded instruction. Specifically, the ALU controller 1192 generates signals for controlling the operation of the ALU 1191. While the CPU is executing a program, the interrupt controller 1194 processes an interrupt request from an external input/output device or a peripheral circuit depending on its priority or a mask state. The register controller 1197 generates an address of the register 1196, and reads/writes data from/to the register 1196 depending on the state of the CPU.

[0289]

The timing controller 1195 generates signals for controlling operation timings of the ALU 1191, the ALU controller 1192, the instruction decoder 1193, the interrupt controller 1194, and the register controller 1197. For example, the timing controller 1195 includes an internal clock generator for generating an internal clock signal on the basis of a reference clock signal, and supplies the internal clock signal to the above circuits.

[0290]

In the CPU illustrated in FIG. 19, a memory cell is provided in the register 1196. For the memory cell of the register 1196, any of the above-described transistors, the above-described memory device, or the like can be used.

[0291]

In the CPU illustrated in FIG. 19, the register controller 1197 selects operation of retaining data in the register 1196 in accordance with an instruction from the ALU 1191. That is, the register controller 1197 selects whether data is held by a flip-flop or by a capacitor in the memory cell included in the register 1196. When data holding by the flip-flop is selected, a power supply voltage is supplied to the memory cell in the register 1196. When data holding by the capacitor is selected, the data is rewritten in the capacitor, and supply of power supply voltage to the memory cell in the register 1196 can be stopped.

[0292]

FIG. 20 is an example of a circuit diagram of a memory element 1200 that can be used as the register 1196. A memory element 1200 includes a circuit 1201 in which stored data is volatile when power supply is stopped, a circuit 1202 in which stored data is nonvolatile even when power supply is stopped, a switch 1203, a switch 1204, a logic element 1206, a capacitor 1207, and a circuit 1220 having a selecting function. The circuit 1202 includes a capacitor 1208, a transistor 1209, and a transistor 1210. Note that the memory element 1200 may further include another element such as a diode, a resistor, or an inductor, as needed.

[0293]

Here, the above-described memory device can be used as the circuit 1202. When supply of a power supply voltage to the memory element 1200 is stopped, GND (0 V) or a potential at which the transistor 1209 in the circuit 1202 is turned off continues to be input to a gate of the transistor 1209. For example, the gate of the transistor 1209 is grounded through a load such as a resistor.

[0294]

Shown here is an example in which the switch 1203 is a transistor 1213 having one conductivity type (e.g., an n-channel transistor) and the switch 1204 is a transistor 1214 having a conductivity type opposite to the one conductivity type (e.g., a p-channel transistor). A first terminal of the switch 1203 corresponds to one of a source and a drain of the transistor 1213, a second terminal of the switch 1203 corresponds to the other of the source and the drain of the transistor 1213, and conduction or non-conduction between the first terminal and the second terminal of the switch 1203 (i.e., the on/off state of the transistor 1213) is selected by a control signal RD input to a gate of the transistor 1213. A first terminal of the switch 1204 corresponds to one of a source and a drain of the transistor 1214, a second terminal of the switch 1204 corresponds to the other of the source and the drain of the transistor 1214, and conduction or non-conduction between the first terminal and the second terminal of the switch 1204 (i.e., the on/off state of the transistor 1214) is selected by the control signal RD input to a gate of the transistor 1214.

[0295]

One of a source and a drain of the transistor 1209 is electrically connected to one of a pair of electrodes of the capacitor 1208 and a gate of the transistor 1210. Here, the connection portion is referred to as a node M2. One of a source and a drain of the transistor 1210 is electrically connected to a line which can supply a low power supply potential (e.g., a GND line), and the other thereof is electrically connected to the first terminal of the switch 1203 (the one of the source and the drain of the transistor 1213). The second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213) is electrically connected to the first

terminal of the switch 1204 (the one of the source and the drain of the transistor 1214). The second terminal of the switch 1204 (the other of the source and the drain of the transistor 1214) is electrically connected to a line which can supply a power supply potential VDD. The second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213), the first terminal of the switch 1204 (the one of the source and the drain of the transistor 1214), an input terminal of the logic element 1206, and one of a pair of electrodes of the capacitor 1207 are electrically connected to each other. Here, the connection portion is referred to as a node M1. The other of the pair of electrodes of the capacitor 1207 can be supplied with a constant potential. For example, the other of the pair of electrodes of the capacitor 1207 can be supplied with a low power supply potential (e.g., GND) or a high power supply potential (e.g., VDD). The other of the pair of electrodes of the capacitor 1207 is electrically connected to the line which can supply a low power supply potential (e.g., a GND line). The other of the pair of electrodes of the capacitor 1208 can be supplied with a constant potential. For example, the other of the pair of electrodes of the capacitor 1208 can be supplied with a low power supply potential (e.g., GND) or a high power supply potential (e.g., VDD). The other of the pair of electrodes of the capacitor 1208 is electrically connected to the line which can supply a low power supply potential (e.g., a GND line).

[0296]

The capacitor 1207 and the capacitor 1208 are not necessarily provided as long as the parasitic capacitance of the transistor, the wiring, or the like is actively utilized.

[0297]

A control signal WE is input to the gate of the transistor 1209. As for each of the switch 1203 and the switch 1204, a conduction state or a non-conduction state between the first terminal and the second terminal is selected by the control signal RD which is different from the control signal WE. When the first terminal and the second terminal of one of the switches are in the conduction state, the first terminal and the second terminal of the other of the switches are in the non-conduction state.

[0298]

A signal corresponding to data retained in the circuit 1201 is input to the other of the source and the drain of the transistor 1209. FIG. 20 illustrates an example in which a signal output from the circuit 1201 is input to the other of the source and the drain of the transistor 1209. The logic value of a signal output from the second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213) is inverted by the logic element 1206, and the inverted signal is input to the circuit 1201 through the circuit 1220.

[0299]

In the example of FIG. 20, a signal output from the second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213) is input to the circuit 1201 through the logic element 1206 and the circuit 1220; however, one embodiment of the present invention is not limited thereto. The signal output from the second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213) may be input to the circuit 1201 without its logic value being inverted. For example, in the case where the circuit 1201 includes a node in which a signal obtained by inversion of the logic value of a signal input from the input terminal is retained, the signal output from the second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213) can be input to the node.

[0300]

In FIG. 20, the transistors included in the memory element 1200 except for the transistor 1209 can each be a transistor in which a channel is formed in a film formed using a semiconductor other than an oxide semiconductor or in the substrate 1190. For example, the transistor can be a transistor whose channel is formed in a silicon film or a silicon substrate. Alternatively, all the transistors in the memory element 1200 may be a transistor in which a channel is formed in an oxide semiconductor. Further alternatively, in the memory element 1200, a transistor in which a channel is formed in an oxide semiconductor can be included besides the transistor 1209, and a transistor in which a channel is formed in a layer or the substrate 1190 including a semiconductor other than an oxide semiconductor can be used for the rest of the transistors.

[0301]

As the circuit 1201 in FIG. 20, for example, a flip-flop circuit can be used. As the logic element 1206, for example, an inverter or a clocked inverter can be used.

[0302]

In a period during which the memory element 1200 is not supplied with the power supply voltage, the semiconductor device of one embodiment of the present invention can retain data stored in the circuit 1201 by the capacitor 1208 which is provided in the circuit 1202.

[0303]

The off-state current of a transistor in which a channel is formed in an oxide semiconductor is extremely low. For example, the off-state current of a transistor in which a channel is formed in an oxide semiconductor is significantly lower than that of a transistor in which a channel is formed in silicon having crystallinity. Thus, when the transistor is used as the transistor 1209, a signal held in the capacitor 1208 is retained for a long time also in a period during which the power supply voltage is not supplied to the memory element 1200. The

memory element 1200 can accordingly retain the stored content (data) also in a period during which the supply of the power supply voltage is stopped.

[0304]

Since the above-described memory element performs pre-charge operation with the switch 1203 and the switch 1204, the time required for the circuit 1201 to retain original data again after the supply of the power supply voltage is restarted can be shortened.

[0305]

In the circuit 1202, a signal retained by the capacitor 1208 is input to the gate of the transistor 1210. Therefore, after supply of the power supply voltage to the memory element 1200 is restarted, the signal retained by the capacitor 1208 can be converted into the one corresponding to the state (the on state or the off state) of the transistor 1210 to be read from the circuit 1202. Consequently, an original signal can be accurately read even when a potential corresponding to the signal retained by the capacitor 1208 varies to some degree.

[0306]

By using the above-described memory element 1200 for a memory device such as a register or a cache memory included in a processor, data in the memory device can be prevented from being lost owing to the stop of the supply of the power supply voltage. Further, shortly after the supply of the power supply voltage is restarted, return to the same state as that before the power supply is stopped can be made. Therefore, the power supply can be stopped even for a short time in the processor or one or a plurality of logic circuits included in the processor. Accordingly, power consumption can be suppressed.

[0307]

Although the memory element 1200 is used in a CPU as an example, the memory element 1200 can also be used in an LSI such as a digital signal processor (DSP), a custom LSI, or a programmable logic device (PLD), and a radio frequency identification (RF-ID).

[0308]

<Display Device>

The following shows configuration examples of a display device of one embodiment of the present invention.

[0309]

[Configuration example]

FIG. 21A is a top view of a display device of one embodiment of the present invention. FIG. 21B illustrates a pixel circuit where a liquid crystal element is used for a pixel of a display device of one embodiment of the present invention. FIG. 21C illustrates a pixel circuit where

an organic EL element is used for a pixel of a display device of one embodiment of the present invention.

[0310]

Any of the above-described transistors can be used as a transistor used for the pixel. Here, an example in which an n-channel transistor is used is shown. Note that a transistor manufactured through the same steps as the transistor used for the pixel may be used for a driver circuit. Thus, by using any of the above-described transistors for a pixel or a driver circuit, the display device can have high display quality and/or high reliability.

[0311]

FIG. 21A illustrates an example of an active matrix display device. A pixel portion 5001, a first scan line driver circuit 5002, a second scan line driver circuit 5003, and a signal line driver circuit 5004 are provided over a substrate 5000 in the display device. The pixel portion 5001 is electrically connected to the signal line driver circuit 5004 through a plurality of signal lines and is electrically connected to the first scan line driver circuit 5002 and the second scan line driver circuit 5003 through a plurality of scan lines. Pixels including display elements are provided in respective regions divided by the scan lines and the signal lines. The substrate 5000 of the display device is electrically connected to a timing control circuit (also referred to as a controller or a control IC) through a connection portion such as a flexible printed circuit (FPC).

[0312]

The first scan line driver circuit 5002, the second scan line driver circuit 5003, and the signal line driver circuit 5004 are formed over the substrate 5000 where the pixel portion 5001 is formed. Therefore, the display device can be manufactured at cost lower than that in the case where a driver circuit is separately formed. Further, in the case where a driver circuit is separately formed, the number of wiring connections is increased. By providing the driver circuit over the substrate 5000, the number of wiring connections can be reduced. Accordingly, the reliability and/or yield can be improved.

[0313]

[Liquid crystal display device]

FIG. 21B illustrates an example of a circuit configuration of the pixel. Here, a pixel circuit which is applicable to a pixel of a VA liquid crystal display device or the like is illustrated.

[0314]

This pixel circuit can be used for a structure in which one pixel includes a plurality of pixel electrodes. The pixel electrodes are connected to different transistors, and the transistors

can be driven with different gate signals. Accordingly, signals applied to individual pixel electrodes in a multi-domain pixel can be controlled independently.

[0315]

A scan line 5012 of a transistor 5016 and a scan line 5013 of a transistor 5017 are separated so that different gate signals can be supplied thereto. In contrast, a signal line 5014 functioning as a data line is shared by the transistors 5016 and 5017. Any of the above-described transistors can be used as appropriate as each of the transistors 5016 and 5017. Thus, the liquid crystal display device can have high display quality and/or high reliability.

[0316]

A first pixel electrode is electrically connected to the transistor 5016 and a second pixel electrode is electrically connected to the transistor 5017. The first pixel electrode and the second pixel electrode are separated. There is no specific limitation on the shapes of the first electrode and the second electrode. For example, the first pixel electrode has a V shape.

[0317]

A gate electrode of the transistor 5016 is electrically connected to the scan line 5012, and a gate electrode of the transistor 5017 is electrically connected to the scan line 5013. When different gate signals are supplied to the scan line 5012 and the scan line 5013, operation timings of the transistor 5016 and the transistor 5017 can be varied. As a result, alignment of liquid crystals can be controlled.

[0318]

Furthermore, a capacitor may be formed using a capacitor line 5010, a gate insulator functioning as a dielectric, and a capacitor electrode electrically connected to the first pixel electrode or the second pixel electrode.

[0319]

The pixel structure is a multi-domain structure in which a first liquid crystal element 5018 and a second liquid crystal element 5019 are provided in one pixel. The first liquid crystal element 5018 includes the first pixel electrode, a counter electrode, and a liquid crystal layer therebetween. The second liquid crystal element 5019 includes the second pixel electrode, the counter electrode, and the liquid crystal layer therebetween.

[0320]

Note that a pixel circuit of the display device of one embodiment of the present invention is not limited to that shown in FIG. 21B. For example, a switch, a resistor, a capacitor, a transistor, a sensor, a logic circuit, or the like may be added to the pixel circuit shown in FIG. 21B.

[0321]

[Organic EL display device]

FIG. 21C illustrates another example of a circuit configuration of the pixel. Here, a pixel structure of a display device using an organic EL element is shown.

[0322]

In an organic EL element, by application of voltage to a light-emitting element, electrons are injected from one of a pair of electrodes included in the organic EL element and holes are injected from the other of the pair of electrodes, into a layer containing a light-emitting organic compound; thus, current flows. The electrons and holes are recombined, and thus, the light-emitting organic compound is excited. The light-emitting organic compound returns to a ground state from the excited state, thereby emitting light. Based on such a mechanism, such a light-emitting element is referred to as a current-excitation type light-emitting element.

[0323]

FIG. 21C illustrates an example of a pixel circuit. Here, one pixel includes two n-channel transistors. Note that any of the above-described transistors can be used as the n-channel transistors. Further, digital time grayscale driving can be employed for the pixel circuit.

[0324]

The configuration of the applicable pixel circuit and operation of a pixel employing digital time grayscale driving will be described.

[0325]

A pixel 5020 includes a switching transistor 5021, a driver transistor 5022, a light-emitting element 5024, and a capacitor 5023. A gate electrode of the switching transistor 5021 is connected to a scan line 5026, a first electrode (one of a source electrode and a drain electrode) of the switching transistor 5021 is connected to a signal line 5025, and a second electrode (the other of the source electrode and the drain electrode) of the switching transistor 5021 is connected to a gate electrode of the driver transistor 5022. The gate electrode of the driver transistor 5022 is connected to a power supply line 5027 through the capacitor 5023, a first electrode of the driver transistor 5022 is connected to the power supply line 5027, and a second electrode of the driver transistor 5022 is connected to a first electrode (a pixel electrode) of the light-emitting element 5024. A second electrode of the light-emitting element 5024 corresponds to a common electrode 5028. The common electrode 5028 is electrically connected to a common potential line provided over the same substrate.

[0326]

As each of the switching transistor 5021 and the driver transistor 5022, any of the above-described transistors can be used as appropriate. In this manner, an organic EL display device having high display quality and/or high reliability can be provided.

[0327]

The potential of the second electrode (the common electrode 5028) of the light-emitting element 5024 is set to be a low power supply potential. Note that the low power supply potential is lower than a high power supply potential supplied to the power supply line 5027. For example, the low power supply potential can be GND, 0 V, or the like. The high power supply potential and the low power supply potential are set to be higher than or equal to the forward threshold voltage of the light-emitting element 5024, and the difference between the potentials is applied to the light-emitting element 5024, whereby current is supplied to the light-emitting element 5024, leading to light emission. The forward voltage of the light-emitting element 5024 refers to a voltage at which a desired luminance is obtained, and includes at least forward threshold voltage.

[0328]

Note that gate capacitance of the driver transistor 5022 may be used as a substitute for the capacitor 5023 in some cases, so that the capacitor 5023 can be omitted. The gate capacitance of the driver transistor 5022 may be formed between the channel formation region and the gate electrode.

[0329]

Next, a signal input to the driver transistor 5022 is described. In the case of a voltage-input voltage driving method, a video signal for turning on or off the driver transistor 5022 is input to the driver transistor 5022. In order for the driver transistor 5022 to operate in a linear region, voltage higher than the voltage of the power supply line 5027 is applied to the gate electrode of the driver transistor 5022. Note that voltage higher than or equal to voltage which is the sum of power supply line voltage and the threshold voltage V_{th} of the driver transistor 5022 is applied to the signal line 5025.

[0330]

In the case of performing analog grayscale driving, a voltage higher than or equal to a voltage which is the sum of the forward voltage of the light-emitting element 5024 and the threshold voltage V_{th} of the driver transistor 5022 is applied to the gate electrode of the driver transistor 5022. A video signal by which the driver transistor 5022 is operated in a saturation region is input, so that current is supplied to the light-emitting element 5024. In order for the driver transistor 5022 to operate in a saturation region, the potential of the power supply line 5027 is set higher than the gate potential of the driver transistor 5022. When an analog video

signal is used, it is possible to supply current to the light-emitting element 5024 in accordance with the video signal and perform analog grayscale driving.

[0331]

Note that in the display device of one embodiment of the present invention, a pixel configuration is not limited to that shown in FIG. 21C. For example, a switch, a resistor, a capacitor, a sensor, a transistor, a logic circuit, or the like may be added to the pixel circuit shown in FIG. 21C.

[0332]

In the case where any of the above-described transistors is used for the circuit shown in FIGS. 21A to 21C, the source electrode (the first electrode) is electrically connected to the low potential side and the drain electrode (the second electrode) is electrically connected to the high potential side. Further, the potential of the first gate electrode may be controlled by a control circuit or the like and the potential described above as an example, e.g., a potential lower than the potential applied to the source electrode, may be input to the second gate electrode.

[0333]

<Electronic Device>

The semiconductor device of one embodiment of the present invention can be used for display devices, personal computers, image reproducing devices provided with recording media (typically, devices which reproduce the content of recording media such as digital versatile discs (DVDs) and have displays for displaying the reproduced images), or the like. Other examples of electronic devices that can be equipped with the semiconductor device of one embodiment of the present invention are mobile phones, game machines including portable game consoles, portable data terminals, e-book readers, cameras such as video cameras and digital still cameras, goggle-type displays (head mounted displays), navigation systems, audio reproducing devices (e.g., car audio systems and digital audio players), copiers, facsimiles, printers, multifunction printers, automated teller machines (ATM), and vending machines. FIGS. 22A to 22F illustrate specific examples of these electronic devices.

[0334]

FIG. 22A illustrates a portable game console including a housing 901, a housing 902, a display portion 903, a display portion 904, a microphone 905, a speaker 906, an operation key 907, a stylus 908, and the like. Although the portable game machine in FIG. 22A has the two display portions 903 and 904, the number of display portions included in a portable game console is not limited to this.

[0335]

FIG. 22B illustrates a portable data terminal including a first housing 911, a second housing 912, a first display portion 913, a second display portion 914, a joint 915, an operation key 916, and the like. The first display portion 913 is provided in the first housing 911, and the second display portion 914 is provided in the second housing 912. The first housing 911 and the second housing 912 are connected to each other with the joint 915, and the angle between the first housing 911 and the second housing 912 can be changed with the joint 915. An image on the first display portion 913 may be switched depending on the angle between the first housing 911 and the second housing 912 at the joint 915. A display device with a position input function may be used as at least one of the first display portion 913 and the second display portion 914. Note that the position input function can be added by provision of a touch panel in a display device. Alternatively, the position input function can be added by provision of a photoelectric conversion element called a photosensor in a pixel portion of a display device.

[0336]

FIG. 22C illustrates a laptop personal computer, which includes a housing 921, a display portion 922, a keyboard 923, a pointing device 924, and the like.

[0337]

FIG. 22D illustrates an electric refrigerator-freezer including a housing 931, a door for a refrigerator 932, a door for a freezer 933, and the like.

[0338]

FIG. 22E illustrates a video camera, which includes a first housing 941, a second housing 942, a display portion 943, operation keys 944, a lens 945, a joint 946, and the like. The operation keys 944 and the lens 945 are provided for the first housing 941, and the display portion 943 is provided for the second housing 942. The first housing 941 and the second housing 942 are connected to each other with the joint 946, and the angle between the first housing 941 and the second housing 942 can be changed with the joint 946. Images displayed on the display portion 943 may be switched in accordance with the angle at the joint 946 between the first housing 941 and the second housing 942.

[0339]

FIG. 22F illustrates an automobile including a car body 951, wheels 952, a dashboard 953, lights 954, and the like.

REFERENCE NUMERALS

[0340]

400: substrate, 401: insulator, 402: insulator, 404: conductor, 406: semiconductor, 406a: semiconductor, 406b: semiconductor, 406c: semiconductor, 408: insulator, 410: insulator, 412:

insulator, 413: conductor, 416: conductor, 416a: conductor, 416b: conductor, 416c: conductor, 418: insulator, 424a: conductor, 424b: conductor, 424c: conductor, 426a: conductor, 426b: conductor, 426c: conductor, 430: ion, 434: region, 436: semiconductor, 438: insulator, 439: insulator, 450: semiconductor substrate, 452: insulator, 454: conductor, 456: region, 460: region, 462: insulator, 464: insulator, 466: insulator, 468: insulator, 470: region, 474a: region, 474b: region, 476a: conductor, 476b: conductor, 478a: conductor, 478b: conductor, 478c: conductor, 480a: conductor, 480b: conductor, 480c: conductor, 490: transistor, 500: substrate, 501: insulator, 502: insulator, 504: conductor, 506: semiconductor, 508: insulator, 510: insulator, 512: insulator, 513: conductor, 516: conductor, 516a: conductor, 516b: conductor, 518: insulator, 524a: conductor, 524b: conductor, 526a: conductor, 526b: conductor, 530: ion, 534: region, 538: insulator, 539: insulator, 590: transistor, 901: housing, 902: housing, 903: display portion, 904: display portion, 905: microphone, 906: speaker, 907: operation key, 908: stylus, 911: housing, 912: housing, 913: display portion, 914: display portion, 915: joint, 916: operation key, 921: housing, 922: display portion, 923: keyboard, 924: pointing device, 931: housing, 932: door for a refrigerator, 933: door for a freezer, 941: housing, 942: housing, 943: display portion, 944: operation key, 945: lens, 946: joint, 951: car body, 952: wheel, 953: dashboard, 954: light, 1189: ROM interface, 1190: substrate, 1191: ALU, 1192: ALU controller, 1193: instruction decoder, 1194: interrupt controller, 1195: timing controller, 1196: register, 1197: register controller, 1198: bus interface, 1199: ROM, 1200: memory element, 1201: circuit, 1202: circuit, 1203: switch, 1204: switch, 1206: logic element, 1207: capacitor, 1208: capacitor, 1209: transistor, 1210: transistor, 1213: transistor, 1214: transistor, 1220: circuit, 2100: transistor, 2200: transistor, 3001: wiring, 3002: wiring, 3003: wiring, 3004: wiring, 3005: wiring, 3200: transistor, 3300: transistor, 3400: capacitor, 5000: substrate, 5001: pixel portion, 5002: scan line driver circuit, 5003: scan line driver circuit, 5004: signal line driver circuit, 5010: capacitor line, 5012: scan line, 5013: scan line, 5014: signal line, 5016: transistor, 5017: transistor, 5018: liquid crystal element, 5019: liquid crystal element, 5020: pixel, 5021: switching transistor, 5022: driver transistor, 5023: capacitor, 5024: light-emitting element, 5025: signal line, 5026: scan line, 5027: power supply line, 5028: common electrode.

This application is based on Japanese Patent Application serial No. 2014-125221 filed with Japan Patent Office on June 18, 2014, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A transistor comprising:

an oxide semiconductor;

a first conductor;

a second conductor;

a third conductor;

a first insulator; and

a second insulator,

wherein the first conductor includes a first region, a second region, and a third region,

wherein the oxide semiconductor includes a fourth region, a fifth region, and a sixth region,

wherein the first region and the sixth region overlap each other with the first insulator positioned between the first region and the sixth region,

wherein the second region and the second conductor overlap each other with the first insulator and the second insulator positioned between the second region and the second conductor,

wherein the third region and the third conductor overlap each other with the first insulator and the second insulator positioned between the third region and the third conductor,

wherein the second conductor is in contact with the fourth region,

wherein the third conductor is in contact with the fifth region, and

wherein the sixth region includes a lower carrier density than the fourth region and the fifth region.

2. A semiconductor device including the transistor according to claim 1, and a p-channel transistor,

wherein the transistor is an n-channel transistor,

wherein a source or a drain of the p-channel transistor is electrically connected to a source or a drain of the n-channel transistor,

wherein a gate of the p-channel transistor is electrically connected to a gate of the n-channel transistor, and

wherein a channel formation region of the p-channel transistor includes silicon.

3. The semiconductor device according to claim 2, wherein the p-channel transistor is formed using a silicon substrate whose crystal plane in a top surface comprises a region of a (110) plane.

4. The semiconductor device according to claim 2, wherein the channel formation region of the p-channel transistor has a concentration gradient where a concentration of an impurity imparting an n-type conductivity gets higher toward a vicinity of a surface of the channel formation region.

5. The semiconductor device according to claim 2, wherein the gate of the p-channel transistor includes a conductor with a work function of 4.5 eV or higher.

6. The semiconductor device according to claim 2, wherein the oxide semiconductor comprises indium.

7. The semiconductor device according to claim 2, wherein the oxide semiconductor includes a first oxide semiconductor, a second oxide semiconductor, and a third oxide semiconductor overlapping each other.

8. A transistor comprising:

an oxide semiconductor;

a first conductor;

a second conductor;

a third conductor;

a first insulator; and

a second insulator,

wherein the first conductor includes a first region, a second region, and a third region,

wherein the oxide semiconductor includes a fourth region, a fifth region, and a sixth region,

wherein the first region and the sixth region overlap each other with the first insulator positioned between the first region and the sixth region,

wherein the second region and the second conductor overlap each other with the first insulator and the second insulator positioned between the second region and the second conductor,

wherein the third region and the third conductor overlap each other with the first insulator and the second insulator positioned between the third region and the third conductor,

wherein the second conductor is in contact with the fourth region,

wherein the third conductor is in contact with the fifth region, and

wherein the sixth region includes a lower conductivity than the fourth region and the fifth region.

9. A semiconductor device including the transistor according to claim 8, and a p-channel transistor,

wherein the transistor is an n-channel transistor,

wherein a source or a drain of the p-channel transistor is electrically connected to a source or a drain of the n-channel transistor,

wherein a gate of the p-channel transistor is electrically connected to a gate of the n-channel transistor, and

wherein a channel formation region of the p-channel transistor includes silicon.

10. The semiconductor device according to claim 9, wherein the p-channel transistor is formed using a silicon substrate whose crystal plane in a top surface comprises a region of a (110) plane.

11. The semiconductor device according to claim 9, wherein the channel formation region of the p-channel transistor has a concentration gradient where a concentration of an impurity imparting an n-type conductivity gets higher toward a vicinity of a surface of the channel formation region.

12. The semiconductor device according to claim 9, wherein the gate of the p-channel transistor includes a conductor with a work function of 4.5 eV or higher.

13. The semiconductor device according to claim 9, wherein the oxide semiconductor comprises indium.

14. The semiconductor device according to claim 9, wherein the oxide semiconductor includes a first oxide semiconductor, a second oxide semiconductor, and a third oxide semiconductor overlapping each other.

15. A transistor comprising:

an oxide semiconductor;

a first conductor;

a second conductor;

a third conductor;

a first insulator; and

a second insulator,

wherein the first conductor includes a first region, a second region, and a third region,

wherein the oxide semiconductor includes a fourth region, a fifth region, and a sixth region,

wherein the first region and the sixth region overlap each other with the first insulator positioned between the first region and the sixth region,

wherein the second region and the second conductor overlap each other with the first insulator and the second insulator positioned between the second region and the second conductor,

wherein the third region and the third conductor overlap each other with the first insulator and the second insulator positioned between the third region and the third conductor,

wherein the second conductor is in contact with the fourth region,

wherein the third conductor is in contact with the fifth region, and

wherein the sixth region includes a lower hydrogen concentration than the fourth region and the fifth region.

16. A semiconductor device including the transistor according to claim 15, and a p-channel transistor,

wherein the transistor is an n-channel transistor,

wherein a source or a drain of the p-channel transistor is electrically connected to a source or a drain of the n-channel transistor,

wherein a gate of the p-channel transistor is electrically connected to a gate of the n-channel transistor, and

wherein a channel formation region of the p-channel transistor includes silicon.

17. The semiconductor device according to claim 16, wherein the p-channel transistor is formed using a silicon substrate whose crystal plane in a top surface comprises a region of a (110) plane.

18. The semiconductor device according to claim 16, wherein the channel formation region of the p-channel transistor has a concentration gradient where a concentration of an impurity imparting an n-type conductivity gets higher toward a vicinity of a surface of the channel formation region.

19. The semiconductor device according to claim 16, wherein the gate of the p-channel transistor includes a conductor with a work function of 4.5 eV or higher.

20. The semiconductor device according to claim 16, wherein the oxide semiconductor comprises indium.

21. The semiconductor device according to claim 16, wherein the oxide semiconductor includes a first oxide semiconductor, a second oxide semiconductor, and a third oxide semiconductor overlapping each other.

FIG. 1A

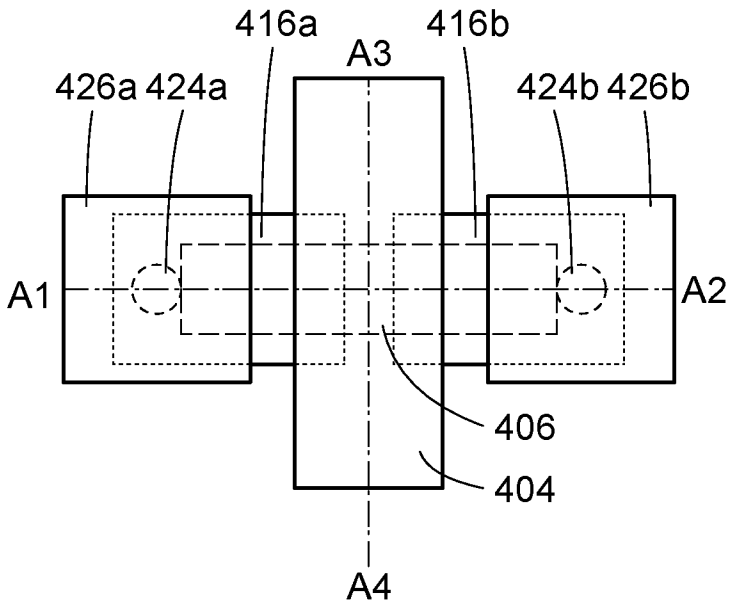

416a
A3
416b
426a 424a
424b 426b
A1
A2
406
404
A4

FIG. 1B

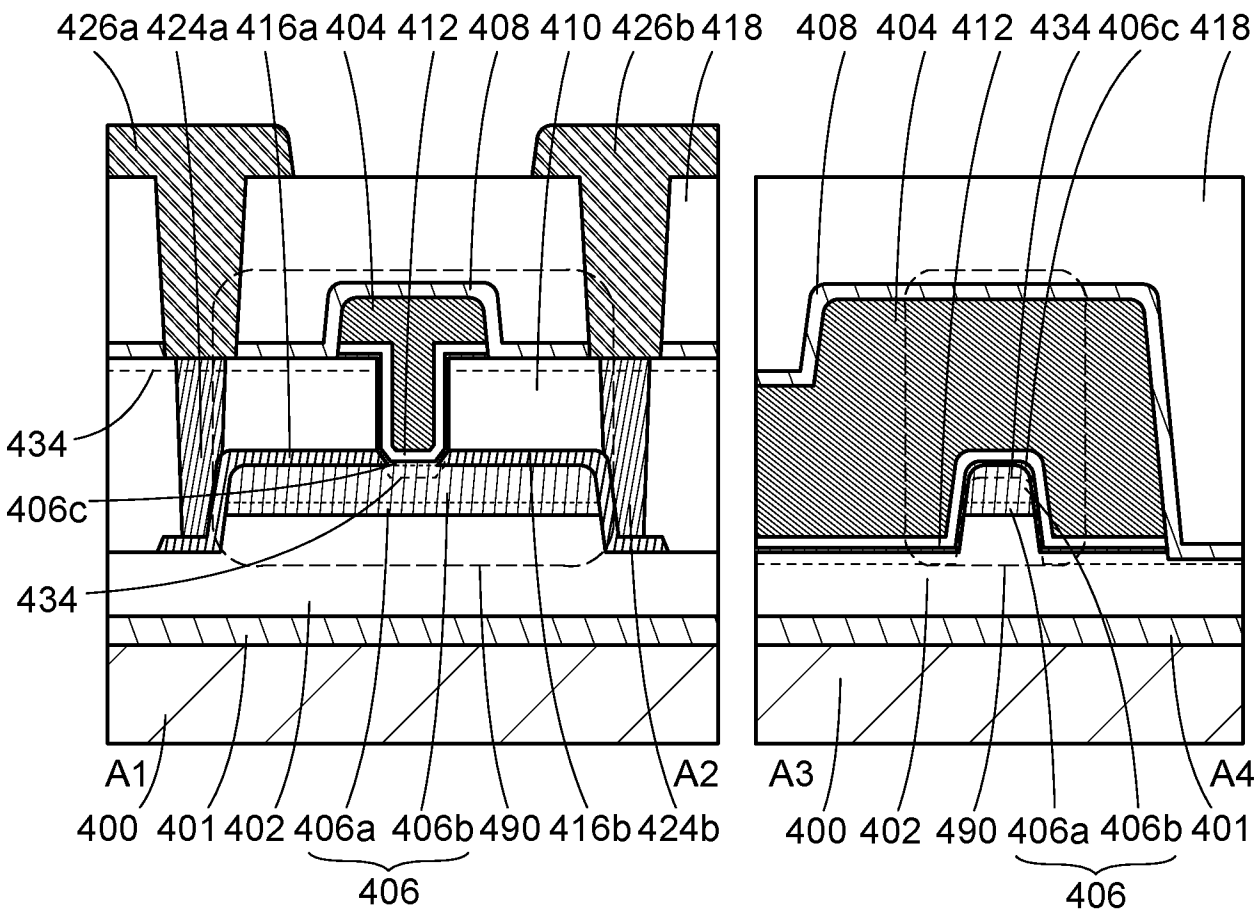

426a 424a 416a 404 412 408 410 426b 418
408 404 412 434 406c 418
434
406c
434
A1
A2
A3
A4
400 401 402 406a 406b 490 416b 424b
400 402 490 406a 406b 401
406
406

FIG. 2A

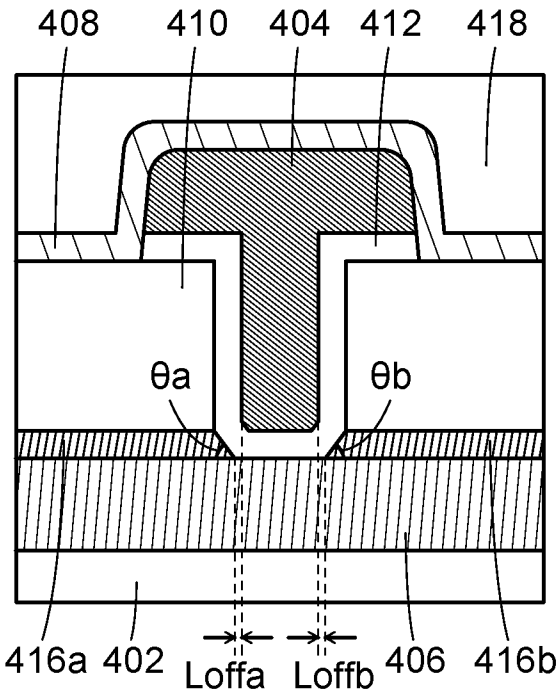


FIG. 2B

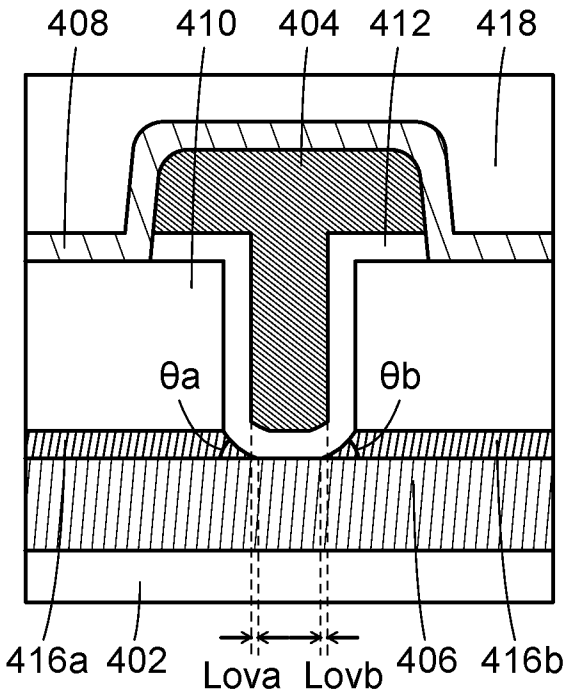


FIG. 2C

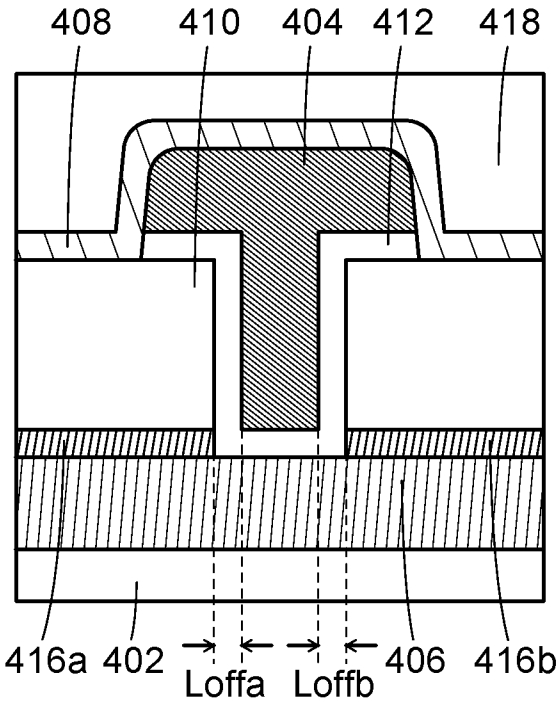


FIG. 2D

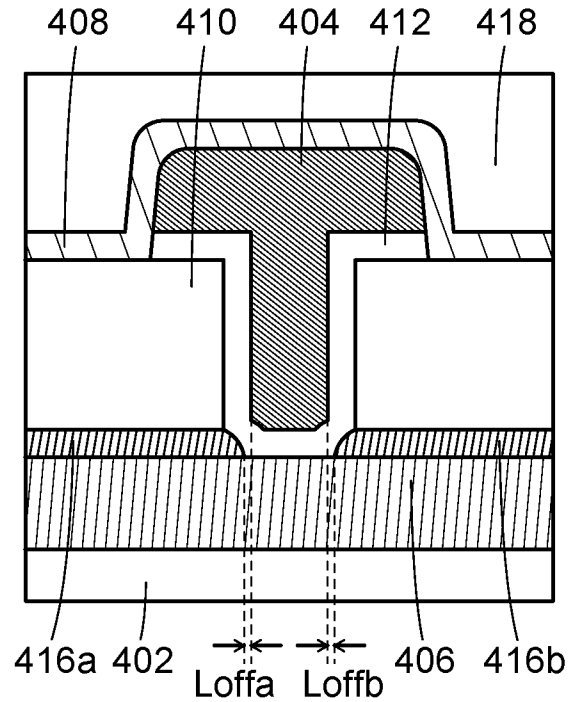


FIG. 3A

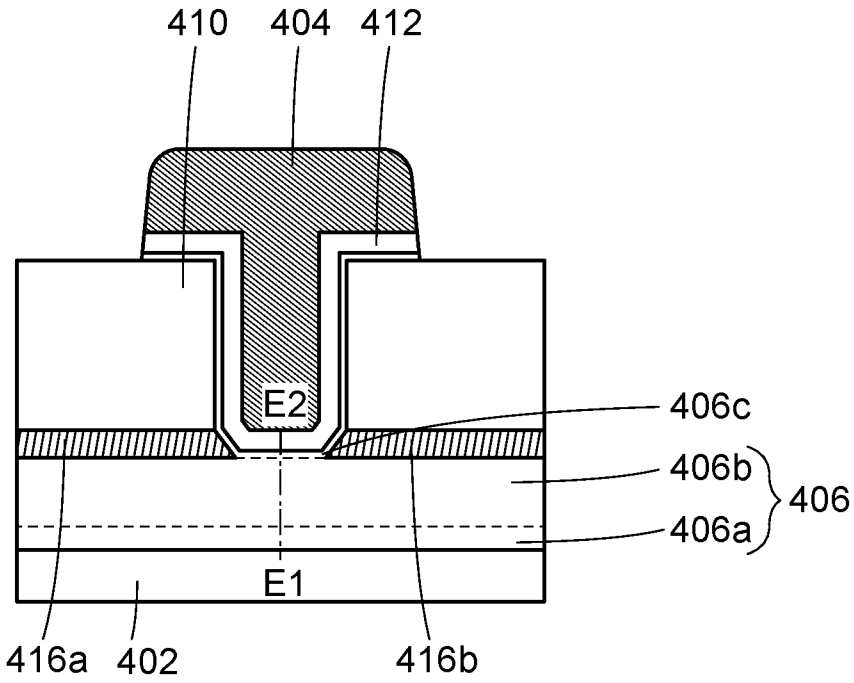

410
404
412
E2
406c
406b
406
406a
E1
416a
402
416b

FIG. 3B

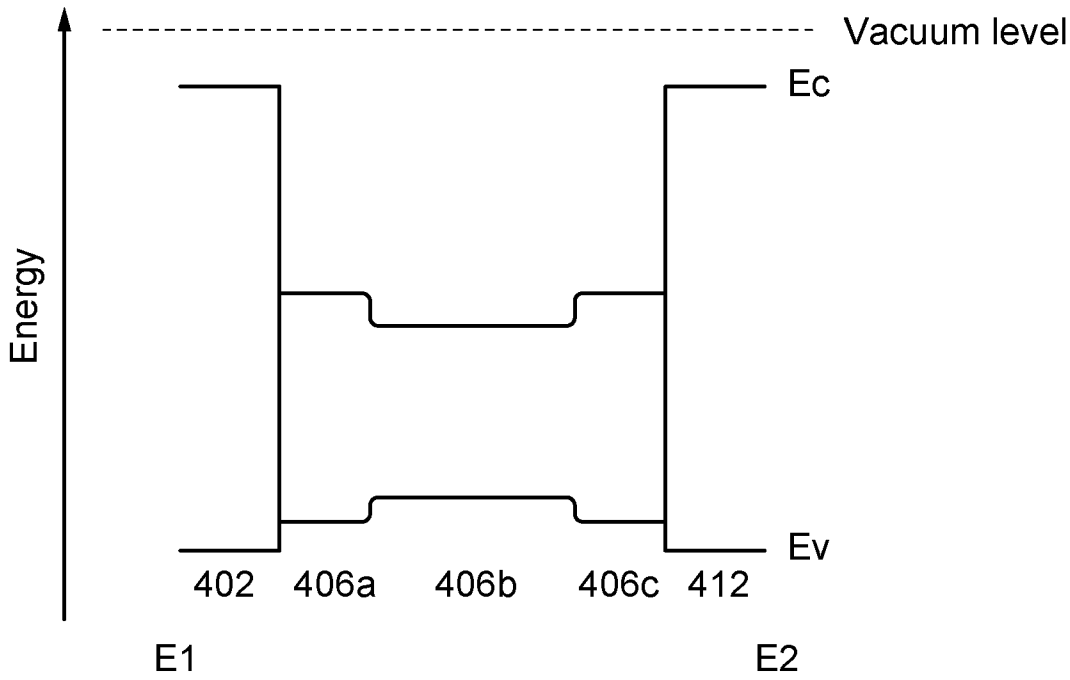

Vacuum level
Ec
Energy
Ev
402
406a
406b
406c
412
E1
E2

FIG. 4A

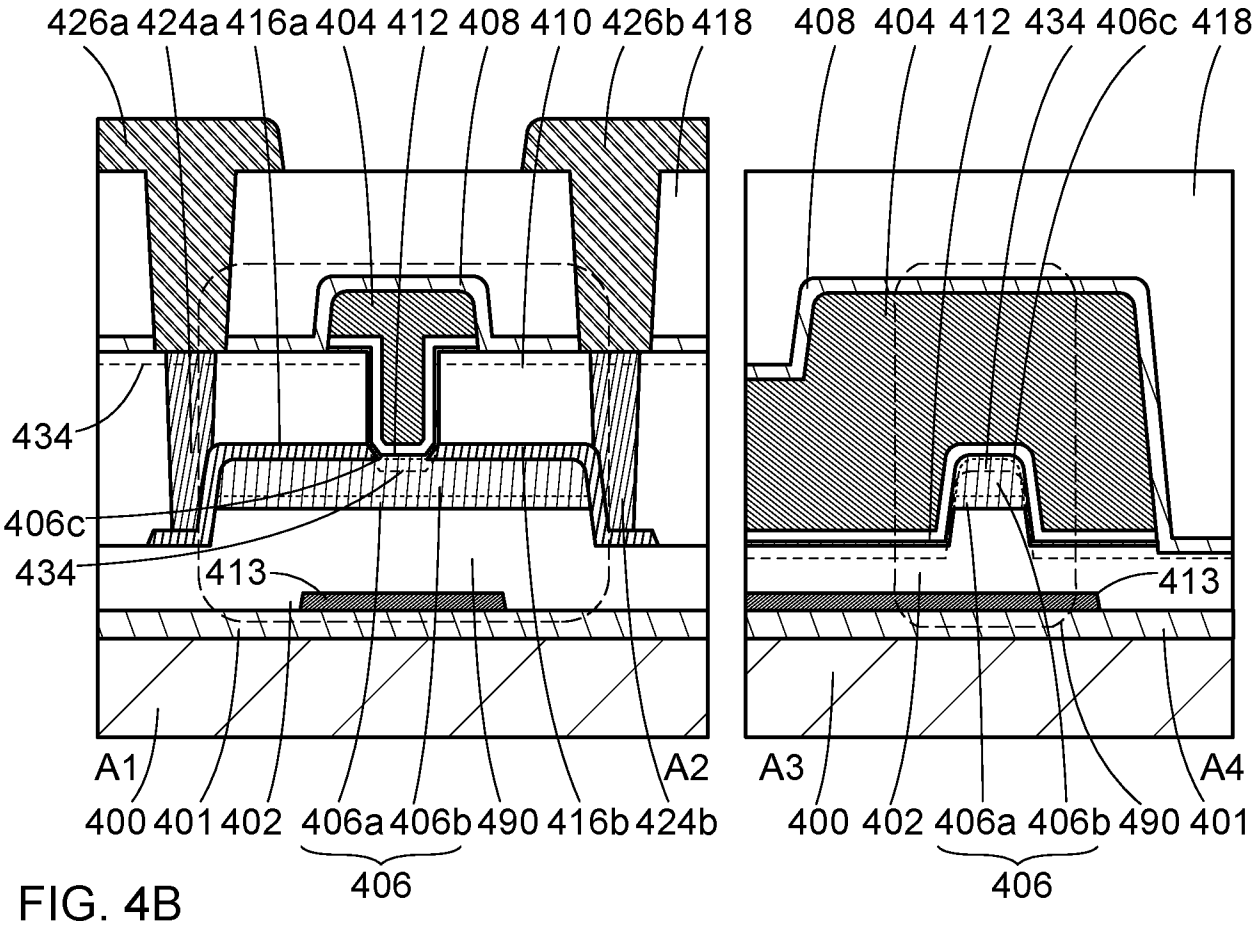

426a 424a 416a 404 412 408 410 426b 418
408 404 412 434 406c 418
434
406c
434
413
413
A1
A2
A3
A4
400 401 402 406a 406b 490 416b 424b
400 402 406a 406b 490 401
406
406

FIG. 4B

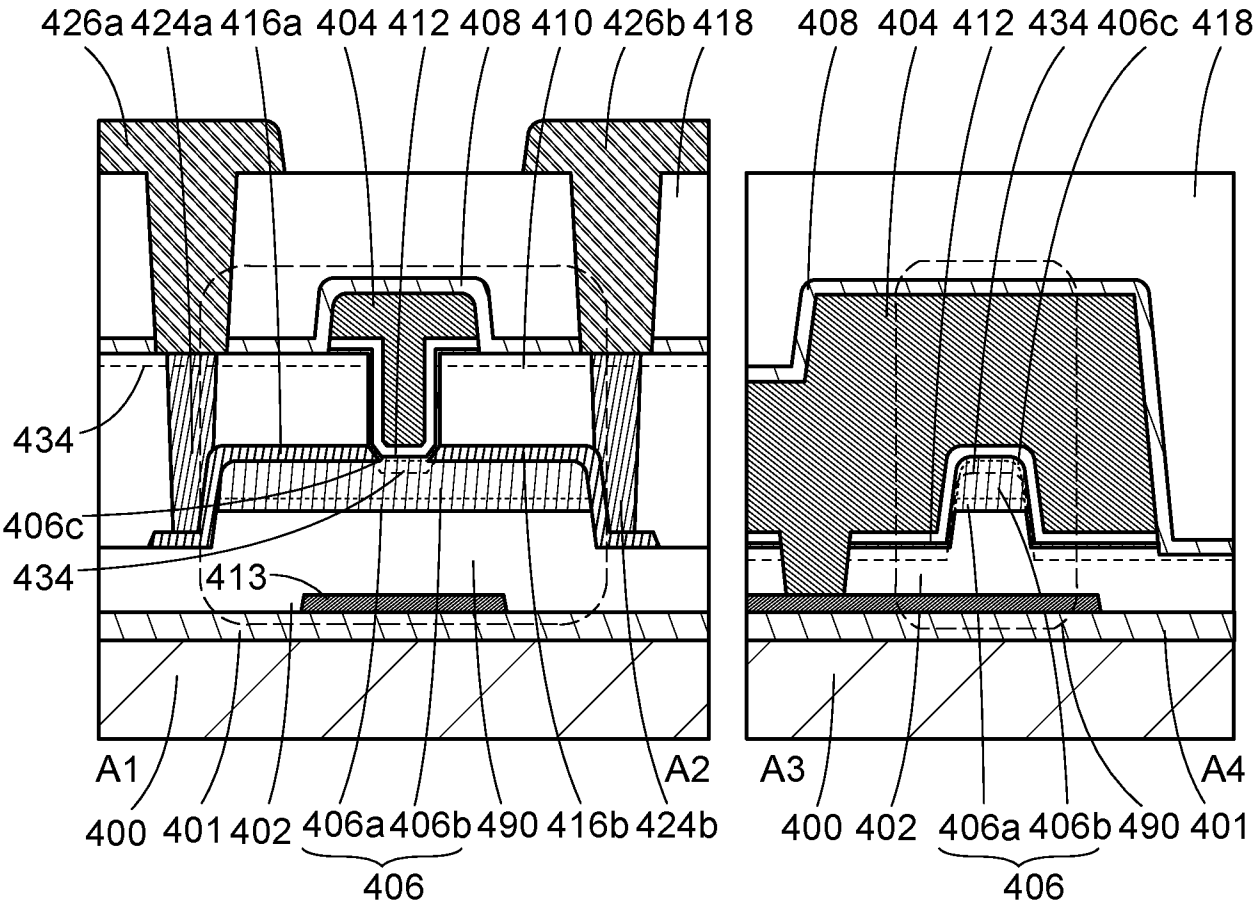

426a 424a 416a 404 412 408 410 426b 418
408 404 412 434 406c 418
434
406c
434
413
A1
A2
A3
A4
400 401 402 406a 406b 490 416b 424b
400 402 406a 406b 490 401
406
406

FIG. 5A

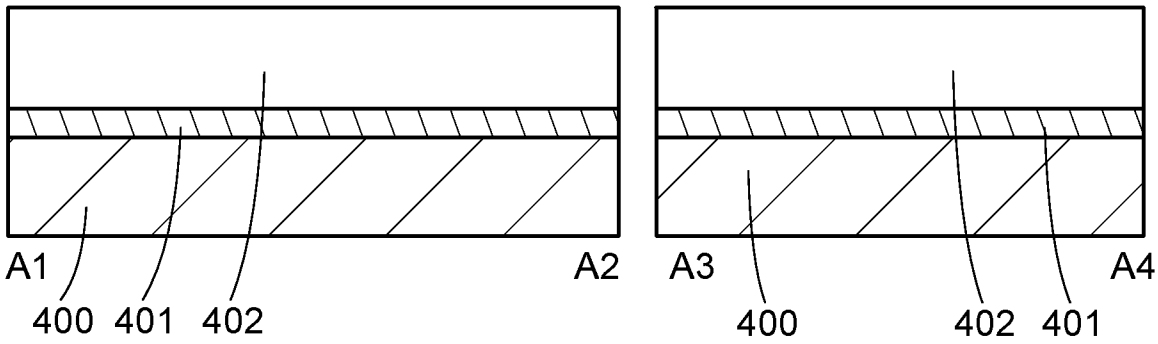

A1
A2
400
401
402
A3
A4
400
402
401

FIG. 5B

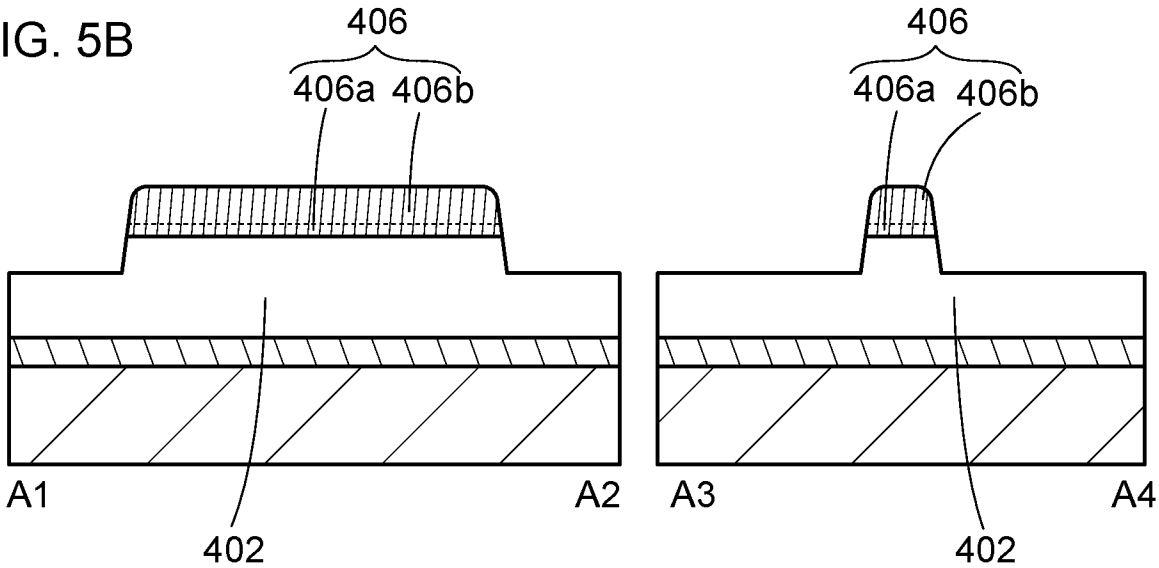

406
406a
406b
A1
A2
402
406
406a
406b
A3
A4
402

FIG. 6A

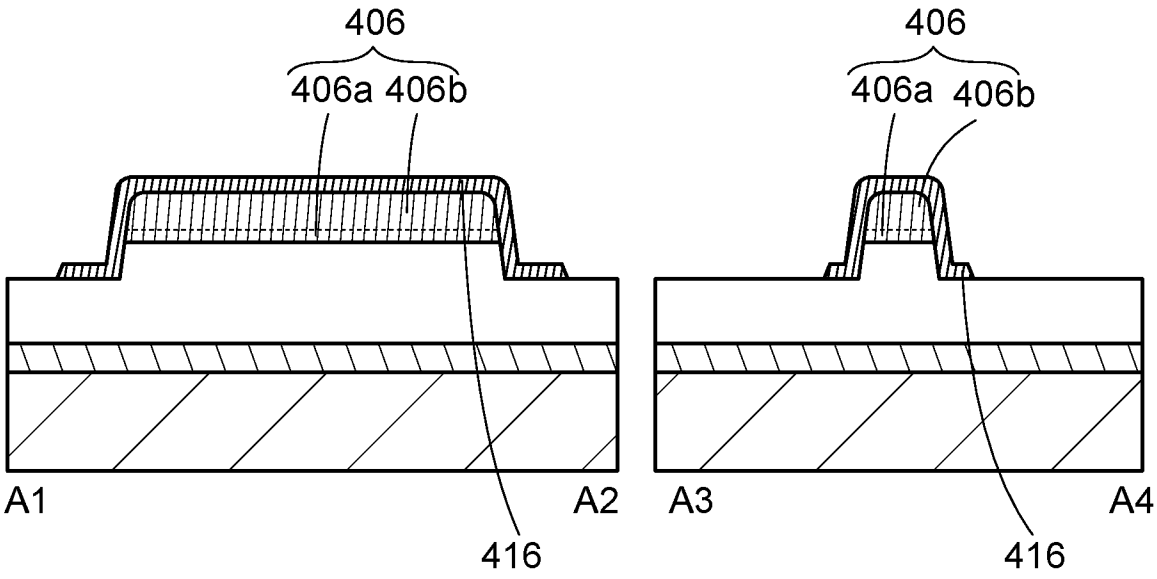

406
406a
406b
406
406a
406b
A1
A2
A3
A4
416
416

FIG. 6B

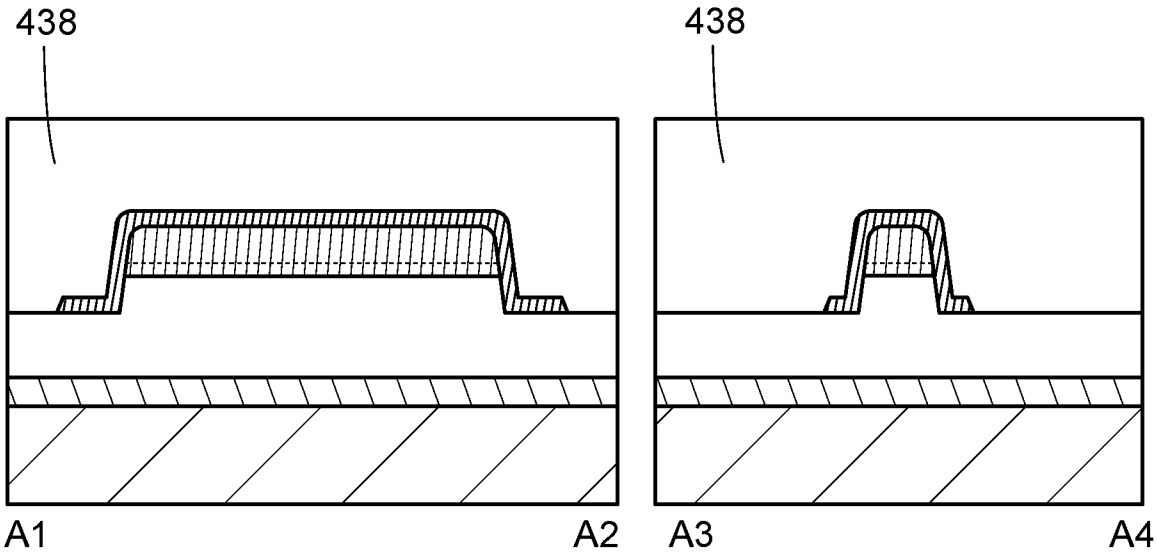

438
438
A1
A2
A3
A4

FIG. 7A

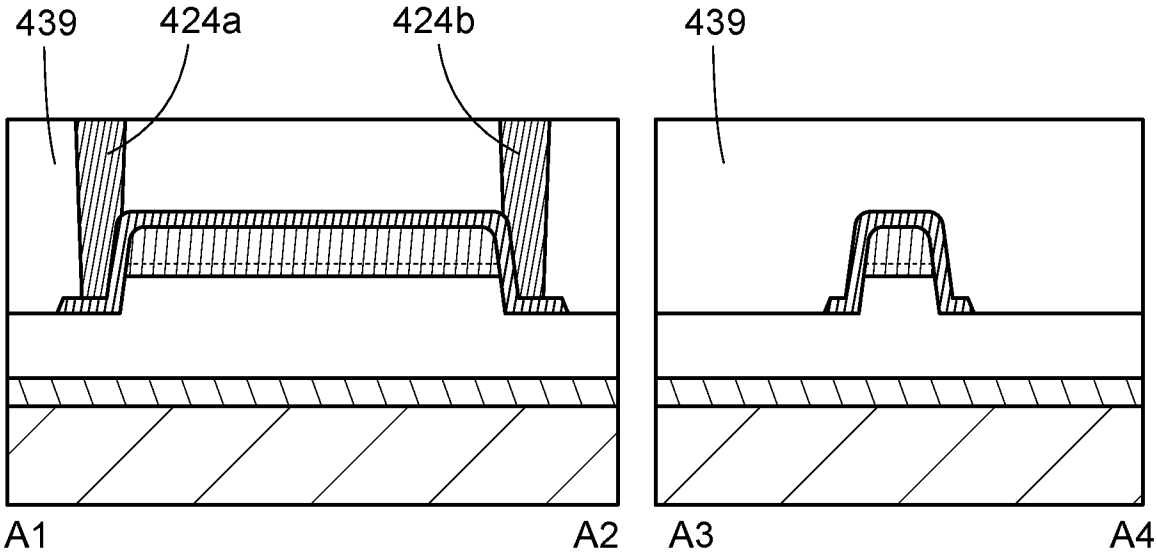


FIG. 7B

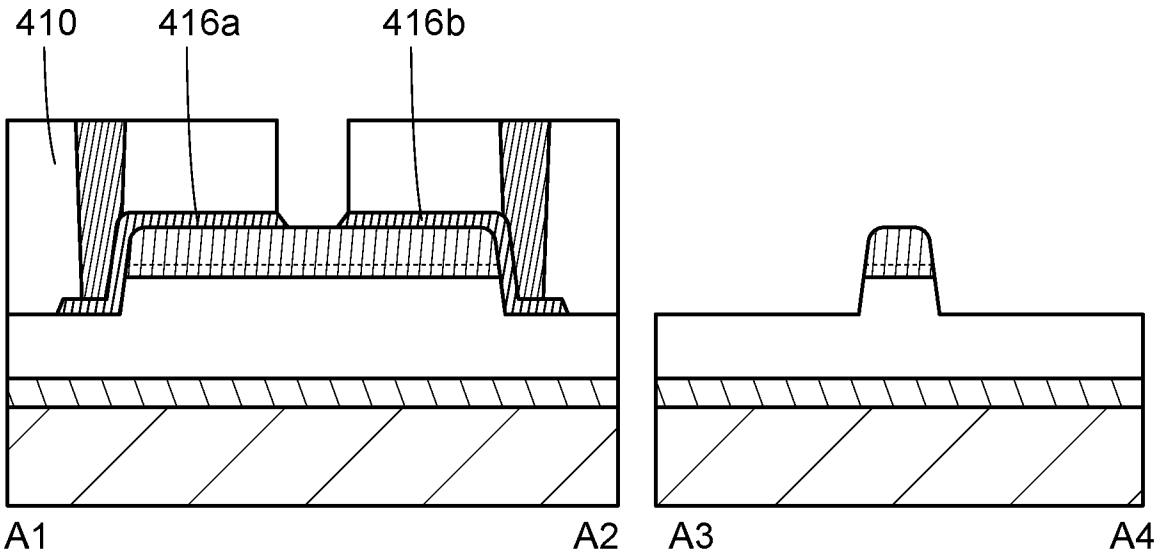


FIG. 8A

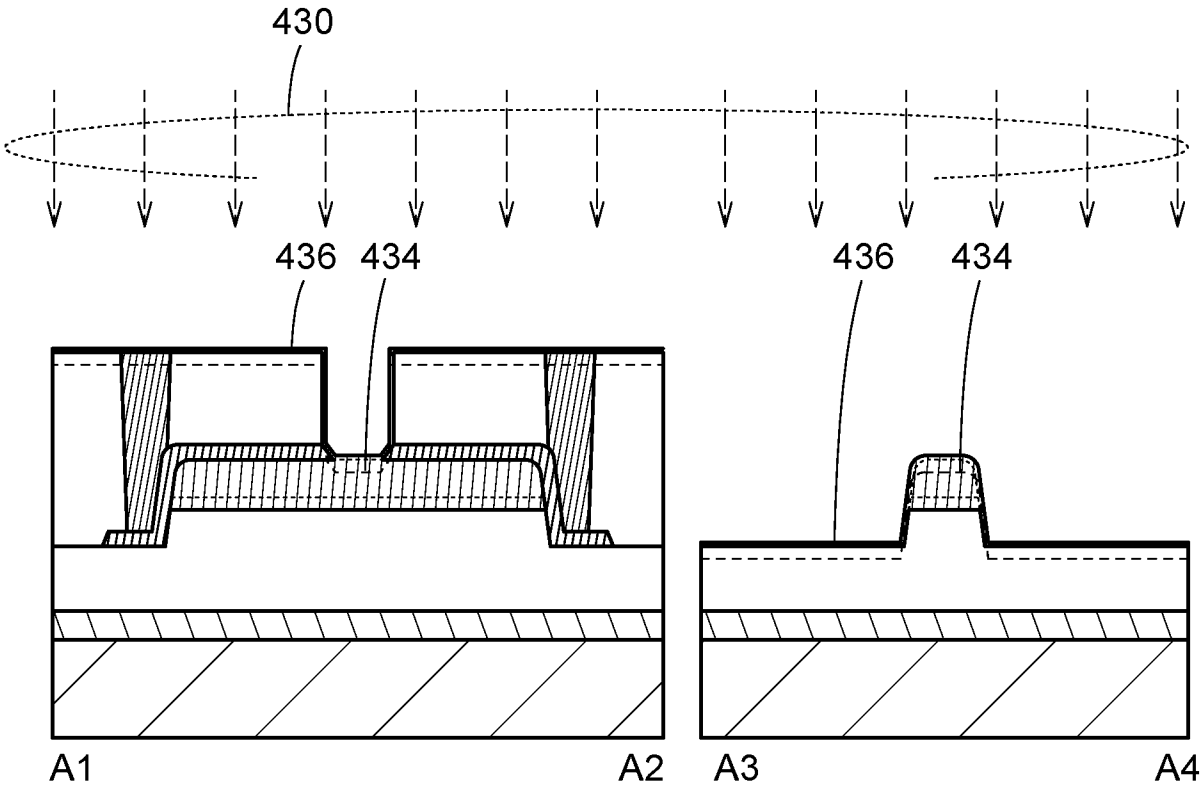

430
436
434
436
434
A1
A2
A3
A4

FIG. 8B

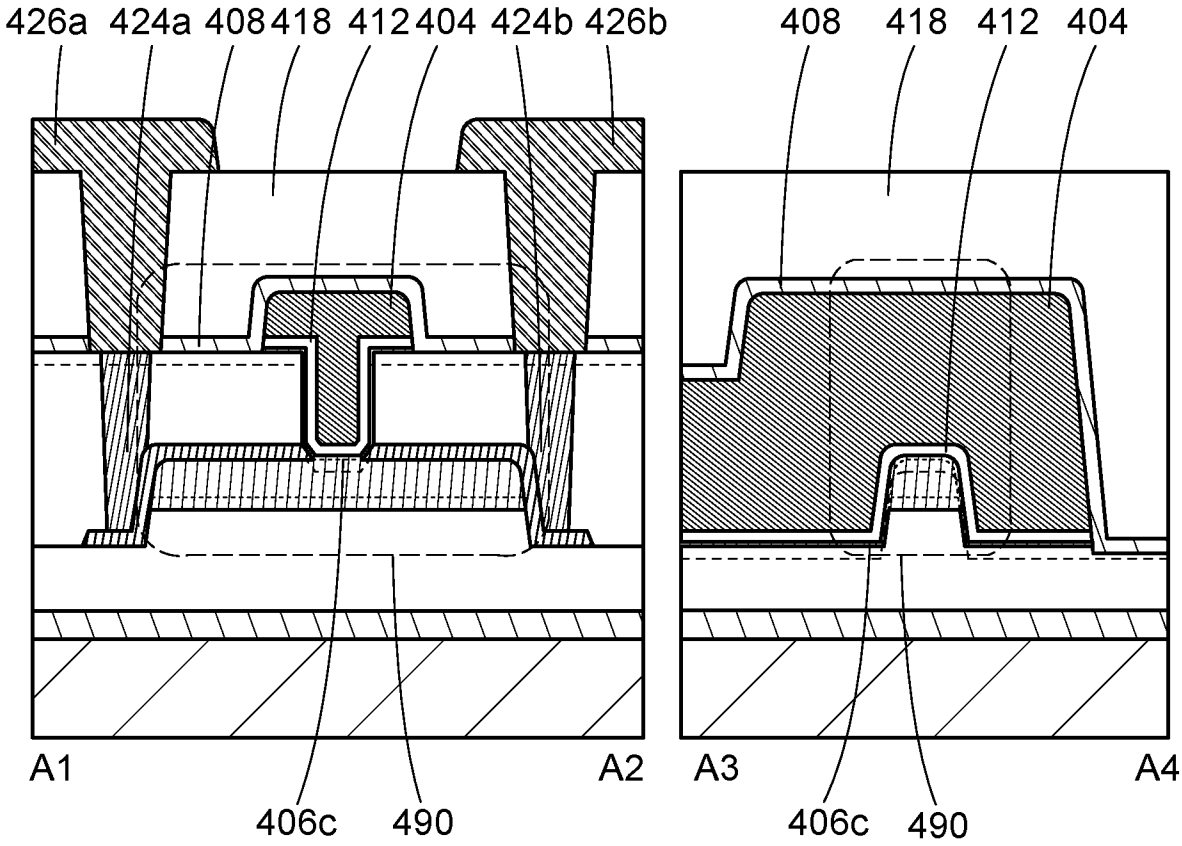

426a
424a
408
418
412
404
424b
426b
408
418
412
404
A1
A2
A3
A4
406c
490
406c
490

FIG. 9A

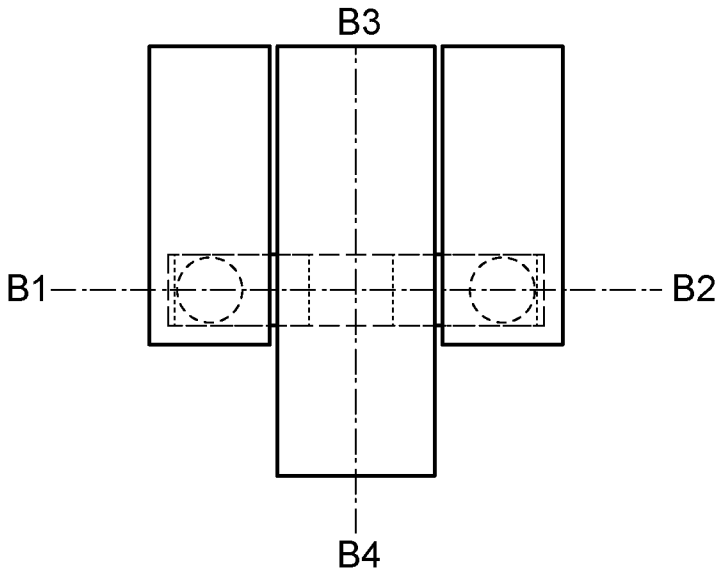

B3
B1
B2
B4

FIG. 9B

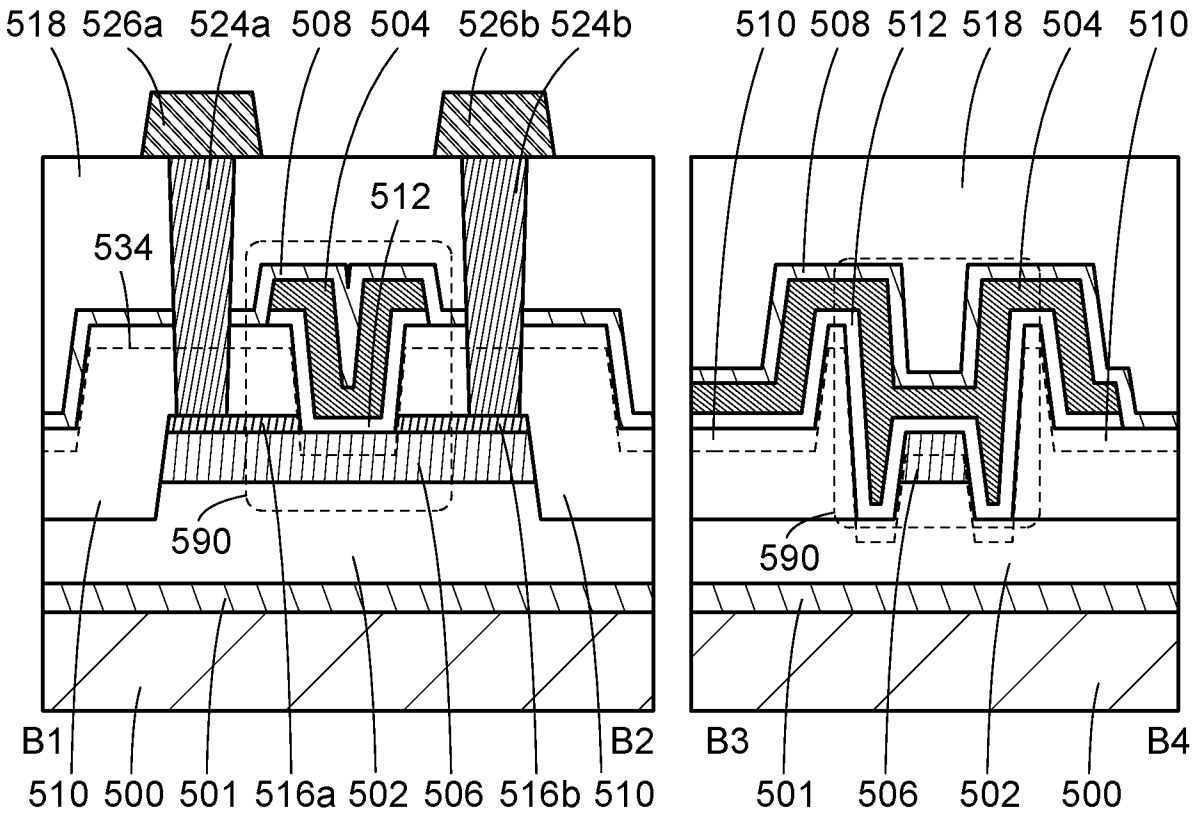

518 526a 524a 508 504 526b 524b
512
534
590
B1
B2
510 500 501 516a 502 506 516b 510
510 508 512 518 504 510
590
B3
B4
501 506 502 500

FIG. 10A

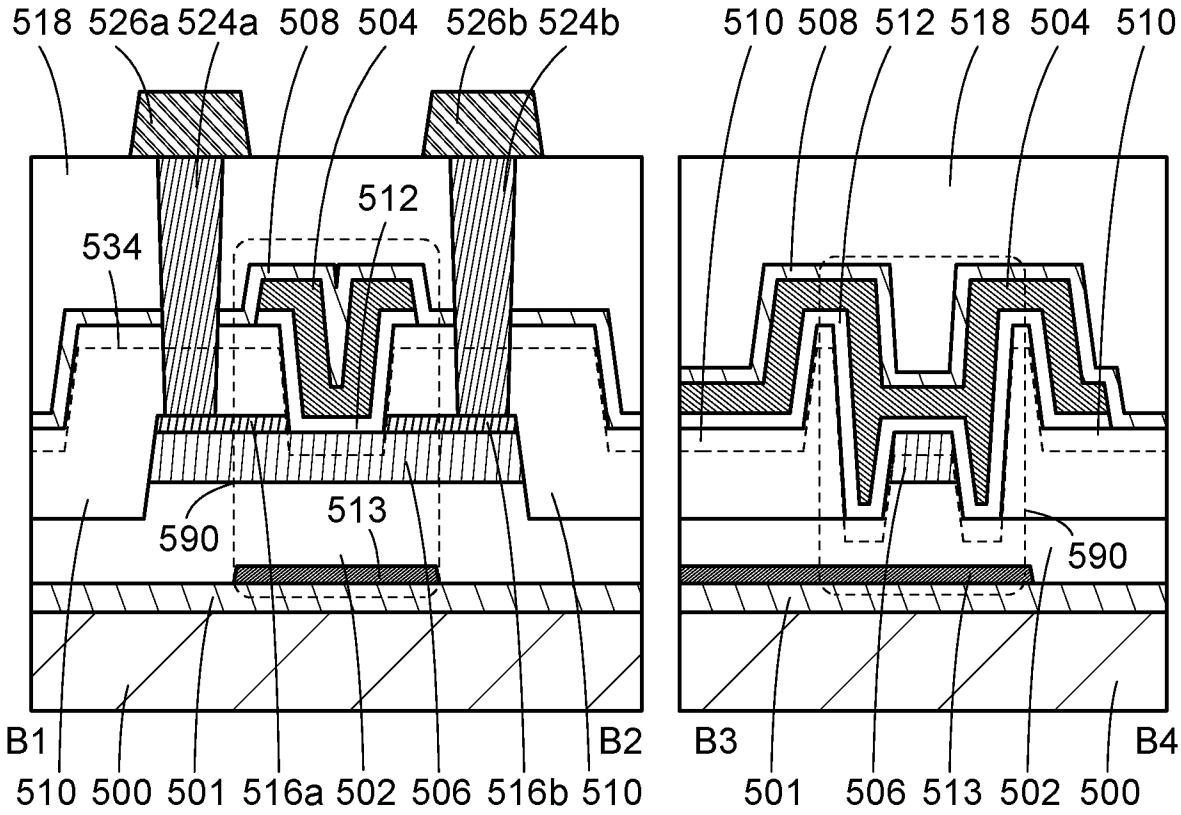


FIG. 10B

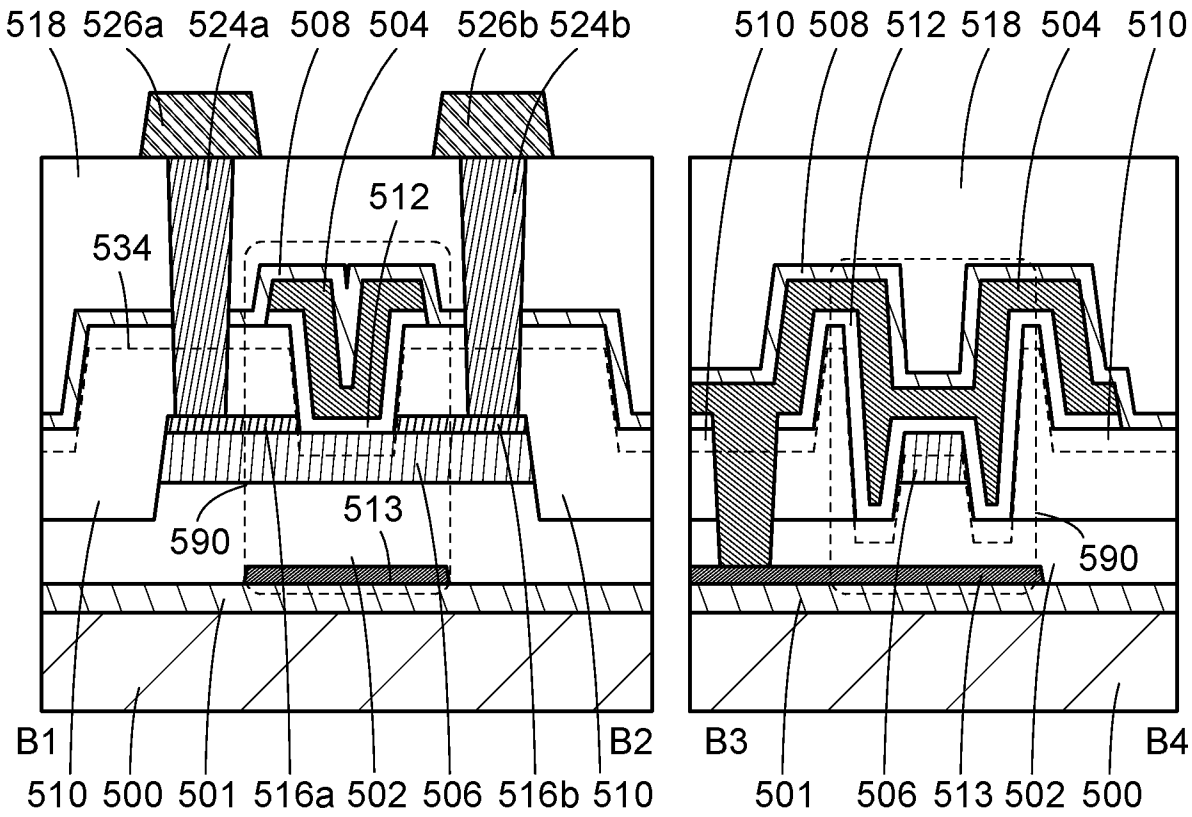


FIG. 11A

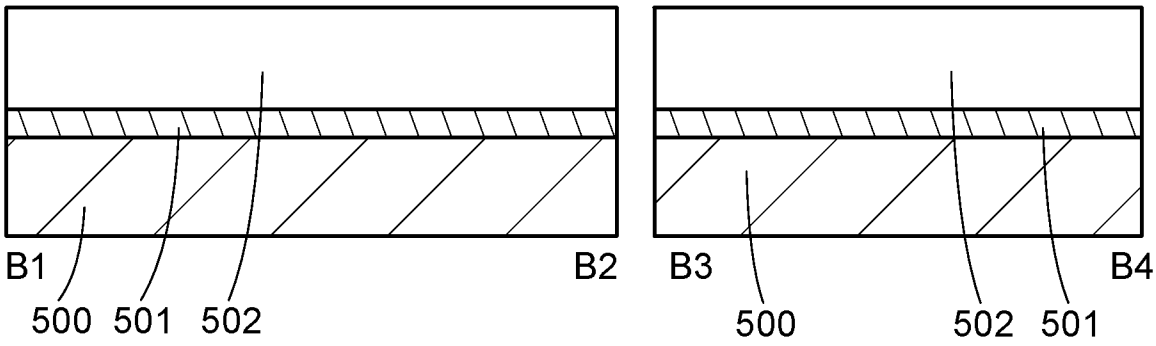


FIG. 11B

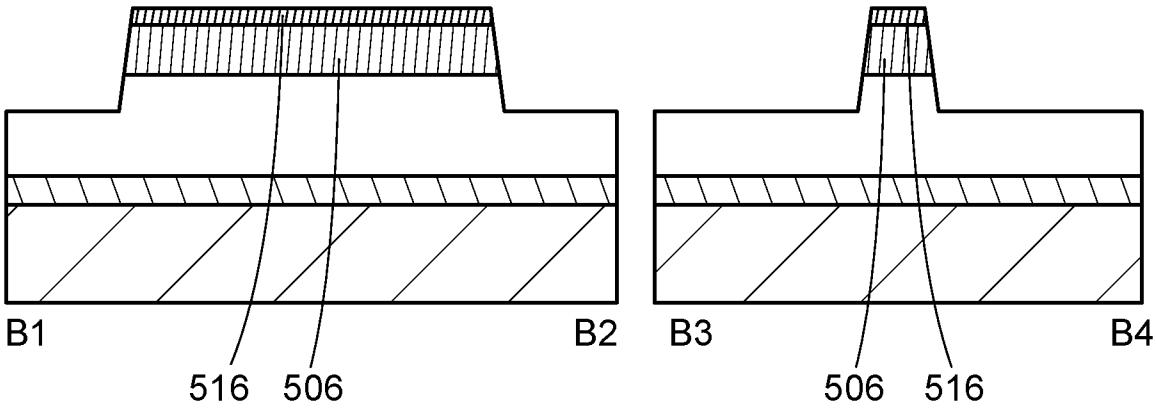


FIG. 12A

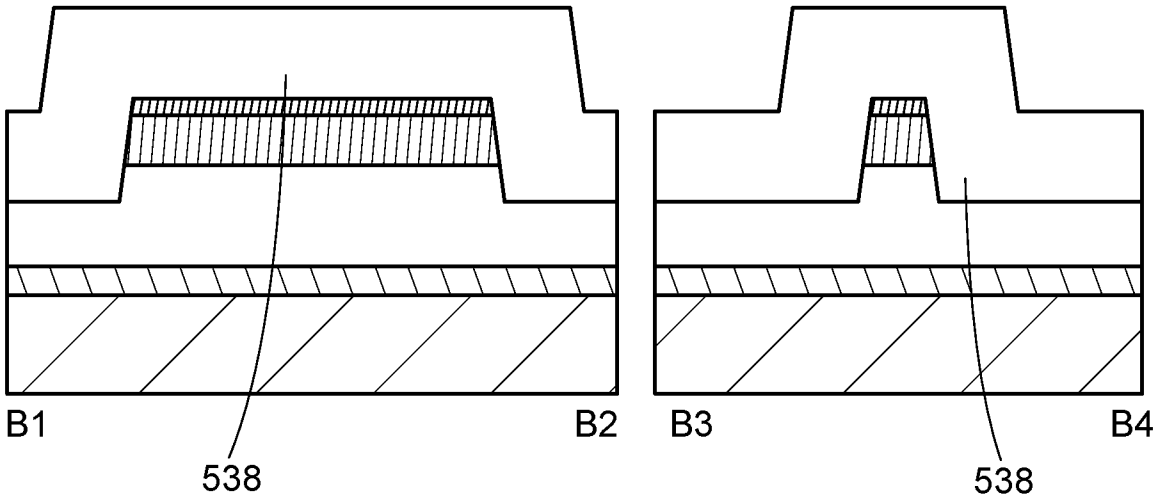


FIG. 12B

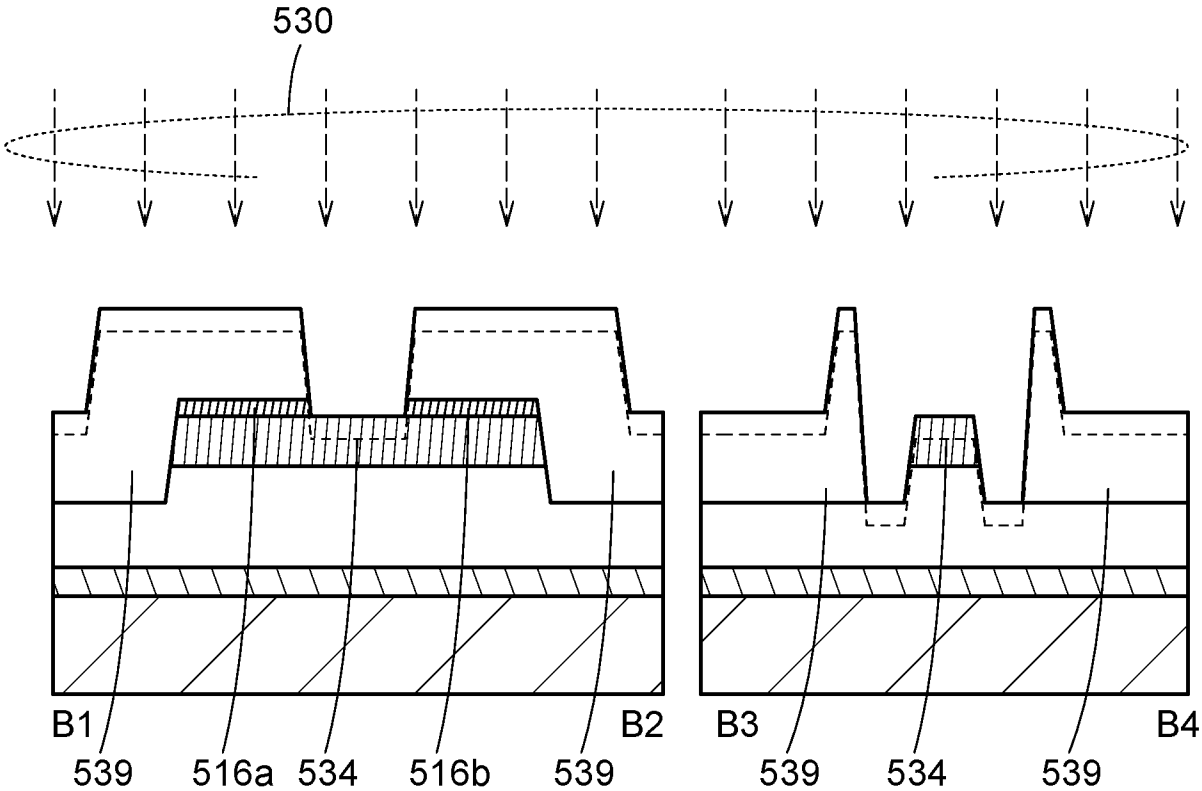


FIG. 13A

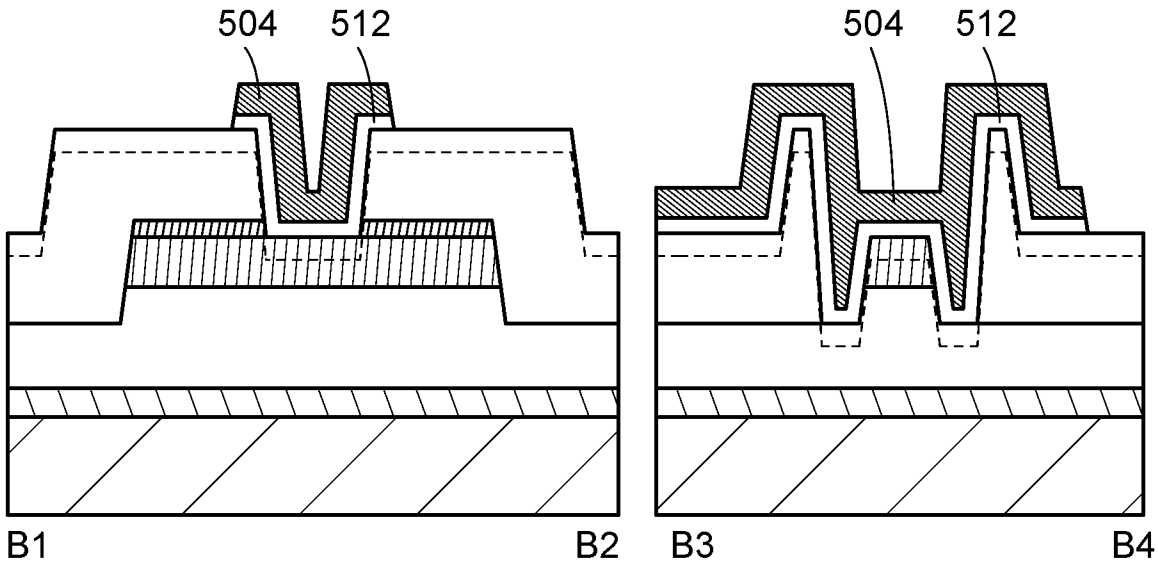


FIG. 13B

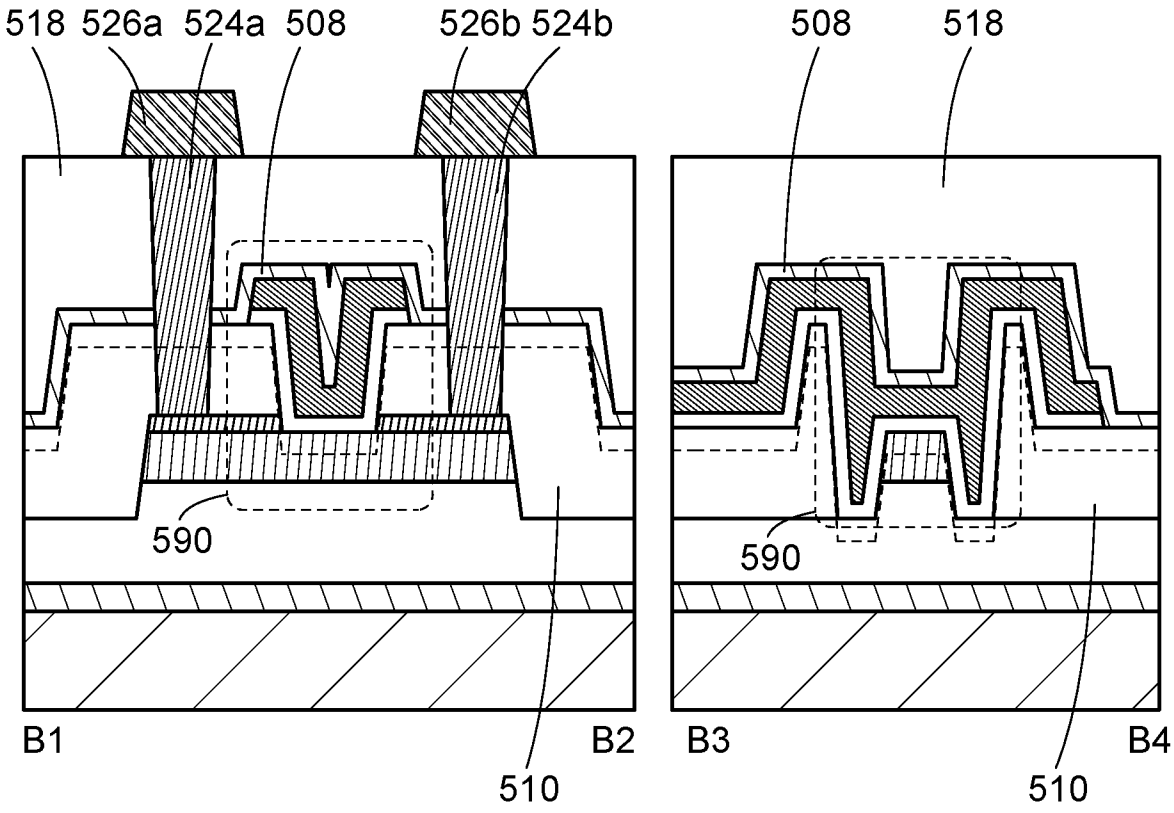


FIG. 14A

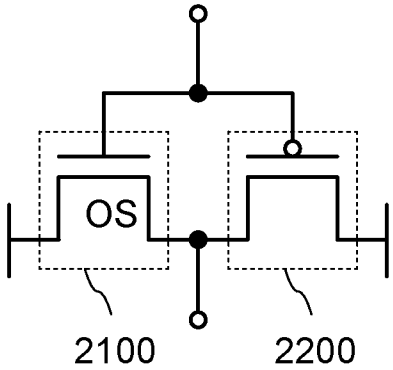


FIG. 14B

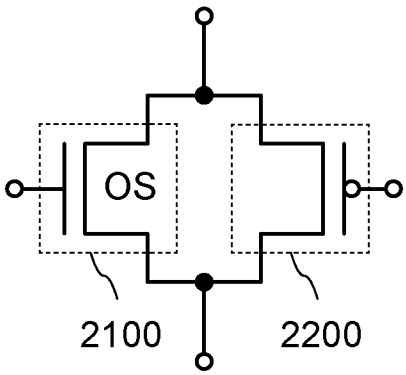


FIG. 15

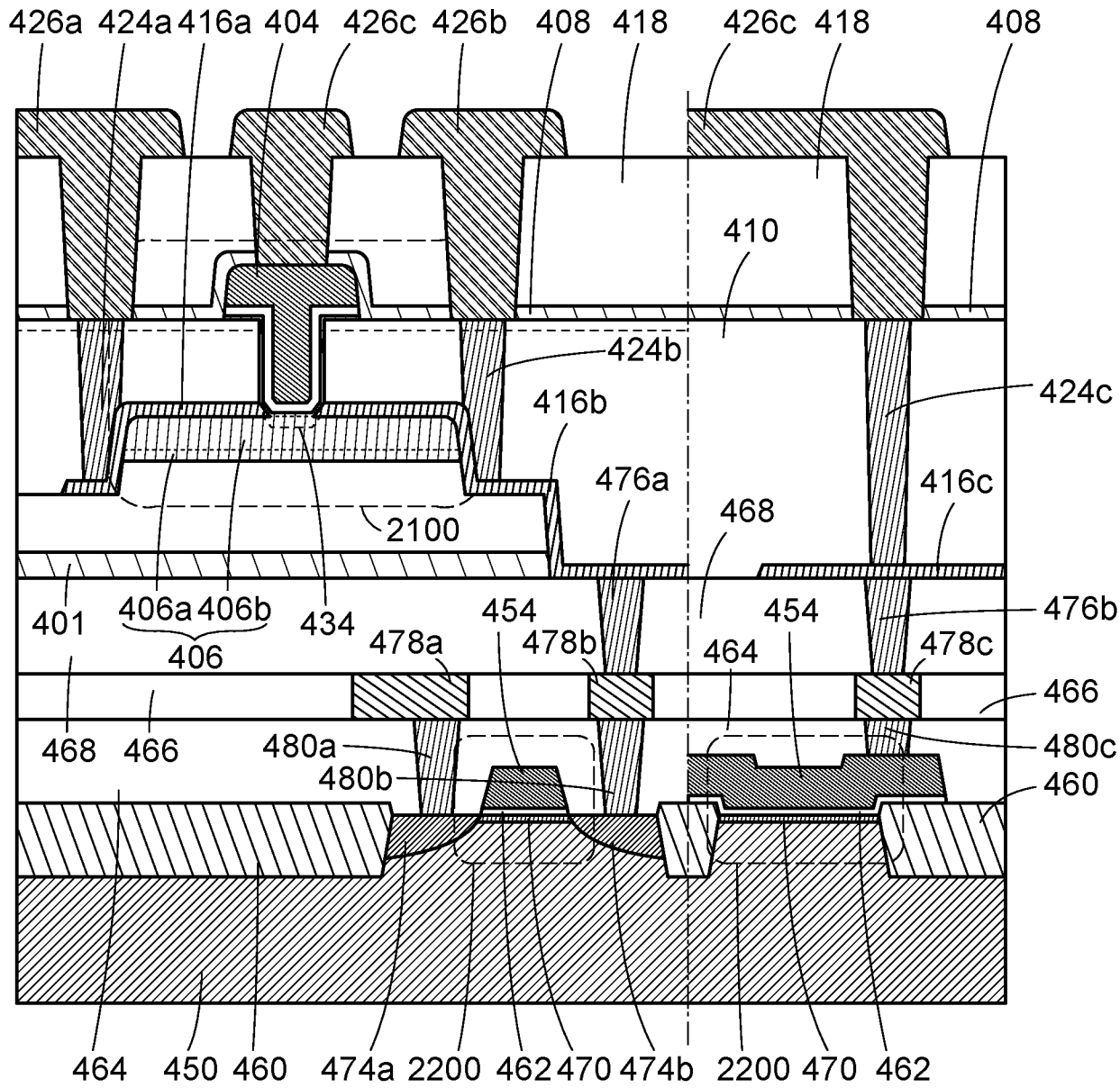

426a
424a
416a
404
426c
426b
408
418
426c
418
408
410
424b
424c
416b
476a
416c
468
2100
401
406a
406b
406
434
454
454
476b
478a
478b
464
478c
466
468
466
480a
480c
480b
460
464
450
460
474a
2200
462
470
474b
2200
470
462

FIG. 16

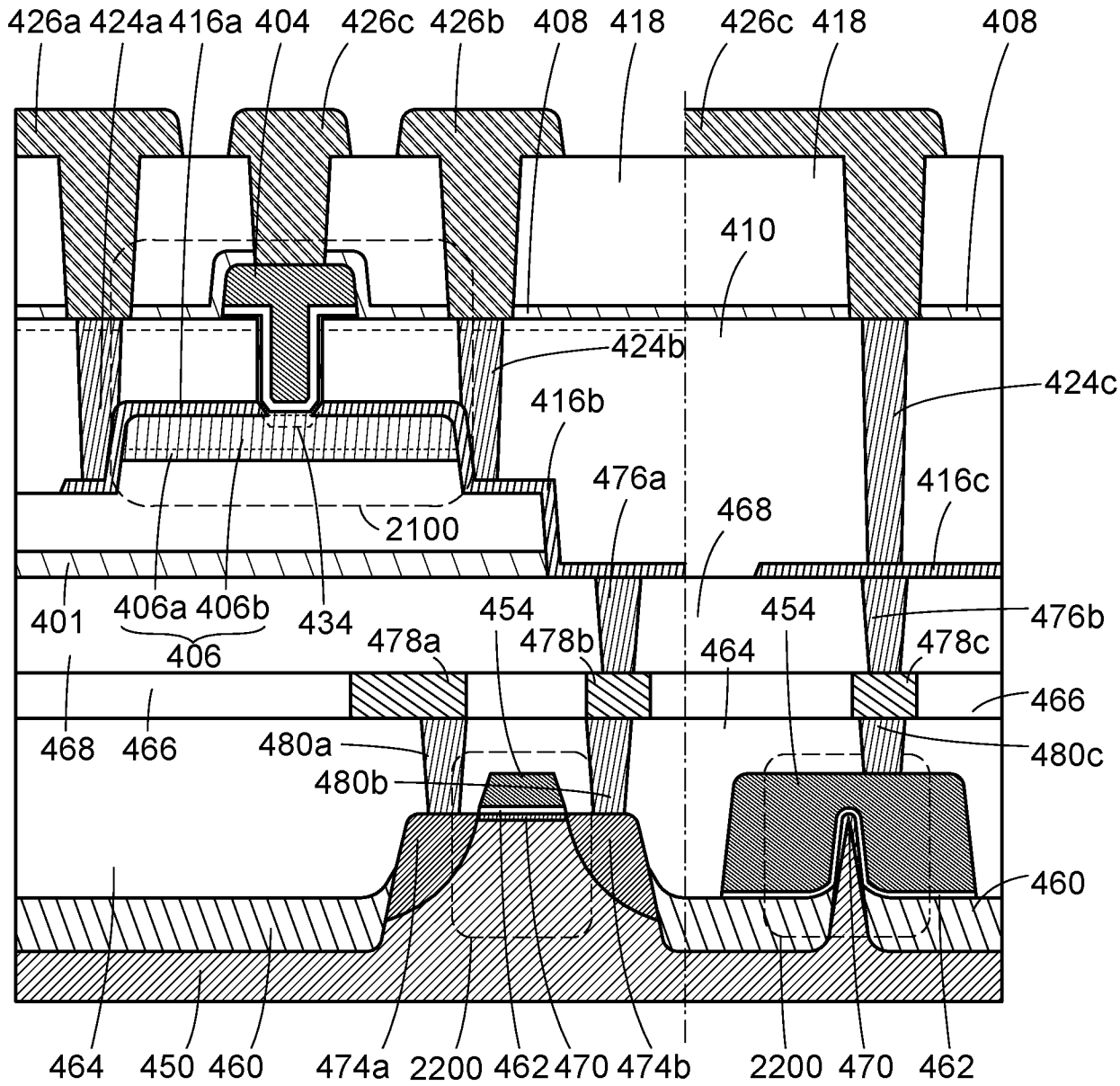

426a
424a
416a
404
426c
426b
408
418
426c
418
408
410
424b
424c
416b
476a
416c
468
2100
401
406a
406b
406
434
454
478a
478b
454
476b
464
478c
466
468
466
480a
480c
480b
460
464
450
460
474a
2200
462
470
474b
2200
470
462

FIG. 17

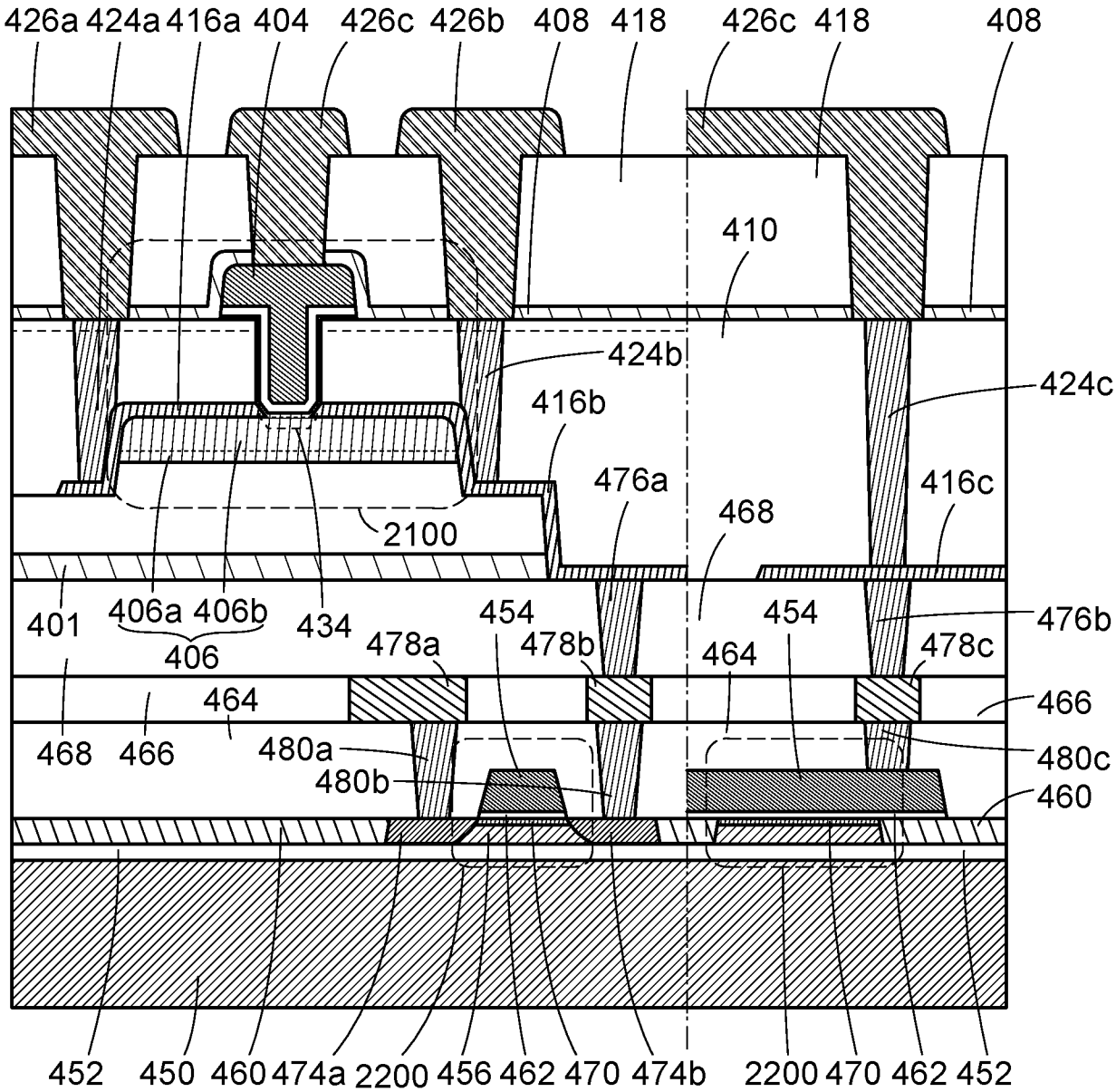

426a
424a
416a
404
426c
426b
408
418
426c
418
408
410
424b
424c
416b
476a
416c
468
2100
401
406a
406b
406
434
454
454
476b
478a
478b
464
478c
464
466
468
466
480a
480c
480b
460
452
450
460
474a
2200
456
462
470
474b
2200
470
462
452

FIG. 18A

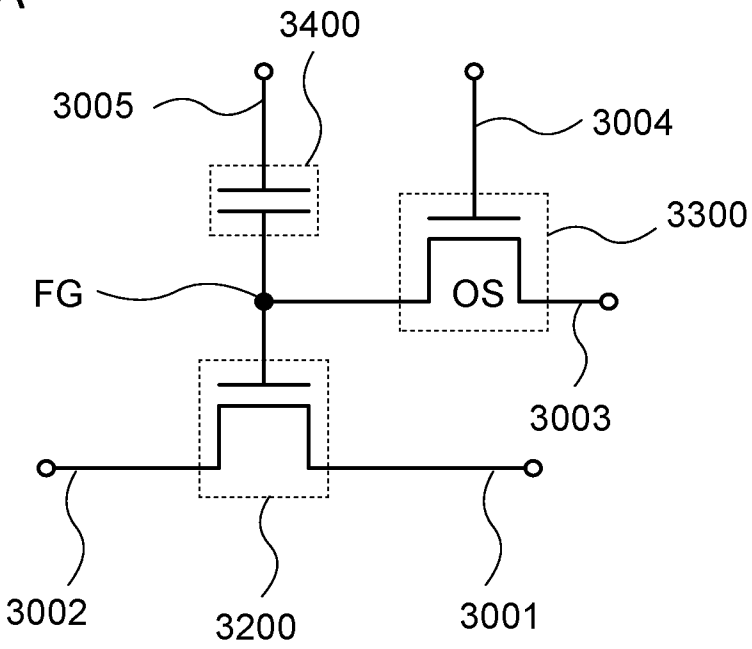


FIG. 18B

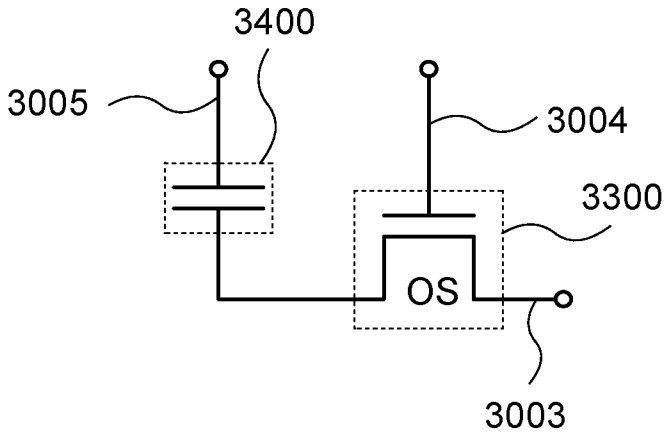


FIG. 19

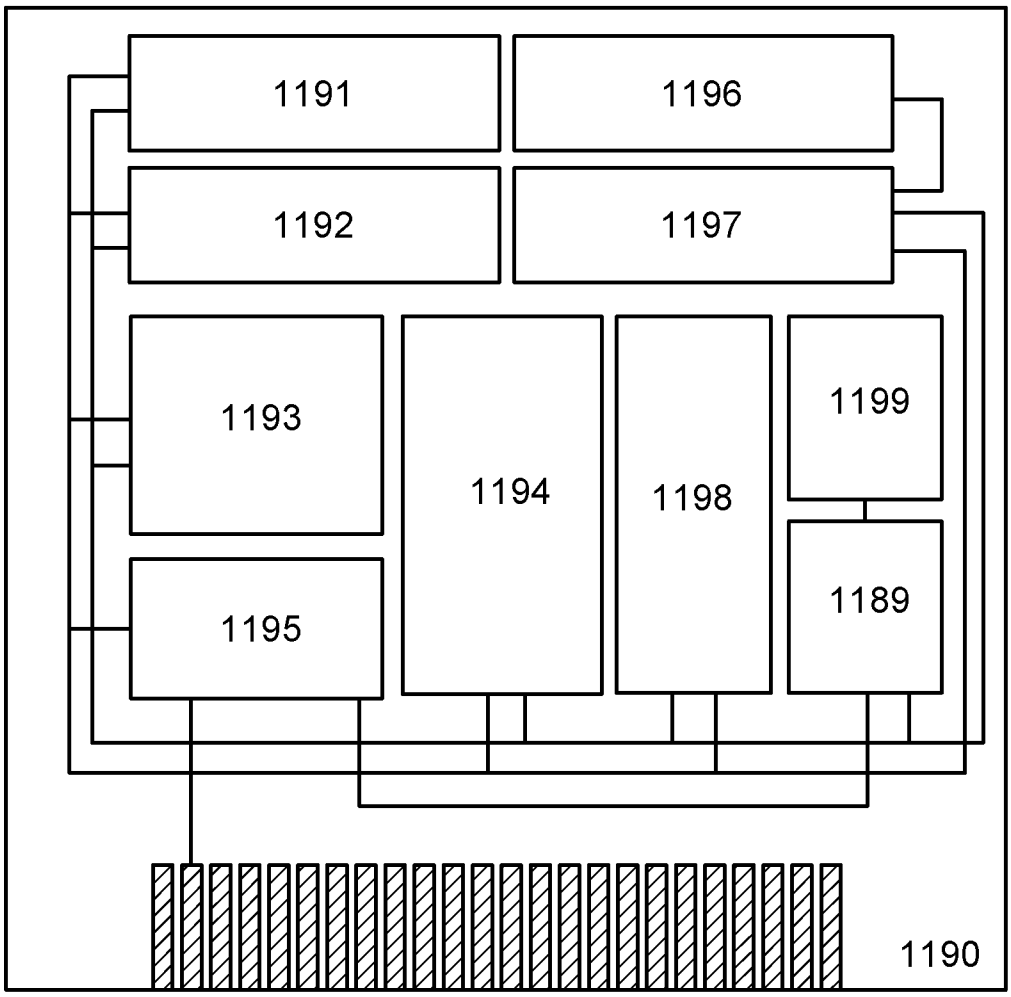


FIG. 20

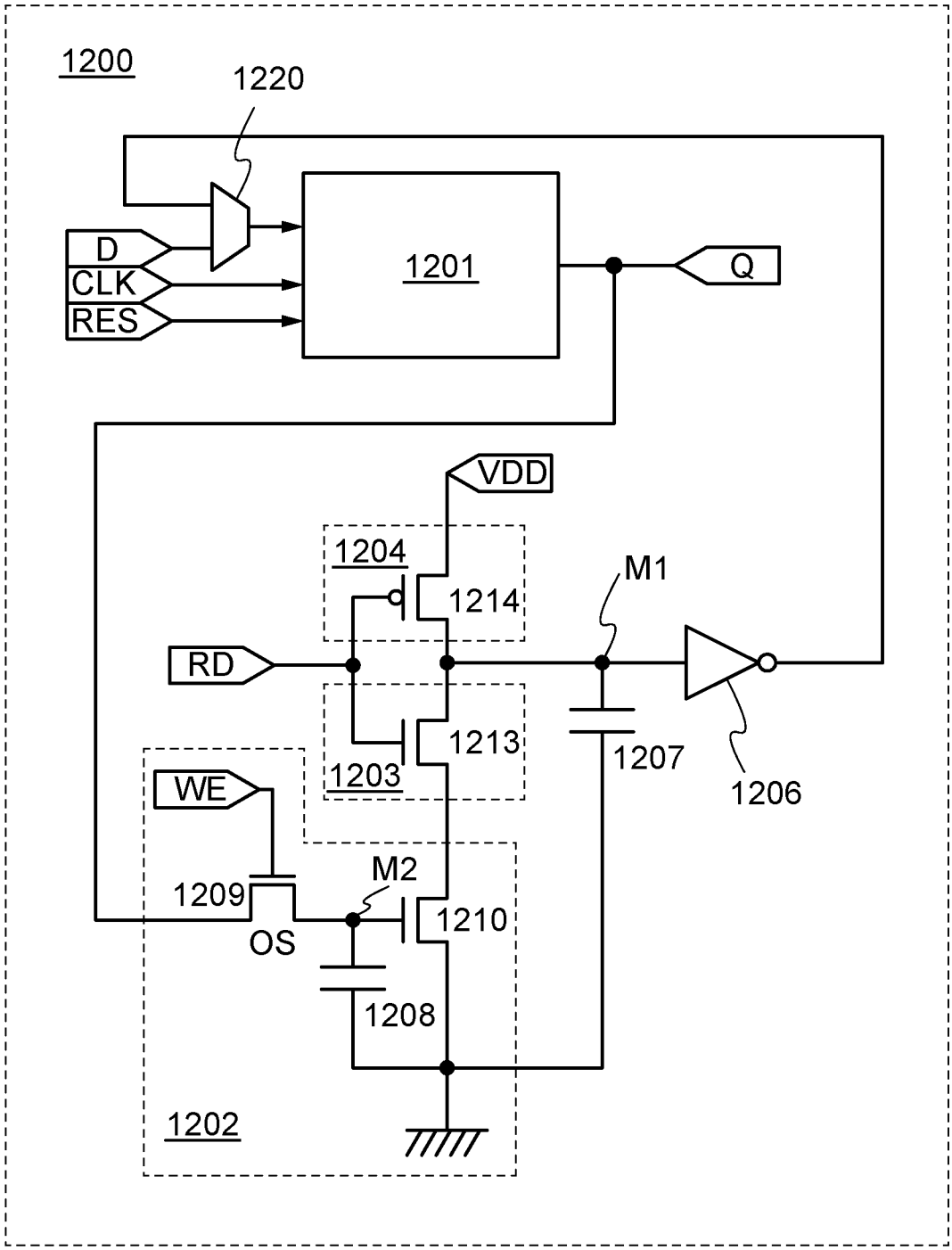

1200
1220
D
CLK
RES
1201
Q
VDD
1204
1214
M1
RD
1213
1203
1207
1206
WE
M2
1209
1210
OS
1208
1202

FIG. 21A

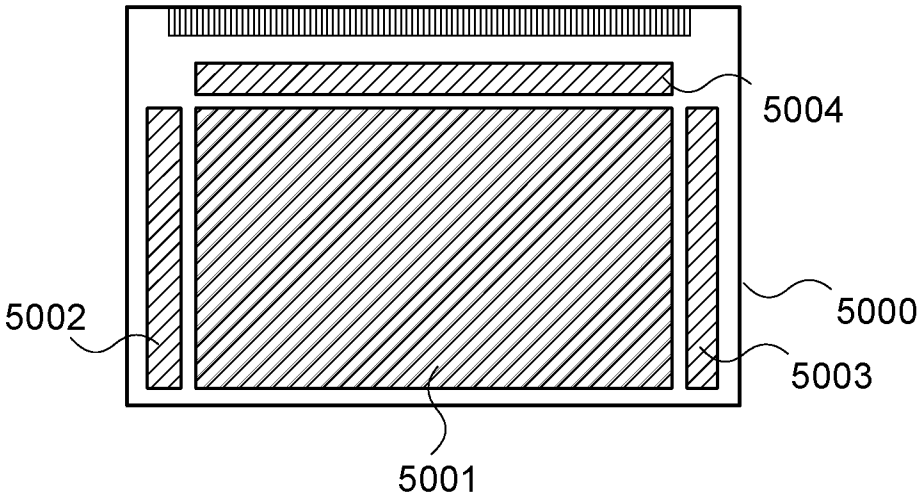


FIG. 21B

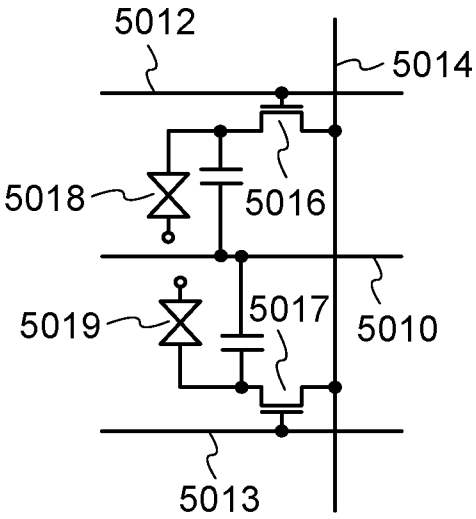


FIG. 21C

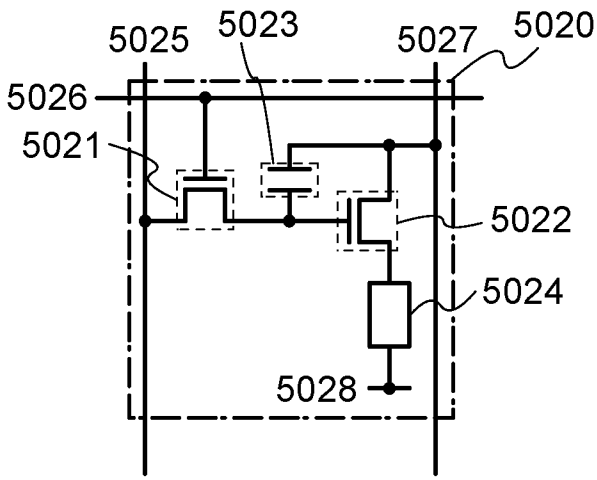


FIG. 22A

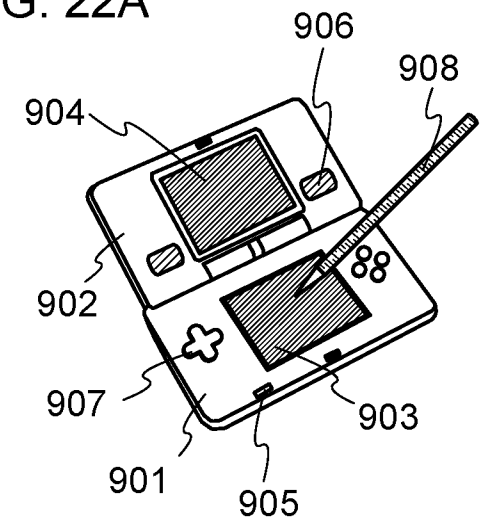


FIG. 22B

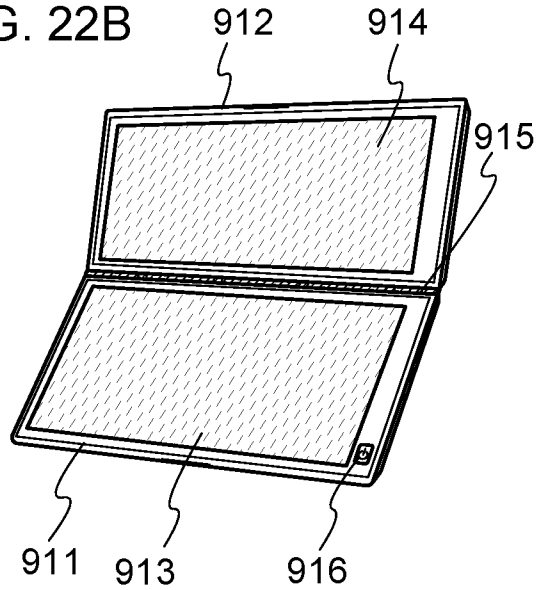


FIG. 22C

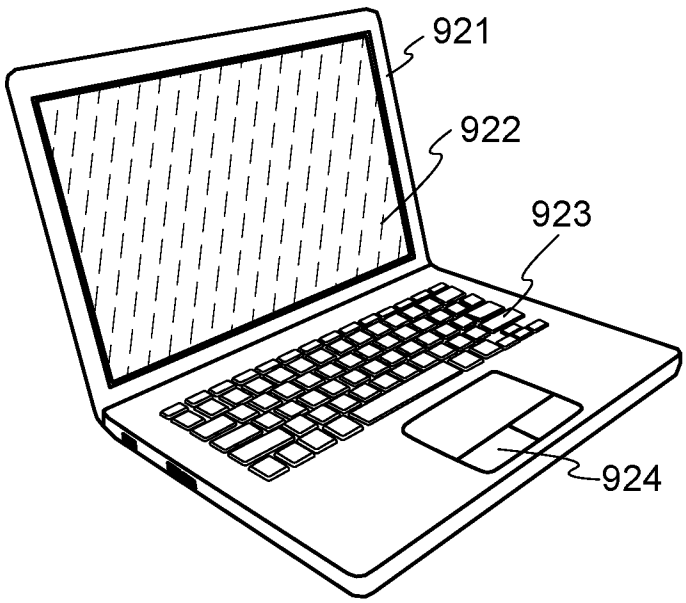


FIG. 22D

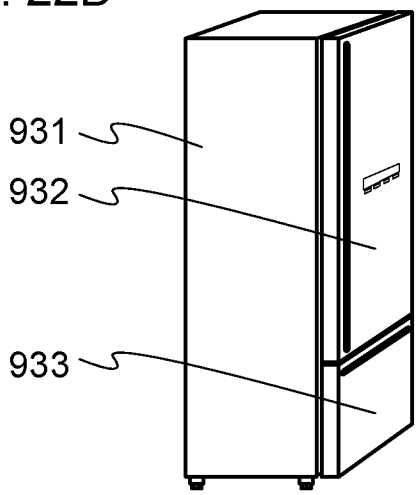


FIG. 22E

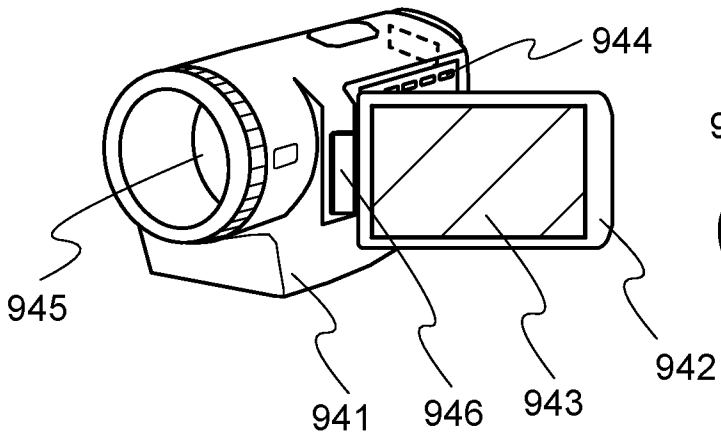


FIG. 22F

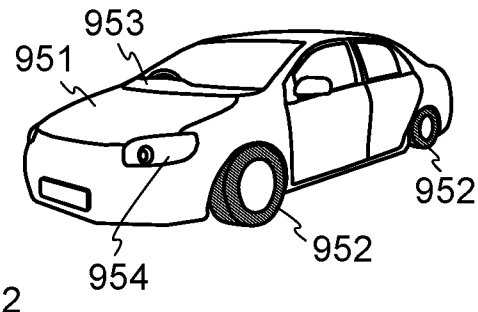


FIG. 23A

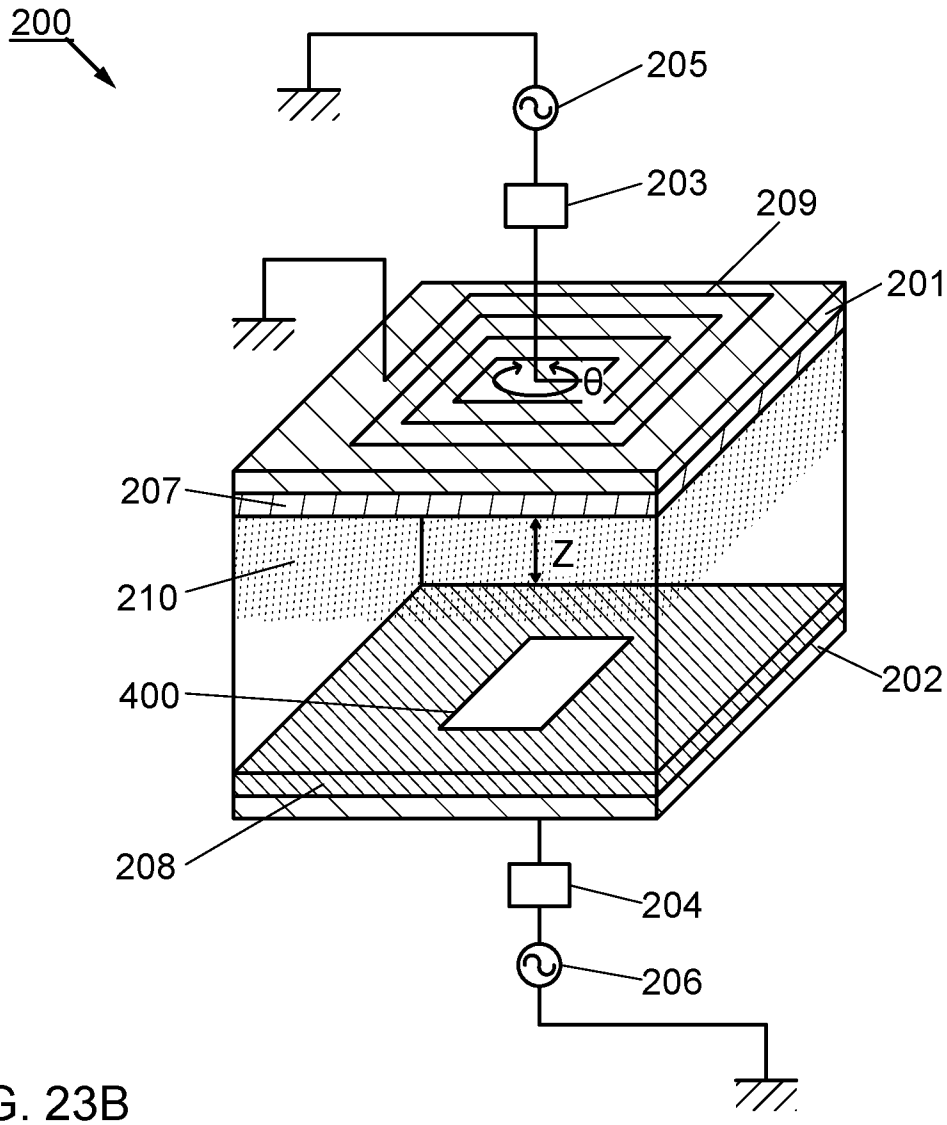
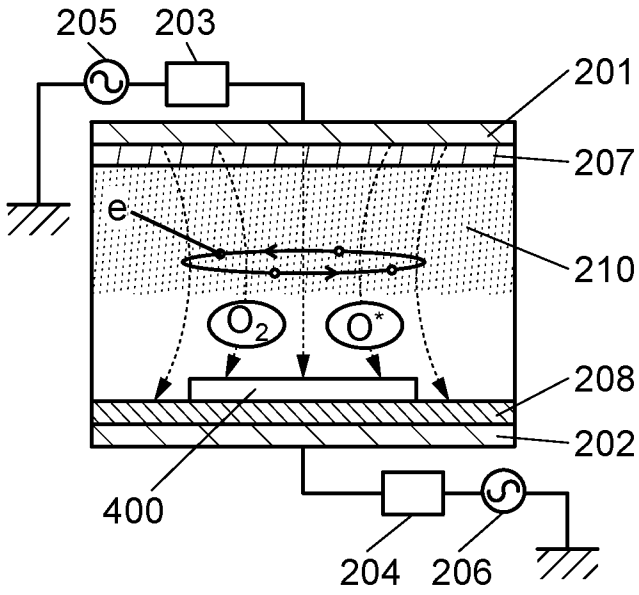


FIG. 23B



INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2015/054367

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, H01L21/336, H01L21/8234, H01L21/8242, H01L21/8247, H01L27/088, H01L27/108, H01L27/115, H01L29/78, H01L29/788, H01L29/792

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2015
Registered utility model specifications of Japan 1996-2015
Published registered utility model applications of Japan 1994-2015

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2014-29994 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2014.02.13, pars. 0144-0174, 0206-0221, figs. 4-6, 8 & US 2014/0004656 A1 & KR 10-2014-0001117 A	1-21
Y	JP 2014-7393 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2014.01.16, pars. 0033-0096, figs. 1-3 & US 2013/0320332 A1	1-21
Y	JP 2012-216776 A (SONY CORPORATION) 2012.11.08, par. 0066, fig. 3 & US 2012/0248544 A1 & CN 102738168 A	3, 10, 17
Y	JP 2008-227165 A (TOSHIBA CORPORATION) 2008.09.25, pars. 0013, 0042 (No Family)	4, 5, 11, 12, 18, 19

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09.09.2015	29.09.2015

Name and mailing address of the ISA/JP	Authorized officer
Japan Patent Office 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	IWAMOTO, Tsutomu 5F 9355 Telephone No. +81-3-3581-1101 Ext. 3516

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2015/054367

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2013-251534 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2013.12.12, pars. 0190-0201, fig. 8 & US 2013/0285050 A1 & KR 10-2013-0122554 A	1-21
A	JP 2014-3280 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2014.01.09, pars. 0175-0183, fig. 8 & US 2013/0277676 A1 & KR 10-2013-0118792 A & TW 201405641 A	1-21
A	JP 2012-54547 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2012.03.15, pars. 0114-0141, figs. 5, 6 & US 2012/0032163 A1 & CN 102376584 A & KR 10-2012-0022614 A & TW 201222734 A	1-21
A	JP 2011-139055 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2011.07.14, pars. 0063-0065, fig. 28(B) & US 2011/0133177 A1 & WO 2011/068028 A1 & TW 201137987 A	1-21

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2015/054367

CLASSIFICATION OF SUBJECT MATTER
H01L29/786(2006.01)i, H01L21/336(2006.01)i, H01L21/8234(2006.01)i,
H01L21/8242(2006.01)i, H01L21/8247(2006.01)i, H01L27/088(2006.01)i,
H01L27/108(2006.01)i, H01L27/115(2006.01)i, H01L29/78(2006.01)i,
H01L29/788(2006.01)i, H01L29/792(2006.01)i