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(54) Title: DEFECT TRANSFERRED AND LATTICE MISMATCHED EPITAXIAL FILM

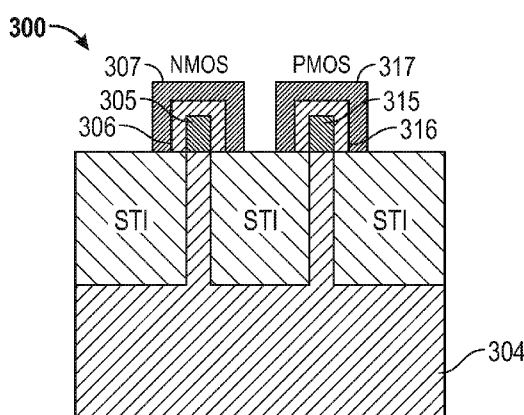


FIG. 3G

(57) Abstract: An embodiment uses a very thin layer nanostructure (e.g., a Si or SiGe fin) as a template to grow a crystalline, non-lattice matched, epitaxial (EPI) layer. In one embodiment the volume ratio between the nanostructure and EPI layer is such that the EPI layer is thicker than the nanostructure. In some embodiments a very thin bridge layer is included between the nanostructure and EPI. An embodiment includes a CMOS device where EPI layers covering fins (or that once covered fins) are oppositely polarized from one another. An embodiment includes a CMOS device where an EPI layer covering a fin (or that once covered a fin) is oppositely polarized from a bridge layer covering a fin (or that once covered a fin). Thus, various embodiments are disclosed from transferring defects from an EPI layer to a nanostructure (that is left present or removed). Other embodiments are described herein.



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Defect Transferred and Lattice Mismatched Epitaxial Film

Background

[0001] A variety of electronic and optoelectronic devices can be enabled by developing, for example, high quality III-V semiconductors on elemental silicon (Si) substrates or IV semiconductors on Si substrates. Surface layers capable of achieving the performance advantages of III-V or IV materials may host a variety of high performance electronic devices such as CMOS and quantum well (QW) transistors fabricated from extremely high mobility materials such as, but not limited to, indium antimonide (InSb), indium arsenide (InAs), germanium (Ge), and silicon germanium (SiGe). Optical devices such as lasers, detectors and photovoltaics may also be fabricated from various other direct band gap materials, such as, but not limited to, gallium arsenide (GaAs) and indium gallium arsenide (InGaAs). These devices can be further enhanced by monolithically integrating them with conventional devices of Si since use of a Si substrate has the additional advantage of cost reduction.

[0002] The growth of III-V and IV materials upon Si substrates, however, presents many challenges. Crystal defects are generated by lattice mismatch, polar-on-nonpolar mismatch, and thermal mismatch between the III-V semiconductor epitaxial (EPI) layer and the Si semiconductor substrate or the IV semiconductor EPI layer and the Si semiconductor substrate. When the lattice mismatch between the EPI layer and substrate exceeds a few percent, the strain induced by the mismatch becomes too large and defects are generated in the EPI layer by relaxing the EPI film. Once the film thickness is greater than the critical thickness (i.e., film is fully strained below this thickness and partially relaxed above this thickness), the strain is relaxed by creating misfit dislocations at the film and substrate interface as well as in the EPI film. The EPI crystal defects may be in the form of threading dislocations, stacking faults and twins. Many defects, particularly threading dislocations and twins, tend to propagate into the "device layer" where the semiconductor device is fabricated. Generally, the severity of defect generation correlates to the amount of lattice mismatch between the III-V semiconductor and the Si substrate or the IV semiconductor and the Si substrate.

Brief Description Of The Drawings

[0003] Features and advantages of embodiments of the present invention will become apparent from the appended claims, the following detailed description of one or more example embodiments, and the corresponding figures, in which:

Figures 1(a)-(f) include an embodiment of the invention comprising a bridge layer and another embodiment where the bridge layer has been removed.

Figures 2(a)-(b) include figures based on transmission electron microscope (TEM) images of fin based (EPI) layer embodiments of the invention.

Figures 3(a)-(g) include a complementary metal–oxide–semiconductor (CMOS) apparatus in an embodiment of the invention.

Figures 4(a)-(g) include a CMOS apparatus in an embodiment of the invention.

Figure 5 includes a method in an embodiment of the invention.

Figure 6 includes a CMOS related method in an embodiment of the invention.

Figure 7 includes a CMOS related method in an embodiment of the invention.

Detailed Description

[0004] In the following description, numerous specific details are set forth but embodiments of the invention may be practiced without these specific details. Well known circuits, structures and techniques have not been shown in detail to avoid obscuring an understanding of this description. “An embodiment”, “various embodiments” and the like indicate embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Some embodiments may have some, all, or none of the features described for other embodiments. “First”, “second”, “third” and the like describe a common object and indicate different instances of like objects are being referred to. Such adjectives do not imply objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner. “Connected” may indicate elements are in direct physical or electrical contact with each other and “coupled” may indicate

elements co-operate or interact with each other, but they may or may not be in direct physical or electrical contact. Also, while similar or same numbers may be used to designate same or similar parts in different figures, doing so does not mean all figures including similar or same numbers constitute a single or same embodiment.

[0005] A conventional technique for lattice mismatched configurations involves deposition of thick buffers (e.g., that are 0.5 or more microns thick) that bridge the lattice constant difference between the substrate and the layers of interest (device layers including III-V materials and the like). In such conventional techniques complicated anneals and compositional grading processes are used to “bend” the defects into each other within the thick buffer so the defects annihilate. Many thick buffer techniques are time consuming, expensive, include undesirable surface roughness of the buffer, and the minimum defect density still remains high.

[0006] Another conventional technique includes Aspect Ratio Trapping (ART). ART is based on threading dislocations that propagate upwards at a specific angle. In ART a trench is made with a high enough aspect ratio such that the defects terminate on the sidewall of the trench and any layer above the terminations is defect free.

[0007] An embodiment differs from the conventional methods described above. For example, an embodiment uses a very thin layer nanostructure (e.g., a Si or SiGe nanostructure) as a template to grow a crystalline, non-lattice matched, EPI layer. The volume ratio between the nanostructure/EPI layers is the opposite of more conventional methods of including, for example, a thick substrate with a thin planar EPI layer. This may transfer strain, and possibly defects, from the EPI layer (often seen with conventional methods) to the underlying nanostructure. In other words, in some embodiments (but not all embodiments) the EPI layer is thicker than the underlying structure (e.g., fin).

[0008] One embodiment may include silicon on insulator (SOI) where the silicon over the insulator is very thin in relation to the EPI layer. However, in another embodiment no SOI is used. Instead (or in addition to SOI), an embodiment compatible with modern manufacturing processes utilizes a generally “vertical” fin

that reaches towards the horizontal substrate (i.e., has a long axis orthogonal to horizontal substrate). In addition to ease of manufacturing, the fin based embodiment also allows for EPI deposition on both sides of the fin. The growth on both sides of the fin allows half the EPI to grow on each side of the fin to collectively (between EPI grown on multiple fin walls) achieve a higher volumetric advantage (i.e., high volume of EPI to lower volume of fin material).

[0009] Figures 1(a)-(f) include an embodiment of the invention comprising a bridge layer (as well as optional embodiments where a bridge layer is removed). Figure 5 includes a method in an embodiment of the invention. Figures 1(a)-(f) and 5 are discussed below.

[0010] In block 505 fin 105 is formed (Figure 1(a)). Fin 105 couples, directly or indirectly, to substrate 104. In one embodiment fin 105 may be adjacent shallow trench isolation (STI) portions but such insulation portions are not included in other embodiments. In block 510 bridge layer 106 is formed over fin 105 (Figure 1(b)). This optional step may be desirable when an EPI layer (e.g., III-V or IV material) cannot be grown directly on fin 105 (e.g., Si or SiGe fin). Bridge layer 106 may change the lattice constant of fin 105 by, for example, driving defects into the fin. A bridge layer differs from thick buffer layers due to, for example, the thickness of the bridge layer (e.g., less than 30-40 nm) versus a conventional buffer (e.g., greater than 0.5 microns). As an option, in one embodiment in block 515 (shown in dash to indicate its optional nature) fin 105 and bridge layer 106 are annealed to close or remove any lattice mismatch between fin 105 and bridge layer 106 (Figure 1(c)). In block 520 (Figure 1(d)) EPI layer 107 is formed over bridge layer 106 (or directly over fin 105 if no bridge layer is used). EPI layer 107 may serve as channel material including, for example, a IV or III-V material such as Ge, SiGe, GaAs, AlGaAs, InGaAs, InAs, and InSb.

[0011] Figures 2(a)-(b) include figures based on transmission electron microscope (TEM) images of fin based (EPI) layer embodiments of the invention. Figure 2(a) includes InAs EPI film 207 on Si fin 205 with an 11% lattice mismatch between the two. EPI 207 is nearly defect free. No bridge layer is present in Figure 2(a).

[0012] Figure 2(b) includes a Ge EPI layer 207 (left portion denoted 207L and right portion denoted 207R, collectively referred to as element 207) on Si fin 205. EPI 207 may not be entirely defect free but includes significantly fewer defects than is the case when Ge is grown directly on planar Si. The Si fin is strained near its top at its interface with Ge EPI 207. No bridge layer is present in Figure 2(b). In both Figures 2(a) and (b) fin 205 is so small the EPI layer 207 is larger (or similar in width) than the fin (or portions of the fin) and the Si fin is strained. In Figure 2(b) the “left” EPI wall 207(L) and the “right” EPI wall 207(R) are divided by the fin long axis/vertical axis 230. Horizontal plane 231 is orthogonal to axis 230 and intersects fin 205 and sidewalls of 207(L) and 207(R). The surface area of fin 205 along plane 231 is less than the collective total surface area of walls 207(L) and 207(R) along the same plane. However, in other embodiments this is not necessarily the case (e.g., Figure 2(a) shows the EPI layer much thinner in relation to the fin). In some embodiments a higher volumetric ratio of EPI/fin may drive defects and strain from the EPI layer into the fin.

[0013] At this point, the wafers can be sent through conventional processing techniques to form, for example, transistors. However, in other embodiments the fin may be removed. If the fin is strained and starting to form defects the defects may form a leakage path that will degrade device performance. Such a fin may be removed to lessen the leakage current. Also, regardless of the defect quality of the silicon, leaving the fin in may worsen electrostatics and thus a fin may be removed where electrostatics are a concern.

[0014] Regarding fin removal, in Figure 5 block 525 STI can be deposited to a height of the top of the fin or higher and then polished down through the top of fin 105 (Figure 1(e)). This exposes fin 105 and bridge layer 106 so portions of the fin and/or bridging layer can be removed via, for example, wet etch (block 530). This will leave 2 epitaxial portions 107 on the STI in the embodiment of Figure 1(f). The remaining portions may be equidistant from the trench that previously included the fin. In other words, distance 110 may generally equal distance 111. Processing may then resume.

[0015] Figures 3(a)-(g) include a CMOS apparatus in an embodiment of the invention. Figure 6 includes a CMOS related method in an embodiment of the invention. Figures 3(a)-(g) and Figure 6 are discussed below.

[0016] An embodiment includes a CMOS apparatus. For example, where there is an EPI deposition step, an oxide hardmask can be deposited and used to determine which polarity EPI is deposited. In block 605 fins 305, 315 are formed (Figure 3(a)). Fins 305, 315 couple, directly or indirectly, to substrate 304. In one embodiment fins 305, 315 may be adjacent STI portions but such insulation portions are not included in other embodiments. In block 610 bridge layers 306, 316 are formed over fins 305, 315 (Figure 3(b)). This optional step may be desirable when an EPI layer (e.g., III-V or IV material) cannot be grown directly on fins 305, 315 (e.g., Si or SiGe fin). Bridge layers 306, 316 may change the lattice constant of fins 305, 315 by, for example, driving defects into the fins. As an option, in one embodiment in block 615 (shown in dash to indicate its optional nature) fins 305, 315 and bridge layers 306, 316 are annealed to lessen or remove any lattice mismatch between the fins and bridge layers (Figure 3(c)). In block 620 oxide is deposited on layers 306, 316 and then a lithography step is performed to pattern photoresist. The photoresist is used to remove the oxide from layer 306 to produce the embodiment of Figure 3(d) with oxide 320 over layer 316. EPI 307 can be formed (Figure 3(e)) and then in block 625 the hard mask is removed and the process is repeated for fin 305, bridge layer 306, EPI 307 so EPI 317 may be formed (Figure 3(f)). EPI 307 may be of opposite polarity to EPI 317 to generate a CMOS device (Figure 3(g)).

[0017] Figures 4(a)-(g) include a CMOS apparatus in an embodiment of the invention. Figure 7 includes a CMOS related method in an embodiment of the invention. Figures 4(a)-(g) and Figure 7 are discussed below.

[0018] In this embodiment instead of depositing two EPI layers of differing polarity to construct a CMOS device (e.g., Figures 3(a)-(g)), a bridging layer is used as the opposite polarity/channel of another oppositely doped bridge layer or EPI layer. In block 705 fins 405, 415, bridge layers 406, 416, and EPI layers 407, 417 are provided (Figure 4(a)) and may be formed as described above. In block 710 STI may be added to reach fin height or above and then fins 405, 415 are revealed (e.g., via

etching) as shown in Figure 4(b). In block 715 the process deposits mask 420 (e.g., photoresist may be used in one embodiment but other embodiments are not so limited and may include oxide and the like) over fin 415/bridge layer 416/EPI layer 417 (Figure 4(c)) to etch out bridge layer 406 and fin 405 (Figure 4(d)) leaving EPI 407, which may serve as a first channel material ("channel1") that may be doped. In block 720 mask 420 is located over EPI 407 (channel1, as shown in Figure 4(d)) and EPI 417 and Si 415 are etched out (Figure 4(f) with oxide, insulator, and/or metal and the like replacing former area occupied by EPI 417) to reveal a CMOS device (Figure 4(g)) where EPI 407 (channel1) is of opposite polarity to bridge layer 416 ("channel2"). In this embodiment the bridging layer is the channel material for one device and an EPI layer is the channel material for another device. In an embodiment two oppositely doped bridge layers could be used to form a CMOS device. In an embodiment two oppositely doped EPI layers could be used to form a CMOS device. In an embodiment, the doped channel may couple to a source (e.g., not shown but in the foreground of Figure 4(g) located on or in another portion of fin 405) and a drain (e.g., not shown but in the background of Figure 4(g) located on or in another portion of fin 405).

[0019] Thus, various embodiments are described above. For example, in one embodiment the fin is left intact so that EPI is on top of the fin and the fin is strained. In the case where the fin is etched out there may still be remaining fin portions for the source/drain regions. In another embodiment, EPI and/or bridge layer side walls may be located equidistant from the fin or where the fin used to be. In various embodiments defects are significantly reduced as compared to forming EPI over a planar substrate or a thick fin.

[0020] An embodiment includes an apparatus comprising: a fin structure including a fin top and opposing fin sidewall portions extending from the fin top towards a substrate; a bridge layer including opposing bridge layer sidewall portions respectively directly contacting the opposing fin sidewall portions; and an EPI layer comprising opposing EPI sidewall portions respectively directly contacting the opposing bridge layer sidewall portions; wherein a lattice constant mismatch between the bridge layer and fin structure is less than a lattice constant mismatch

between the bridge layer and EPI layer. In some embodiments the fin reaches the substrate but not so in other embodiments. In some embodiments no bridge layer is used. In some embodiments the lattice constants for the EPI layer, bridge layer, and fin are all the same due to annealing or without annealing. However, in other embodiments the lattice constants for each/some of the EPI layer, bridge layer, and fin are different.

[0021] In an embodiment the EPI layer comprises an EPI material including one of a IV and a III-V material, the fin structure includes a fin structure material including silicon (e.g., SiGe), and the bridge layer includes a bridge layer material unequal to either of the fin structure material and the EPI material. For example, the fin may include $\text{Si}_x\text{Ge}_{1-x}$ and the bridge layer may include $\text{Si}_y\text{Ge}_{1-y}$ where x is unequal to y .

[0022] An embodiment includes an apparatus comprising: a fin structure including a fin top and opposing fin sidewall portions extending from the fin top towards a substrate; a bridge layer including opposing bridge layer sidewall portions respectively directly contacting the opposing fin sidewall portions; and an epitaxial (EPI) layer comprising opposing EPI sidewall portions respectively directly contacting the opposing bridge layer sidewall portions; wherein a lattice constant differential between the bridge layer and fin structure is less than a lattice constant differential between the bridge layer and the EPI layer. In an embodiment the EPI layer comprises an EPI material including one of a group IV material and a group III-V material, the fin structure includes a fin structure material including silicon, and the bridge layer includes a bridge layer material unequal to either of the fin structure material and the EPI material. In an embodiment the EPI layer is included in a channel of a transistor and couples to a source and a drain of the transistor. In an embodiment the substrate does not include a silicon on insulator (SOI) configuration. In an embodiment the EPI layer is included in a channel of a transistor and couples to a source and a drain of the transistor, the source and drain both directly contacting the fin structure. In an embodiment the fin includes a concentration of strain adjacent the fin top. In an embodiment the EPI layer lacks defects along the entire border between the EPI layer and the bridge layer. In an embodiment a single plane, orthogonal to a long vertical axis of the fin, intersects the fin over a first area and the

EPI sidewalls over a second area and the second area is greater than the first area. In an embodiment the fin is monolithic with the substrate and the EPI layer sidewall portions are monolithic with one another. An embodiment comprises: an additional fin structure, adjacent the fin structure, including the first lattice constant and opposing additional fin sidewall portions extending from the fin top to a substrate; and an additional bridge layer including the first lattice constant and opposing additional bridge layer sidewall portions respectively directly contacting the opposing additional fin sidewall portions; wherein the EPI layer has a first polarity, the additional bridge layer has second polarity opposite the first polarity, and the EPI layer and the additional bridge layer are included in a CMOS device. An embodiment comprises: an additional fin structure, adjacent the fin structure, including the first lattice constant and opposing additional fin sidewall portions extending from the fin top to a substrate; an additional bridge layer including the first lattice constant and opposing additional bridge layer sidewall portions respectively directly contacting the opposing additional fin sidewall portions; and an additional EPI layer, including the second lattice constant and opposing additional EPI sidewall portions respectively directly contacting the opposing additional bridge layer sidewall portions; wherein the EPI layer has a first polarity, the additional EPI layer has second polarity opposite the first polarity, and the EPI layer and the additional EPI layer are included in a CMOS device. In an embodiment the bridge sidewall layers are equidistant from the fin structure.

[0023] An embodiment comprises: an interlayer dielectric including a first trench and a second trench proximate the first trench; at least one semiconductor channel including a first layer formed along a sidewall of the first trench, the first layer including one of a group III-V material layer and a group IV material layer; and at least one semiconductor channel including a second layer formed along a sidewall of the second trench, the second layer including one of a group III-V material layer and a group IV material layer; wherein both channels are used in a CMOS transistor device and the first and second layers are epitaxial (EPI). In an embodiment the first layer has an opposite polarity of the second layer. An embodiment comprises: a substrate upon which the interlayer dielectric is formed; wherein the first layer has a first lattice constant, the second layer has a second lattice constant, and the

substrate has a third lattice constant different from at least one of the first and second lattice constants. In an embodiment the first and second trenches are formed on and directly over fins. An embodiment comprises: a third layer formed along another sidewall of the first trench, the third layer including one of a group III-V material layer and a group IV material layer; a fourth layer formed along another sidewall of the second trench, the fourth layer including one of a group III-V material layer and a group IV material layer; wherein the first and third layers are generally equidistant from the first trench and the second and fourth layers are generally equidistant from the second trench. In an embodiment the first layer includes the group III-V material layer; and the second layer includes the group IV material layer.

[0024] An embodiment comprises: a fin structure including a first lattice constant and a fin top and opposing fin sidewall portions extending from the fin top towards a substrate; an epitaxial (EPI) layer, including a second lattice constant different than the first lattice constant, comprising opposing EPI sidewall portions respectively directly contacting the opposing fin sidewall portions; wherein (a) the EPI layer comprises one of a IV and a III-V material, (b) the fin structure includes silicon, and (c) the EPI layer is included in a channel of a transistor. In an embodiment the fin includes a concentration of strain adjacent the fin top and the EPI layer lacks defects along the entire border between the EPI layer and the fin structure.

[0025] An embodiment comprises: an interlayer dielectric on a substrate and including a trench formed on and directly over one of an additional trench and a fin; and an epitaxial (EPI) layer, formed along a sidewall of the trench, including one of a group IV material and a group III-V material; wherein the EPI layer and the substrate have different lattice constants. In an embodiment the EPI layer comprises a group III-V material. In an embodiment the trench is formed on and directly over the fin. In an embodiment the EPI layer is included entirely between the sidewall of the trench and a sidewall of the one of the additional trench and the fin. In an embodiment an additional EPI layer, formed along an additional sidewall of the trench, including another one of a group IV material and a group III-V material; wherein the additional EPI layer and the substrate have different lattice constants. In an embodiment the EPI layer and the additional EPI layer are generally equidistant from the trench.

[0026] An embodiment includes an apparatus comprising: a first trench structure including opposing first sidewall portions extending towards a substrate; a bridge layer including a bridge layer sidewall portion formed on one of the first sidewall portions; a second trench structure including opposing second sidewall portions extending towards the substrate; and an EPI layer including an EPI layer sidewall portion respectively formed on one of the second sidewall portions; wherein the bridge layer sidewall portion is included in a first transistor channel. In an embodiment the EPI layer sidewall portion is included in a second transistor channel that has an opposite polarity of the first transistor channel. In an embodiment the EPI layer sidewall portion is included in a second transistor channel and the bridge layer has an opposite polarity of the EPI layer. In an embodiment the EPI layer and the bridge layer have unequal lattice constants. In an embodiment the first and second trench structures each couple to a silicon fin. In an embodiment the bridge layer includes an additional bridge layer sidewall portion formed on one of the first sidewall portions; the EPI layer includes an additional EPI layer sidewall portion formed on one of the second sidewall portions; and the first sidewall portions are equidistant from the first trench structure and the second sidewall portions are equidistant from the second trench structure.

[0027] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. This description and the claims following include terms, such as left, right, top, bottom, over, under, upper, lower, first, second, etc. that are used for descriptive purposes only and are not to be construed as limiting. For example, terms designating relative vertical position refer to a situation where a device side (or active surface) of a substrate or integrated circuit is the "top" surface of that substrate; the substrate may actually be in any orientation so that a "top" side of a substrate may be lower than the "bottom" side in a standard terrestrial frame of reference and still fall within the meaning of the term "top." The term "on" as used herein (including in the claims) does not indicate that a first layer "on" a second layer is directly on and in immediate contact with the second layer unless such is specifically stated; there may be a third layer or other structure between the first layer and the second layer on the first layer. The

embodiments of a device or article described herein can be manufactured, used, or shipped in a number of positions and orientations. Persons skilled in the relevant art can appreciate that many modifications and variations are possible in light of the above teaching. Persons skilled in the art will recognize various equivalent combinations and substitutions for various components shown in the Figures. It is therefore intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

What is claimed is:

- 1 1. An apparatus comprising:
2 a fin structure including a fin top and opposing fin sidewall portions extending
3 from the fin top towards a substrate;
4 a bridge layer including opposing bridge layer sidewall portions respectively
5 directly contacting the opposing fin sidewall portions; and
6 an epitaxial (EPI) layer comprising opposing EPI sidewall portions
7 respectively directly contacting the opposing bridge layer sidewall portions;
8 wherein a lattice constant differential between the bridge layer and fin structure is
9 less than a lattice constant differential between the bridge layer and the EPI layer.
- 1 2. The apparatus of claim 1 wherein the EPI layer comprises an EPI material
2 including one of a group IV material and a group III-V material, the fin structure
3 includes a fin structure material including silicon, and the bridge layer includes a
4 bridge layer material unequal to either of the fin structure material and the EPI
5 material.
- 1 3. The apparatus of claim 2 wherein the EPI layer is included in a channel of a
2 transistor and couples to a source and a drain of the transistor.
- 1 4. The apparatus of claim 3 wherein the substrate does not include a silicon on
2 insulator (SOI) configuration.
- 1 5. The apparatus of claim 2 wherein the EPI layer is included in a channel of a
2 transistor and couples to a source and a drain of the transistor, the source and drain
3 both directly contacting the fin structure.
- 1 6. The apparatus of claim 2 wherein the fin includes a concentration of strain
2 adjacent the fin top.

1 7. The apparatus of claim 2 wherein the EPI layer lacks defects along the entire
2 border between the EPI layer and the bridge layer.

1 8. The apparatus of claim 1 wherein a single plane, orthogonal to a long vertical
2 axis of the fin, intersects the fin over a first area and the EPI sidewalls over a second
3 area and the second area is greater than the first area.

1 9. The apparatus of claim 1 wherein the fin is monolithic with the substrate and
2 the EPI layer sidewall portions are monolithic with one another.

1 10. The apparatus of claim 1 comprising:
2 an additional fin structure, adjacent the fin structure, including the first lattice
3 constant and opposing additional fin sidewall portions extending from the fin top to a
4 substrate; and
5 an additional bridge layer including the first lattice constant and opposing additional
6 bridge layer sidewall portions respectively directly contacting the opposing additional
7 fin sidewall portions;
8 wherein the EPI layer has a first polarity, the additional bridge layer has second
9 polarity opposite the first polarity, and the EPI layer and the additional bridge layer
10 are included in a CMOS device.

1 11. The apparatus of claim 1 comprising:
2 an additional fin structure, adjacent the fin structure, including the first lattice
3 constant and opposing additional fin sidewall portions extending from the fin top to a
4 substrate;
5 an additional bridge layer including the first lattice constant and opposing
6 additional bridge layer sidewall portions respectively directly contacting the opposing
7 additional fin sidewall portions; and
8 an additional EPI layer, including the second lattice constant and opposing
9 additional EPI sidewall portions respectively directly contacting the opposing
10 additional bridge layer sidewall portions

11 wherein the EPI layer has a first polarity, the additional EPI layer has second polarity
12 opposite the first polarity, and the EPI layer and the additional EPI layer are included
13 in a CMOS device.

1 12. The apparatus of claim 1 wherein the bridge sidewall layers are equidistant
2 from the fin structure.

1 13. An apparatus comprising:
2 an interlayer dielectric including a first trench and a second trench proximate
3 the first trench;
4 at least one semiconductor channel including a first layer formed along a
5 sidewall of the first trench, the first layer including one of a group III-V material layer
6 and a group IV material layer; and
7 at least one semiconductor channel including a second layer formed along a
8 sidewall of the second trench, the second layer including one of a group III-V
9 material layer and a group IV material layer;
10 wherein both channels are used in a CMOS transistor device and the first and
11 second layers are epitaxial (EPI).

1 14. The apparatus of claim 13 wherein the first layer has an opposite polarity of
2 the second layer.

1 15. The apparatus of claim 14 comprising:
2 a substrate upon which the interlayer dielectric is formed;
3 wherein the first layer has a first lattice constant, the second layer has a second
4 lattice constant, and the substrate has a third lattice constant different from at least
5 one of the first and second lattice constants.

1 16. The apparatus of claim 13 wherein the first and second trenches are formed
2 on and directly over fins.

1 17. The apparatus of claim 13 comprising:
2 a third layer formed along another sidewall of the first trench, the third layer
3 including one of a group III-V material layer and a group IV material layer;
4 a fourth layer formed along another sidewall of the second trench, the fourth
5 layer including one of a group III-V material layer and a group IV material layer;
6 wherein the first and third layers are generally equidistant from the first trench and
7 the second and fourth layers are generally equidistant from the second trench.

1 18. The apparatus of claim 13 wherein:
2 the first layer includes the group III-V material layer; and
3 the second layer includes the group IV material layer.

1 19. An apparatus comprising:
2 a fin structure including a first lattice constant and a fin top and opposing fin
3 sidewall portions extending from the fin top towards a substrate;
4 an epitaxial (EPI) layer, including a second lattice constant different than the
5 first lattice constant, comprising opposing EPI sidewall portions respectively directly
6 contacting the opposing fin sidewall portions;
7 wherein (a) the EPI layer comprises one of a IV and a III-V material, (b) the fin
8 structure includes silicon, and (c) the EPI layer is included in a channel of a
9 transistor.

1 20. The apparatus of claim 19 wherein the fin includes a concentration of strain
2 adjacent the fin top and the EPI layer lacks defects along the entire border between
3 the EPI layer and the fin structure.

1 21. An apparatus comprising:
2 an interlayer dielectric on a substrate and including a trench formed on and
3 directly over one of an additional trench and a fin; and
4 an epitaxial (EPI) layer, formed along a sidewall of the trench, including one of
5 a group IV material and a group III-V material;
6 wherein the EPI layer and the substrate have different lattice constants.

1 22. The apparatus of claim 21 wherein the EPI layer comprises a group III-V
2 material.

1 23. The apparatus of claim 21, wherein the trench is formed on and directly over
2 the fin.

1 24. The apparatus of claim 21, wherein the EPI layer is included entirely between
2 the sidewall of the trench and a sidewall of the one of the additional trench and the
3 fin.

1 25. The apparatus of claim 21 comprising an additional EPI layer, formed along
2 an additional sidewall of the trench, including another one of a group IV material and
3 a group III-V material; wherein the additional EPI layer and the substrate have
4 different lattice constants.

1 26. The apparatus of claim 25, wherein the EPI layer and the additional EPI layer
2 are generally equidistant from the trench.

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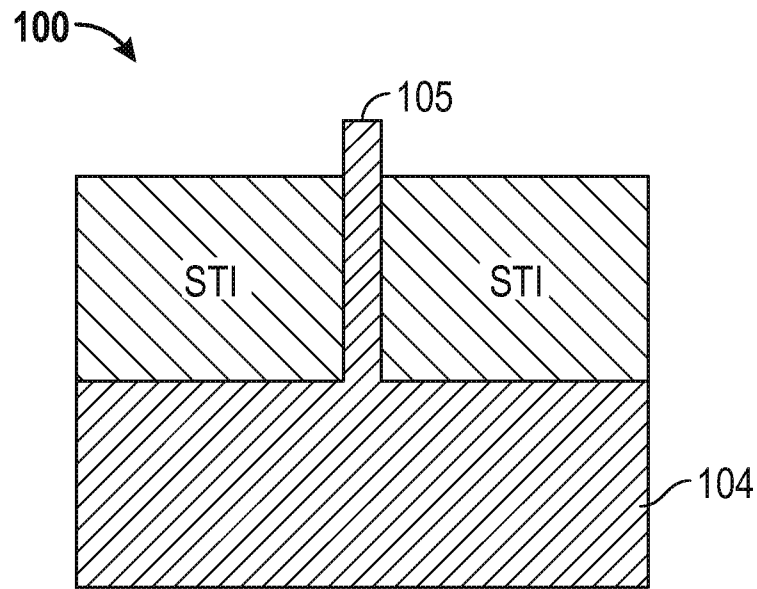


FIG. 1A

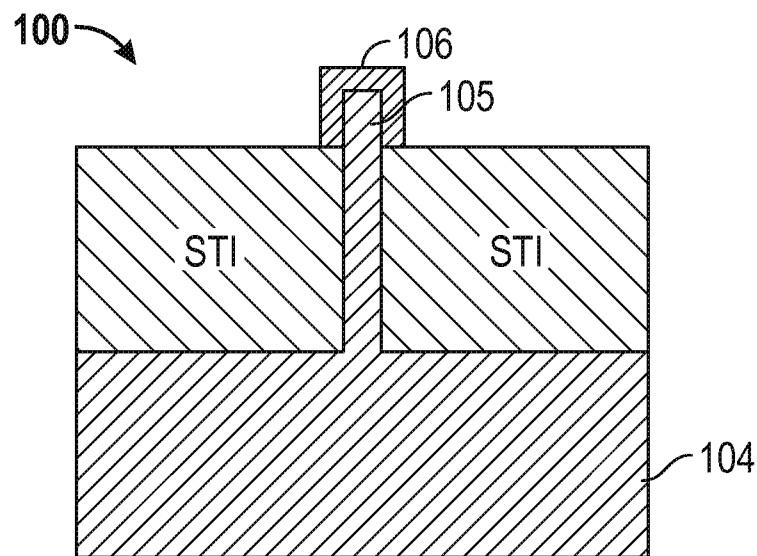


FIG. 1B

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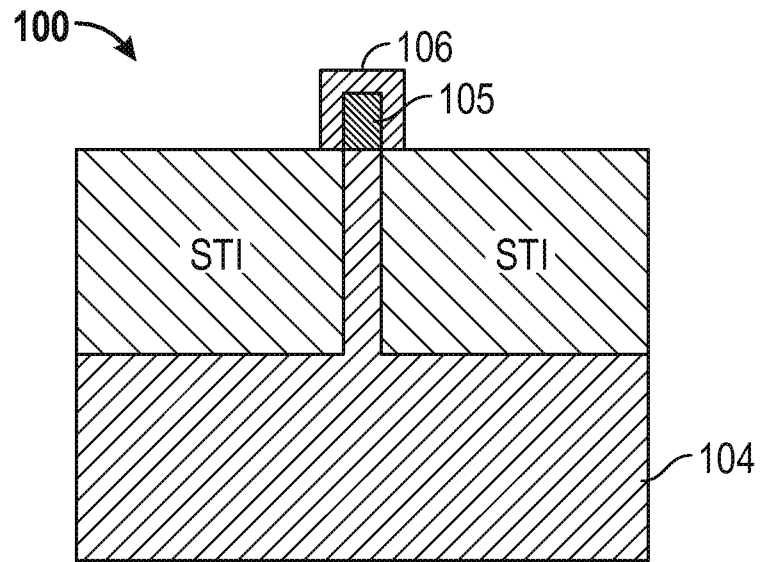


FIG. 1C

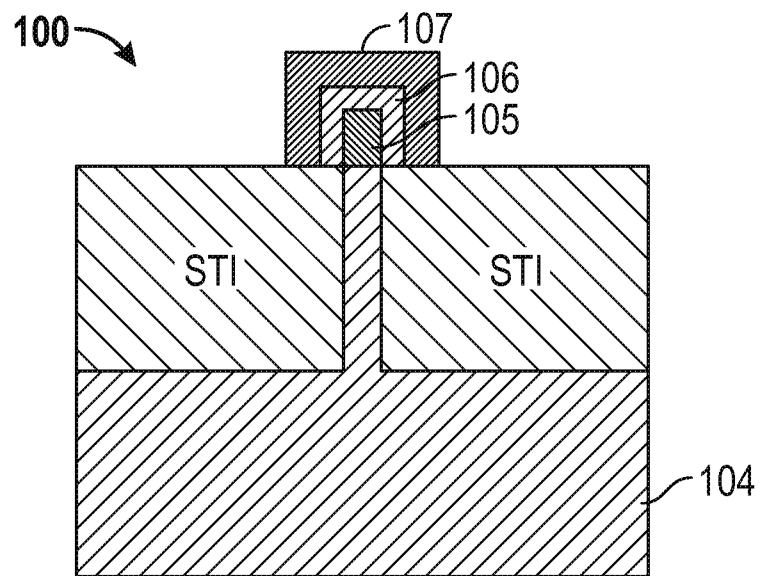


FIG. 1D

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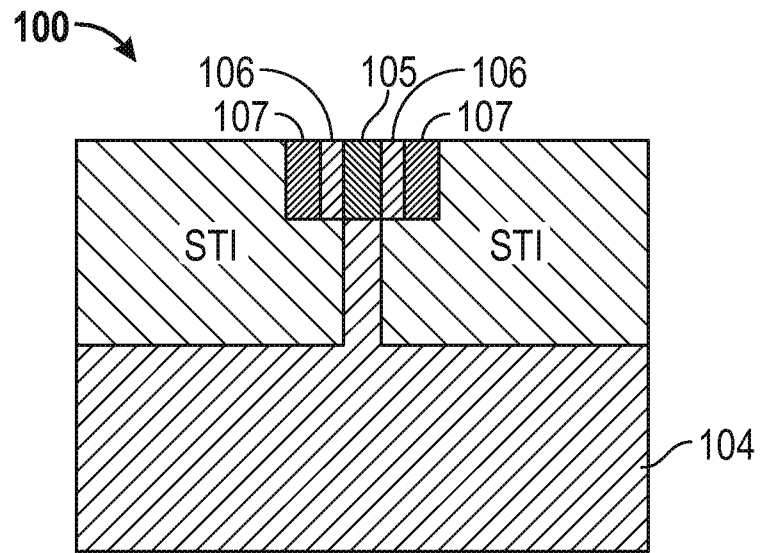


FIG. 1E

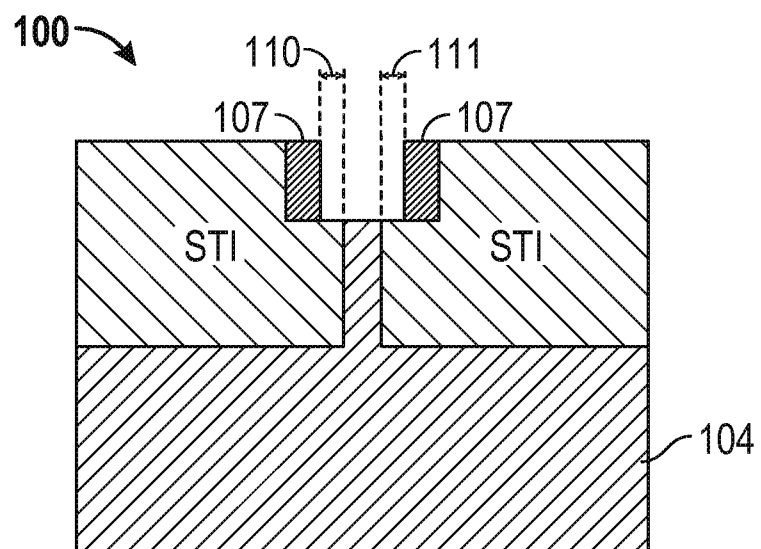


FIG. 1F

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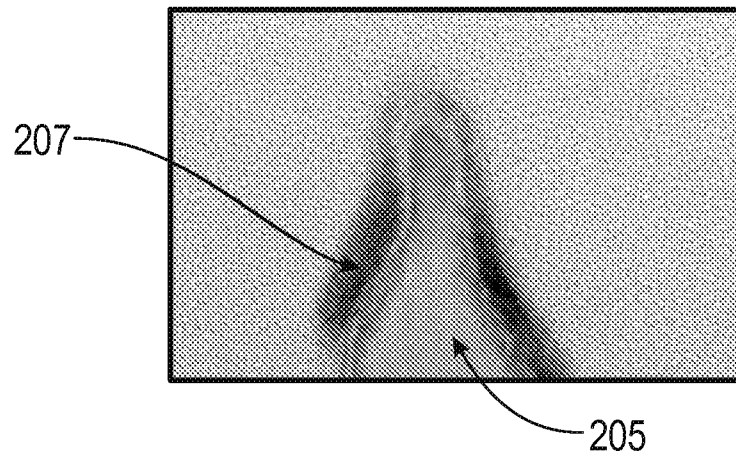


FIG. 2A

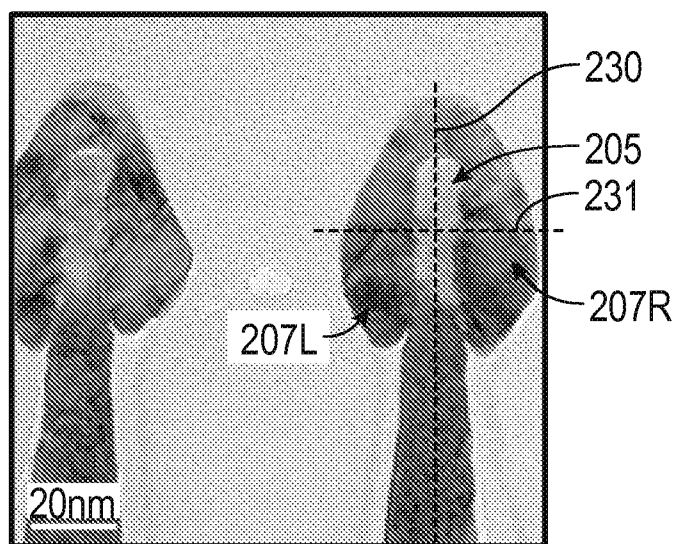


FIG. 2B

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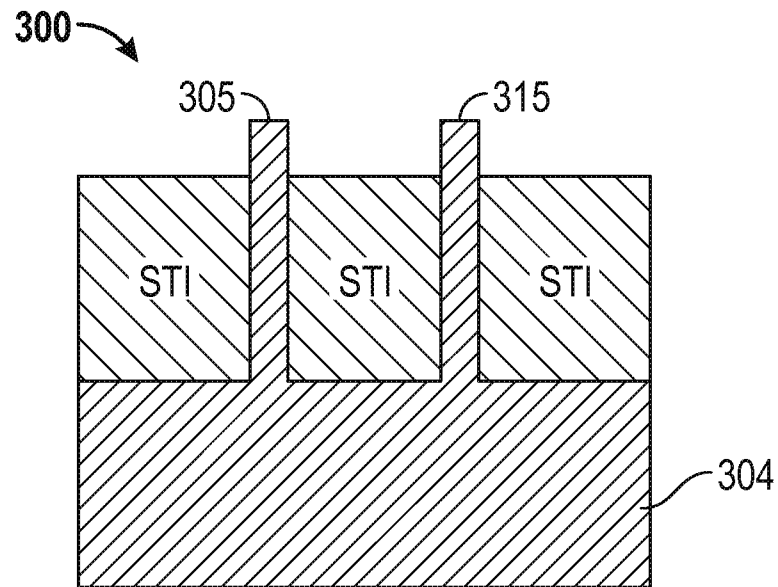


FIG. 3A

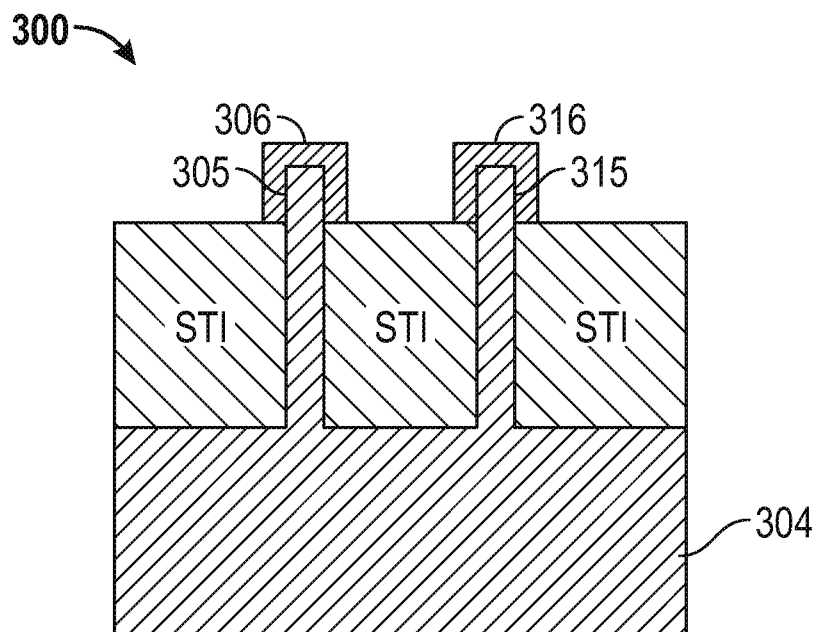


FIG. 3B

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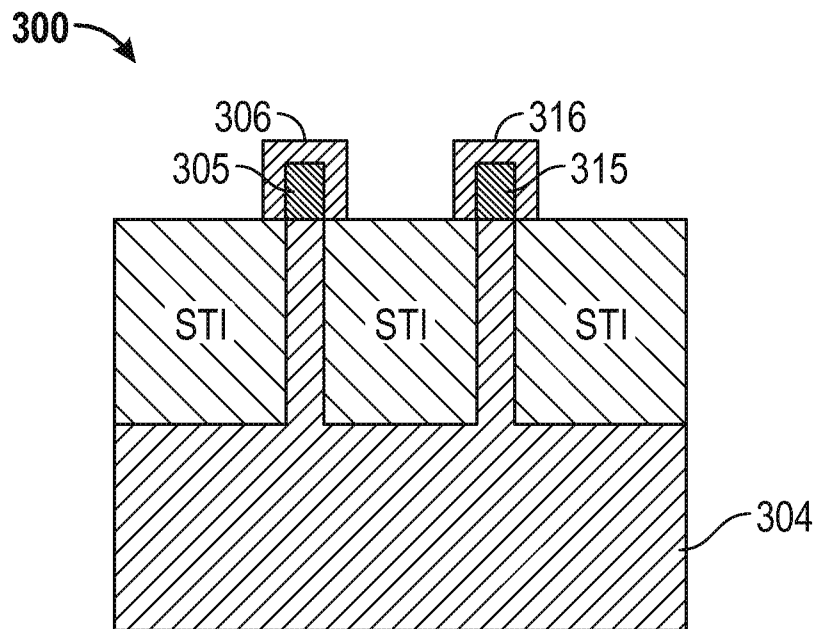


FIG. 3C

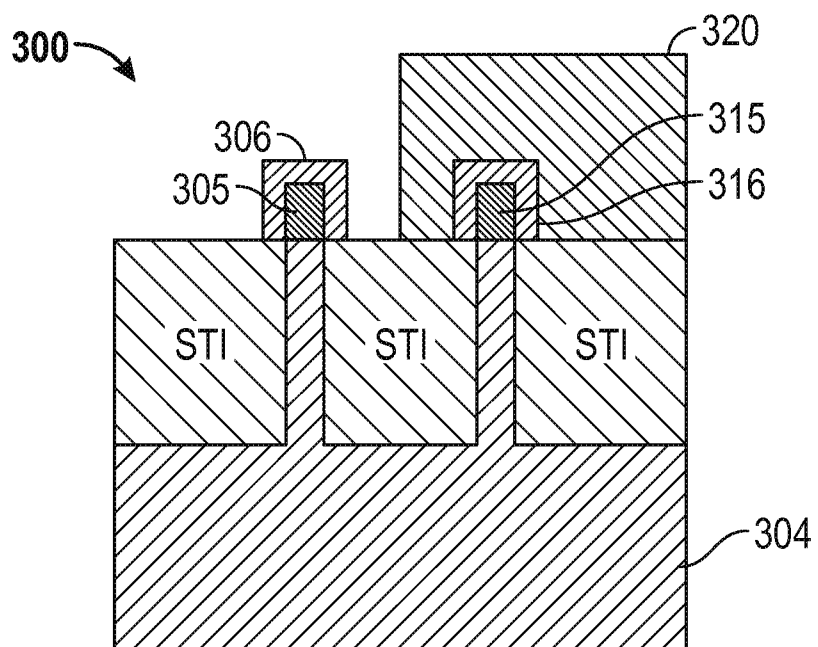


FIG. 3D

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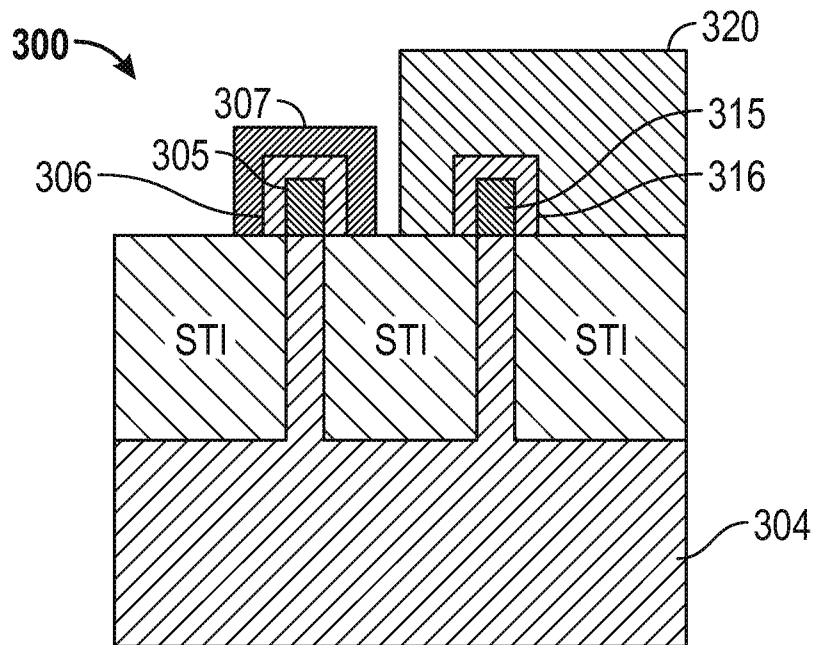


FIG. 3E

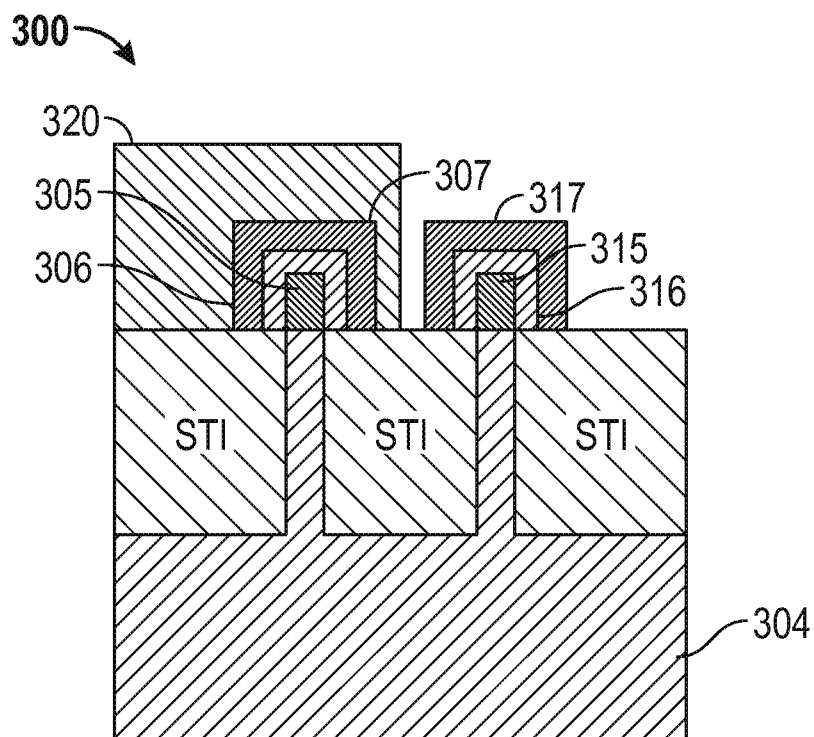


FIG. 3F

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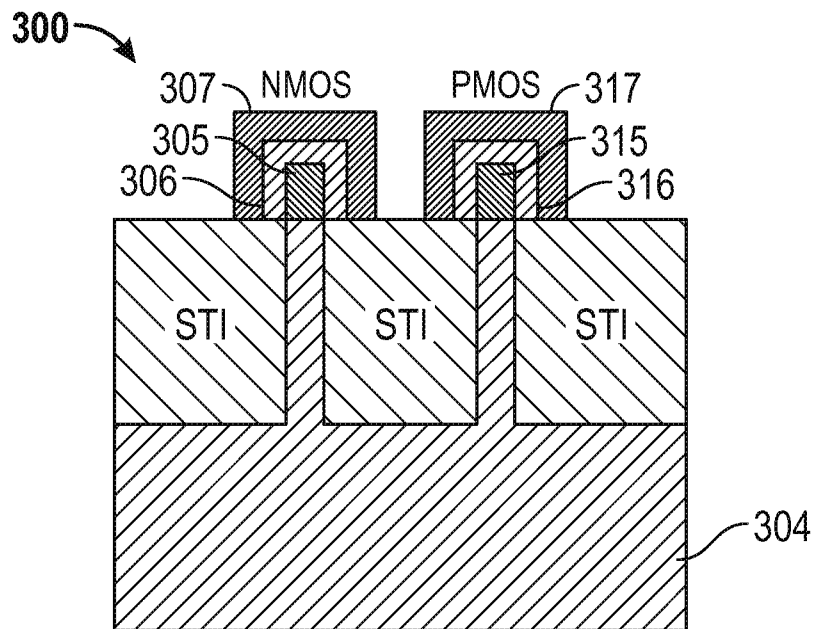


FIG. 3G

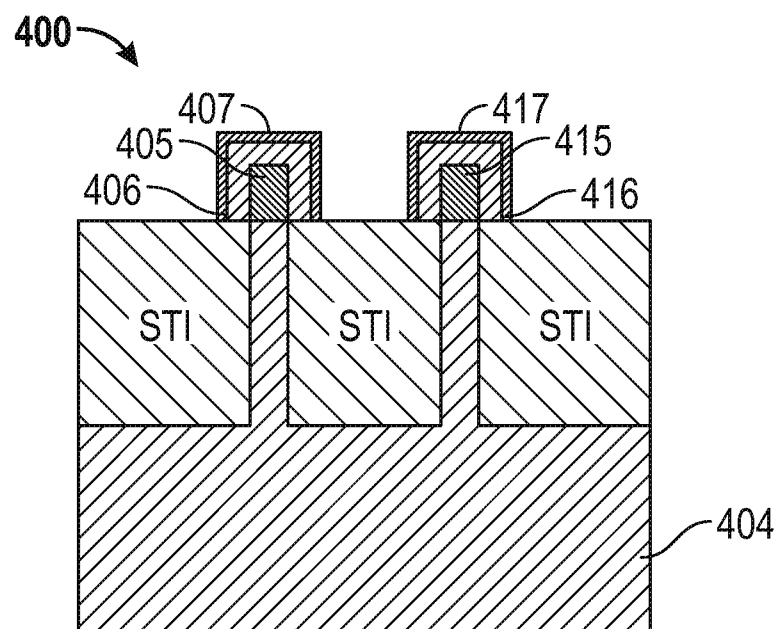


FIG. 4A

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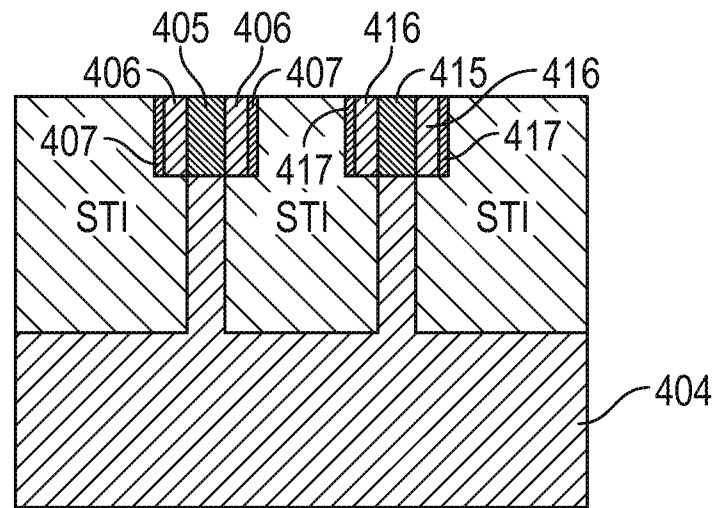


FIG. 4B

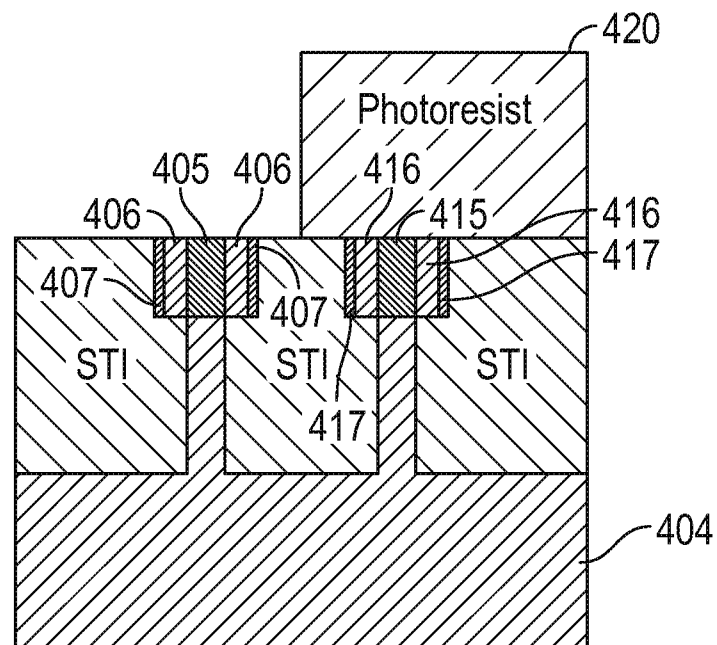


FIG. 4C

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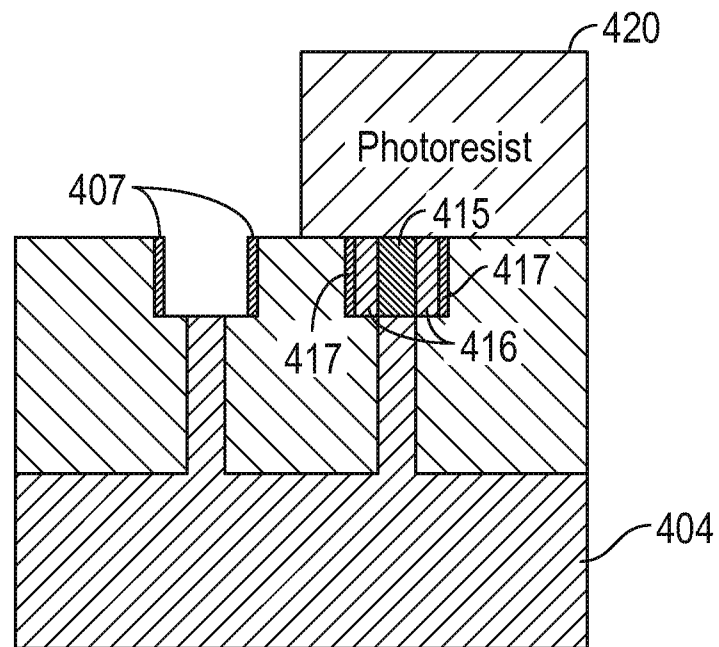


FIG. 4D

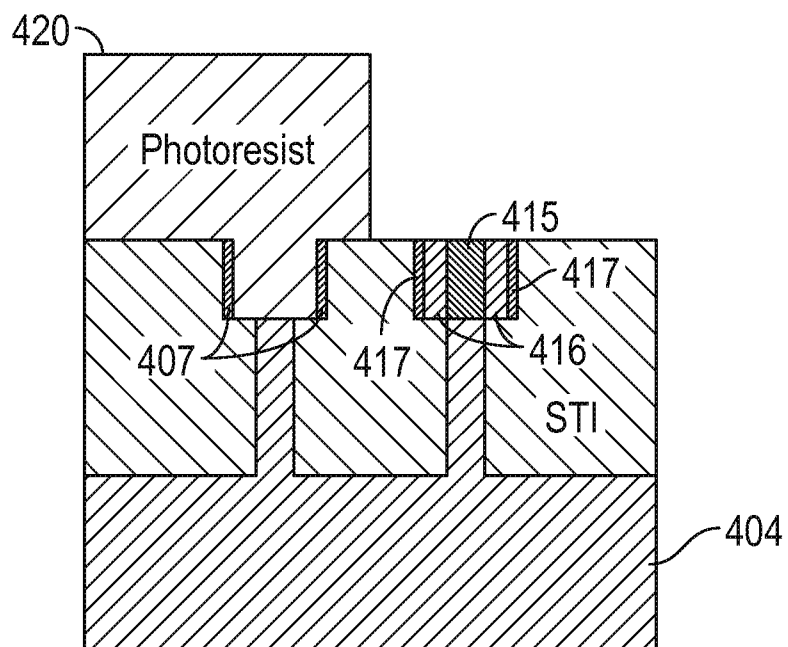


FIG. 4E

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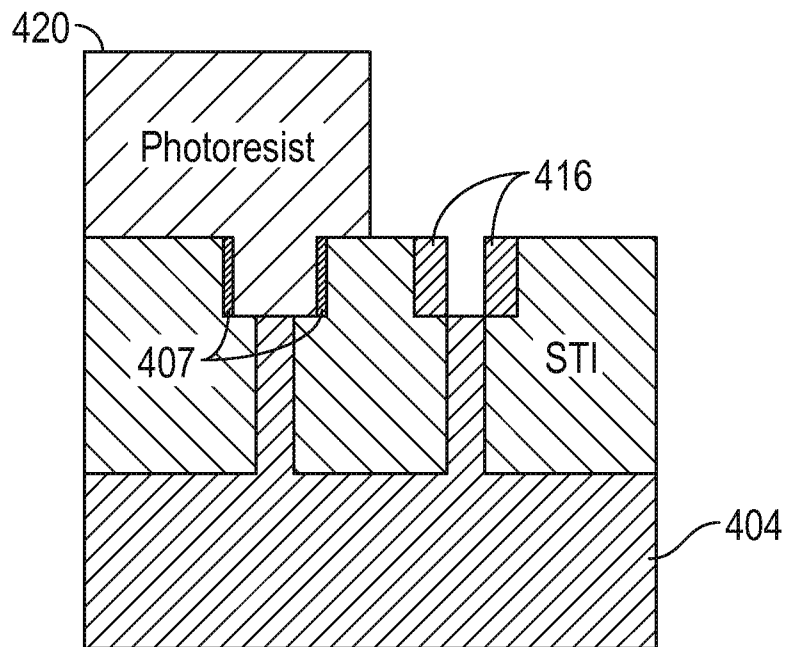


FIG. 4F

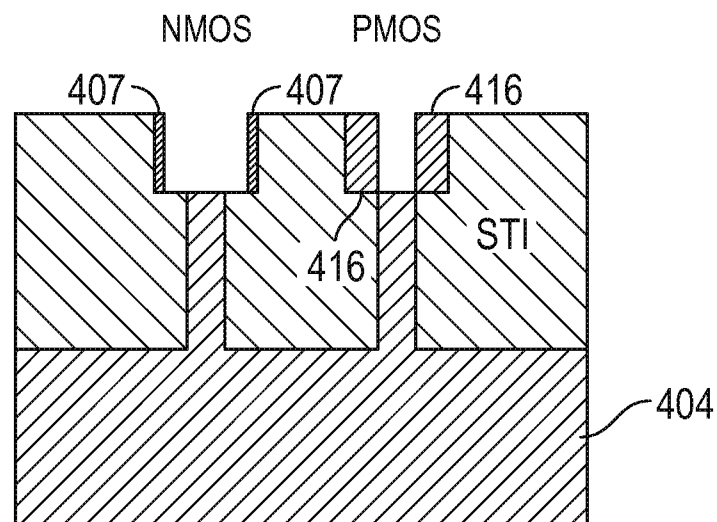


FIG. 4G

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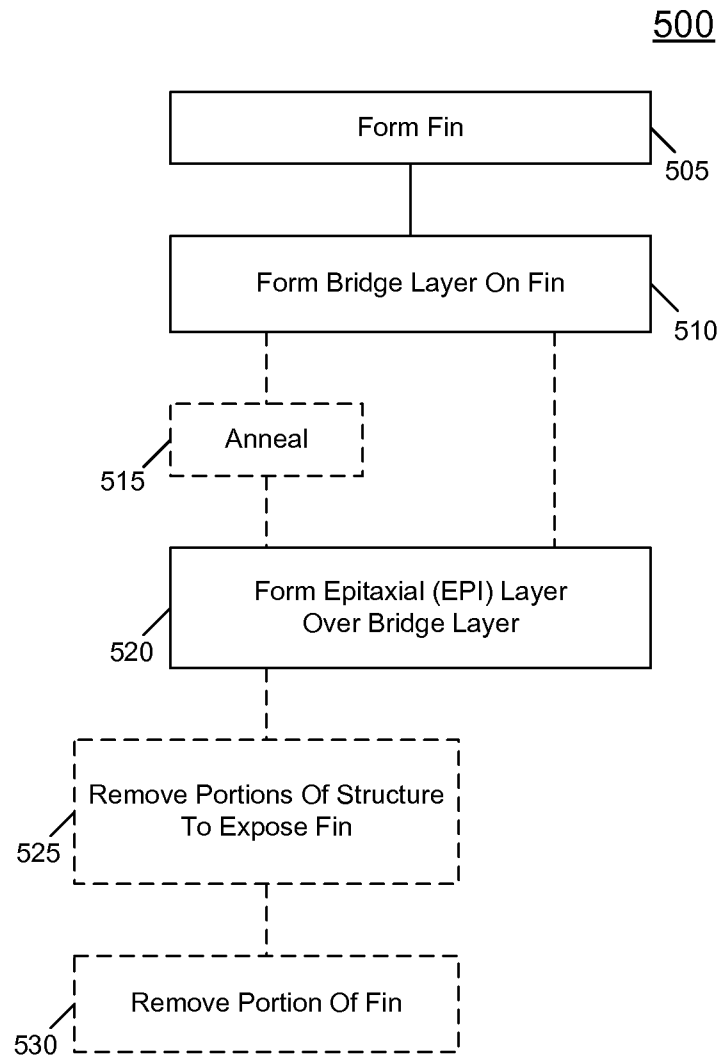


FIG. 5

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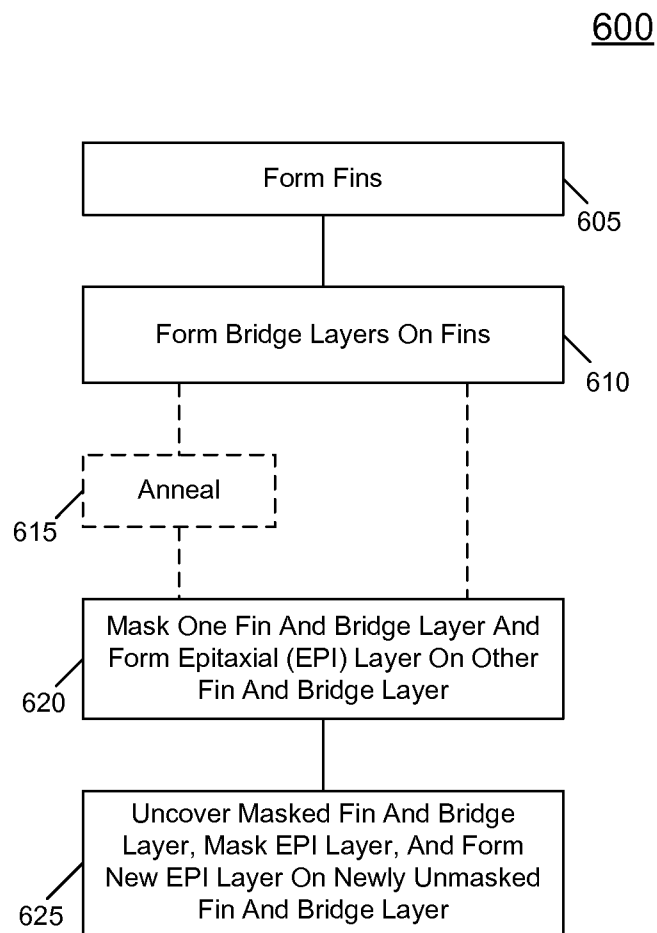


FIG. 6

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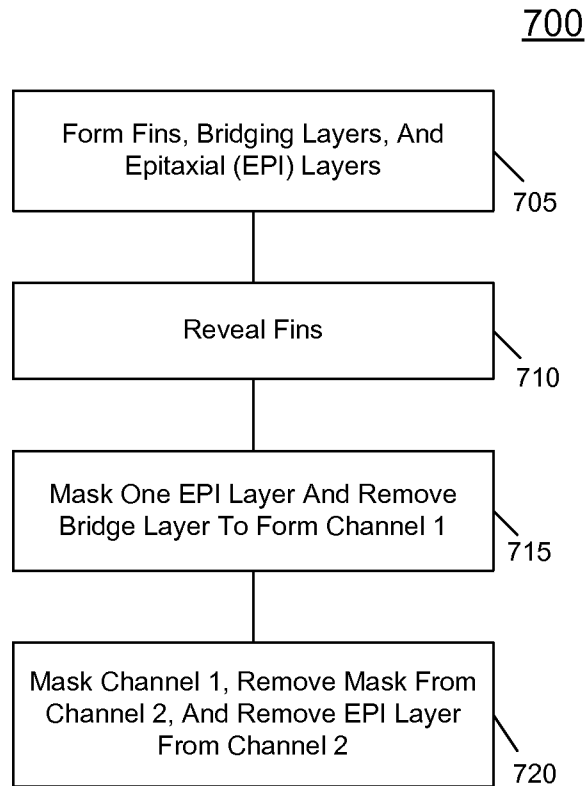


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/048025**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/20(2006.01)i, H01L 29/78(2006.01)i, H01L 21/336(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/20; H01L 21/205; H01L 21/8242; H01L 29/12; H01L 29/78; H01L 31/119; H01L 27/01; H01L 21/8238; H01L 29/76; H01L 21/336

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: fin, bridge, channel, dielectric, trench, CMOS and lattice constant

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 7785958 B2 (MARK L. DOCZY et al.) 31 August 2010 See column 2, lines 21-31, column 6, line 58 - column 7, line 6, column 9, lines 35-47, claim 1 and figures 1A-1C, 4E.	13-14, 17-18, 21-22, 24-26
A		1-12, 15-16, 19-20, 23
Y	US 2009-0085027 A1 (BEEN-YIH JIN et al.) 02 April 2009 See paragraphs [0016], [0038]-[0042], claim 1 and figures 1A-1D.	13-14, 17-22, 24-26
Y	US 6803631 B2 (SRIKANTESWARA DAKSHINA-MURTHY et al.) 12 October 2004 See column 3, line 57 - column 4, line 30, claims 1, 10 and figures 4A, 5.	19-22, 24-26
A	US 2012-0187482 A1 (LAHIR S. ADAM et al.) 26 July 2012 See paragraphs [0014]-[0028], claims 1-4 and figures 1-7.	1-26
A	US 2001-0038130 A1 (SANG YEON KIM) 08 November 2001 See abstract, paragraphs [0036], [0046]-[0055] and figures 4, 5L-50.	1-26



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

25 October 2013 (25.10.2013)

Date of mailing of the international search report

28 October 2013 (28.10.2013)

Name and mailing address of the ISA/KR

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CHOI, Sang Won

Telephone No. +82-42-481-8291



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/048025

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