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[54] **DISPLAY SYSTEM AND METHOD FOR REGISTRATION CONTROL EQUIPMENT**

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[52] **U.S. Cl.**..... **235/92 MP;** 235/92 DN; 235/92 V; 235/92 R; 340/259

[51] **Int. Cl.**[2]..... **G06M 3/02**

[58] **Field of Search**..... 235/92 MP, 92 V, 92 CV, 235/92 DN; 250/563, 561, 559, 571; 340/259, 324 A

[56] **References Cited**

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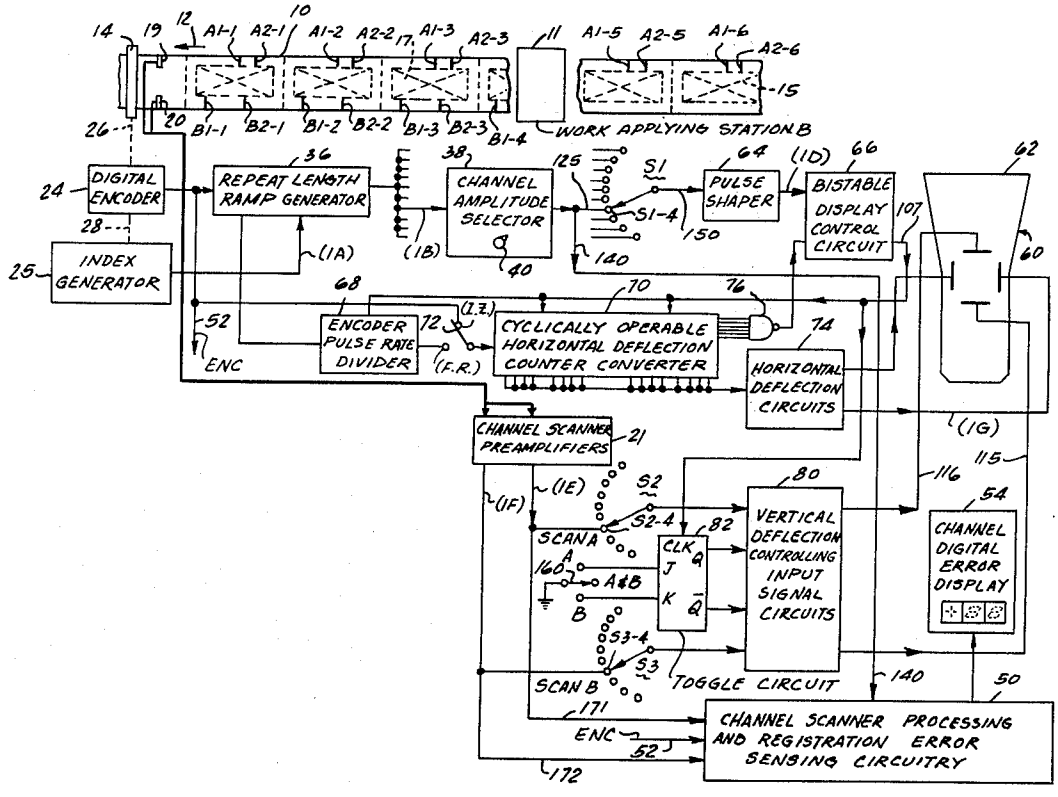
Primary Examiner—Joseph M. Thesz, Jr.

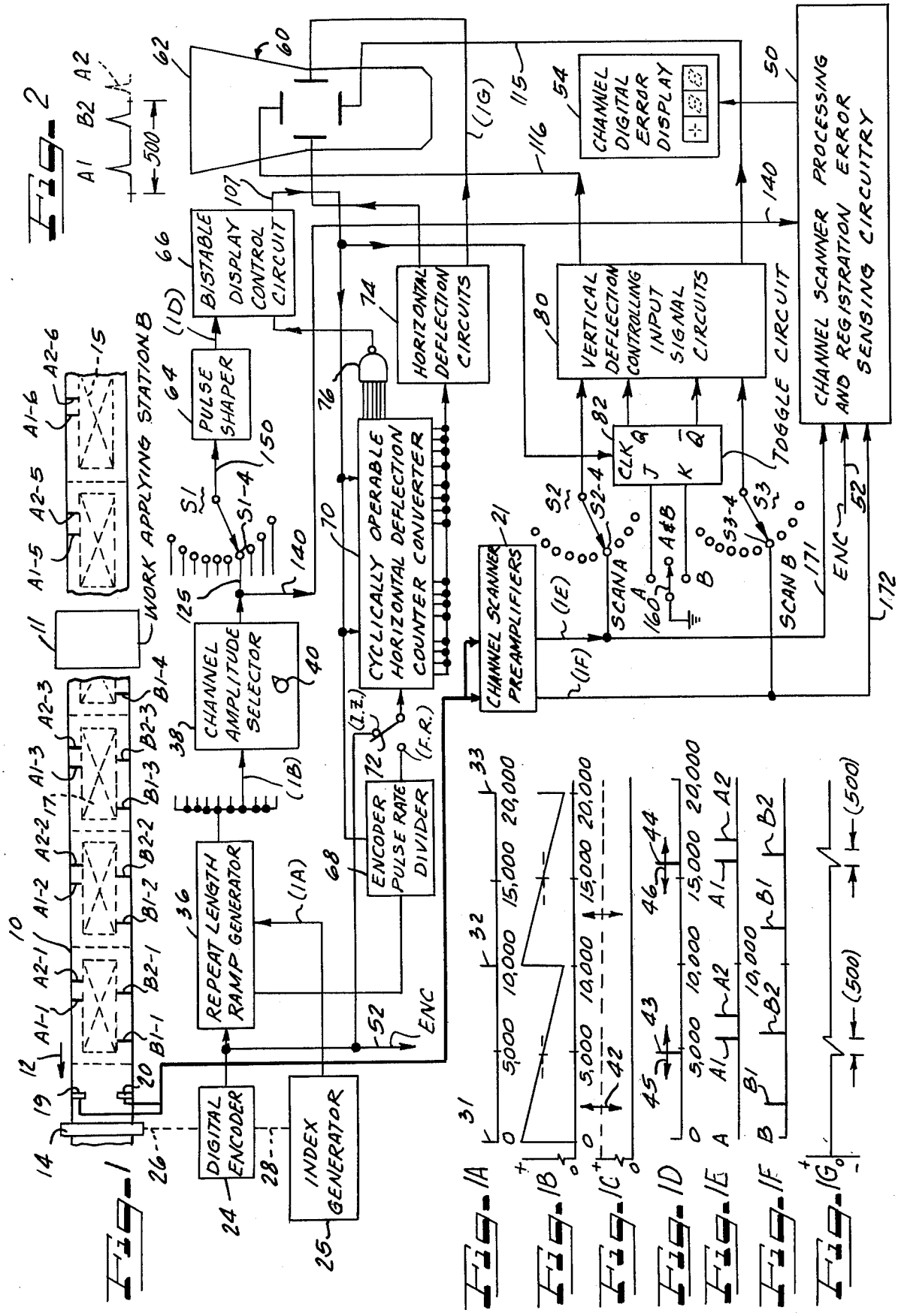
Attorney, Agent, or Firm—Hill, Gross, Simpson, Van Santen, Steadman, Chiara & Simpson

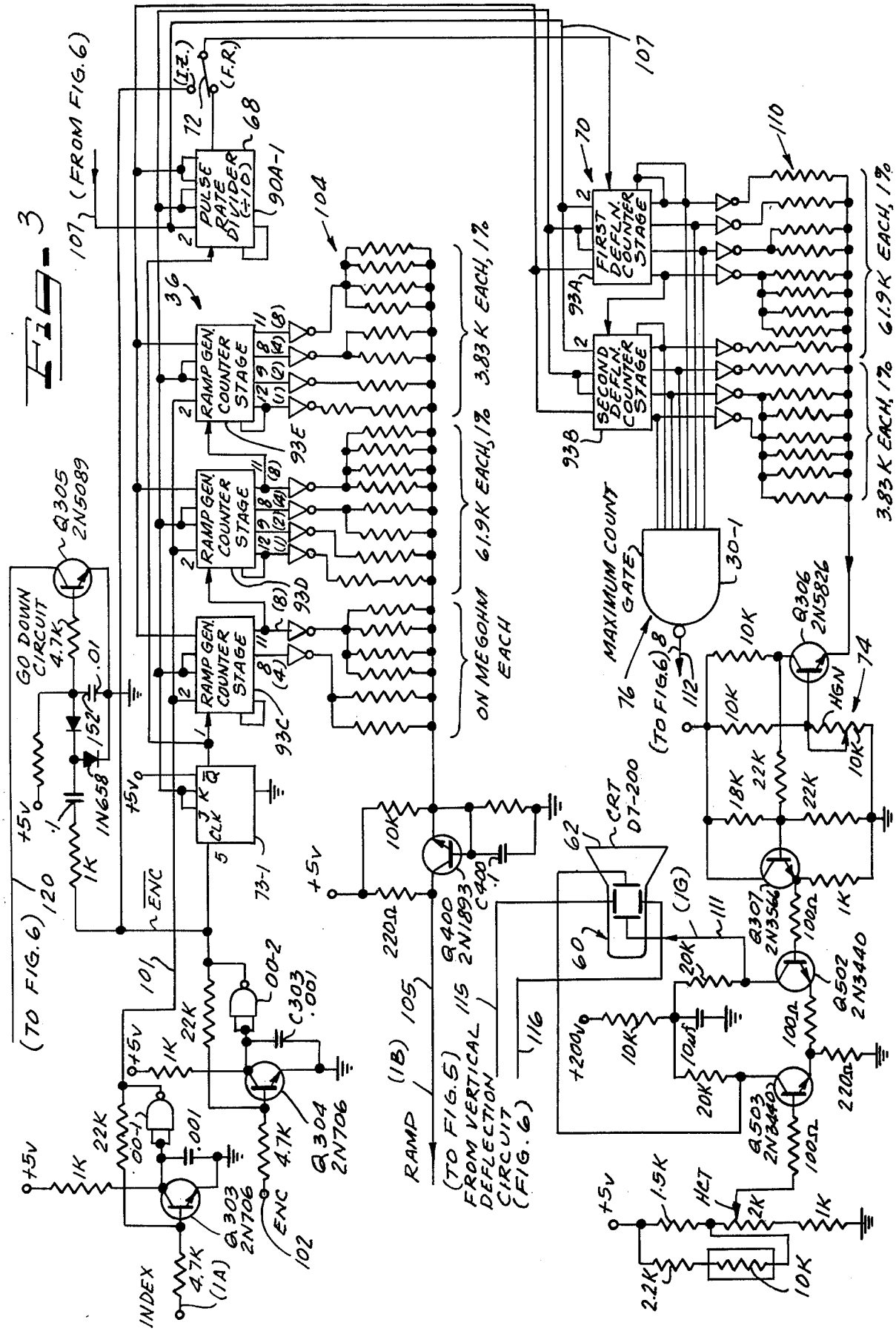
[57] **ABSTRACT**

A display system is disclosed which operates its repetitive horizontal deflection as a function of encoder pulses keyed to web movement (rather than time), and which displays scanner signals as vertical deflection. For accurate viewing, the full horizontal deflection can take place while scanning a fraction of the repeat length of the web. In order to select marks for registration control, the portion of a repeat length to be displayed can be continuously changed until potentially suitable marks appear on the display, whereupon such marks can be checked for stability, and spurious signals can be excluded from the inspection zone, since horizontal deflection is precisely locked to the desired portion of the repeat length and is synchronized with the inspection zone of the registration control. A master unit including the display apparatus can be selectively coupled with a number of different work stations in succession and can selectively display outputs of one or both of a pair of scanners at each station.

6 Claims, 18 Drawing Figures




FIG. 1
FIG. 2
FIG. 1A
FIG. 1B
FIG. 1C
FIG. 1D
FIG. 1E
FIG. 1F
FIG. 1G
WORK APPLYING STATION B
DIGITAL ENCODER
INDEX GENERATOR
REPEAT LENGTH RAMP GENERATOR
CHANNEL AMPLITUDE SELECTOR
ENCODER PULSE RATE DIVIDER
CYCLICALLY OPERABLE HORIZONTAL DEFLECTION COUNTER CONVERTER
PULSE SHAPER
BISTABLE DISPLAY CONTROL CIRCUIT
HORIZONTAL DEFLECTION CIRCUITS
VERTICAL DEFLECTION CONTROLLING INPUT SIGNAL CIRCUITS
CHANNEL SCANNER PREAMPLIFIERS
TOGGLE CIRCUIT
CHANNEL DIGITAL ERROR DISPLAY
CHANNEL SCANNER PROCESSING AND REGISTRATION ERROR SENSING CIRCUITRY
SCAN A
SCAN B
ENC
A&B
CLK
J
K
Q
5,000
10,000
15,000
20,000
(500)


FIG. 3
(FROM FIG. 6)
PULSE RATE DIVIDER (÷10)
RAMP GEN. COUNTER STAGE
FIRST DEFLN. COUNTER STAGE
SECOND DEFLN. COUNTER STAGE
MAXIMUM COUNT GATE
GO DOWN CIRCUIT
RAMP
ON MEGOHM EACH
61.9K EACH, 1%
3.83K EACH, 1%
CRT 07-200
(TO FIG. 6)
(TO FIG. 5)
FROM VERTICAL DEFLECTION CIRCUIT (FIG. 6)
INDEX
ENC
Q305 2N5089
Q306 2N5826
Q307 2N3566
Q400 2N1893
Q502 2N3440
Q503 2N3440
Q303 2N706
Q304 2N706
1N658
HCT
HGN

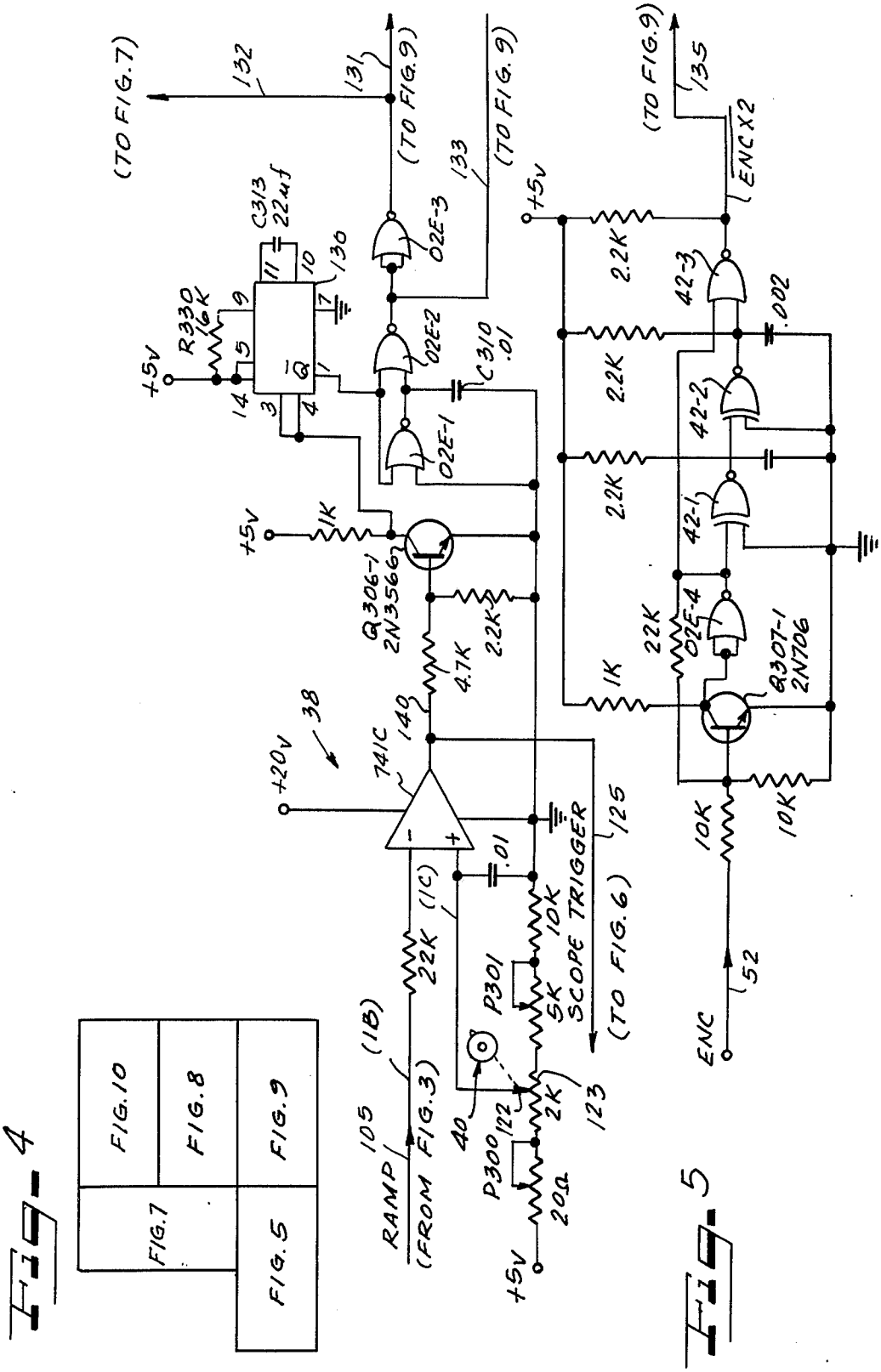

(TO FIG.7)
132
131
(TO FIG.9)
133
(TO FIG.9)
(TO FIG.9)
135
ENC X2
+5V
C313 22μf
R330 6K
130
02E-3
02E-2
02E-1
C310 .01
2.2K
42-3
42-2
42-1
.002
22K
1K
Q306-1 2N3566
4.7K
+20V
38
74IC
140
02E-4
Q307-1 2N706
10K
.01
(1C)
(1B)
22K
P301
5K
SCOPE TRIGGER
125
(TO FIG.6)
105
RAMP
(FROM FIG.3)
40
P300
122
2K
20Ω
123
ENC
52

FIG. 5

FIG. 4

FIG.10
FIG.8
FIG.9
FIG.7
FIG.5

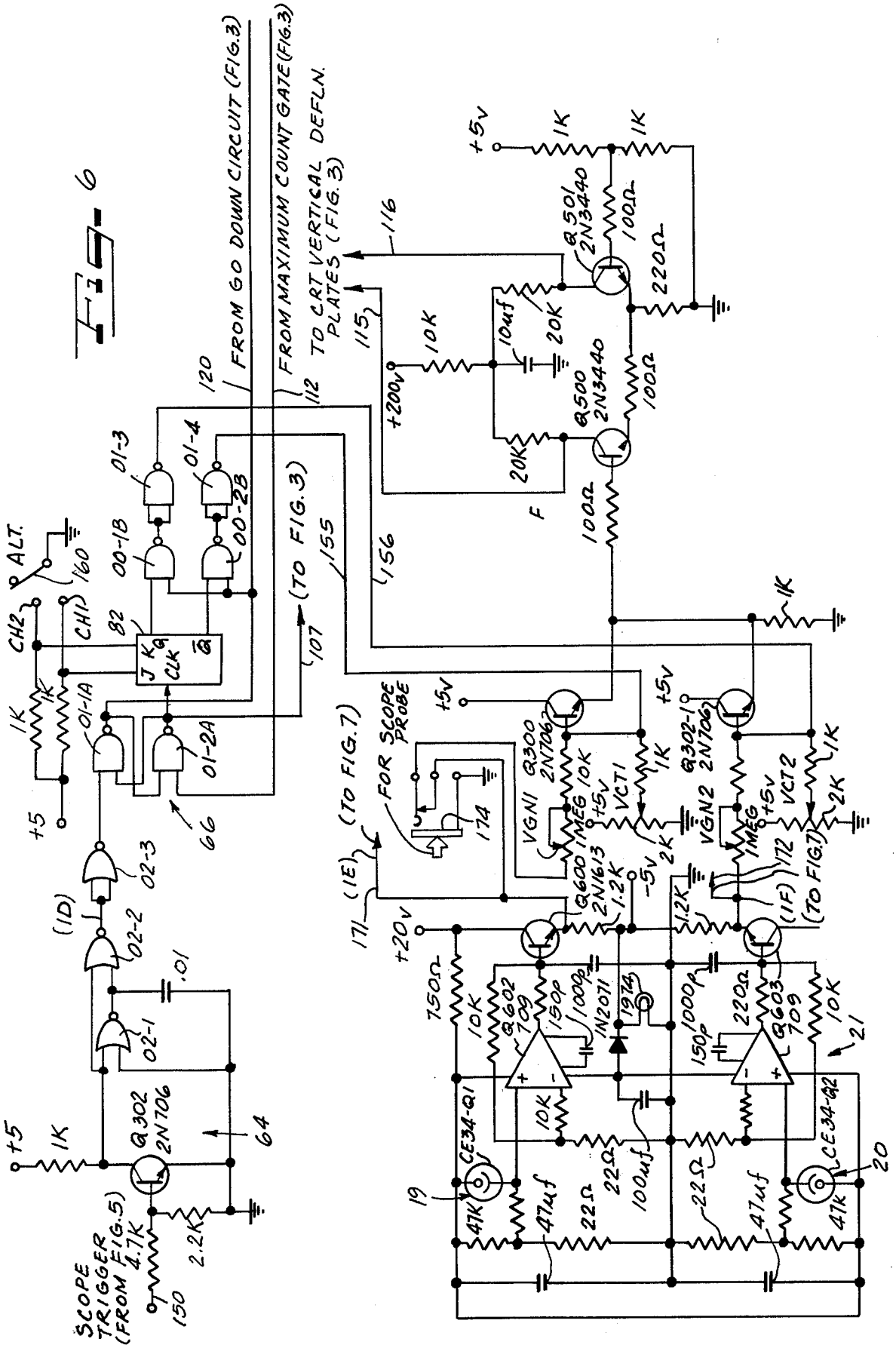

FIG. 6
FROM GO DOWN CIRCUIT (FIG.3)
FROM MAXIMUM COUNT GATE (FIG.3)
TO CRT VERTICAL DEFLN. PLATES (FIG. 3)
(TO FIG. 3)
(TO FIG. 7)
FOR SCOPE PROBE
SCOPE TRIGGER (FROM FIG. 5)
ALT.
CH1
CH2
+5
+20V
-5V
+200V
Q501 2N3440
Q500 2N3440
Q300 2N706
Q302 2N706
Q302-1 2N706
Q600 2N1613
Q602 709
Q603 709
VGN1
VGN2
VCT1
VCT2
CE34-Q1
CE34-Q2
IN2071
01-1A
01-2A
01-3
01-4
00-1B
00-2B
02-1
02-2
02-3
J K CLK
1K
2K
10K
20K
47K
100Ω
220Ω
750Ω
1.2K
2.2K
4.7K
22Ω
47μf
100μf
10μf
.01
1MEG
150p
1000p
1974
64
66
82
107
112
115
116
120
150
155
156
160
171
172
174
(1D)
(1E)
(1F)
19
20
21
F

Fig-10

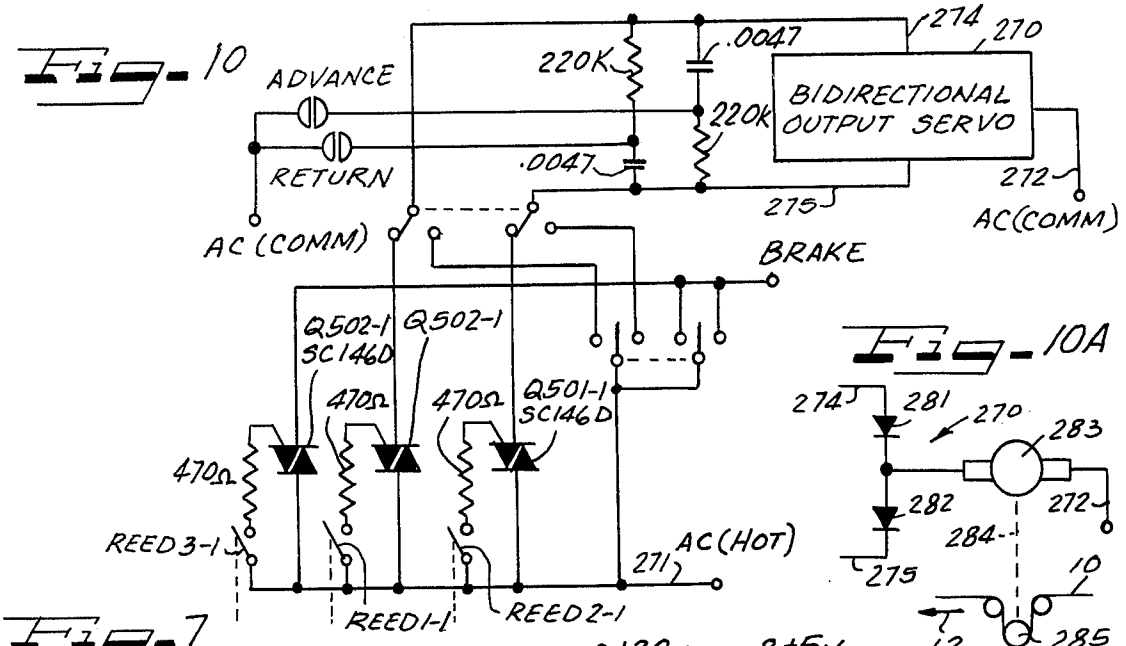
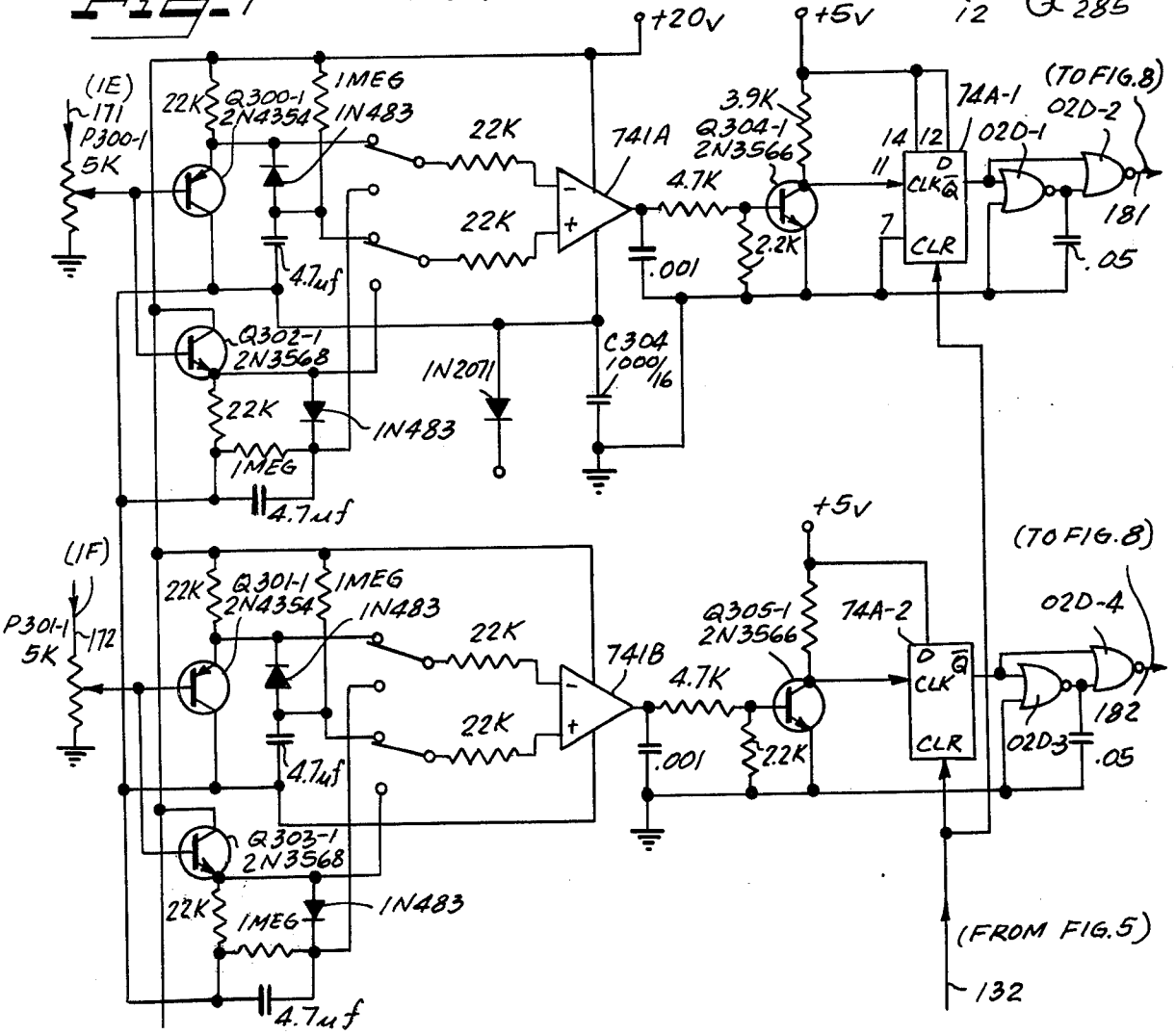


Fig-10A

Fig-7



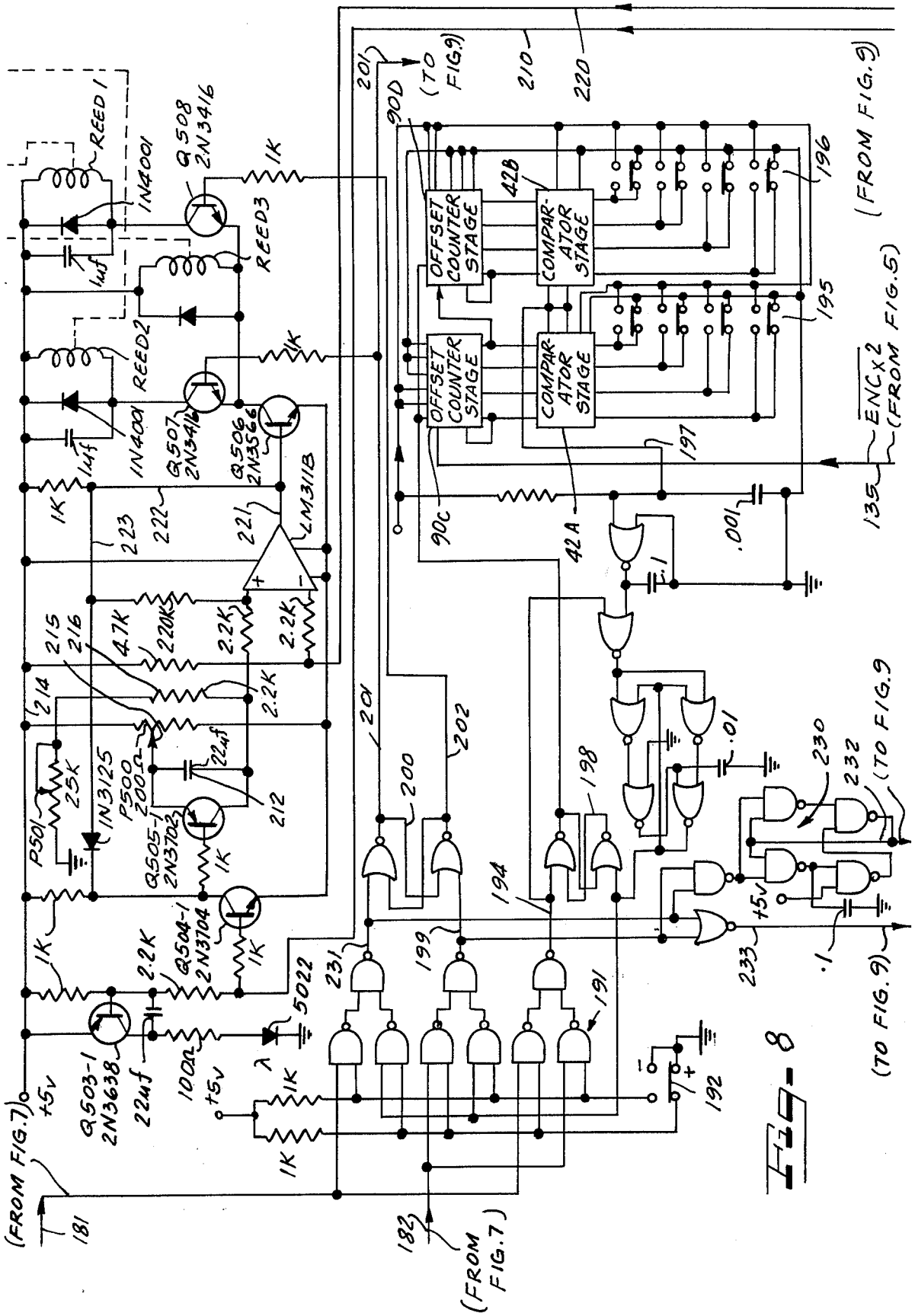

REED 1
IN4001
Q508 2N3416
1K
REED3
1uf
REED2
IN4001
Q507 2N3416
Q506 2N3566
LM3118
1K
223
222
221
215
216
47K
220K
2.2K
2.2K
214
2.2K
P501
25K
IN3125
P500 200Ω
22uf
212
Q505-1 2N3702
1K
Q504-1 2N3704
1K
2.2K
5022
Q503-1 2N3638
22uf
100Ω
+5v
1K
1K
(FROM FIG.7)
181
182
(FROM FIG.7)
201
(TO FIG.9)
90D
210
220
OFFSET COUNTER STAGE
OFFSET COUNTER STAGE
42B
COMPAR-ATOR STAGE
COMPAR-ATOR STAGE
196
195
197
90C
42A
ENC X2
(FROM FIG.5)
135
(FROM FIG.9)
.001
1
201
202
200
198
194
199
231
191
.01
230
232
(TO FIG.9)
+5v
233
.1
(TO FIG.9)
192

FIG-8

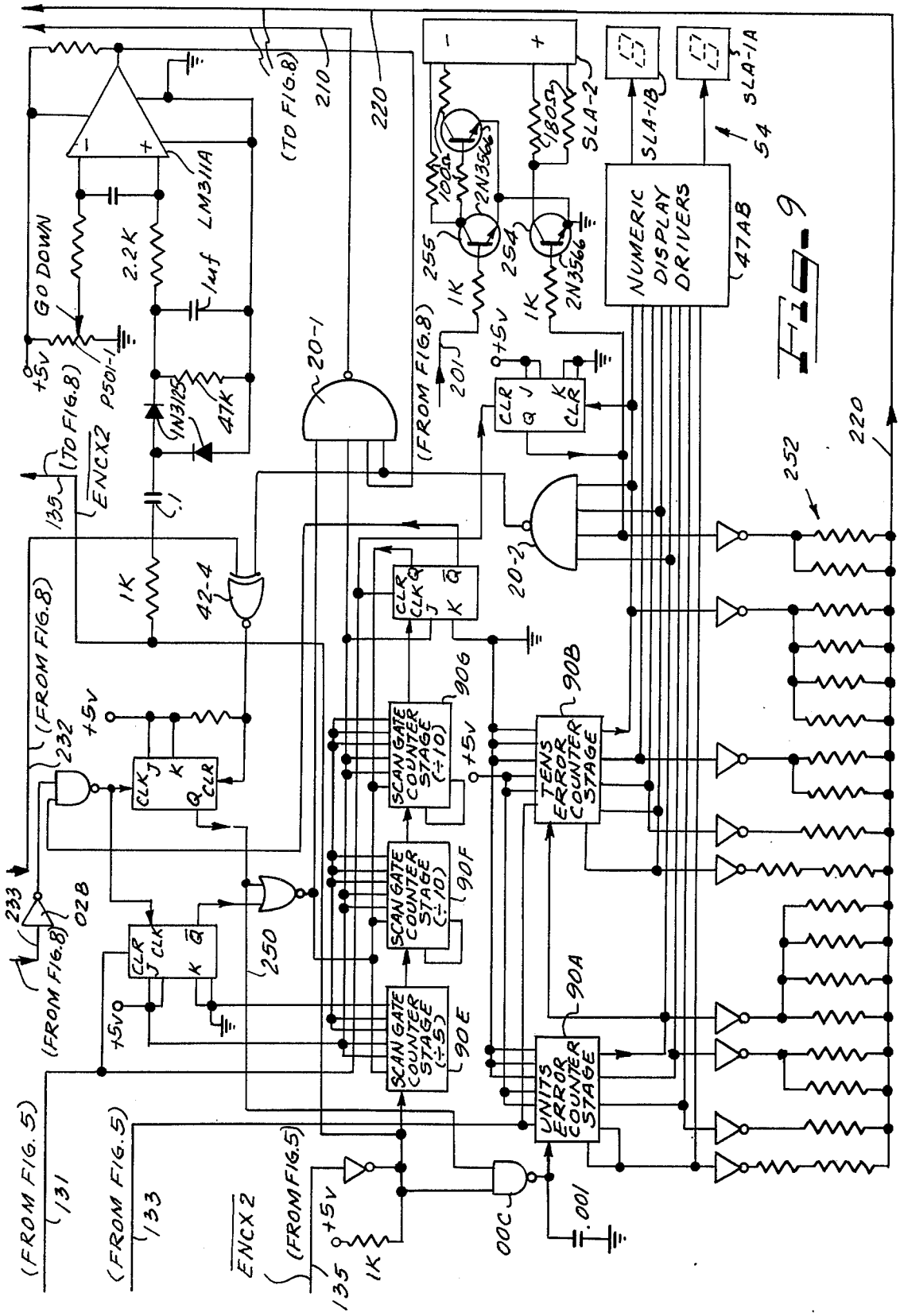

GO DOWN
+5v
P501-1
2.2K
1uf
LM311A
1N3128
47K
.1
1K
42-4
(TO FIG.8)
ENCX2
135
(FROM FIG.8)
232
233
02B
250
+5v
CLK J K Q CLR
CLR J CLK K Q
(FROM FIG.5)
131
133
ENCX2
(FROM FIG.5)
135
1K
+5v
.001
00C
20-1
20-2
210
220
(TO FIG.8)
(FROM FIG.8)
201
255
254
100Ω
2N3565
1K
2N3566
1/8Ω
SLA-2
SLA-1B
SLA-1A
54
NUMERIC DISPLAY DRIVERS
47AB
252
SCAN GATE COUNTER STAGE (÷10)
906
90F
SCAN GATE COUNTER STAGE (÷5)
90E
TENS ERROR COUNTER STAGE
90B
UNITS ERROR COUNTER STAGE
90A

Fig. 9

DISPLAY SYSTEM AND METHOD FOR REGISTRATION CONTROL EQUIPMENT

BACKGROUND OF THE INVENTION

In setting up registration control systems, it is essential to select marks for control purposes which occur reliably in the successive repeat lengths of the web and to exclude spurious marks from the inspection zone of the control. Longitudinal or lateral control of the web relative to a work station can be effected by selecting a suitable pair of marks and producing pulses as a function thereof during scanning of each repeat length of the web. Typically once suitable marks have been selected, the system is adjusted to that the pulses will occur in time coincidence when the web is in proper longitudinal or lateral register condition. Phase errors between such pulses can be used to generate error signals, and the web can be acted upon in response to such error signals to tend to maintain the desired register condition. Such controls may include blanking circuitry such that only pulses occurring during a fractional part of each cycle of operation will be processed for control purpose. The time interval in each cycle of operation when scanner pulses are accepted may be termed an inspection zone, and the system may be visualized as having an inspection window of limited extent through which a given section of the repeat length of the web will be viewed in each cycle of operation. By the provision of such an inspection window, and proper selection of the marks to be used for control purposes, spurious signals due to extraneous markings on the web can be excluded so as to insure a reliable operation of the registration control.

SUMMARY OF THE INVENTION:

The present invention relates to a display system and method for use with registration controls, and to a registration sensing system.

It is a principal object of the invention to provide a display system and method for displaying scanner signals during set-up of a registration control which display system provides for a high resolution display of a fraction of a repeat length of the web, but yet enables a convenient and simple progressive examination of the entire repeat length and a reliable locking onto a potential inspection zone, with the result that unstable or spurious scanner signals are readily discovered and excluded from the inspection window.

Another object of the invention is to provide a master display unit for a registration control which can be readily coupled to a series of work stations in succession during a set-up operation and wherein the outputs of one or both of a pair of scanners at each station are readily displayed.

A feature of the invention resides in the provision of a single multiturn continuous adjustment knob for manual turning to progressively examine successive potential inspection zones relative to the repeat length of a moving web. When rotation of the knob is interrupted the display is locked to the web so as to provide an apprently stationary view of the signals occurring during a potential inspection zone, that is a view through the inspection window. The cycling of a scan gate counter can be synchronized with the horizontal deflection of the display so that the inspection window of the register control will be accurately displayed for each setting of the adjustment knob.

A further object of the invention is to provide a register error sensing system for progressively adjusting the set point of the system in a convenient and economical manner.

A further feature of the invention resides in the provision of a continuously operable analog setting control for selectively setting any of a series of analog values of an analog characteristic within a given range, a cyclically operable pulse responsive generator generating an analog signal successively changing in the analog characteristics thereof over the given range, and the set point for the register error sensing circuit bearing a fixed relationship to the instant of time when a matching relationship is established between the selected analog setting and the generator output in each generating cycle.

Further objects, features and advantages of the invention will be readily apparent from the following detailed description taken in connection with the accompanying drawings, althrough variations and modifications may be effected without departing from the spirit and scope of the novel concepts of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS:

FIG. 1 is a diagrammatic illustration of an embodiment of the present invention, given by way of example and not by way of limitation;

FIG. 1A is a waveform diagram illustrating an exemplary pulse output from the index generator of FIG. 1;

FIG. 1B is a waveform diagram illustrating an analog signal successively changing in an analog characteristic thereof in successive generating cycles of a pulse responsive generator, specifically illustrated as a repeat length ramp generator in FIG. 1;

FIG. 1C illustrates an analog variable whose analog value with respect to the analog characteristic of the waveform of FIG. 1B is progressively adjustable within the range of values illustrated in FIG. 1B;

FIG. 1D illustrates the output of the analog selector circuit specifically shown as a channel amplitude selector in FIG. 1 in dependence on the amplitude setting as represented in FIG. 1C;

FIG. 1E shows scanner pulses as applied by one of the channel scanner preamplifiers of FIG. 1, the horizontal axis in FIG. 1E being in terms of encoder pulses the same as FIGS. 1A throught 1D;

FIG. 1F is a view similar to FIG. 1E, showing the output of the other channel scanner preamplifier of FIG. 1;

FIG. 1G is a waveform diagram intended to be on the same horizontal scale as FIGS. 1A through 1F, and showing a display reference displacement signal, specifically a horizontal deflection signal from the horizontal deflection circuits component of FIG. 1, in successive cycles of the cyclically operable reference displacement generator, specifically implemented as a cyclically operable horizontal deflection counter converter in FIG. 1;

FIG. 2 is a diagrammatic illustration of a display as produced pursuant to the operation as illustrated in FIGS. 1A through 1G, the horizontal axis in FIG. 2 representing the display reference displacement axis, and the vertical axis in FIG. 2 representing the signal display axis with respect to the display apparatus of FIG. 1;

FIG. 3 is a schematic electric circuit diagram illustrating a portion of a specific embodiment in accordance with the block diagram of FIG. 1;

FIG. 4 is a diagrammatic view illustrating the physical relationship between FIGS. 5 and 7–10, which taken together illustrate further portions of the electric circuit;

FIG. 5 illustrates exemplary electric circuitry for implementing the channel amplitude selector component of FIG. 1 in particular, as well as certain circuitry in accordance with the diagram of FIG. 1;

FIG. 6 illustrates circuitry which is coupled with the "scope trigger" output of FIG. 5 and which interconnected with the circuitry of FIG. 3 and FIG. 7 at the points indicated;

FIG. 7 illustrates certain of the scanner processing circuitry of the channel scanner processing and registration error sensing circuitry of FIG. 1;

FIG. 8 illustrates certain of the registration error sensing circuitry of the channel scanner processing and registration error sensing circuitry component of FIG. 1;

FIG. 9 illustrates further circuitry including a scan gate counter and an error counter of the channel scanner processing and registration error sensing circuitry of FIG. 1, and also illustrates certain details of the circuitry of the channel digital error display component of FIG. 1;

FIG. 10 on sheet 5 of the drawings illustrates an exemplary output driving circuit which is controlled by means of relay coils diagrammatically indicated at the upper right in FIG. 8; and FIG. 10A on sheet 5 of the drawings is an exemplary detailed view of a typical embodiment of the bidirectional output servo component of FIG. 10 and showing the coupling of the output motor with an error correction device for the moving web, an edge view of the web being shown in FIG. 10A, and a diagrammatic fragmentary plan view of the web being shown in FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS:

The block diagram of FIG. 1 shows components of the illustrated embodiment which are labeled so as to conform with the corresponding components of the detailed electric circuit of FIGS. 3 through 10. Thus, FIG. 1 is presented for the purpose of facilitating an understanding of the detailed embodiment, and is shown by way of illustration and not by way of limitation.

Description of FIG. 1

The present invention is particularly adapted for use with registration error sensing circuitry such as employed for the purpose of sensing a longitudinal or lateral registration condition between a moving web such as indicated at 10 and a work applying station such as work applying station B indicated diagrammatically at 11. Prior patents such as U.S. Pat. No. 3,468,201 issued Sept. 23, 1969, U.S. Pat. No. 3,594,552 issued July 20, 1971, U.S. Pat. Nos. 3,601,587 and 3,624,359 will illustrate the background with reference to typical longitudinal register control systems. Entirely similar circuitry is applicable with respect to the problem of control of the lateral position of the web relative to a work applying station or the like.

In the illustrated embodiment, web 10 is shown as being driven in the direction of arrow 12 by means of a suitable web drive 14. It may be assumed that at a work applying station A (not shown) marks such as indicated at A1–1 through A1–6 and such as A2–1 through A2–6 are applied to successive repeat lengths on the web along with patterns of work such as diagrammatically indicated at 15.

By way of example, at work applying station B, it may be desired to superimpose on the pattern of work 15 a further pattern of work so as to provide a resultant pattern of work as indicated at 17, the work applying station B being indicated as applying also marks B1–1 through B1–4 and B2–1 through B2–3 (the mark B2–4, not shown, being visualized as being currently applied to the web at the work applying station B).

For the sake of maintaining a longitudinal register condition between the patterns 15 applied at station A (not shown) and the further patterns applied at station B to form the composite pattern such as indicated at 17, scanners are arranged as indicated at 19 and 20 for photoelectrically sensing the passage of the respective A and B marks in longitudinal alignment therewith. The scanners 19 and 20 produce electrical signals as a result of the contrasting light reflective properties of the marks, and these signals are supplied to respective channel scanner preamplifiers as represented by block 21 in FIG. 1. The output scanner pulses from the preamplifiers are diagrammatically indicated in FIGS. 1E and 1F, the notation A1 in FIG. 1E, for example, indicating a pulse produced in response to scanning of one of the marks such as A1–1 on the web 10. Similarly, FIG. 1F indicates the output resulting from the sensing by scanner 20 of the different light reflective properties of the marks such as indicated at B1–1 and B2–1.

For the sake of the diagrammatic showing of FIG. 1, it is assumed that web drive 14 is suitably driven by a prime mover (not shown), and that the mechanical movement of the drive element 14 is coupled with a digital encoder component 24 and an index generator 25 by means of mechanical couplings as indicated at 26 and 28. For the sake of a specific example, it may be assumed that digital encoder 24 is driven so as to make one complete revolution during the movement of a repeat length of the web, the rotation of the digital encoder 24 being essentially in synchronism with the movement of the web, and the digital encoder providing a predetermined number of encoder pulses per revolution such as 10,000 so that each encoder pulse represents a predetermined uniform increment of movement of the web 10. FIGS. 1A through 1G each shows a horizontal axis measured in terms of encoder pulses, the number 20,000 in FIGS. 1A and 1B representing 20,000 encoder pulses, or two complete revolutions of the digital encoder 24. As explained in U.S. Pat. No. 3,468,201, for example, a single pulse per revolution of the digital encoder 24 may be generated by means of a device which is herein termed an index generator and represented by component 25. The output of the index generator is indicated in FIG. 1A as a series of pulses 31–33, one occurring for each 10,000 pulses (indicated by the symbol ENC). The index pulses of FIG. 1A thus represent electrically the successive repeat lengths of the web 10, and serve to coordinate the cycles of operation of the electrical system with the mechanical movement of the web 10. The successive index pulses 31–33 are also coordinated with the cyclical work operation at the work applying station B, for example. The index generator is shown as applying its index

pulse output to a repeat length ramp generator component **36** so as to reset this component in preparation for a new cycle of operation. As illustrated in FIG. **1B**, the ramp generator **36** may respond to successive encoder pulses to provide a progressively changing amplitude output as represented in FIG. **1B**. The output of the ramp generator **36** may be suppled in parallel to a number of channels, each channel associated with one of the work applying stations, and a channel amplitude selector component **38** being indicated which is associated with the work applying station B. The channel amplitude selector **38** is provided with a continuously rotatable knob **40** which in the illustrated embodiment is operable to continuously adjust an amplitude level over a range such as indicated by the arrows **42** in FIG. **1C**, corresponding to the range of variation of the analog output from generator component **36** as represented in FIG. **1B**. The amplitude selector **38** provides a pulse output as indicated at **43** and **44** in FIG. **1D** at the instant of time when the amplitude setting of knob of **40** coincides with the analog output from the ramp generator **36**. Thus, the phase of the pulses **43** and **44** may vary as a function of encoder pulses as represented by arrows **45** and **46** in dependence on the setting of the knob **40**.

Referring to the terminology of U.S. Pat. No. 3,594,552, the output pulse from the amplitude selector component **38** corresponds to an UNIT ZERO pulse and is herein termed an initiating signal. As will be understood from a consideration of U.S Pat. No. 3,594,552, and particularly the tenth figure of this patent, the output signal from selector **38** may represent the start of an inspection zone or a scanner gate interval, during which scanner pulses supply to the channel scanner processing and registration error sensing circuitry **50** will be effective in determining the registration condition with respect to a given repeat length of the web. As will be understood in the art, the effective scanner pulses may give rise to registration pulses within the circuitry **50** which will be time coincident when a given repeat length of the web is in register with respect to the work station **11**. The circuitry **50** receives encoder pulses from component **24** as indicated by coupling line **52** and is operable to show the number of encoder pulses corresponding to any registration error by means of the error display component **54**.

As previously discussed, in order to set up a registration error sensing circuitry, it is unnecessary to select suitable marks on the web which occur reliably in the successive repeat lengths, and are sufficiently clear of spurious signals so that they can be discriminated by means of the inspection zone or inspection window of the system. In the illustrated embodiment a cathode ray tube is indicated at **60** having a display face **62** with a horizontal or reference displacement axis and a vertical or signal display axis.

The illustrated circuitry provides for the initation of a display cycle of the apparatus **60** in response to the initiating signal output from component **38**. In particular a selector switch **S1** is shown as having a position **S1–4** whereby the switch is connected with the output of the selector component **38**. In other positions of the selector **S1**, connection is made with the output of corresponding amplitude selectors with respect to other work stations (such as a work station C, not shown). With the selector **S1** in the position shown, the output of selector **38** is supplied through a pulse shaper **64** so as to provide a cyclically occurring display control pulse as represented in FIG. **1D** and whose occurrence relative to web movement is progressively adjustable by means of knob **40**. The pulses of FIG. **1D** are shown as being supplied to a bistable display control circuit indicated at **66** which serves to initiate the successive display cycles by resetting an encoder pulse rate divider **68** and a cyclically operable horizontal deflection counter converter **70** in the specific illustrated embodiment. The component **70** is shown as having a switch **72** at its input for selectively supplying encoder pulses directly thereto, or supplying pulses via the pulse rate divider **68**. With the switch **72** in the position shown, the display apparatus **60** will essentially provide a full horizontal deflection corresponding to the inspection zone of the circuitry **50**, and this switch position has accordingly been designated I.Z. In the alternative lower position of switch **72**, full deflection of the display apparatus **60** will take place during all revolution of encoder **24** and thus will correspond to a full repeat length on the web. The lower switch contact has accordingly been designated (F.R.). FIG. **1G** shows the output from horizontal deflection circuits component **74** with the switch **72** in the upper position. As indicated in FIG. **1G** and FIG. **2**, under these circumstances, the full deflection of the display apparatus **60** with respect to the horizontal or reference axis will take place in response to **500** encoder pulses as supplied from component **24**. Thus, the pulses appearing in FIG. **2** in solid outline, are intended to correspond to an inspection zone such as defined by the occurrence of display pulse **44** in FIG. **1D**. FIG. **2** may be taken as indicating that the pulse **A2** which occurs in response to marks such as **A2–1** and **A2–2** during continuous movement of the web, will not be displayed since it occurs outside of the **500** encoder pulse inspection zone which is actually shown at the display face **62** of apparatus **60** in response to a display signal **44**.

Component **70** may conveniently comprise a counter for counting encoder pulses and for actuating gate **76** at such time as the counter has reached a count of 500. Thus at the end of the 500 count interval indicated in FIG. **2**, gate **76** will signal the display control circuits **66** and thus cause the termination of a display cycle prior to the occurence of the signal as indicated at **A2** in FIG. **1E** and FIG. **2**. The counter of component **70** may drive a digital to analog converter also a part of component **70** and the output of the digital to analog converter of component **70** may supply the input to the horizontal deflection circuits **74** so as to provide the deflection signal as represented in FIG. **1G**.

As further represented in FIG. **1**, the scanner signals of FIGS. **1E** and **1F** may be selected by means of selector switches **S2** and **S3** which may be ganged for joint operation with selector **S1**. Thus, selectors **S2** and **S3** are shown as disposed at positions **S2–4** and **S3–4** so as to receive the scanner signals with reference to station B. These scanner signals are supplied to a vertical deflection control input signal circuits component **80** which in turn controls the vertical or signal display axis of apparatus **60** corresponding to the vertical axis in FIG. **2**. For displaying the outputs of both scanners **19** and **20** during an inspection zone interval, the output of display control circuit **66** may be coupled to the clock input of a JK flip-flop **82**, the outputs of the flip-flop alternately enabling transmission of the A and B scanner signals, so that a signal **A1** is generated during

one display cycle, and a signal B2 is generated in the next display cycle, the two signals being in effect superimposed on the display face **62** where the display face **62** has a suitable persistence or other memory feature, properly related to the normal operating speed range of the web **10.** Thus if at a normal speed of the web, movement would be at a rate of two repeat lengths per second, then the display apparatus **60** should be capable of providing a persistent signal without substantial flicker where the signals occur at the rate of one pulse per second. Of course, the persistence of the display face **62** should not be such as to interfere with an accurate appraisal of the currently occurring scanner pulses.

Description of the Circuitry of FIGS. 3–10A

Certain of the circuit detail of the illustrated circuit is similar in principle so that described in detail U.S. Pat. No. 3,812,351 issued May 21, 1974, so that a less detailed description is suitable herein. In numerous cases, as in the mentioned patent, reference characters are applied which correspond to the last two digits of commercial designations for transistor transistor logic integrated circuits. Thus, for example, in FIG. **3** the ramp generator counter stages are given designations **93C, 93D** and **93E,** and suitable implementing circuitry would comprise mediumscale integration four-bit binary counters commercially available as circuit types SN 7493. Similarly, the input JK flip-flop designated **73–1** could be implemented as a circuit type SN 7473. The reference characters utilized in FIG. **1** have been repeated in FIGS. **3** through **10** where applicable so as to further facilitate a review of the detailed circuit. Also, reference characters in such as (1A) shown at the left in FIG. **3** indicate that the waveform of the corresponding figure number, i.e. FIG. 1A, would be supplied at the indicated circuit location.

In order to facilitate implementation of the specific illustrated circuit, should be desired, specific circuit values have been indicated for the components of the detailed circuit. In this respect, the notation K as applied to a resistor refers to a value of resistance in kilohms. Capacitance values are indicated by a decimal number are in microfarads in each case. Other values of capacitance are indicated using the notation μf, standing for microfarads or *pf* standing for picofarads (10^{-12} farads). Resistance values or less than 1 kilohm (1K) are indicated with the conventional symbol for ohms(Ω).

FIG. 3

Referring to FIG. **3,** at the upper left, the input index pulses are supplied to transistor **Q303,** driving a gate **00–1** (a circuit type SN 7400, for example). The output of this circuit via conductor **101** serves to reset the stages of the ramp generator **36,** whereupon it begins counting encoder pulses as applied to input **102** at the left in FIG. **3.** A digital to analog converter **104** of component **36** generates the ramp output waveform of FIG. **1B** at output conductor **105.** A reset pulse is supplied to conductor **107** shown at the upper right in FIG. **3** from component **66,** FIG. **1,** and serves to reset pulse rate divider **68** (circuit type SN 7490, for example), and counter stages **93A** and **93B** of horizontal deflection counter coverter component **70,** shown at the lower right in FIG. **3.** The component **70** includes a digital to analog converter **110** for driving horizontal deflection circuits **74** to produce the horizontal deflection waveform of FIG. **1G** at conductor **111** leading to one of the horizontal deflection plates of cathode ray tube **60.** When the counter stages **93A** and **93B** of component **70** reach a count corresponding to the extent of the inspection zone of circuitry **50,** FIG. **1,** gate component **76** (for example a type SN 7430) will supply an output signal to its output line **112** leading to FIG. **6.**

The vertical deflection signal from component **80,** FIG. **1** is supplied to the vertical deflection plates of cathode ray tube **60** via conductors **115** and **116** which originate in FIG. **6.**

The circuit associated with transistor **Q305** at the upper left of FIG. **3** controls circuitry in FIG. **6** via a conductor **120.**

FIG. 5

Referring to FIG. **5,** it will be observed that the waveform of FIG. **1B** is supplied via line **105** to a minus input of a differential/operational amplifier **741C** (circuit type SN 72741, for example). The plus input terminal of amplifier **741C** is coupled with the movable contact **122** of a potentiometer **123** which is operated by the knob **40** and may be implemented as a ten turn, 2,000 ohm potentiometer for controlling the analog setting represented in FIG. **1C.** Upon the matching of analog signal levels at the two inputs of the amplifiers **741C,** an output signal termed "Scope Trigger" is supplied to conductor **125** leading to FIG. **6.**

The output of amplitude selector **38** is also applied to a transistor **Q306–1,** whose output triggers a monostable circuit **130.** The output of monostable **130** in turn drives a series of gates so as to produce output pulses at conductors **131, 132** and **133.**

The circuit at the lower part of FIG. **5** involving transistor **Q307–1** may serve to double the encoder pulse rate so as to supply at output conductor **135** pulses at a rate of 20,000 per revolution of encoder **24,** for example.

The monostable multivibrator **130** may comprise a type SN 74121, for example. The commercial data for this type of circuit indicates that for an applied voltage between five and **5.25** volts, pulse width is defined by the relationship t_p (out)$=C_T R_T \log_e 2$. Jitter-free operation is said to be maintained over the full temperature range for more than six decades of timing capacitance (10 *pf* to 10 μf) and more than one decade of timing resistance (2,000 ohms to 40,000 ohms). Thus, the circuit parameters for R330 (16 kilohms) and C313 (22 microfarads) are assumed to give a time constant of roughly 255 milliseconds.

Since with this type of circuit, once the monostable has been triggered, the outputs are independent of further transitions on the input and are a function only of the timing components, monostable **130** will inherently adaptably regulate the number of cycles which can be initiated by the "Scope Trigger", and is selected to reduce the number of error cycles of the error sensing circuitry at relatively high web speeds, while accommodating error correction operation for each repeat length of the web at somewhat lower speeds.

For an embodiment with a similar output circuit, but utilized for lateral register control of a moving web, the type SN 74121 monostable utilized a resistor such as **R330** with a value of 30,000 ohms, and a capacitor corresponding to **C313** again of 22 microfarads.

The monostable **130** of FIG. **5** is part of the registration error sensing circuitry of component **50,** and the connection between component **38** and the monostable circuit is indicated by conductor **140** in FIG. **5** and by line **140** in FIG. **1.**

FIG. **6**

The Scope Trigger input **150** at the upper left in FIG. **6** corresponds to line **150** at the output of selector S1 in FIG. **1.** The bistable **66** is triggered in response to the display control signals such as **43** and **44** in FIG. **1D,** and the output from gate **01–2A** which is applied to conductor **107** serves to reset the horizontal deflection counter converter component **70,** FIGS. **1** and **3.** The output of gate **01–1A,** at this time, will be effective to enable gates **00–1B** and **00–2B,** providing the go down circuit associated with transistor Q305 at the top of FIG. **3** has not applied a ground potential to conductor **120.** That is, if the web speed is below a selected minimum, the corresponding encoder pulse rate will be such as to enable charging of capacitor **152** at the top of FIG. **3,** turning the transistor W305 at the top of FIG. **3** "on", that is to the conducting condition, so as to apply ground potential to conductor **120.** Thus at speeds of the web below the minimum speed, gates **00–1B** and **00–2B** in FIG. **6** will be blocked, and output lines **155** and **156** will be at ground potential to block transistor Q300 and Q302–1, thus preventing the appearance of vertical deflection signals at output conductors **115** and **116** at the right in FIG. **6** in response to scanner signals occuring during the inspection zone. If the web speed is adequate for suitable operation of the display apparatus **60,** then gates **00–1B** and **00–2B** will be enabled in response to the successive display control signals such as **43** and **44** in FIG. **1B** so as to enable display of selected scanner signals during the inspection zone.

As indicated in the top center of FIG. **6,** a display control switch **160** has three positions. In the indicated open circuit condition, scanner signals A1 and B2 are displayed in alternative cycles of the display apparatus so as to provide a resultant composite display as indicated in FIG. **2.** If selector **160** is placed in the second position designated "Ch2" in FIG. **6,** then flip-flop **82** (which may be a circuit type SN 7473) is placed in an actuated condition in response to the first occurring clock pulse, and thereafter continuously enables the lower scanner channel involving transistor Q302–1. Similarly, if selector **160** is in the lower position, flip-flop **82** is locked in the opposite (reset) state to enable transistor Q300.

Regardless of the state of transistors Q300 and Q302–1, the scanner signals such as indicated at FIGS. **1E** and **1F** are supplied via conductors **171** and **172** to the error sensing circuitry of FIG. **7.** A socket is indicated at **174** for receiving a scope probe useful in trouble shooting the circuitry and the like. With a probe inserted in socket **174,** signals from the probe are substituted for the usual scanner signals from the scanners **19** and **20.**

FIG. **7**

FIG. **7** illustrates channel scanner processing circuitry which forms part of component **50,** FIG. **1,** the pulse outputs at conductors **181** and **182** being supplied to the circuitry of FIG. **8.** It will be noted that flip-flops **74A–1** and **74A–2** at the right in FIG. **7** must be reset from conductor **132** at the beginning of each inspection zone, or else the error sensing circuitry will be unable to carry an sensing cycle. Thus, at relatively high web speed, where a monostable circuit **130,** FIG. **5,** fails to respond to alternate scope trigger pulses, for example, scanner pulses will also be blocked during alternate potential inspection zones.

FIG. **8**

In FIG. **8,** the scanner signals arrive via conductors **181** and **182** and are selectively routed by means of a three pole double throw switch **191** controlled by means of a shiftable contact **192.** The condition of the switch **191** may be selected so that the leading scanner pulse, such as pulse A1 as seen in FIG. **2,** will be transmitted to output **194** and thence to the offset counter comprising stages **90C** and **90D.** The offset counter as indicated has thumb wheel switches as indicated at **195** and **196** for selecting a desired count value between zero and **99** with respect to the double rate encoder pulses supplied via conductor **135** from FIG. **5.**

When the offset counter has completed the desired counting cycle, an output is supplied from comparator stages **42A** and **42B** via conductor **197,** and this pulse serves to reset bistable circuit **198** and supply a delayed scanner pulse to output **199** of the switch **191.** Accordingly bistable **200** will assume a final condition in accordance with any significant error in phase between the two scanner pulses and supply a corresponding polarity siganl to conductor **201** or conductor **202.**

If polarity indicating conductor **201** is high, transistor Q507 will be enabled to allow energization of the relay coil designated REED **2.** On the other hand, polarity indicating conductor **202** is "high," then transistor Q508 will be enabled to permit energization of the actuating coil designated REED **1.**

During the counting of encoder pulses to determine the error between the signals arriving at the respective inputs to flip-flop **200,** the potential at conductor **210** at the extreme right in FIG. **8** will be high, turning on transistor Q504–1 at the upper left in FIG. **8.** This in turn will turn on transistor Q505–1, and allow the discharge of capacitor **212.** At the end of the inspection zone during proper operation, the potential conductor **210** will return to ground level, turning off transistors Q504–1 and Q505–1 and enabling the charging of capacitor **212.** The charging circuit for capacitor **212** extends from supply line **214** to movable tap **215** of potentiometer P500, and to the upper plate of capacitor **212,** and from the lower plate of capacitor **212** through resistor **216** and potentiometer P501 to ground. As the capacitor **212** pregressively charges, the potential of the plus input of amplifier RM311B progressively decreases. The extreme right hand conductor **220** in FIG. **8** reads from the error analog output of the error sensing circuitry and is applied to the minus input of amplifier LM311B. Thus, when capacitor **212** has charged sufficiently so that the potential at the upper input of LM311B matches the error signal at the lower input, and output pulse occurs at output line **221** (providing transistor Q504–1 is nonconducting so that conductors **222** and **223** can approach supply potential. As capacitor **212** continues to charge, transistor Q506 is held on energizing the selected one of the coils REED **1** or REED **2,** and this results in turn on of the error correction servo for a time interval substantially linearly proportional to the error count determined by the error

sensing circuitry. The linearity of the digital to analog converter circuit associated with the error counter is compensated by the complementary nonlinearity of the capacitor charging circuit for capacitor **212**, so that the resultant on time of the selected REED relay will be linearly proportional to error count within approximately ten percent, for example. Potentiometer **P500** is adjustable to define the extent of a "dead zone" within which small errors will not cause the actuation of the output circuitry. Potentiometer **P501** serves as a gain adjustment for the error count of "on time" circuit.

Referring to the circuitry at the lower left in FIG. **8**, monostable circuit **230** responds to substantial simultaneity at the conductors **231** and **199** of switch **191** and supplies a corresponding control signal to output conductor **232** leading to the circuitry of FIG. **9**. Conductor **233** transmits the information with respect to the scanner phase to the circuitry of FIG. **9**.

FIG. 9

As indicated at the upper left in FIG. **9**, a reset signal is received from conductor **131** of FIG. **5** in response to the Scope Trigger signal. The result is that the inspection zone of the sensing circuitry of FIG. **9** is synchronized with the active display cycle of the display apparatus as represented in FIG. 1G. Thus, the display apparatus will display the scanner signals which are actually effective within the error sensing circuitry of FIG. **9**. In particular, the reset signal at conductor **131** at the upper left in FIG. **9** serves to reset the scan gate counter comprising stages **90E**, **90F** and **90G** at the center left of FIG. **9**. Similarly, the reset pulse of conductor **133** at the upper left serves to reset the stages **90A** and **90B** of the error counter at the beginning of the inspection zone, or scan gate interval.

When the leading pulse such as pulse A1 shown in FIG. **2** arrives via conductor **233** at the upper left of FIG. **9**, the counter error counter stages **90A** and **90B** are enabled via conductor **250**, and the error counter begins counting the double rate encoder pulses supplied at input **135**. The digital to analog converter **252** serves to supply an analog error signal to conductor **220** leading to the output control circuit of FIG. **8** previously discussed. The error count is also supplied to component **47AB** at the lower right in FIG. **9** and to transducer **254** so as to produce the digital error display in accordance with the registered error count. Transistor **255** of the display **54** is controlled from conductor **201** leading from the polarity sensing bistable **200** of FIG. **8**. Thus, the correct polarity (plus or minus) is displayed in accordance with the time of arrival of the pulses at conductors **199** and **231** in FIG. **8**.

If the error sensing circuitry is operating properly and the second scanner signal arrives within the inspection zone, the output of gate **20–1** will supply a ground potential to conductor **210** at the end of the inspection zone, enabling the output circuit of FIG. **8** as previously described.

FIGS. 10 and 10A

FIGS. **10** and **10A** on sheet **5** of the drawings illustrate the output drive circuit which is indicated as being controlled by the relays REED **1**, REED **2** and REED **3** of FIG. **8**. Component **270** in FIG. **10** represents any suitable bidirectional output servo which may respond to alternating current energization applied between supply lines **271** and **272**. With the energization of reed coil REED **1**, alternating current potential may be supplied to conductor **274** in FIG. **10**, while with the energization or reed relay coil REED **2**, alternating current potential may be supplied to conductor **275**.

FIG. **10A** illustrates an exemplary embodiment of bidirectional output servo **270** comprising a pair of rectifiers **281** and **282** controlling the polarity of energization of the armature winding of a direct current motor **283** having a permanent magnet field. The output of the motor as indicated by dash line **284** may be coupled to a web compensating device **285** so as to actuate the device in a direction tending to return the web to the desired longitudinal registration condition at the work station B indicated in FIG. **1**.

Summary of Operation

Thus, with the illustrated embodiment, an analog adjustment knob **40** shown at the upper center at FIG. **1** and at the left center of FIG. **5** is continuously adjustable, for example, through ten turns, to continuously vary the portion of a repeat length of the web which is displayed by means of the display apparatus **60**. The portion displayed is advantageously keyed to the inspection zone or scanner gate interval defined by the sensing circuitry **50** shown at the lower right in FIG. **1**. This inspection zone is defined by the count capacity of the scan gate counter stages **90E**, **90F** and **90G** at the center left in FIG. **9**. Where the scan gate interval corresponds to 500 encoder pulses, gate **76** shown at the center right of FIG. **1**, may be coupled with the horizontal deflection counter to terminate a display cycle at a corresponding count of encoder pulses. In the specific circuitry indicated, the scan gate counter counts double rate encoder pulses, and the deflection counter of component **70** indicated at the lower right in FIG. **3** is set to trigger gate **76** at a count of 248 (corresponding to 496 double rate encoder pulses). Thus, the display indicated in FIG. **2** would actually represent 496 double encoder pulses, but would still essentially correspond to the extent of the inspection zone or scan gate interval of the registration error sensing circuitry of component **50** shown at the lower right in FIG. **1**.

Of course, if switch **72** shown in the center of FIG. **1** is shited to the lower portion, then the encoder pulse rate may be divided be a factor such as **20** prior to being supplied to the horizontal deflection counter of component **70**, and gate **76** may not terminate a display cycle unitl a count of 9,920 encoder pulses (corresponding to 19,840 double rate encoder pulses).

With the aid of the display apparatus **60**, the control **40** may be manipulated until stable scanner pulses appear on the display as represented in FIG. **2**. Since the display apparatus is locked to web movement, stable scanner pulses occurring in response to uniform marks in the successive repeat lengths of the web will be readily apparent, while unstable marks can be avoided and spurious markings are readily excluded from the inspection zone.

It should be noted that the control knob **40** is convenient and economical method of adjusting the phase of the inspection zone with respect to a repeat length on the web, irrespective of whether the control also effects a corresponding adjustment with respect to an inspection zone display.

While a cathode tube is a convenient type of display and relatively economical at the present time, it will be understood that other types of displays having acyclical

reference displacement axis and a display signal axis can be readily substituted for the particular device illustrated herein by way of example.

It will be apparent that many further modifications and variations may be effected without departing from the scope of the novel concepts of the present invention.

We claim as our invention:

1. A display system for use with equipment involving coordinated mechanical movements during the operation thereof, comprising,

an encoder for coupling with mechanical movement in the equipment and operable for generating encoder pulses as a function of successive uniform increments of the mechanical movement coupled thereto,

display apparatus having a visual display and having a first scanning control input for producing scanning along a first coordinate axis in successive scanning cycles of the display and having a second scanning control input for producing display of input signals with respect to a second coordinate axis of the display,

a cyclically operable deflection counter converter connected with said encoder and operable for cyclically generating a first deflection signal as a function of the mechanical movement coupled to the encoder, and connected with said first scanning control input of said display apparatus and operable in response to an actuating signal for supplying said first deflection signal thereto to control a scanning cycle of said display apparatus,

input signal means responsive to mechanical movement to be coordinated with the mechanical movement coupled to said encoder to produce cyclically occurring input signals and connected with said second scanning control input to supply said input signals thereto,

a cyclically operable ramp generator connected with said encoder and responsive to successive encoder pulses from said encoder to produce a ramp output incrementally changing in amplitude over a given amplitude range in each cycle of operation, and

an amplitude selector progressively adjustable to any selected amplitude setting corresponding to any of the amplitudes of said ramp output within said amplitude range and operable to generate an actuating signal in each cycle of operation of the ramp generator when the amplitude of the ramp output reaches the selected amplitude setting, and connected with said deflection counter converter to supply said actuating signal thereto and thus to initiate the successive scanning cycles of said display apparatus in accordance with the selected amplitude setting of said amplitude selector.

2. A display system in accordance with claim 1 with said ramp generator having a cycle of operation corresponding to a predetermined number of encoder pulses representing mechanical movement corresponding to a repeat length of a moving material being acted upon by the equipment, and

said deflection counter converter being operable to produce full deflection of the display apparatus in response to a lesser number of encoder pulses which lesser number is only a fraction of said predetermined number of encoder pulses, thereby to enable full deflection visual display on input signals with respect to any selected portion of successive repeat lengths of the moving material.

3. A display system in accordance with claim 2 with a pulse rate divider selectively connectable in circuit between said encoder and said deflection counter converter to provide for full deflection of said display apparatus in response to said predetermined number of encoder pulses, thereby to selectively visually display input signals occurring with respect to substantially a complete repeat length of the moving material.

4. A display system in accordance with claim 1 with said counter converter having a bistable display control coupled to said amplitude selector for actuation by said actuating signal to an active condition to initiate a cycle of operation of said counter converter and for actuation to an inactive condition when the counter converter has completed its cycle of operation, said input signal means having a pair of controllable input signal circuits for selectively transmitting respective input signals to the second scanning control input of said display apparatus, and a toggle circuit connected with said bistable display control for actuation to alternate states in alternate cycles of said counter converter, and controlling said input signal circuits to provide for the alternate activation of said pair of input signal circuits and thereby to enable the super position at said visual display of the respective input signals transmitted by the respective input signal circuits.

5. A display system in accordance with claim 1 with respective amplitude selectors for association with respective stations along a path of movement through the equipment, and selector switches for selectively connecting the respective amplitude selectors in circuit with said ramp generator and said first scanning control input, and for simultaneously supplying input signals from the respective corresponding stations to said second scanning control input.

6. In a register error sensing system for sensing errors in register between successive repeat lengths of a moving web and successive work stations operatively disposed along the path of the web, said system comprising:

an encoder responsive to web movement and operable for generating encoder pulses as a function of successive uniform increments of such movement,

an index generator operable to issue an index pulse each time the web moves a distance corresponding to a repeat length thereof and thereby to define successive cycles of operation relative to said web movement,

register error sensing circuitry responsive to an initiating signal in said successive cycles of operation to define a set point representing a registration condition between the web and one of said stations and operable in response to a scanner signal from such station to generate an error signal as a function of any departure from the desired register condition as defined by said set point,

a cyclically operable pulse responsive generator connected with said encoder and with said index generator and responsive to the successive index pulses to initiate successive generating cycles, and operable in response to said encoder pulses in each generating cycle to generate an analog signal successively changing in an analog characteristic thereof over a given range of analog values, and

an analog selector circuit progressively adjustable to any selected analog setting corresponding to any of the analog values of said analog characteristic within said given range and responsive to a matching relationship in said analog characteristic between said successively changing analog signal and said selected analog setting of said selector circuit for generating said initiating signal and connected with said register error sensing circuitry for supplying said initiating signal thereto, whereby the set point for said register error sensing circuitry is progressively adjustable to establish the desired set point relative to said successive cycles of operation.

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