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3,383,526

CURRENT DRIVER CIRCUIT UTILIZING TRANSISTORS

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2 Sheets-Sheet 1

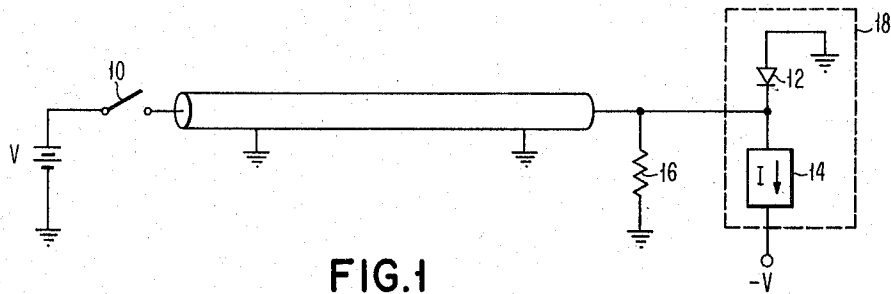


FIG. 1

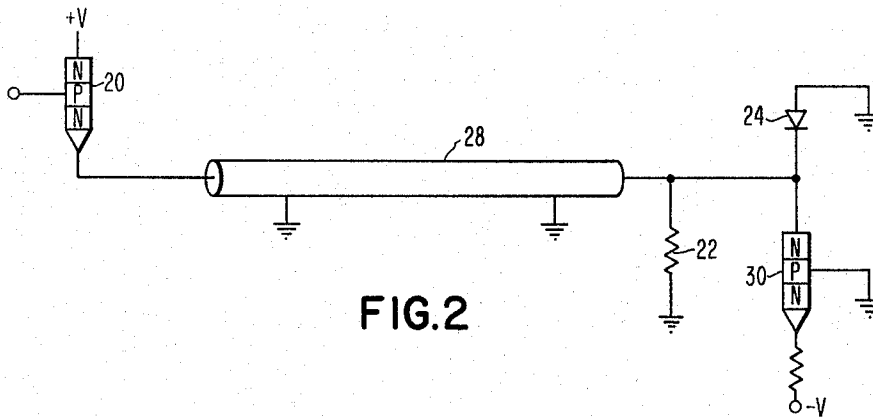


FIG. 2

FIG. 4b

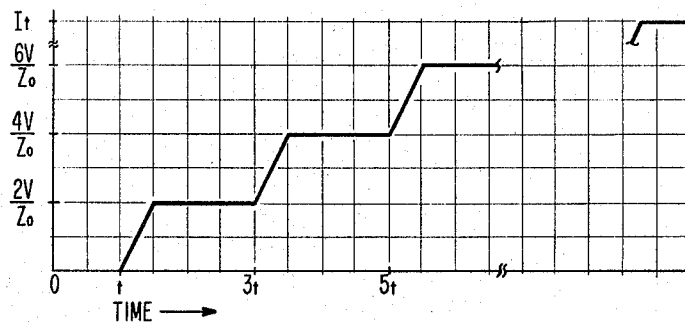
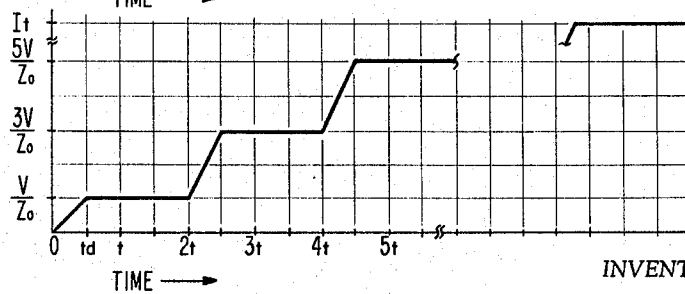


FIG. 4a



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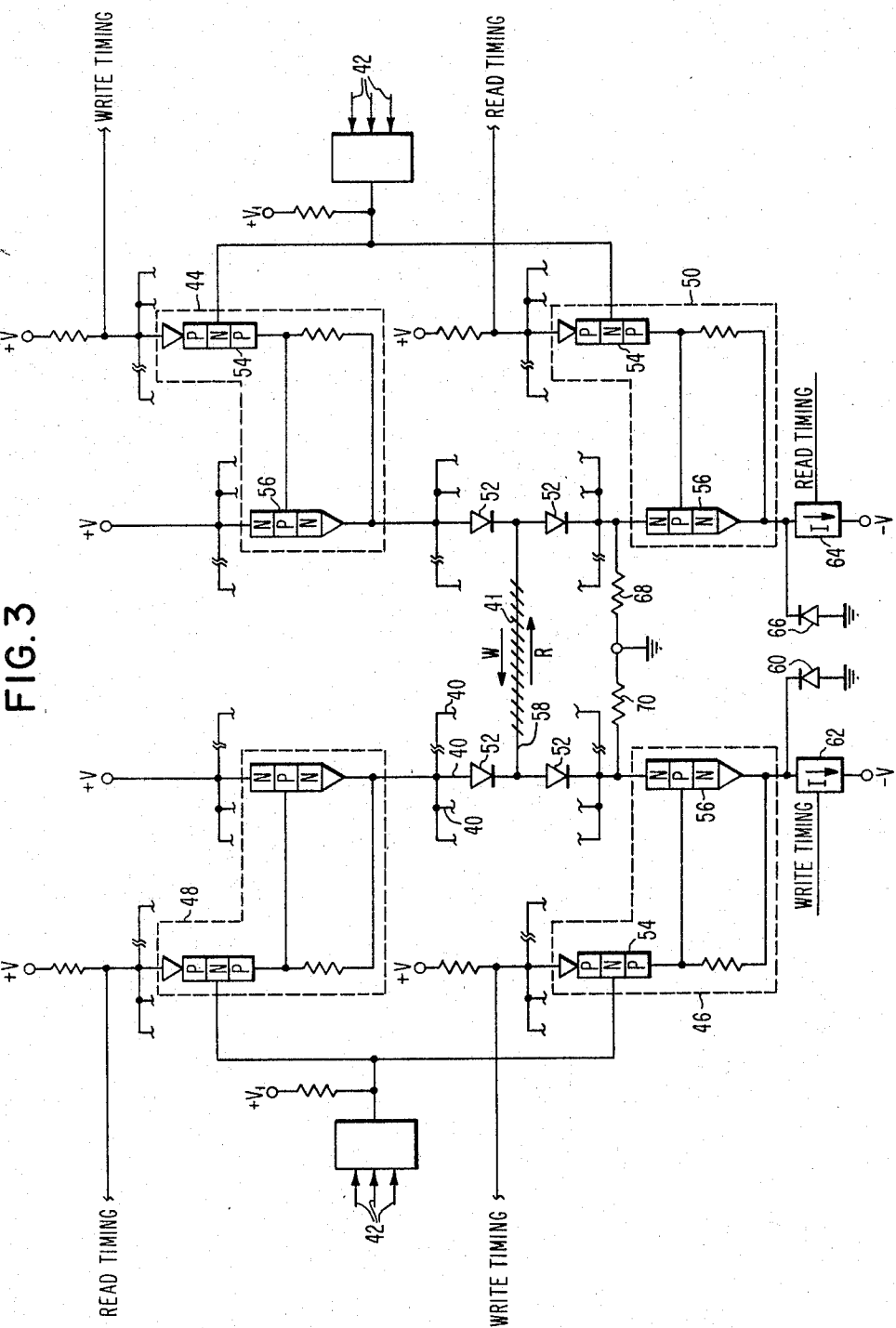
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CURRENT DRIVER CIRCUIT UTILIZING TRANSISTORS

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ABSTRACT OF THE DISCLOSURE

A low impedance voltage source is coupled to drive a current pulse down a line terminated by an impedance element shunted by a second termination comprising a current sink coupled to normally forward bias a diode. The voltage source is turned on to produce an initial current wave on the line and the forward biased diode appears as a short circuit to this initial current wave on the line. The current wave is reflected successively between the shorted termination and the voltage source, and the reflected current adds to the incident current to produce a higher current. When this current amplitude reaches the current accepted by the current sink, the diode becomes reverse biased and the line is then terminated by the impedance element. The result is a current pulse having the fastest rise time to the final line current from a given voltage source.

Background of invention

This invention relates to driver circuits and, more particularly, to current driver circuits useful for driving inductive loads such as magnetic cores.

High speed transistor logic circuits are characterized by the use of small signal swings so that only a relatively small voltage is required by such circuitry. However, when current drivers are utilized in a system with only the low voltage available, a problem is encountered in obtaining a current drive pulse having a sufficiently fast rise time in applications where an inductive load is driven, such as in drivers for a magnetic core memory, for example. It is therefore a principal object of this invention to provide an improved driver circuit having the ability to deliver a current pulse having the fastest possible rise time to a predetermined current from a given supply voltage.

It is another object of this invention to utilize the normally detrimental reflections on a drive line to build up the current to a predetermined amplitude in the fastest possible time from a given supply voltage.

It is a further object of this invention to utilize a nonlinear termination on a line to obtain fast rise time to a predetermined current.

According to the invention, a current sensitive device having a nonlinear impedance is provided to terminate a line to obtain the fastest possible rise time to a predetermined current from a given supply voltage. The initial driving current pulse is propagated down the line and reflected from the nonlinear termination due to the low impedance state of the termination. The reflected wave is in phase with the incident wave and adds thereto. The wave is again reflected at the input end of the line due to the low impedance of the driving source. The wave is continually reflected from the input end of the line to the termination end until the current on the line reaches the predetermined value. At this time, the nonlinear termination changes to the high impedance state so that the line is then terminated by an impedance element.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment

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of the invention, as illustrated in the accompanying drawings.

FIG. 1 is a diagrammatic, schematic diagram of a drive system embodying the invention.

FIG. 2 is a specific embodiment of a circuit employing the invention.

FIG. 3 is a schematic diagram of a magnetic core memory drive circuit embodying the invention.

FIG. 4a is a plot of current amplitude versus time at the input end of the line.

FIG. 4b is a plot of current amplitude versus time at the output end of the line.

With reference to the drawings in FIGS. 1 and 4, a voltage source V is coupled to drive a current pulse down a line terminated by an impedance element 16 shunted by a current sensitive device 18 comprising a current sink 14 coupled to normally forward bias a diode 12 . With switch 10 open, the only current flowing in the circuit is from the signal reference potential through the diode 12 to the current sink 14 , and this current flow forward biases diode 12 . When switch 10 is closed, an initial current wave is propagated down the line of amplitude V/Z_0 , where Z_0 is the characteristic impedance of the line. The forward biased diode 12 appears as a short circuit to the current wave on the line so that, when the current wave front approaches the termination end of the line, the current is reflected, and the reflected current adds to the incident current since they are in phase. The amplitude of the resultant current is then $2V/Z_0$. If this current amplitude is less than the current I accepted by current sink 14 , then diode 12 remains forward biased and the reflected current travels back to the input end of the line. The reflected current again reflects off the low impedance voltage source, and at this time the resultant current amplitude of $3V/Z_0$ exists on the line. The current wave continues to reflect back and forth until the current at the terminating end of the line exceeds I . When this condition occurs, diode 12 becomes reverse biased and thus changes to the high impedance state. The resulting termination is current sink 14 shunted by R_0 . By Thevenin's theorem, this is equivalent to the line being terminated in a voltage $I R_0$ in series with R_0 . The line is thus terminated in R_0 , resulting in no further reflections, and the amplitude of the final current on the line is

$$\frac{V + I R_0}{R_0}$$

which is equal to

$$\frac{V}{R_0} + I$$

From this relationship, any desired current amplitude can be obtained by the choice of I for a given voltage and characteristic impedance.

A specific circuit embodying the invention is shown in FIG. 2. The voltage source is provided by a transistor 20 which is saturated when a positive voltage pulse is applied to the base electrode. The output of the voltage source is coupled from the emitter to the input end of the line 28 to be driven, and the termination of the line to be driven comprises a resistor 22 returned to the signal reference potential of ground potential. The current sensitive device comprises a diode 24 connected to the line and returned to ground and a current sink comprising a transistor 30 connected in a grounded base circuit so that diode 24 is normally forward biased due to the current flow from ground through the diode and the current sink. Line 28 comprises any suitable device whose characteristics resemble a transmission line. Although the invention is not so limited, the invention is especially suitable for applications wherein a current pulse is driven to an inductive load such as the drive lines of a magnetic core

memory, for example. The incident current wave on line 28 is reflected by the substantially short circuit termination comprising forward biased diode 24. The current wave then doubles in amplitude, and the wave is reflected back toward the input. The low impedance of conducting transistor 20 causes the current wave to be reflected again toward the load end of line 28. The reflections continue with each reflection adding a unit of current equal to the incident current wave until the current value exceeds the current accepted by current sink transistor 30. At this time, diode 24 is back biased so that the line is then terminated in resistor 22, which is chosen equal to the characteristic resistance of line 28, in series with a voltage $I R_0$ as stated above. Thus, it can be seen that part of the final current on the line is supplied by the voltage source 20 and part of the current is supplied by the current sink 30. Thus, the circuit possesses the advantage of the most rapid buildup of current on the line to the final value from a particular voltage supply V .

FIG. 3 shows the invention embodied in a magnetic core memory drive system. A cross section of the drive system is shown. A plurality of array lines 40 are provided, and each array line is coupled for driving a plurality of magnetic cores 41. To select any one array line 58, a driver and a gate are simultaneously selected by their respective address lines. For example, to select the array line shown for current in the write direction, the write gate 46 and the write driver 44 must be turned on to cause current flow through the array line in the write direction. To select the array line for current in the read direction, the read driver 48 and read gate 50 must be active. The array diodes 52 are necessary to insure that there are no paths for the current through the array other than the one desired. When write time occurs, write driver 44 and write gate 46 are turned on by the corresponding address lines 42 being positive and the positive write timing pulse being present. These input pulses cause transistors 54 to turn on, thereby turning on transistors 56, which conduct heavily. A predetermined current, determined by the voltage transition and the characteristic impedance of the line, is driven down the array line 58. The current is reflected from the termination of the line comprising diode 60 forward biased by the current source 62. The reflected pulse is again reflected by the low impedance driver 44, which appears as a short circuit to the reflected pulse. The pulse is continually reflected, and at each reflection an increment i of current is added to the current on the line until the current on the line equals or exceeds the current I supplied by the current source. The line is then terminated in resistor 70, which is preferably equal to the characteristic impedance of the line. The sum of the currents supplied by the driver and the current sink is the current required to switch the cores. In the same manner, current in the read direction is obtained by actuating read driver 48 and read gate 50. The termination comprising current source 64, diode 66 and resistor 68 then causes buildup of the current on the line by successive reflections as described above.

The final current I_t on the line may be chosen as one-half the current required to change the remanent state of magnetic cores 41 in cases where a coincident current selection technique is used. The final current may be chosen as the full select current necessary to change the remanent state of the cores when a word selection scheme is used. Any desired number of reflections may be used to obtain the desired final current.

It can be shown by analysis of the equivalent circuits that driving an inductive load in the conventional manner from a voltage source V (assuming a lossless line) and series current limiting resistor produces a current rise time i_t from 10% to 90%

$$i_t = \frac{2.2Li}{V}$$

whereas in using the circuit of the invention

$$i_t = \frac{8Li}{V}$$

The rise time t_r of the final current I_t , when driving a transmission line having a transmission time of t , can be calculated from the following equation

$$t_r = t_d + \frac{I_t}{V/Z_0} \cdot t$$

where t_d is the rise time of the initial current.

Thus, it can be seen that the use of the invention results in improvement in rise time by a factor of almost three-to-one. This improvement has been achieved in practice by a circuit similar to that shown in FIG. 3 wherein the voltage $V=6$ volts, $-V=-6$ volts and $V_1=3$ volts. Extremely close correlation was obtained between the predicted rise time and the measured rise time.

While the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that the foregoing and other changes in the form and details may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. A circuit for supplying a current pulse of a predetermined amplitude to a line comprising:

a line having a determinable characteristic impedance with respect to a reference potential, said line having an input end and a termination end;

voltage source means having an impedance low with respect to said characteristic impedance coupled to the input end of said line;

a first and a second terminating means coupled to the termination end of said line, said first terminating means presenting an impedance low with respect to said characteristic impedance in response to a current pulse on the line having an amplitude less than said predetermined current to thereby cause said current pulse having an amplitude less than a predetermined termination current to be reflected toward the input end of said line, said first terminating means presenting a high impedance to a current pulse on said line having an amplitude equal to or greater than said predetermined termination current;

said second terminating means comprising an impedance element coupled between the termination end of said line and said reference potential; and

means for selectively energizing said voltage source means to produce a current pulse at the input end of said line having an amplitude less than said predetermined current whereby said current pulse on said line is reflected back and forth between said first terminating means and said voltage source means until the amplitude of the current pulse on said line reaches said predetermined amplitude whereby said first terminating means assumes its high impedance state and said second terminating means then terminates said line and a current amplitude equal to said predetermined current is present on the line.

2. The circuit according to claim 1 wherein said first terminating means comprises a current sink coupled to said termination end of said line and a current sensitive device coupled between said termination end of said line and said reference potential.

3. The circuit according to claim 1 wherein said current sensitive device comprises a diode.

4. A circuit for supplying a current pulse of a predetermined amplitude to a line comprising:

a line having a determinable characteristic impedance with respect to a reference potential, said line having an input end and a termination end;

voltage source means having an impedance low with

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respect to said characteristic impedance coupled to the input end of said line;

a first terminating means comprising a current sink and a current sensitive device coupled across the termination end of said line, said first terminating means presenting an impedance low with respect to said characteristic impedance in response to a current pulse on the line having an amplitude less than the current produced by said current sink to thereby cause said current pulse having an amplitude less than said sink current to be reflected toward the input end of said line, said first terminating means presenting a high impedance to a current pulse on said line having an amplitude equal to or greater than said sink current;

a second terminating means comprising an impedance element coupled between the termination end of said line and said reference potential; and

means for selectively energizing said voltage source means to produce an incident current pulse at the input end of said line having an amplitude less than said predetermined current whereby said current pulse on said line is reflected back and forth between said first terminating means and said voltage source means until the sum of the current produced by said voltage source and the current produced by said current sink reaches said predetermined amplitude whereby said first terminating means assumes its high impedance state and said second terminating means then terminates said line and a current amplitude equal to said predetermined current is present on the line.

5. The circuit according to claim 4 wherein said current sensitive device comprises a diode.

6. A circuit for supplying a current pulse of a predetermined amplitude to a line comprising:

a line having a determinable characteristic impedance with respect to a reference potential, said line having an input end and a termination end;

voltage source means having substantially zero impedance coupled to the input end of said line;

a first terminating means comprising a current sink coupled to the termination end of said line and a diode coupled from the termination end of said line to said reference potential, said first terminating means presenting substantially zero impedance in response to a current pulse on the line having an amplitude less than said current sink output to thereby cause said current pulse having an amplitude less than said sink current to be reflected toward the input end of said line, said first terminating means presenting a substantially infinite impedance to a current pulse on said line having an amplitude equal to or greater than said sink current;

a second terminating means comprising an impedance

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element coupled between the termination end of said line and said reference potential; and

means for selectively energizing said voltage source means to produce a current pulse at the input end of said line having an amplitude less than said predetermined current whereby said current pulse on said line is reflected back and forth between said first terminating means and said voltage source means until the sum of the current produced by said voltage source means and the current produced by said current sink reaches said predetermined amplitude whereby said first terminating means assumes its high impedance state and said second terminating means then terminates said line and a current amplitude equal to said predetermined current is present on the line.

7. The circuit according to claim 6 wherein said voltage source means comprises a transistor having emitter, base and collector;

a voltage source having a first polarity with respect to said reference potential;

means for coupling the emitter of said transistor to the input end of said line; and

means for coupling the collector of said transistor to said voltage source.

8. The circuit according to claim 7 wherein said current sink comprises a second transistor having emitter, base and collector, a resistor and a voltage source having a second polarity with respect to said reference potential;

means for coupling the collector of said second transistor to the termination end of said line;

means for connecting the resistor between the emitter of said second transistor and said voltage source having said second polarity; and

means for coupling the base of said second transistor to said reference potential.

9. The circuit according to claim 8 wherein said second terminating means comprises a resistor substantially equal to the characteristic impedance of said line.

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