(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
01 November 2018 (01.11.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/200843 A1

(51) International Patent Classification:
H03K 5/153 (2006.01) *H03K 17/13* (2006.01)

(21) International Application Number:
PCT/US2018/029609

(22) International Filing Date:
26 April 2018 (26.04.2018)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
15/498,385 26 April 2017 (26.04.2017) US

(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(71) Applicant *(for JP only)*: **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1, Nishi-shinjuku 6-chome, Shinjuku-ku, Tokyo, 160-8366 (JP).

(72) Inventors: **XU, Jingwei**; 5801 Furneaux Dr., Plano, TX 75093 (US). **DEVARAJAN, Vijayalakshmi**; 7505 Higgins Lane, Plano, TX 75024 (US). **ZHANG, Gangqiang**; 3709 Stoneway Dr., Plano, TX 75025 (US). **PEREIRA, Angelo William**; 6509 Renewal Rd., Plano, TX 75074 (US).

(74) Agent: **DAVIS, Michael A. Jr.** et al.; Texas Instruments Incorporated, P.O. Box 655474, Mail Station 3999, Dallas, Texas 75265-5474 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

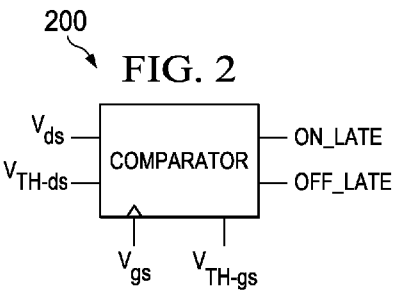
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:
— *with international search report (Art. 21(3))*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

WO 2018/200843 A1

(54) Title: HIGH-RESOLUTION FET VDS ZERO-VOLT-CROSSING TIMING DETECTION SCHEME



(57) Abstract: In methods and apparatus for detecting zero-volt crossing in a field-effect transistor, a comparator (200) compares a drain-to source voltage (V_{ds}) of the transistor to a threshold voltage (V_{TH-ds}). A gate voltage signal (V_{gs}) of the transistor is provided to a clock input of the comparator (200), such that the gate voltage signal (V_{gs}) is used to latch a result of the comparison to an output of the comparator (200). A control function with respect to the transistor is performed based on the value of the comparator (200) output.

HIGH-RESOLUTION FET VDS ZERO-VOLT-CROSSING TIMING DETECTION SCHEME

BACKGROUND

[0001] In a zero-volt switching (ZVS) scheme, a field-effect transistor (FET) delivering power to a load is switched on or off only when the drain-source voltage is at or near zero volts. ZVS uses pulse width modulation (PWM), but with an additional separate phase to the PWM timing to allow for ZVS operation. Zero-volt switching enables the voltage regulator to engage in "soft switching," thus avoiding the switching losses that are typically incurred during conventional PWM operation and timing.

[0002] ZVS is useful in a variety of power conversion systems that require high switching frequencies at higher input voltages and voltage drops. Wireless power transfer and charging systems are an example of a technology that can benefit greatly from zero-volt switching. The Alliance For Wireless Power (A4WP) is an industry standard group that uses the principles of magnetic resonance to develop a wireless energy transfer system over distance. A4WP wireless power transfer uses directed and controlled magnetic fields to replace traditional power cords. To do this, the transmitter has one or more primary windings to induce an even magnetic field above its surface. A receiver in the magnetic field has a secondary winding to capture the magnetic energy and convert it back to electrical energy. In A4WP wireless power transfer, the switching frequencies are multiples of 6.78MHz. Accurate zero-voltage crossing (ZVC) detection is a starting point for high efficiency ZVS control. With such high-frequency switching, the timing accuracy of the zero-volt switching needs to be on the order of a nanosecond. Conventional zero-voltage crossing detection methods employ very fast comparators and gate drivers that have very little delay. However, typical comparator delay is already above the aforementioned nanosecond range.

SUMMARY

[0003] In described examples of a control module for controlling a field-effect transistor, the control module includes a comparator and control circuitry. The comparator receives the drain-to-source voltage of the transistor and compares it to a threshold voltage. The comparator has a clock input that receives a gate voltage of the transistor, such that the received gate voltage is used to latch a result of the comparison to an output of the comparator. The control circuitry

receives the comparator output and performs a control function with respect to the transistor based on the value of the comparator output.

[0004] In other described examples of a control module for controlling a field-effect transistor, the control module includes a drain-to-source voltage comparator, a gate-to-source voltage comparator, and at least one latching element. The drain-to-source voltage comparator receives the drain-to-source voltage (V_{ds}) of the transistor and compares it to a V_{ds} threshold. The V_{ds} comparator has at least one output configured to provide a V_{ds} edge transition signal indicative of V_{ds} crossing the V_{ds} threshold. The gate-to-source voltage comparator receives the gate-to-source voltage (V_{gs}) of the transistor and compares it to a V_{gs} threshold. The V_{gs} comparator has at least one output configured to provide a V_{gs} edge transition signal indicative of V_{gs} crossing the V_{gs} threshold. The at least one latching element has a data input, a clock input, and an output. The data input is operably coupled to receive a V_{ds} edge transition signal from the V_{ds} comparator, and the clock input is operably coupled to receive a V_{gs} edge transition signal from the V_{gs} comparator, such that the V_{gs} edge transition signal serves to latch the V_{ds} edge transition signal to the latch output.

[0005] In a method of controlling a field-effect transistor, a comparator compares a drain-to-source voltage of the transistor to a threshold voltage. A gate voltage signal of the transistor is provided to a clock input of the comparator, such that the gate voltage signal is used to latch a result of the comparison to an output of the comparator. A control function with respect to the transistor is performed based on the value of the comparator output.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 is a schematic block diagram of an illustrative wireless power transfer system.

[0007] FIG. 2 is a functional block diagram of a comparator for use in a zero-volt switching detection circuit in accordance with illustrative embodiments.

[0008] FIG. 3 is a timing diagram demonstrating timing relationships between the Vds signal, the Vgs signal, the ON_LATE flag, and the OFF_LATE flag in accordance with illustrative embodiments.

[0009] FIG. 4 is a functional block diagram of a comparator system capable of implementing a comparator, such as the comparator described with respect to FIG. 2 in accordance with illustrative embodiments.

[0010] FIG. 5 is a timing diagram timing showing timing relationships for various signals in a

comparator system, such as that shown in FIG. 4 in accordance with illustrative timing and control schemes.

[0011] FIG. 6 is a flowchart of a method of controlling a field-effect transistor in accordance with illustrative embodiments.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0012] Illustrative aspects are directed to techniques for achieving accurate and efficient zero-volt crossing detection in a high-frequency zero-volt-switching system. For purposes of illustration, the zero-volt-crossing detection methods are described herein with respect to an A4WP wireless power transfer and charging system. However, aspects of example embodiments are applicable to substantially any system that employs zero-volt switching.

[0013] FIG. 1 is a schematic block diagram of an illustrative wireless power transfer system 100. The primary side 105 of the wireless power transfer system 100 includes a primary-side control module 110, which illustratively comprises an integrated circuit controller. The primary-side control module 110 generates control signals and provides them to external switches Q1, Q2, Q3 and Q4. In the illustrative embodiment shown in FIG. 1, the switches Q1, Q2, Q4 and Q4 are metal-oxide-semiconductor field-effect transistors (MOSFETs) and the control signals provided by the primary-side control module 110 are gate-driver signals. The junction of switches Q1 and Q3 define a tank node N1, and the junction of switches Q2 and Q4 define a tank node N2. Specifically, in the illustrative embodiment of FIG. 1, tank node N1 is defined by the junction of the source of transistor Q1 and the drain of transistor Q3. Tank node N2 is defined by the junction of the source of transistor Q2 and the drain of transistor Q4. The drains of transistors Q1 and Q2 are coupled to an input voltage V_{in}. The sources of transistors Q3 and Q4 are coupled to ground. Tank nodes N1 and N2 are coupled to a primary-side LC tank circuit comprising primary-side capacitor $C_{primary}$ and primary-side inductor $L_{primary}$. The tank node N1 is coupled to a first terminal of primary-side capacitor $C_{primary}$. The primary-side inductor $L_{primary}$ is coupled between the second terminal of capacitor $C_{primary}$ and tank node N2.

[0014] Primary-side inductor $L_{primary}$ is inductively coupled across air gap M to secondary-side inductor $L_{secondary}$. On the secondary side 115 of the wireless power transfer system 100, an LC tank circuit comprising secondary-side inductor $L_{secondary}$ and secondary-side capacitor $C_{secondary}$ is coupled to tank nodes N3 and N4. The tank node N3 is coupled to a first terminal of the secondary-side inductor $L_{secondary}$. The secondary-side capacitor $C_{secondary}$ is coupled between the

second terminal of inductor $L_{secondary}$ and tank node N4. A secondary-side control module 120, which in an illustrative embodiment comprises an integrated circuit controller, generates control signals and provides them to external switches Q5, Q6, Q7 and Q8 arranged in an H-bridge configuration. In illustrative embodiments, the primary-side control module 110 and the secondary-side control module 120 are part of a single integrated circuit. In the illustrative embodiment shown in FIG. 1, the switches Q5, Q6, Q7 and Q8 are MOSFETs and the control signals provided by the secondary-side control module 120 are gate-driver signals. The junction of switches Q5 and Q7 define tank node N3, and the junction of switches Q6 and Q8 define tank node N4. Specifically, in the illustrative embodiment of FIG. 1, tank node N3 is defined by the junction of the source of transistor Q5 and the drain of transistor Q7. Tank node N4 is defined by the junction of the source of transistor Q6 and the drain of transistor Q8. The sources of transistors Q7 and Q8 are coupled to ground. The drains of transistors Q5 and Q6 define an output node NO that provides an output voltage V_{BRIDGE_OUT}.

[0015] In illustrative embodiments, an integrated phase-locked loop (PLL) (not shown) locks onto an external high-frequency crystal oscillator (also not shown). The phase-locked loop is illustratively integrated on the same integrated circuit as the primary-side control module 110 and the secondary-side control module 120. The primary-side control module 110 includes a digital pulse-width modulation (PWM) generation state machine that works in tandem with the phase-locked loop to generate the driving waveforms that drive four gate-driver circuits in the primary-side control module 110. The four gate-driver circuits, in turn, drive the gates of the primary-side transistors Q1, Q2, Q3 and Q4 and the series LC resonant tank to transmit power across the air gap M. On the secondary side 115, the recovered signal captured across the resonator capacitor $C_{secondary}$ is sliced to generate the digital reference signal for the phase-locked loop. The secondary-side control module 120 includes a PWM generation state machine seeks to drive the gates of the transistors Q5, Q6, Q7 and Q8 of the secondary-side H-bridge for synchronous rectification. To maximize efficiency on the primary side 105 and the secondary side 115, it is important to optimize the switching times for the transistors Q1-Q8. Zero-volt switching (ZVS) is an effective means of optimizing these switching times. Precise zero-volt crossing (ZVC) detection is crucial for maximizing the efficiency of a ZVS scheme.

[0016] A zero-volt switching event determines the turn-on event of each of the primary-side transistors Q1-Q4. The turn-off edge is conveniently synced to the reference clock, which sets

up the timing reference of the whole system. On the secondary side 115, the timing reference is based on the current waveform I_P through the primary-side inductor $L_{primary}$. The secondary-side control module 120 performs synchronous rectification that emulates a full bridge diode rectifier. Zero-volt switching conditions are detected for both turn-on and turn-off edges of the secondary-side transistors Q5-Q8.

[0017] To illustrate aspects of switching control in accordance with example embodiments, the operation and control of transistor Q1 is described hereinbelow. This description regarding transistor Q1 also pertains to the other primary-side transistors Q2-Q4 and, in many respects, the secondary-side transistors Q5-Q8. The drain-to-source voltage signal V_{ds} of transistor Q1 is complex due to the ringing generated by the bond wires of the transistor. The additional voltage resulting from $L_{primary}(dI_P/dt)$ can be greater than $I_{ds}R_{ds}$. A ZVS detection circuit in the primary-side control module 110 detects if the V_{ds} of the corresponding transistor Q1 is above or below a predetermined threshold $V_{TH\text{-}ds}$. In an illustrative embodiment, the ZVS detection circuit includes a comparator that compares V_{ds} to the predetermined threshold $V_{TH\text{-}ds}$. FIG. 2 is a functional block diagram of a comparator 200 for use in such a ZVS detection circuit in accordance with illustrative aspects. In illustrative embodiments, a comparator such as the comparator 200 of FIG. 2 corresponds to each of the external transistors Q1-Q8. Ideally, the threshold $V_{TH\text{-}ds}$ would be set at 0 V. But in an illustrative embodiment, $V_{TH\text{-}ds}$ is set at a value which is still reasonably close to ZVS condition, but relatively immune to parasitic effects, such as 1 V. The gate-to-source voltage V_{gs} of the transistor is used as a clock to latch the comparator output. The comparator 200 has two outputs, which are referred to herein as ON_LATE and OFF_LATE. The latched outputs, ON_LATE and OFF_LATE, indicate whether the switching edge is early or late relative to ZVS condition. The primary-side control module 105 uses the ON_LATE and OFF_LATE flags to adjust the timing control of the gate-driver signal provided to transistor Q1 to minimize the delay between the transistor switching time and the V_{ds} zero-crossing time. The flags are illustratively used by the PWM state machine to generate desired switching waveforms. In illustrative embodiments, both the ON_LATE and OFF_LATE signals are averaged over multiple (such as eight) PWM cycles to obtain the average value over a longer time period and thereby reduce noise sensitivity. It is again noted that, while this switching control scheme is described with respect to transistor Q1, the same or similar principles apply to the other primary-side transistor Q2-Q4 and to the secondary-side transistors

Q5-Q8.

[0018] When the V_{gs} signal transitions from low to high, as indicated by the V_{gs} crossing a gate-to-source threshold voltage $V_{TH\text{-}gs}$, the result of the comparison of the V_{ds} signal to the drain-to-source threshold voltage $V_{TH\text{-}ds}$ is latched to the ON_LATE output of the comparator 200. If the drain-to-source voltage V_{ds} is less than the threshold voltage when the V_{gs} signal goes high (thereby latching the comparator output), the ON_LATE output signal becomes (or remains) 1 (logic-high), indicating that the gate-driver signal went high (turning the transistor Q1 on) after the V_{ds} signal dropped to zero. Thus, the gate-driver signal turned the transistor Q1 on late. If, on the other hand, the drain-to-source voltage V_{ds} is still greater than the threshold voltage when the V_{gs} signal goes high, the ON_LATE output signal becomes (or remains) 0 (logic-low), indicating that the gate-driver signal went high before the V_{ds} signal dropped to zero. Note that the V_{ds} signal can change earlier than, or later than, the gate-driver signal switches the transistor on or off due to the effects of current driven through the LC tank circuit by the associated load. In either case, V_{ds} will become low before V_{gs} becomes high. For maximum switching efficiency, it is desirable that the gate-driver signal (and therefore the V_{gs} signal) goes high and the V_{ds} signal goes low as close to simultaneously as possible.

[0019] When the V_{gs} signal transitions from high to low, the result of the comparison of the V_{ds} signal to the threshold voltage $V_{TH\text{-}ds}$ is latched to the OFF_LATE output of the comparator 200. If the drain-to-source voltage V_{ds} starts to rise and crosses the threshold voltage $V_{TH\text{-}ds}$ immediately after the V_{gs} signal goes low (thereby latching the comparator output), the OFF_LATE output signal becomes (or remains) 1 (logic-high), indicating that the gate-driver signal held the transistor Q1 on and kept V_{ds} low, otherwise the LC tank circuit would have driven V_{ds} high (to its off-state voltage level). Thus, the gate-driver signal turned the transistor Q1 off late. If, on the other hand, the drain-to-source voltage V_{ds} does not immediately rise when the V_{gs} signal goes low, the OFF_LATE output signal becomes 0 (logic-low), indicating that the gate-driver signal went low before the V_{ds} signal dropped to zero. For maximum switching efficiency, it is desirable that the gate-driver signal (and therefore the V_{gs} signal) goes low and the V_{ds} signal goes high as close to simultaneously as possible.

[0020] FIG. 3 is a timing diagram demonstrating illustrative timing relationships between the V_{ds} signal, the V_{gs} signal, the ON_LATE flag, and the OFF_LATE flag. For purposes of demonstrating the use of the V_{gs} signal to latch the V_{ds} comparator, the timing diagram of FIG. 3

represents an ideal system without taking into account various system delays that exist in real-world systems. Such delays are described and accounted for hereinbelow. As described hereinabove, the gate-to-source voltage V_{gs} is used to latch the outputs of the comparator 200. When the V_{gs} signal goes high, the result of the comparison of the drain-to-source voltage V_{ds} to the threshold voltage $V_{TH\text{-}ds}$ is latched to the ON_LATE output. At a time t_1 in FIG. 3, the V_{gs} signal goes high, by virtue of the gate-driver signal provided by the primary-side control module 110 (or, for secondary-side transistors Q5-Q8, by the secondary-side control module). As shown in FIG. 3, at time t_1, the drain-to-source voltage V_{ds} has already dropped below the comparator threshold voltage $V_{TH\text{-}ds}$, which in the illustrative embodiment of FIG.3 is shown to be approximately 1V. Thus V_{ds} is less than $V_{TH\text{-}ds}$ and the ON_LATE flag goes high, indicating that the gate-driver signal turned the transistor on late, i.e., after the V_{ds} signal has already gone low.

[0021] As described hereinabove, when the V_{gs} signal goes low, the result of the comparison of the drain-to-source voltage V_{ds} to the threshold voltage $V_{TH\text{-}ds}$ is latched to the OFF_LATE output. At a time t_2 in FIG. 3, the V_{gs} signal goes low, by virtue of the gate-driver signal provided by the primary-side control module 110 (or, for secondary-side transistors Q5-Q8, by the secondary-side control module). As shown in FIG. 3, at time t_2, the drain-to-source voltage V_{ds} starts to rise and crosses the threshold voltage $V_{TH\text{-}ds}$ immediately after the V_{gs} signal goes low. Thus the OFF_LATE flag goes high, indicating that the gate-driver signal turned the transistor off late.

[0022] At a time t_3 in FIG. 3, the V_{gs} signal goes high again. As shown in FIG. 3, at time t_3, the drain-to-source voltage V_{ds} is still greater than the threshold voltage V_{TH}, and therefore the ON_LATE flag goes low, indicating that the gate-driver signal turned the transistor on early, i.e., before the V_{ds} signal has gone low. At a time t_4 in FIG. 3, the V_{gs} signal goes low again. At time t_3, the drain-to-source voltage V_{ds} is still less than the threshold voltage V_{TH}, and therefore the OFF_LATE flag goes low, indicating that the gate-driver signal turned the transistor off early, i.e., before the V_{ds} signal has gone high.

[0023] In illustrative embodiments, a PWM state machine in the primary-side control module 110 uses the latched outputs from the V_{ds} comparators corresponding to each of the primary-side transistors Q1-Q4 to regulate control bits to the phase-locked loop. Similarly, a PWM state machine in the secondary-side control module 120 uses the latched outputs from the V_{ds}

comparators corresponding to each of the secondary-side transistors Q5-Q8 to regulate control bits to the phase-locked loop. The PWM state machines employ control algorithms that seek to obtain locking positions for the rising and falling edges of the gate-driver waveforms. These algorithms illustratively employ an initial pulse-width value for the gate-driver waveforms. For example, in an illustrative embodiment, the hard-coded values for the initial pulse widths at the beginning of the search algorithm are set to ~40% DC on the primary side and ~10% DC on the secondary side. During operation, the pulse widths are then adjusted dynamically based on the values of the ON_LATE and OFF_LATE flags (illustratively averaged over multiple PWM cycles) to maximize the alignment of the V_{ds} and V_{gs} signals.

[0024] In an illustrative embodiment, the primary-side PWM state machine and the secondary-side PWM state machine each first seeks to lock the rising edge of the gate-driver waveform to the ON_LATE flag. This is done by successively shifting the position of the rising edge of the gate-driver signal until the ON_LATE flag changes state. In illustrative embodiments, the time period between position changes is programmable via non-volatile memory (NVM) and can be tuned based on the bandwidth requirements of the system. The PWM state machine next repeats the process for the falling edge. The PWM state machine performs this process with respect to all four external transistors (transistors Q1-Q4 for the primary-side PWM state machine and transistors Q5-Q8 for the secondary-side PWM state machine). When both the rising and falling edges for all four external transistors have attained optimal positions for zero-volt switching, the state machine toggles the edges around those positions.

[0025] FIG. 4 is a functional block diagram of a comparator system 400 that implements a comparator such as the comparator 200 described with respect FIGS. 2 and 3 in accordance with illustrative embodiments. The comparator system 400 implements the timing control scheme, described with respect to FIGS. 2 and 3, whereby the V_{gs} signal is used as a clock signal controlling the latching of the outputs of the comparator 200 (or the outputs of the comparator system 400). The comparator system 400 also accounts for some of the above-described timing delays in a real-world system. As shown in FIG. 4, the comparator system 400 actually employs two comparators – a V_{ds} comparator 410 and a V_{gs} comparator 420. V_{ds} comparator 410 receives the drain-to-source voltage V_{ds} and compares it to the predetermined threshold $V_{TH\text{-}ds}$. As described with respect to FIG. 2, ideally, the threshold $V_{TH\text{-}ds}$ would be set at 0 V. But in an illustrative embodiment, $V_{TH\text{-}ds}$ is set at a value, such as 1 V, which is still reasonably close to

ZVS condition, but relatively immune to parasitic effects. The V_{ds} comparator 410 has two outputs, referred to herein as RISE_P and FALL_P. The RISE_P output responds to the rising edge of the V_{ds} signal by going high when the V_{ds} signal rises above the voltage threshold $V_{TH\text{-}ds}$. The FALL_P output responds to the falling edge of the V_{ds} signal by going high when the V_{ds} signal drops below the voltage threshold $V_{TH\text{-}ds}$.

[0026] V_{gs} comparator 420 receives the gate-to-source voltage V_{ds} and compares it to a predetermined value that corresponds to the turn-on threshold voltage of the associated transistor. In an illustrative embodiment, the V_{gs} input of the V_{gs} comparator 420 is coupled directly to the gate-up and gate-down pins of the gate-driver circuit. The Vg_s comparator 420 has two outputs, referred to herein as ON_CLK and OFF_CLK. The ON_CLK output responds to the rising edge of the V_{ds} signal by going high when the V_{gs} signal rises above the voltage threshold $V_{TH\text{-}gs}$. The OFF_CLK output responds to the falling edge of the V_{ds} signal by going high when the V_{gs} signal drops below the voltage threshold $V_{TH\text{-}gs}$.

[0027] The V_{ds} comparator 410 and V_{gs} comparator 420 are both subject to an inherent amount of delay. Accordingly, an inherent amount of delay exists between the time that the V_{ds} signal changes state (i.e., rises above, or drops below, the voltage threshold $V_{TH\text{-}ds}$) and the time that the corresponding V_{ds} output (RISE_P or FALL_P) changes state (i.e., goes high or goes low). Likewise, an inherent amount of delay exists between the time that the V_{gs} signal changes state (i.e., rises above, or drops below, the voltage threshold $V_{TH\text{-}gs}$) and the time that the corresponding V_{ds} output changes state. The amount of delay introduced by the V_{ds} comparator 410 and V_{gs} comparator 420 can vary from part to part, and also in response to process variance. The delay matching/trimming module 430 includes circuitry that accounts for and adjusts for these inherent delays. Each of the outputs of both the V_{ds} comparator 410 and the V_{gs} comparator 420 are provided to a delay element in the delay matching/trimming module 430. Specifically, the RISE_P signal is provided to delay element 435, the FALL_P signal is provided to delay element 440, the OFF_CLK signal is provided to delay element 445, and the ON_CLK signal is provided to delay element 450. Each of the delay elements 435-450 also includes a trim input (not shown) for receiving a trim value that dictates an amount of delay that is to be introduced by the corresponding delay element. These trim values can be determined during or after manufacture by various methods that can include testing. In an illustrative embodiment, the trim values are stored in non-volatile memory. In this way, the delay matching/trimming module

430 can compensate for the delays inherent in the V_{ds} comparator 410 and V_{gs} comparator 420. In illustrative embodiments, the delay matching/trimming module 430 also compensates for the delay that exists between the time that the PWM signal controlling the gate-driver circuit changes state and the time that the gate voltage changes in response thereto.

[0028] The delay matching/trimming module 430 thus produces delay-adjusted versions of the signals received from the V_{ds} comparator 410 and V_{gs} comparator 420. Specifically, delay element 435 outputs a signal referred to herein as RISE_P_DLY, delay element 440 outputs a signal referred to herein as FALL_P_DLY, delay element 445 outputs a signal referred to herein as OFF_CLK_DLY, and delay element 450 outputs a signal referred to herein as ON_CLK_DLY.

[0029] The output latches and averaging logic module 460 receives the delay-adjusted outputs of the V_{ds} comparator 410 and V_{gs} comparator 420 from the delay matching/trimming module 430. The output latches and averaging logic module 460 implements the latching of the outputs of the V_{ds} comparator 410 at times dictated by the rising and falling edges of the V_{gs} signal as represented by the outputs of the V_{gs} comparator 420. In the illustrative embodiment represented by FIG. 4, the latching of the ON_LATE and ON_LATE flags is implemented using two D flip-flops 465 and 470. D flip-flop 470 receives the FALL_P_DLY signal from the delay matching/trimming module 430 at its D input and receives the ON.CLK.DLY signal at its clock input. Thus, when the ON_CLK_DLY signal goes high, indicating that the gate-to-source voltage V_{gs} has gone high, the value existing at the D input, i.e., the value of the FALL_P_DLY signal, is latched to the output Q as the ON_LATE flag. This value will be a digital 1 (logic-high) if the V_{ds} voltage dropped below the V_{ds} threshold $V_{TH\text{-}ds}$ before the V_{gs} signal rose above the V_{gs} threshold $V_{TH\text{-}gs}$. In other words, ON_LATE = 1 indicates that the transistor turned on "late," i.e., after the drain-to-source voltage dropped below its threshold $V_{TH\text{-}ds}$.

[0030] D flip-flop 465 receives the RISE_P_DLY signal from the delay matching/trimming module 430 at its D input and receives the OFF.CLK.DLY signal at its clock input. Thus, when the OFF_CLK _DLY signal goes high, indicating that the gate-to-source voltage V_{gs} has gone low, the value existing at the D input, i.e., the value of the RISE_P_DLY signal, is latched to the output Q as the OFF_LATE flag. This value will be a digital 1 (logic-high) if the V_{ds} voltage rose above the V_{ds} threshold $V_{TH\text{-}ds}$ before the V_{gs} signal dropped below the V_{gs} threshold $V_{TH\text{-}gs}$. In other words, OFF_LATE = 1 indicates that the transistor turned off "late," i.e., after the drain-

to-source voltage rose above its threshold V_{TH-ds}.

[0031] As described hereinabove with respect to FIGS. 2 and 3, the PWM state machines of the primary-side control module 110 and secondary-side control module 120 use the ON_LATE and OFF_LATE flags to generate desired switching waveforms, such as by iteratively adjusting, based on those ON_LATE and OFF_LATE flags, the positions of the rising and falling edges of the PWM signals used to generate the gate driver signals that are provided to transistors Q1-Q8. In illustrative embodiments, the output latches and averaging logic module 460 includes averaging logic that serves to average the ON_LATE and OFF_LATE signals over multiple (for example, eight) PWM cycles to obtain the average value over a longer time period and thereby reduce noise sensitivity.

[0032] FIG. 5 is a timing diagram timing showing timing relationships for various signals in a comparator system such as comparator system 400 of FIG. 4 in accordance with illustrative timing and control schemes. The timing diagram of FIG. 5 shows the PWM control signal, the gate-to-source voltage V_{gs}, the drain-to-source voltage V_{ds}, the ON_CLK signal, the ON_CLK_DLY signal, the FALL_P signal, the FALL_P_DLY signal, and the ON_LATE flag. These signals are described hereinabove with respect to FIG. 4. The PWM/V_{gs} plot shows both the pulse-width modulation signal PWM and the gate-to-source voltage V_{gs}. The PWM signal is illustratively generated by the pulse-width-modulation state machine and provided to the gate-driver circuit, which generates a gate-driver signal based on the PWM signal. The gate-to-source voltage V_{gs} is representative of the gate-driver signal provided to the gate of the transistor by the gate-driver circuit. At a time t_1 in FIG. 5, the PWM signal goes high. After a driver delay 500, the gate-to-source voltage V_{gs} crosses the transistor turn on threshold V_{TH-gs}, which in the illustrative embodiment of FIG. 5, is 2.5V, at a time t_2. After a V_{gs} comparator delay 510, the ON_CLK output of the V_{gs} comparator 420 goes high at a time t_4 in response to the V_{gs} signal crossing the V_{TH-gs} threshold at time t_2. At a time t_3, the drain-to-source voltage V_{ds} of the transistor crosses the drain-to-source voltage threshold V_{TH-ds}, which in the illustrative embodiment of FIG. 5 is set at 1 V. After a V_{ds} comparator delay 520, the FALL_P output of the V_{ds} comparator 410 goes high at a time t_5 in response to the V_{ds} signal crossing the V_{TH-ds} threshold at time t_3.

[0033] As shown in FIG. 5, a delay mismatch exists between the V_{gs} comparator delay 510 and the V_{ds} comparator delay 520. Accordingly, in the illustrative example of FIG. 5, the V_{gs}

comparator 420 is subject to a longer delay than the V_{ds} comparator 410. The delay matching/trimming module 430 compensates for this delay mismatch by performing delay matching on the ON_CLK and FALL_P signals. Specifically, the delay elements 440 and 450 apply a delay to the FALL_P and ON_CLK signals, respectively. The amount of delay applied is defined by the trim value that is supplied to the delay elements 440 and 450. The trim values are based on the amount of delay that is inherent in each of the comparators 410 and 420 as determined, illustratively, during and after manufacture via testing and other means. The output of delay element 440, referred to as FALL_P_DLY, constitutes the delay-adjusted version of the FALL_P signal, and the output of delay element 450, referred to as ON_CLK_DLY, constitutes the delay-adjusted version of the ON_CLK signal. In accordance with the implemented delay adjustments, the FALL_P_DLY signal goes high at a time t_6 and the ON_CLK_DLY signal goes high at a time t_7. The FALL_P_DLY signal is provided to the D-flip-flop 470 of the output latches and averaging logic module 460, and the ON_CLK_DLY signal is provided to the clock input of D flip-flop 470. Thus when the ON_CLK_DLY signal goes high at time t_7, the value at the D input is latched to the Q output of the flip-flop, which provides the ON_LATE flag. Because the FALL_P_DLY signal is high at time t_7, the ON_LATE flag goes accordingly. Due to a small delay inherent in the D flip-flop 460, the ON_LATE goes high at time t_8, reflecting the fact that the V_{gs} signal went high, thereby turning the transistor on, late (i.e., after the drain-to-source voltage V_{ds} dropped below the $V_{TH\text{-}ds}$).

[0034] FIG. 6 is a flowchart of a method of controlling a field-effect transistor in accordance with illustrative embodiments. At block 600, a comparator compares a drain-to source voltage of the transistor to a threshold voltage. At block 610, a gate voltage signal of the transistor is provided to a clock input of the comparator such that the gate voltage signal is used to latch a result of the comparison to an output of the comparator. At block 620, a control function with respect to the transistor is performed based on the value of the comparator output.

[0035] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims. For example, described embodiments include a zero-volt-crossing detection scheme performed by a V_{ds} comparator that uses the gate voltage of the transistor as a clock input to latch the comparator output, but other variations are possible. Also, for example, described embodiments include a wireless power transfer system using zero-volt switching, but other systems may likewise use zero-volt switching.

CLAIMS

What is claimed is:

1. A control module for controlling a field-effect transistor having a gate, a drain and a source, the control module comprising:

a comparator operable to receive the drain-to-source voltage of the transistor and compare it to a threshold voltage, the comparator comprising a clock input operable to receive a gate voltage of the transistor, wherein the received gate voltage is used to latch a result of the comparison to an output of the comparator; and

control circuitry operable to receive the comparator output and to perform a control function with respect to the transistor based on the value of the comparator output.

2. The control module of claim 1 wherein the comparator comprises:

a first output configured to provide an on-late flag indicative of whether the gate voltage turned the transistor on before or after the drain-to-source voltage went from high to low, wherein a rising edge of the received gate voltage is used to latch a result of the comparison to the first output of the comparator; and

a second output configured to provide an off-late flag indicative of whether the gate voltage turned the transistor off before or after the drain-to-source voltage went from low to high, wherein a falling edge of the received gate voltage is used to latch a result of the comparison to the second output of the comparator.

3. The control module of claim 2 wherein the control circuitry is operable to perform at least one control function with respect to the transistor based on the value of the on-late flag and the value of the off-late flag.

4. The control module of claim 3 wherein the control circuitry is operable to adjust the timing of the rising edge of a gate driver signal driving the transistor based on the value of the on-late flag, and to adjust the timing of the falling edge of the gate driver signal based on the value of the off-late flag.

5. The control module of claim 3 wherein the control circuitry is operable to adjust the timing of the rising edge of a pulse-width modulation (PWM) signal used to generate a gate driver signal driving the transistor based on the value of the on-late flag, and to adjust the timing of the falling edge of the PWM signal based on the value of the off-late flag.

6. The control module of claim 5 wherein the control circuitry is operable to average the

value of the on-late flag over a plurality of PWM cycles and to average the value of the off-late flag over a plurality of PWM cycles, and to adjust the timing of the rising edge of the PWM signal based on the average value of the on-late flag and to adjust the timing of the falling edge of the PWM signal based on the average value of the off-late flag.

7. A control module for controlling a field-effect transistor having a gate, a drain and a source, the control module comprising:

a drain-to-source voltage comparator operable to receive the drain-to-source voltage (V_{ds}) of the transistor and compare it to a V_{ds} threshold, the V_{ds} comparator having at least one output configured to provide a V_{ds} edge transition signal indicative of V_{ds} crossing the V_{ds} threshold;

a gate-to-source voltage comparator operable to receive the gate-to-source voltage (V_{gs}) of the transistor and compare it to a V_{gs} threshold, the V_{gs} comparator having at least one output configured to provide a V_{gs} edge transition signal indicative of V_{gs} crossing the V_{gs} threshold; and

at least one latching element having a data input, a clock input, and an output, the data input operably coupled to receive a V_{ds} edge transition signal from the V_{ds} comparator and the clock input operably coupled to receive a V_{gs} edge transition signal from the V_{gs} comparator such that the V_{gs} edge transition signal serves to latch the V_{ds} edge transition signal to the latch output.

8. The control module of claim 7 further comprising a delay-matching module operably coupled to receive the V_{ds} edge transition signal from the V_{ds} comparator and the V_{gs} edge transition signal from the V_{gs} comparator, apply a matching delay to at least one of the V_{ds} edge transition signal and the V_{gs} edge transition signal to compensate for any disparity in delays inherent in the V_{ds} comparator and the V_{gs} comparator, and to provide a delay-adjusted V_{ds} edge transition signal to the data input of the at least one latching element and a delay-adjusted V_{gs} edge transition signal to the clock input of the at least one latching element.

9. The control module of claim 7 further comprising control circuitry operable to receive the output of the at least one latching element and to perform a control function with respect to the transistor based on the value of the output of the at least one latching element.

10. The control module of claim 7 wherein the at least one latching element comprises at least one D flip-flop.

11. The control module of claim 7 wherein:

the V_{ds} comparator comprises first and second outputs, the first output configured to

provide a V_{ds} rising-edge signal indicative of V_{ds} rising above the V_{ds} threshold, the second output configured to provide a V_{ds} falling-edge signal indicative of V_{ds} falling below the V_{ds} threshold; and

the V_{gs} comparator comprises first and second outputs, the first output configured to provide a V_{gs} rising-edge signal indicative of V_{gs} rising above the V_{gs} threshold, the second output configured to provide a V_{gs} falling-edge signal indicative of V_{gs} falling below the V_{gs} threshold.

12. The control module of claim 11 wherein the at least one latching element comprises:

a first latching element having a data input, a clock input, and an output, the data input operably coupled to receive the V_{ds} falling-edge signal from the V_{ds} comparator and the clock input operably coupled to receive the V_{gs} rising-edge signal from the V_{gs} comparator such that the V_{gs} rising-edge signal serves to latch the V_{ds} falling-edge signal to the latch output, the latch output thus serving as an on-late flag indicative of whether the V_{gs} signal turned the transistor on before or after the drain-to-source voltage went from high to low; and

a second latching element having a data input, a clock input, and an output, the data input operably coupled to receive the V_{ds} rising-edge signal from the V_{ds} comparator and the clock input operably coupled to receive the V_{gs} falling-edge signal from the V_{gs} comparator such that the V_{gs} falling-edge signal serves to latch the V_{ds} rising-edge signal to the latch output, the latch output thus serving as an off-late flag indicative of whether the V_{gs} signal turned the transistor off before or after the drain-to-source voltage went from low to high.

13. The control module of claim 12 further comprising control circuitry operable to receive the on-late flag and the off-late flag and to perform at least one control function with respect to the transistor based on the value of the on-late flag and the value of the off-late flag.

14. The control module of claim 12 further comprising:

a first delay-matching element operable to apply a matching delay to the V_{ds} rising-edge signal to compensate for any disparity in delays inherent in the V_{ds} comparator and the V_{gs} comparator, and to provide a delay-adjusted V_{ds} rising-edge signal to the data input of the second latching element;

a second delay-matching element operable to apply a matching delay to the V_{ds} falling-edge signal to compensate for any disparity in delays inherent in the V_{ds} comparator and the V_{gs} comparator, and to provide a delay-adjusted V_{ds} falling-edge signal to the data input of the first

latching element;

a third delay-matching element operable to apply a matching delay to the V_{gs} falling-edge signal to compensate for any disparity in delays inherent in the V_{ds} comparator and the V_{gs} comparator, and to provide a delay-adjusted V_{gs} falling-edge signal to the clock input of the second latching element; and

a fourth delay-matching element operable to apply a matching delay to the V_{gs} rising-edge signal to compensate for any disparity in delays inherent in the V_{ds} comparator and the V_{gs} comparator, and to provide a delay-adjusted V_{gs} rising-edge signal to the clock input of the first latching element.

15. A method of controlling a field-effect transistor, comprising:

comparing, with a comparator, a drain-to source voltage of the transistor to a threshold voltage;

providing a gate voltage signal of the transistor to a clock input of the comparator such that the gate voltage signal is used to latch a result of the comparison to an output of the comparator; and

performing a control function with respect to the transistor based on the value of the comparator output.

16. The method of claim 15 further comprising:

providing, at a first output of the comparator, an on-late flag indicative of whether the gate voltage signal turned the transistor on before or after the drain-to-source voltage went from high to low;

providing, at a second output of the comparator, an off-late flag indicative of whether the gate voltage signal turned the transistor off before or after the drain-to-source voltage went from low to high;

latching a result of the comparison to the first output of the comparator in response to receiving a rising edge of the gate voltage signal at the clock input; and

latching a result of the comparison to the second output of the comparator in response to receiving a falling edge of the gate voltage signal at the clock input.

17. The method of claim 16 wherein the performing a control function comprises performing at least one control function with respect to the transistor based on the value of the on-late flag and the value of the off-late flag.

18. The method of claim 17 wherein the performing a control function comprises adjusting the timing of the rising edge of a gate driver signal driving the transistor based on the value of the on-late flag and adjusting the timing of the falling edge of the gate driver signal based on the value of the off-late flag.

19. The method of claim 18 wherein the performing a control function comprises adjusting the timing of the rising edge of a pulse-width modulation (PWM) signal used to generate a gate driver signal driving the transistor based on the value of the on-late flag and adjusting the timing of the falling edge of the PWM signal based on the value of the off-late flag.

20. The method of claim 19 wherein the performing a control function comprises averaging the value of the on-late flag over a plurality of PWM cycles, averaging the value of the off-late flag over a plurality of PWM cycles, adjusting the timing of the rising edge of the PWM signal based on the average value of the on-late flag, and adjusting the timing of the falling edge of the PWM signal based on the average value of the off-late flag.

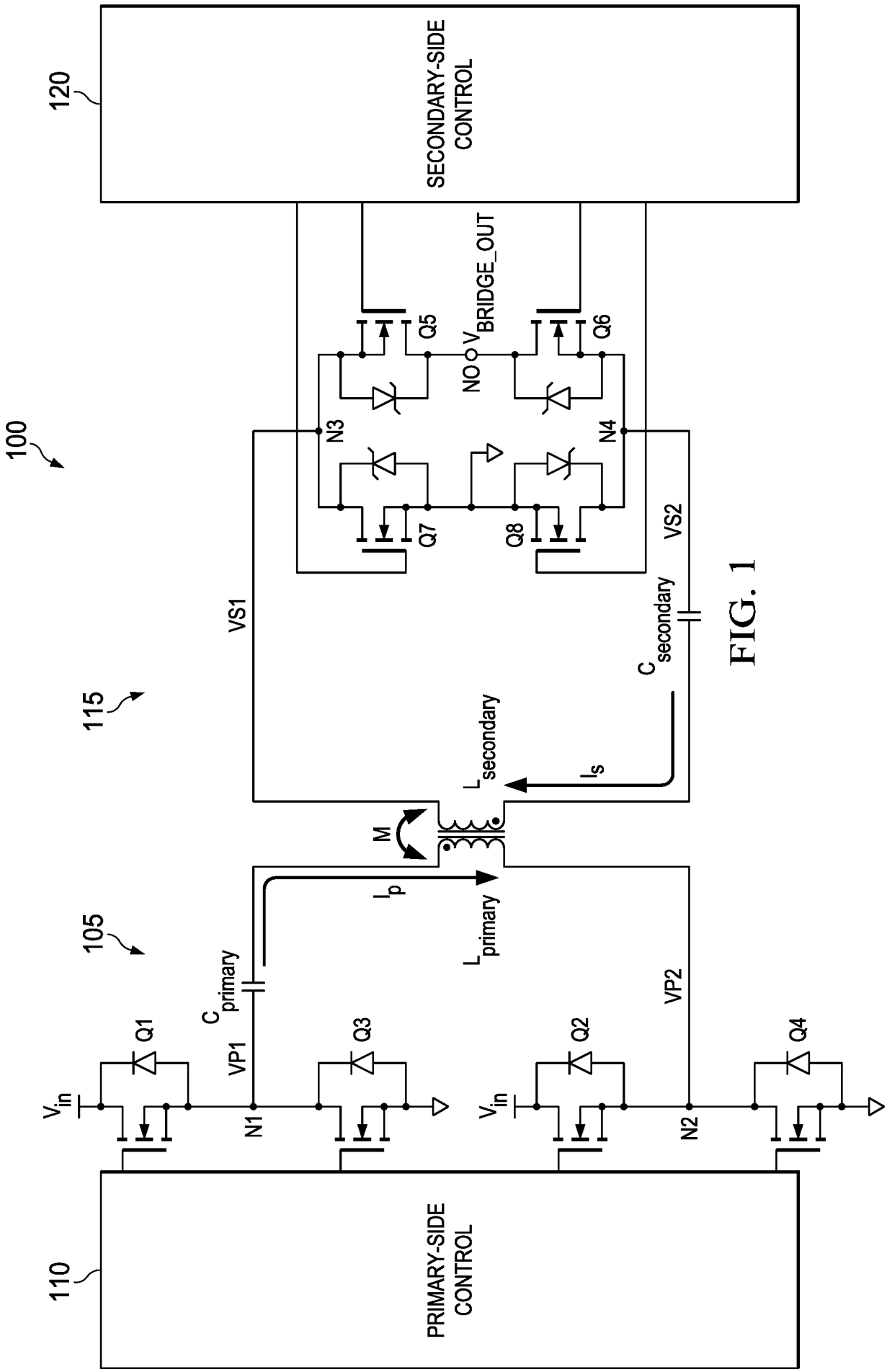

120
SECONDARY-SIDE CONTROL
100
115
105
110
PRIMARY-SIDE CONTROL
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
V_{in}
V_{in}
N1
N2
N3
N4
VP1
VP2
VS1
VS2
NO
V_{BRIDGE_OUT}
$C_{primary}$
$C_{secondary}$
$L_{primary}$
$L_{secondary}$
M
I_p
I_s

FIG. 1

FIG. 6

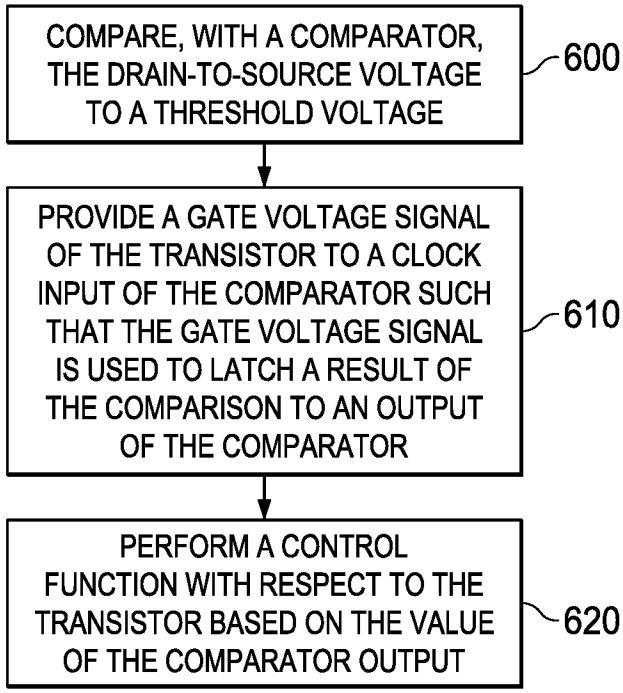


FIG. 2

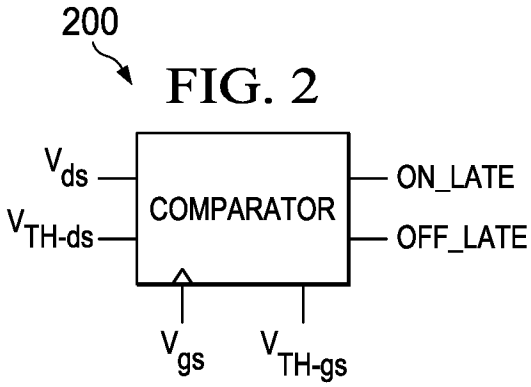
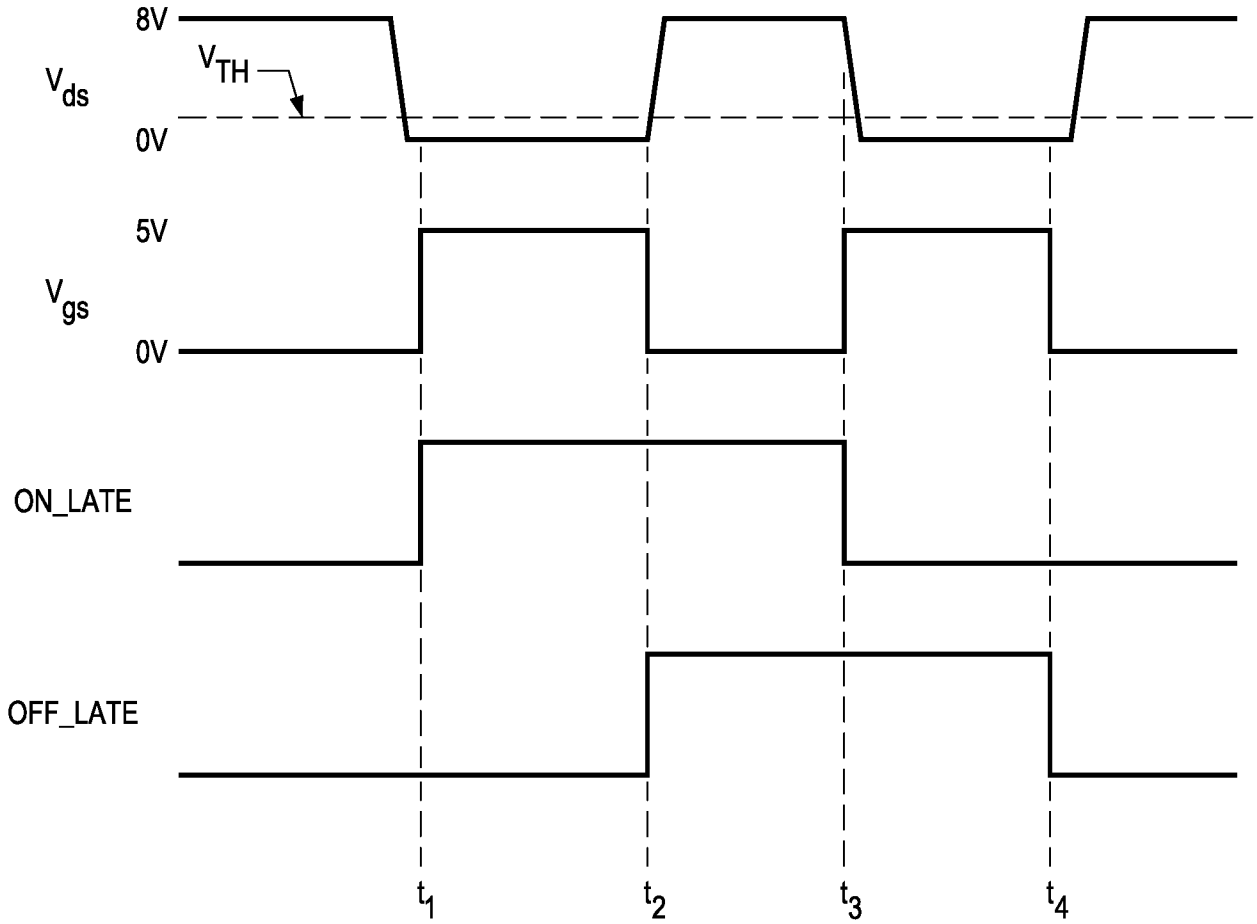


FIG. 3



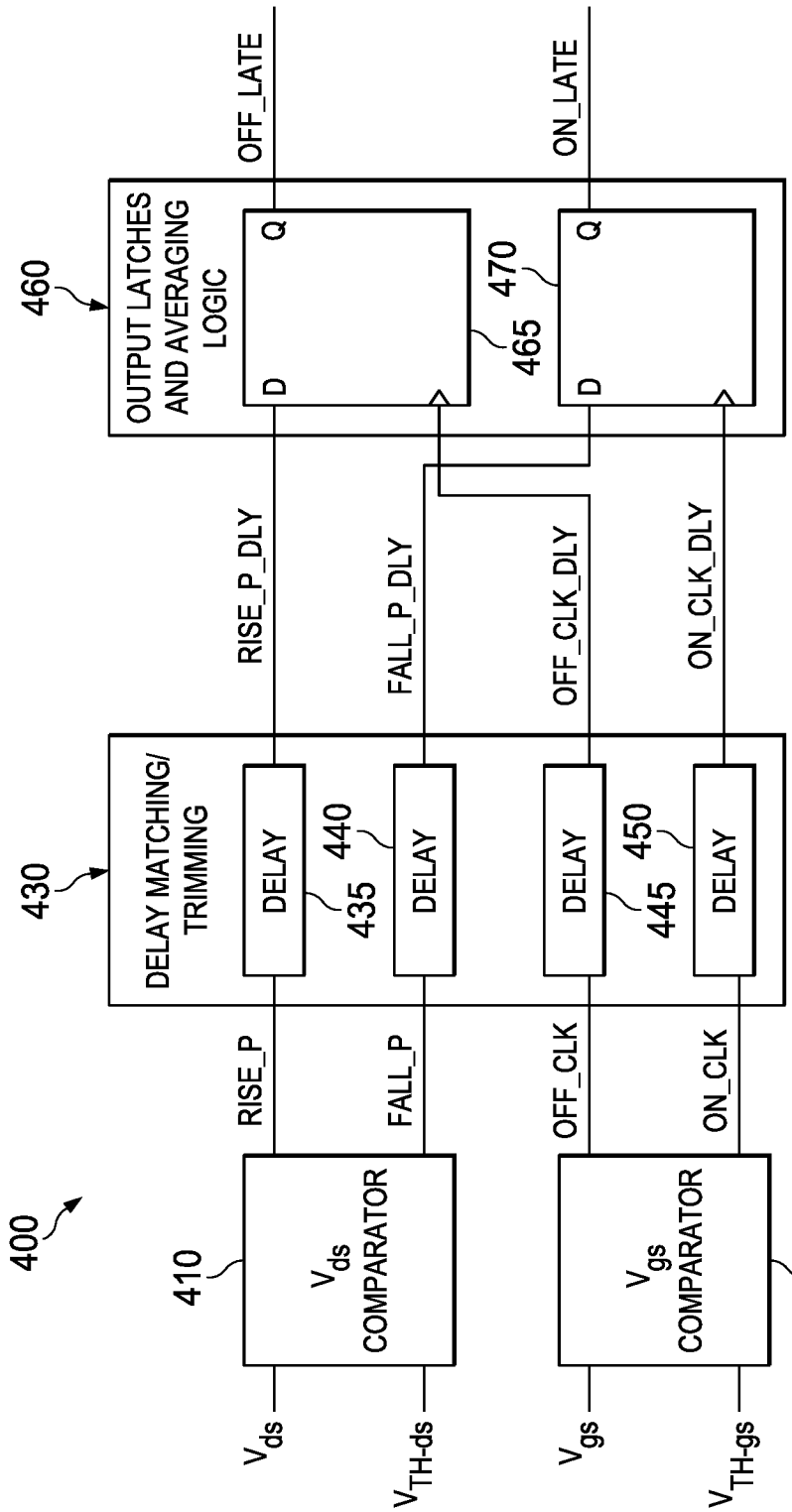

400
410
V_{ds} COMPARATOR
420
V_{gs} COMPARATOR
V_{ds}
V_{TH-ds}
V_{gs}
V_{TH-gs}
RISE_P
FALL_P
OFF_CLK
ON_CLK
430
DELAY MATCHING/ TRIMMING
DELAY
435
440
445
450
RISE_P_DLY
FALL_P_DLY
OFF_CLK_DLY
ON_CLK_DLY
460
OUTPUT LATCHES AND AVERAGING LOGIC
D
Q
465
470
OFF_LATE
ON_LATE

FIG. 4

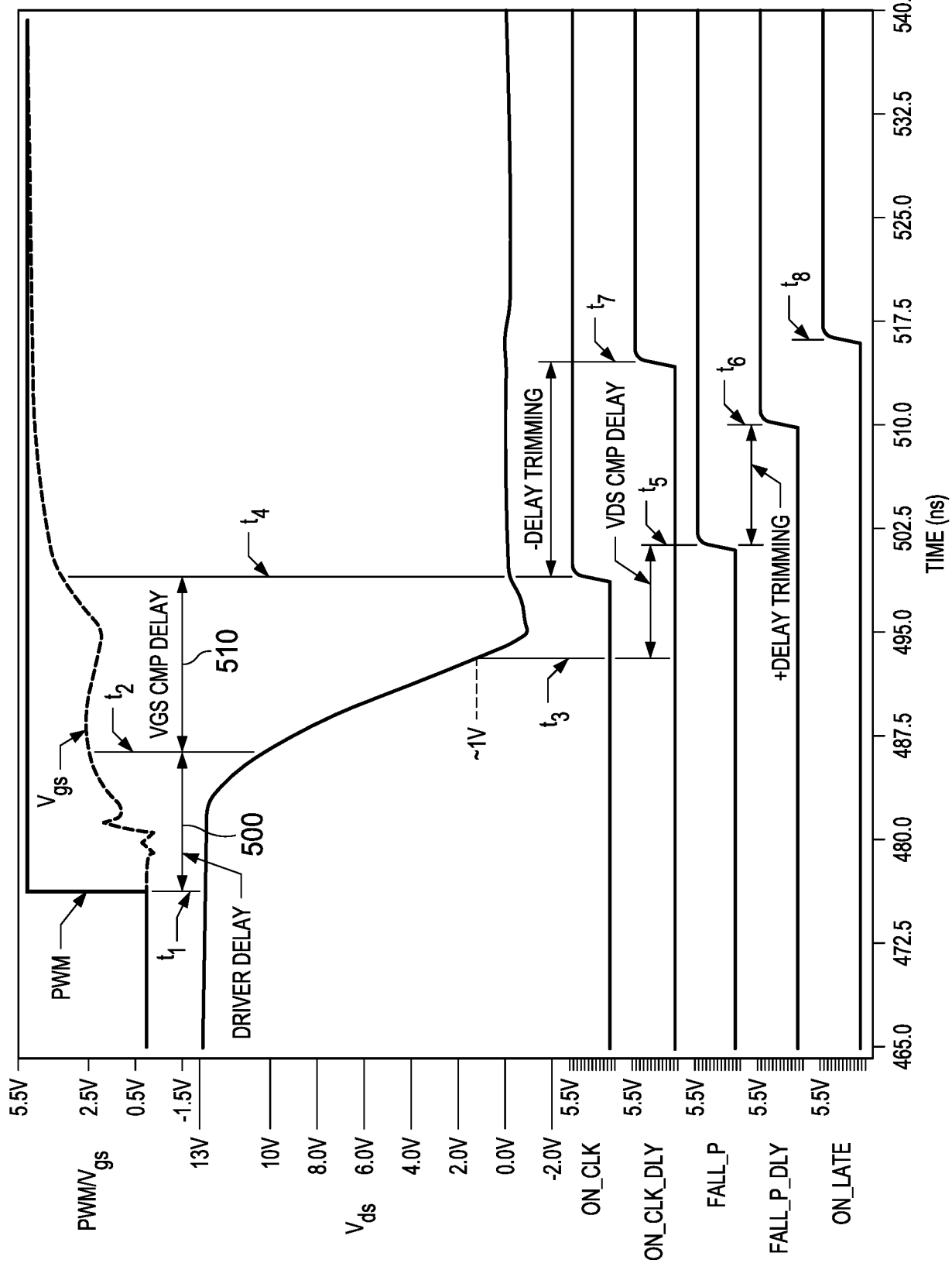

PWM
V_{gs}
t_1
t_2
t_3
t_4
t_5
t_6
t_7
t_8
VGS CMP DELAY
510
DRIVER DELAY
500
~1V
-DELAY TRIMMING
VDS CMP DELAY
+DELAY TRIMMING
PWM/V_{gs}
V_{ds}
ON_CLK
ON_CLK_DLY
FALL_P
FALL_P_DLY
ON_LATE
5.5V
2.5V
0.5V
-1.5V
13V
10V
8.0V
6.0V
4.0V
2.0V
0.0V
-2.0V
465.0
472.5
480.0
487.5
495.0
502.5
510.0
517.5
525.0
532.5
540.0
TIME (ns)

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 2018/029609

A. CLASSIFICATION OF SUBJECT MATTER

H03K 5/153 *(2006.01)*
H03K 17/13 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M 1/00, 1/08; H03K 17/00, 17/13; 17/51, 17/56; H03K 5/00, 5/153

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2010/0327947 A1 (HAVANUR SANJAY) 30.12.2010, abstract, fig.2, [0056].	1, 7, 9-10, 15 2-6, 8, 11-14, 16-20
A	US 2015/0145565 A1 (FLEXTRONICS AP, LLC) 28.05.2015	1-20
A	US 7330065 B2 (LINEAR TECHNOLOGY CORPORATION) 12.02.2008	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
04 September 2018 (04.09.2018)	13 September 2018 (13.09.2018)

Name and mailing address of the ISA/RU:	Authorized officer
Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	V. Alexandrov Telephone No. 8 499 240 25 91