Office de la Propriété Intellectuelle du Canada
Un organisme d'Industrie Canada

Canadian Intellectual Property Office
An agency of Industry Canada

CA 2581938 C 2014/02/11

(11)(21) 2 581 938

(12) BREVET CANADIEN
CANADIAN PATENT

(13) C

(86) Date de dépôt PCT/PCT Filing Date: 2005/09/21
(87) Date publication PCT/PCT Publication Date: 2006/04/06
(45) Date de délivrance/Issue Date: 2014/02/11
(85) Entrée phase nationale/National Entry: 2007/03/27
(86) N° demande PCT/PCT Application No.: US 2005/034030
(87) N° publication PCT/PCT Publication No.: 2006/036751
(30) Priorités/Priorities: 2004/09/28 (US60/613,871);
2004/10/29 (US10/977,091)

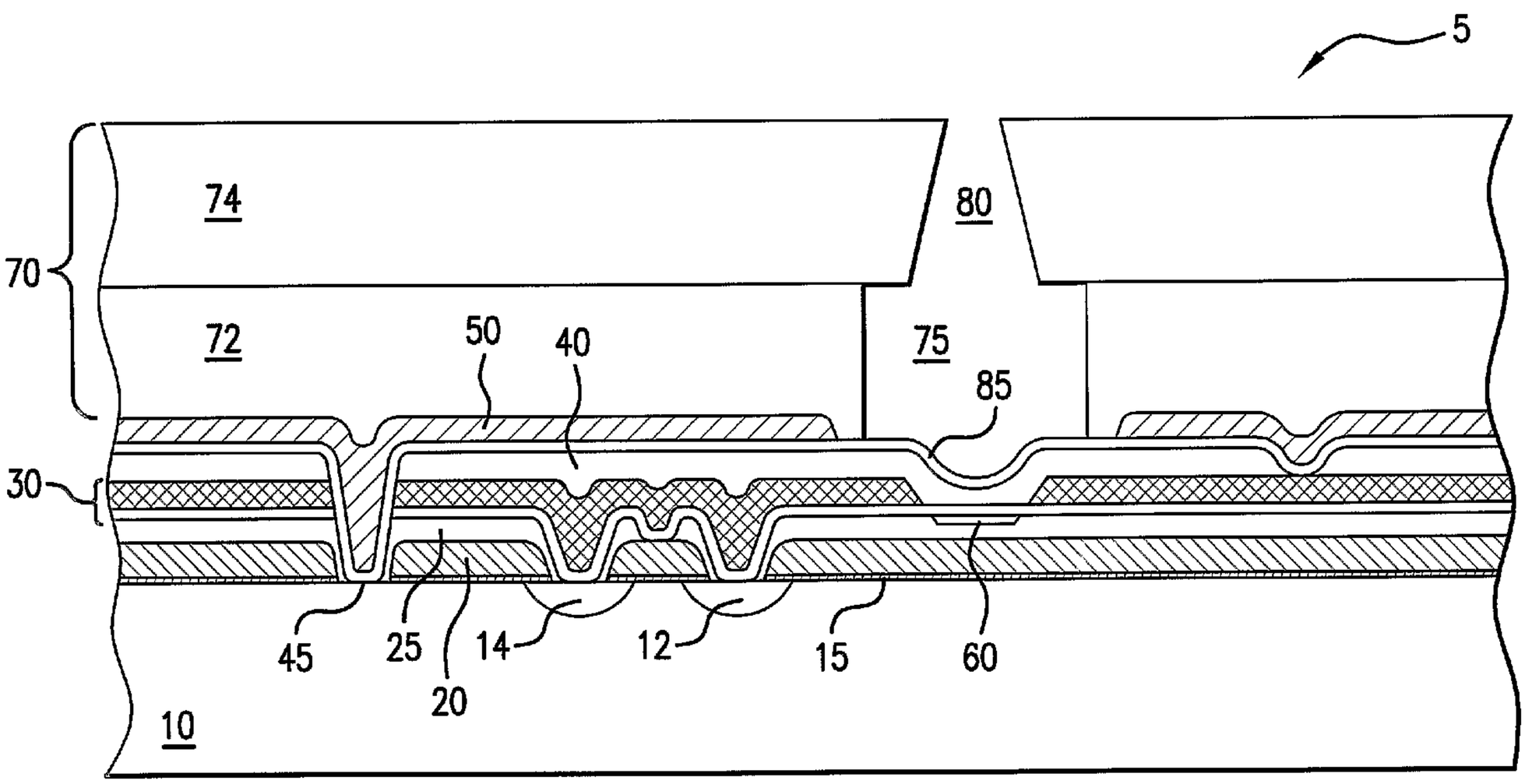
(51) Cl.Int./Int.Cl. *H01L 23/31* (2006.01),
B41J 2/14 (2006.01), *H01L 21/31* (2006.01)

(72) Inventeurs/Inventors:
DODD, SIMON, US;
WANG, S. JONATHAN, US;
TOM, DENNIS W., US;
BRYANT, FRANK R., US;
MCMAHON, TERRY E., US;
MILLER, RICHARD TODD, US;
HINDMAN, GREGORY T., US

(73) Propriétaire/Owner:
HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P., US

(74) Agent: SIM & MCBURNEY

(54) Titre : CIRCUIT INTEGRE ET PROCEDE DE PRODUCTION ASSOCIE
(54) Title: INTEGRATED CIRCUIT AND METHOD FOR MANUFACTURING



(57) Abrégé/Abstract:
A semiconductor structure (5), fluid ejection device, and methods for manufacturing the same are provided, such that a contact to a substrate (10) is formed from a conductive layer (30).

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 April 2006 (06.04.2006)

PCT

(10) International Publication Number
WO 2006/036751 A3

(51) International Patent Classification:
B41J 2/14 (2006.01) *H01L 23/31* (2006.01)
B41J 2/16 (2006.01)

(21) International Application Number:
PCT/US2005/034030

(22) International Filing Date:
21 September 2005 (21.09.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/613,871 28 September 2004 (28.09.2004) US
10/977,091 29 October 2004 (29.10.2004) US

(71) Applicant *(for all designated States except US)*: **HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.** [US/US]; Hewlett-Packard Company, Intellectual Property Administration, 20555 S.H. 249, Houston, Texas 77070 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **DODD, Simon** [US/US]; 1000 NE Circle Blvd., Corvallis, Oregon 97330-4239 (US). **WANG, S. Jonathan** [US/US]; 1000 NE Circle Blvd., Corvallis, Oregon 97330-4239 (US). **TOM, Dennis W.** [US/US]; 1000 NE Circle Blvd., Corvallis, Oregon 97330-4239 (US). **BRYANT, Frank R.** [US/US]; ST-Microelectronics, 1310 Electronics Drive, m/s 900, Carlton, Texas 75006 (US). **MCMAHON, Terry E.** [US/US]; 1000 NE Circle Blvd., Corvallis, Oregon 97330-4239 (US). **MILLER, Richard Todd** [US/US]; 1000 NE Circle Blvd., Corvallis, Oregon 97330-4239 (US). **HINDMAN, Gregory T.** [US/US]; 1000 NE Circle Blvd., Corvallis, Oregon 97330-4239 (US).

(74) Agents: **MCDANIEL, James R.** et al.; Hewlett-Packard Company, Intellectual Property Administration, P.O. Box 272400, Mail Stop 35, Fort Collins, Colorado 80527-2400 (US).

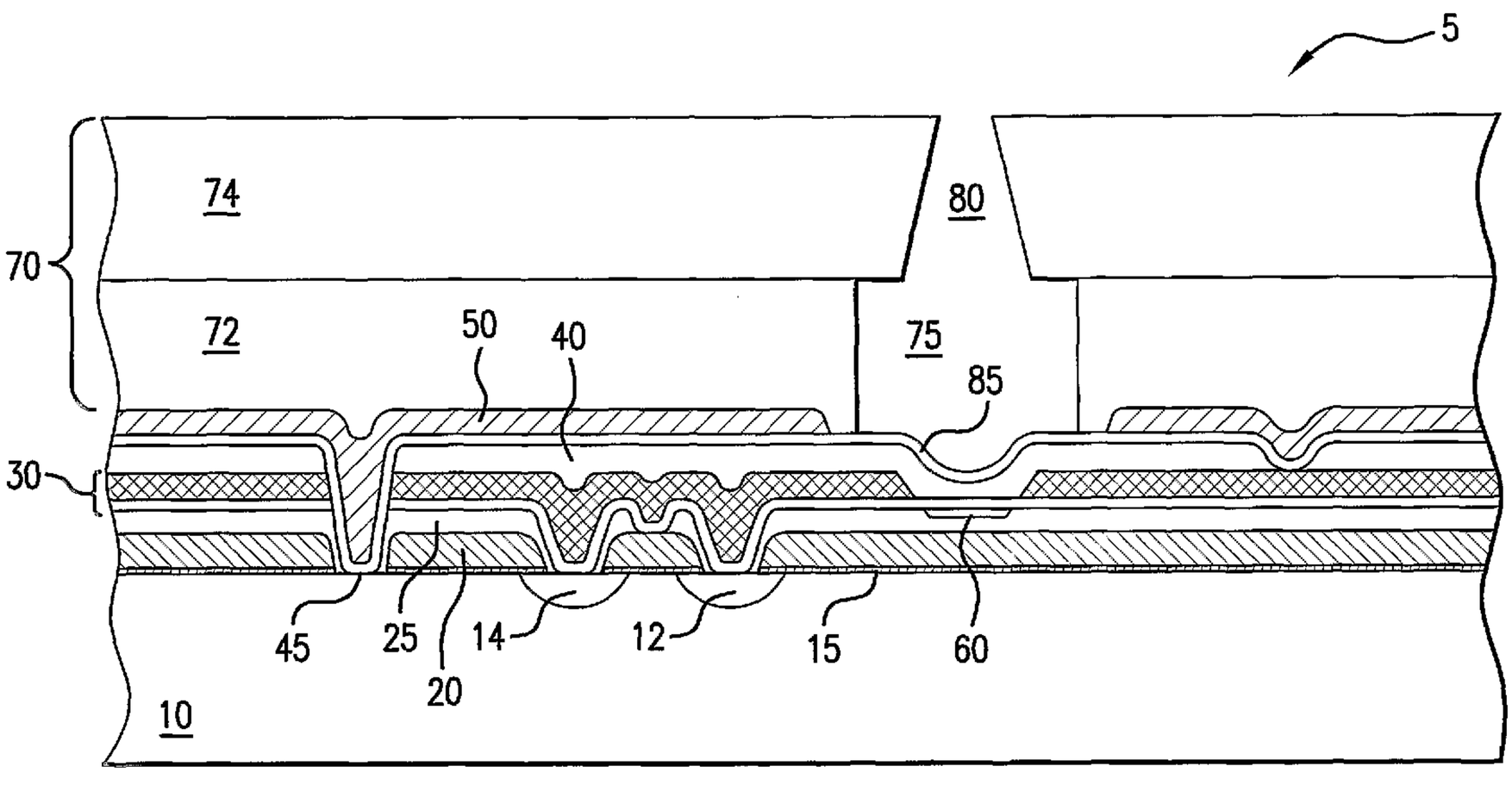
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *as to the identity of the inventor (Rule 4.17(i))*

[Continued on next page]

(54) Title: INTEGRATED CIRCUIT AND METHOD FOR MANUFACTURING



(57) Abstract: A semiconductor structure (5), fluid ejection device, and methods for manufacturing the same are provided, such that a contact to a substrate (10) is formed from a conductive layer (30).

WO 2006/036751 A3

WO 2006/036751 A3

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:
— *with international search report*

(88) Date of publication of the international search report:
22 June 2006

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTEGRATED CIRCUIT AND METHOD FOR MANUFACTURING

BACKGROUND

[0001] The market for electronic devices continually demands increased performance at decreased costs. In order to meet these requirements the components which comprise various electronic devices are desired to be made more efficiently and to more demanding design specifications.

[0002] One type of electronic device is a metal oxide silicon transistor device. These oxide silicon transistor devices are formed in large numbers on a single substrate, such as a silicon substrate. A problem in operating such devices at high voltages is that continuous operation may cause formation of a number of electron-hole pairs at junctions of the transistor, e.g. drain-gate junction. The electron-hole pairs, if they form sufficiently large charge concentrations, may decrease threshold voltage of the transistors or may lead to a turning of parasitic lateral bipolar transistor formed in the substrate.

[0003] Two countervailing factors in the design and manufacture of electronic devices are improved performance and decreased cost. Often these two factors are in direct opposition, since the formation of more precise geometries and additional structures require additional processing and masks that add to the cost of devices. On the other hand, reducing processing and masks may lead to performance problems or the inability to provide operation

within performance specifications, since structures may have to be omitted from the electronic device.

SUMMARY

[0004] Accordingly, in one aspect there is provided a semiconductor structure comprising a substrate comprising a first surface; a first insulative material disposed on at least a portion of the first surface, the first insulative material comprising a plurality of openings forming a path to the first surface; a first conductive material disposed on the first insulative material, the first conductive material being disposed so that the plurality of openings are substantially free of the first conductive material; a second insulative material disposed on the first conductive material and portions of the first insulative material, the second insulative material being disposed so that the plurality of openings are substantially free of the second insulative material; and a second conductive material being disposed on second insulative material and within plurality of openings so that some of the second conductive material disposed upon the second insulative material is in electrical contact with the substrate.

[0004a] According to another aspect there is provided a method of forming a semiconductor device, the method comprising forming a first insulative material over a first surface of a substrate; forming at least one opening in the first insulative material, the at least one opening forming a path to the substrate; forming a first conductive material over the first insulative material; etching the first conductive material so that the at least one opening forming the path to the substrate is substantially free of the first conductive material and the first insulative material; forming a second insulative material over the first conductive material; and forming a second conductive material over the second insulative material, wherein the second conductive material is formed in the at least one opening and is in contact with the substrate.

[0004b] According to another aspect there is provided a method of forming a semiconductor device, the method comprising forming a plurality of contact regions over a surface of a substrate; forming a first insulative material over the plurality of contact regions; forming at least one opening through the first insulative material and a portion of at least one contact of the plurality of contact

regions; forming a first conductive material over the first insulative material, so that the at least one opening is substantially free of the first conductive material; forming a second insulative material over the first conductive material; and forming a second conductive material over the second insulative material, wherein the second conductive material is formed in the at least one opening and forms an electrical contact with the substrate.

[0004c] According to another aspect there is provided a method of forming a semiconductor device, the method comprising forming a first insulative material over a first surface of the substrate; forming a first conductive material over the first insulative material; etching the first conductive material to form at least one opening that forms a path to the substrate that is substantially free of the first conductive material and the first insulative material; forming a second insulative material over the first conductive material; and forming a second conductive material over the second insulative material, wherein the second conductive material is formed in the at least one opening and contacts regions of the substrate.

[0004d] According to another aspect there is provided a fluid ejection device comprising a substrate comprising a first surface; a first insulative material disposed on at least a portion of the first surface, the first insulative material comprising a plurality of openings formed to the first surface; a first conductive material disposed on the first insulative material, the first conductive material being disposed so that the plurality of openings are substantially free of the first conductive material; a second insulative material disposed on the first conductive material and portions of the first insulative material, the second insulative material being disposed so that the plurality of openings are substantially free of the second insulative material; a second conductive material disposed on the second insulative material and within the plurality of openings so that some of the second conductive material disposed upon the second insulative material is in electrical contact with the substrate; a plurality of chambers formed in a material on the surface of the substrate; and a second plurality of openings formed to allow passage of a fluid from the plurality of chambers out through the second plurality of openings.

[0004e] According to another aspect there is provided a fluid ejection device comprising a substrate; a first insulative material overlying at least a portion of a first surface of the substrate, the first insulative material disposed to include a plurality of openings between portions that allow contact with the substrate; a first conductive material overlying at least a portion of the first insulative material, the first conductive material being positioned so that the plurality of openings are substantially free of the first conductive material; a second insulative material overlying at least a portion of the first conductive material and portions of the first insulative material, the second insulative material positioned so that the plurality of openings are substantially free of the second insulative material; a second conductive material overlying at least a portion of the second insulative material and disposed within the plurality of openings so that some of the second conductive material disposed upon the second insulative material is in electrical contact with the substrate; and a plurality of resistor elements configured to heat fluid in response to a current, the plurality of resistors being coupled to the first conductive material so that the current is conducted by the first conductive material.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Features of the invention will readily be appreciated by persons skilled in the art from the following detailed description of exemplary embodiments thereof, as illustrated in the accompanying drawings, in which:

[0006] Fig. 1 illustrates a cross-sectional view of a fluid ejection device according to one embodiment.

[0007] Fig. 2 illustrates a cross-sectional view of a fluid ejection device according to another embodiment.

[0008] Fig. 3 illustrates an exploded cross-sectional view of a portion of the fluid ejection device of Fig. 1 according to one embodiment.

[0009] Fig. 4 illustrates a schematic of a circuit used to selectively control fluid ejection according to one embodiment.

[00010] Fig. 5 illustrates a flow chart of a process for forming a fluid ejection device according to one embodiment.

[00011] Fig. 6 illustrates a flow chart of a process for forming a fluid ejection device according to another embodiment.

[00012] Fig. 7 illustrates a flow chart of a process for forming a fluid ejection device according to another embodiment.

[00013] Fig. 8 illustrates a top-view of a fluid ejection device according to one embodiment.

[00014] Fig. 9 illustrates a fluid ejection assembly according to one embodiment.

DETAILED DESCRIPTION OF THE DRAWINGS

[00015] Referring to Fig. 1, a cross-sectional view of a fluid ejection device according to one embodiment is illustrated. A semiconductor device 5 is formed on and/or in substrate 10, which is preferably silicon though other substrates known to those skilled in the art may be used. Substrate 10 is processed using

conventional semiconductor processing techniques to form one or more areas 12 and 14 having different impurity concentrations, e.g. active regions that form a transistor or diode. In this embodiment, where semiconductor device 5 includes Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) active areas may include drain and source regions formed in substrate 10.

[00016] A gate oxide layer 15 is disposed over a surface of the substrate 10. A semiconductor layer 20, e.g. formed of polysilicon, is disposed over the gate oxide layer 15. In some areas, a passivation layer 25, e.g. phosphosilicate glass, is disposed over semiconductor layer 20. In other areas, a conductive layer 30 disposed over semiconductor layer 20. However, other structures with only a conductive layer may be utilized.

[00017] In the embodiment depicted in Fig. 1, conductive layer 30 comprises a resistive material, e.g. a tantalum-aluminum material, which has a conductive material, e.g. aluminum, disposed thereon. It should also be noted that conductive layer 30 is disposed over passivation layer 25 as well. Further, the materials used to form resistive material and/or conductive material may vary and depend upon the application and specifications.

[00018] A passivation layer 40 is disposed over conductive layer 30 in order to insulate and protect conductive layer 30. The passivation layer 40 may be formed of one or more silicon carbide and silicon nitride, or multiple layers of each of these or combinations thereof. Further, other materials or combinations thereof may be utilized for passivation layer 40.

[00019] A plurality of openings 45 are formed in gate oxide layer 15, semiconductor layer 20, passivation layer 25, conductive layer 30, and passivation layer 40 to allow conductive layer 50, which is also disposed over passivation layer 40 to contact the surface, or if the surface is partially removed, other portions of substrate 10. In one embodiment, conductive layer 50 contacts body regions of a transistor device that are formed in substrate 10. In these embodiments, the body region may be a p- doped region, however, other dopings may be utilized.

[00020] In one embodiment, the openings 45 and the resulting contacts formed therein are formed as close to active regions or devices formed in the

substrate as possible, without affecting the operation of the devices or active regions. The exact positioning, may be dependent on the substrate type and doping concentration of the active regions. In addition, the number of contacts is dependent on the number of active regions or devices formed in the substrate. In one embodiment, there may be one contact for every device formed in the substrate. In certain embodiments, the number of contacts may be a function of the power of the devices formed in the substrate, the doping concentration of active regions, and the substrate material.

[00021] The creation of a direct contact to the body of a MOSFET can be used to prevent an increase of hole pairs at a drain/gate interface, which in turn can reduce the likelihood that the MOSFET is switched on due to small leakage currents provided at its gate.

[00022] In certain embodiments, direct contact may be made between one or more transistors formed in substrate 10. In these embodiments, contact may be made adjacent a source region of one or more of the transistors. In these embodiments contacts to the source region and the body may be made at the same or different times. In an embodiment where semiconductor device 5 is a fluid ejection device, the direct contact may be between a logic transistor and a drive transistor that operate ejection elements.

[00023] The resistor 60 and the passivation layer 40 are protected from damage, due to for example bubble collapse, in fluid chamber 75 after fluid ejection from orifice 80 by a cavitation layer 85 that is disposed over passivation layer 40. In certain embodiments, cavitation layer 85 comprises a metal selected from the group consisting of tantalum, tungsten, and molybdenum.

[00024] An orifice layer 70, shown as a barrier layer 72 and a nozzle layer 74 are provided to create a chamber 75 and orifice 80 through which fluid may be ejected. Generally, the other layers that are disposed on substrate 10 before applying the orifice layer 70. The orifice layer 70 can be a single or multiple layer(s) of polymers, epoxy materials, metals, or the like. Several methods, materials, and structures for creating the orifice layer 70 are known and may be utilized with the structure of Fig. 1.

[00025] Referring to Fig. 2, a cross-sectional view of a fluid ejection device according to another embodiment is illustrated. The fluid ejection device of Fig. 2 is substantially similar to Fig. 1. However, a field oxide 90 is disposed on some portions of the surface of substrate 10. The field oxide 90 is provided adjacent to contact regions 95 through which conductive layer 50 is to contact substrate 10. Field oxide 90 generally provides a greater barrier to diffusion than does gate oxide 15.

[00026] While Figs. 1 and 2 provide descriptions of embodiments of fluid ejection devices, however, other semiconductors devices and structures may be utilized having similar layouts and designs. For example, such structures would have orifice layer 70 and cavitation layer 85, and a passivation structure that is different in structure and/or material from passivation layer 40.

[00027] Referring to Fig. 3, an exploded cross-sectional view of a portion of the fluid ejection device of Fig. 1 according to one embodiment is illustrated. Opening 45 extend from a top surface of passivation layer 40 to a surface of substrate 10. Conductive layer 50, which comprises a resistive layer 115 and a conductive layer 120 disposed over resistive layer 115 is contact with the surface of substrate 10. It can be seen that some portions of conductive layer 50 that overlie conductive layer 30, and passivation layer 40 are in electrical contact with those portions of conductive layer 50 that are in physical contact with a surface of substrate 10. As such a robust substrate contact may be created that provides benefits with respect to parasitic turn of devices formed in substrate 10.

[00028] An additional design feature of the embodiment depicted in Fig. 3 is that resistive layer 105, conductive layer 110, and passivation layer 40 form a stair-step pattern when viewed from a cross-sectional perspective. This allows for simpler manufacturing. Other embodiments, may utilize different layouts.

[00029] Referring to Fig. 4, a schematic of a circuit 150 used to selectively control fluid ejection according to one embodiment is illustrated. The ejection element 100 is coupled to receive power 105 and to the drain of transistor 110. The source of transistor 110 is connected to ground 115. The gate of transistor 110 is connected to the source of transistor 122 and the drain of transistor 125.

The source of transistor 125 is connected to ground 115. The gate of transistor 125 is coupled to receive a first control signal 130. The gate of transistor 122 is coupled to receive a second control signal 135, while its gate is coupled to receive an address signal 140.

[00030] In certain embodiments, contacts to body regions may be formed between a source region of transistor 110 and the source region of any of transistors 122 or 125. In some embodiments, where each ejection element is operated using the circuit 150 depicted in Fig. 4, a body contact can be made in each circuit 150 or some of the circuits 150.

[00031] Referring to Fig. 5, a flow chart of a process for forming a fluid ejection device according to one embodiment is illustrated. A substrate, e.g. substrate 10, may be doped with a p-dopant for an NMOS process, block 100. However, the substrate may also be doped with an n-dopant for a PMOS process. A gate oxide material is then provided over a surface of the substrate, block 205. After the gate oxide material is provided, a semiconductor material, such as polysilicon, is provided over the gate oxide material, block 210. An insulative material, such as phosphosilicate glass, is provided over semiconductor material, block 215.

[00032] After providing the insulative material, one or more vias are formed in the insulative material, block 220. For example, the one or more vias may be formed in areas where a contact to a body of a transistor may be desired to be formed. The vias may be etched to a surface of the semiconductor material provided in block 215. After formation of the one or more vias, a first conductive layer is provided over the insulative material and into the one or more vias, block 220. The one or more vias are then overetched such that not only the conductive material in the one or more vias, but also the semiconductor material that underlie the one or more vias are removed, block 230. In this embodiment, the gate oxide formed still remains in the vias. In one embodiment, the overetching process is a reactive ion etching process.

[00033] After the conductive material and semiconductor material are removed, a passivation material is provided onto the conductive material, block 235. In some embodiments the passivation material is not provided into the one

or more vias. In other embodiments, the passivation material is applied into the vias and then removed. The gate oxide remaining in the vias is then etched away so that the vias are open to the substrate, block 240. A second conductive material is then provided that contacts the substrate in the vias, block 245. Additional layers that are required to form a semiconductor device are then provided, block 250.

[00034] Referring to Fig. 6 a flow chart of a process for forming a fluid ejection device according to another embodiment is illustrated. A substrate, e.g. substrate 10, may be doped with a p-dopant for an NMOS process, block 260. However, the substrate may also be doped with an n-dopant for a PMOS process, as described with respect to Fig. 5.

[00035] One or more contact regions are formed on the substrate, block 265. The one or more contact regions may be formed by, for example, disposing a semiconductor material upon a gate oxide which is disposed upon a surface of the substrate. A field oxide is then provided adjacent the contacts, block 270. Alternatively, field oxide may be provided, such that openings remain where contacts may be formed.

[00036] An insulative material, such as phosphosilicate glass, is provided over the contacts and field oxide, block 275. One or more vias are then formed through the insulative material, block 280. The vias are formed to overlie one or more of the contact areas. In such a way, the vias may correspond to regions where contact is to be made to the substrate or to areas where transistor gate contacts are to be formed.

[00037] After formation of the vias, a conductive material is provided overlying the insulative material and in the vias, block 285. The conductive material in the vias, and other regions as desired, is etched away, block 290. In one embodiment, the etching of the conductive material in the vias also etches, at least a portion of the contacts. The etching of at least a portion of the contacts may be accomplished, for example, by overetching utilizing a reactive ion etching process. In some embodiments, a secondary etching process may utilized after the first etching process, in order to remove any remaining contact material.

[00038] After the etching the conductive material, a second insulative material is provided onto the first conductive material, block 295. In one embodiment, the second insulative material is provided such that it does not fill or enter into the vias. In other embodiments, the second insulative material may be provided into the vias along with being provided onto the first conductive material. The second insulative material that is provided into the vias can then be removed utilizing know processes.

[00039] After the second insulative material is provided, a second conductive material is provided overlying second insulative material and into the vias, block 300. The second conductive material is provided into vias, such that portions of the second conductive material provided into the vias is in contact with the substrate, and an electrical contact to portions of the second conductive material overlying the second insulative material is provided. Additional passivation material may then be provided over the second conductive material and other portions of the device, block 305.

[00040] The embodiment depicted in Fig. 5, may be altered by omitting block 255 and only utilizing a field oxide. In this embodiment block 260 would entail providing field oxide over the entire area of a substrate where structures are to be formed. Further, block 280 may entail overetching the first conductive material so that the field oxide underlying the vias is etched away to allow contact to the substrate. Alternatively, a separate process block to remove the oxide prior to providing the first conductive material may be utilized and a standard etching process utilized at block 180.

[00041] Referring to Fig. 7, a flow chart of a process for forming a fluid ejection device according to another embodiment is illustrated. In the embodiment of Fig. 7, blocks 320-340 are substantially the same as blocks 200-215 and 225 of as described with respect to Fig. 5. However, instead of forming a via in the first insulative material prior to providing the first conductive layer, as in Fig. 5, vias are formed by etching through the first conductive layer and the first insulative layer in one process block, i.e. block 345. After formation of these vias, blocks 330-340 are substantially the same as blocks 235-245 as described with respect to Fig. 5.

[00042] As can be seen from Figs. 4-6 the number of processing blocks need not be increased, in fact the number of blocks is substantially the same. Further, since an overetching process may be utilized, in some embodiments, the actual processes used to form a structure with a body contact are the same as those without. Further, since additional processing is not utilized to form the opening, i.e. other then etching the conductive layer, there is less likelihood that misalignment or diffusion into the substrate would occur then would result if additional processing was used to form the contact to the substrate.

[00043] In some embodiments of the methods described with respect to Figs. 4 and 6, overetching can be such that portions of the substrate are removed along with the conductive, semiconductor, and gate oxide layers. This approach may be utilized, for example, where a contact is being made to a body of a substrate through a region of the device which has been doped as a source region of a transistor. The second conductive layer can then be provided such that it contacts the body region of the substrate, where the substrate has been etched away.

[00044] Fig. 8 illustrates an enlarged view of one embodiment of the printhead 500 in perspective view. The printhead 500 in this embodiment has multiple features, including an edge step 505 for an edge fluid feed to resistors (or fluid ejectors) 510. The printhead may also have a trench 515 that is partially formed into the substrate surface. A slot (or channel) 520 to feed fluid to resistors 510, and/or a series of holes 525 feeding fluid to resistors 510 are also shown on this printhead. In one embodiment there may be at least two of the features described on the printhead 500 in Fig. 8. For example, only the feed holes 525 and the slot 520 are formed in the printhead 500, while the edge step 505 and/or the trench 515 are absent. In another embodiment, the edge step 505, and the slot 520 are formed in the printhead 520, while trench 515 and/or the feedholes 525 are absent. Different combinations of these features, with other features, or wholly different features may also be provided.

[00045] Fig. 9 shows a diagrammatic representation of an exemplary print cartridge 600 that can be utilized in an exemplary printing device. The print cartridge is comprised of a printhead 602 and a cartridge body 604 that

supports the printhead. Though a single printhead 602 is employed on this print cartridge 600 other embodiments may employ multiple printheads on a single cartridge.

[00046] Print cartridge 600 is configured to have a self-contained fluid or ink supply within cartridge body 604. Other print cartridge configurations alternatively or additionally may be configured to receive fluid from an external supply. Other exemplary configurations will be recognized by those of skill in the art.

[00047] The semiconductor device structures described herein are applicable to a broad range of semiconductor devices technologies and can be fabricated from a variety of semiconductor materials. Therefore, while the above description describes several embodiments of semiconductor devices implemented in silicon substrates, the methods and structures described herein and depicted in the drawings may also be employed in gallium arsenide, germanium, and other semiconductor materials. Accordingly, the methods and structures described herein and depicted in the drawings is not intended to be limited to those devices fabricated in silicon semiconductor materials, but will include those devices fabricated in one or more of the available semiconductor materials and technologies available to those skilled in the art.

[00048] Further, while the illustrated embodiments have been shown to include specific p and n type regions, it should be clearly understood that the teachings herein are equally applicable to semiconductor devices in which the conductivities of the various regions have been reversed, for example, to provide the dual of the illustrated device.

[00049] In addition, although the embodiments illustrated herein are shown in two-dimensional views with various regions having depth and width, it should be clearly understood that these regions are illustrations of only a portion of a single cell of a device, which may include a plurality of such cells arranged in a three-dimensional structure. Accordingly, these regions will have three dimensions, including length, width, and depth, when fabricated on an actual device.

[00050] It should be noted that the drawings are not true to scale. Moreover, in the drawings, heavily doped regions (typically concentrations of impurities of at least $1x10^{19}$ impurities/cm.sup.^{3}) are designated by a plus sign (e.g., n^+ or p^+) and lightly doped regions (typically concentrations of no more than about $5x10^{16}$ impurities/cm^3) by a minus sign (e.g. p^- or n^-).

[00051] Active area component, e.g. the source and drain, isolation of a MOSFET (metal oxide semiconductor field effect transistor) is conventionally accomplished by using two mask layers, an island layer and a gate layer. The island layer is used to form an opening within thick field oxide grouse on a substrate. The gate layer is used to create the gate of the transistor and forms the self-aligned and separate active areas (the source and drain) of the transistor within the island opening of the thick field oxide.

[00052] Although the inventive concepts have been described in language specific to structural features and methodological steps, it is to be understood that the appended claims are not limited to the specific features or steps described. Rather, the specific features and steps are disclosed as preferred forms of implementing the inventive concepts.

What is claimed is:

What is claimed is:

1. A semiconductor structure comprising:

a substrate comprising a first surface;

a first insulative material disposed on at least a portion of the first surface, the first insulative material comprising a plurality of openings forming a path to the first surface;

a first conductive material disposed on the first insulative material, the first conductive material being disposed so that the plurality of openings are substantially free of the first conductive material;

a second insulative material disposed on the first conductive material and portions of the first insulative material, the second insulative material being disposed so that the plurality of openings are substantially free of the second insulative material; and

a second conductive material being disposed on second insulative material and within plurality of openings so that some of the second conductive material disposed upon the second insulative material is in electrical contact with the substrate.

2. The semiconductor structure of claim 1, further comprising a gate oxide and a polysilicon material underlying the first insulative material, whereas the plurality of openings are substantially free of the polysilicon material and the gate oxide.

3. The semiconductor structure of claim 1, further comprising a field oxide underlying the first insulative material and wherein the plurality of openings are free of the field oxide.

4. The semiconductor structure of any one of claims 1 to 3, wherein the second conductive material comprises tantalum.

5. The semiconductor structure of any one of claims 1 to 3, wherein the second conductive material comprises a resistive portion and a conductive portion disposed upon the resistive portion.

6. The semiconductor structure of any one of claims 1 to 5, further comprising a plurality of doped regions formed within the substrate and wherein each of the plurality of openings is formed adjacent to one of the plurality of doped regions.

7. The semiconductor structure of claim 6, wherein the plurality of doped regions form transistors.

8. The semiconductor structure of any one of claims 1 to 7, further comprising a fluid handling slot between the first surface and a second surface of the substrate.

9. The semiconductor structure of any one of claims 1 to 3, wherein the second insulative material comprises phosphosilicate glass.

10. The semiconductor structure of claim 1, wherein the first conductive material comprises a resistive portion and a conductive portion disposed upon the resistive portion.

11. The semiconductor structure of claim 1, wherein the plurality of openings form a path to a region below the first surface of the substrate.

12. A method of forming a semiconductor device, the method comprising:

forming a first insulative material over a first surface of a substrate;

forming at least one opening in the first insulative material, the at least one opening forming a path to the substrate;

forming a first conductive material over the first insulative material;

etching the first conductive material so that the at least one opening forming the path to the substrate is substantially free of the first conductive material and the first insulative material;

forming a second insulative material over the first conductive material; and

forming a second conductive material over the second insulative material, wherein the second conductive material is formed in the at least one opening and is in contact with the substrate.

13. The method of claim 12, further comprising forming a third insulative material and a polysilicon material on the substrate and below the first insulative material prior to forming the first insulative material and wherein forming the at least one opening comprises forming the at least one opening through the polysilicon material to the third insulative material.

14. The method of claim 13, wherein etching the first conductive material comprises etching the third insulative material.

15. The method of claim 13, further comprising etching the first conductive material comprises etching the third insulative material after etching the first conductive material.

16. The method of claim 12, further comprising forming a third insulative material and a polysilicon material on the substrate and below the first insulative material, wherein forming the at least one opening comprises forming the at least one opening so that the path is between the third insulative material and the top surface of the first insulative material.

17. The method of any one of claims 12 to 16, wherein forming the second conductive material comprises forming a resistive portion and a conductive portion disposed upon the resistive portion.

18. The method of claim 12, further comprising forming a field oxide on the substrate prior to forming the first insulative layer.

19. The method of claim 12, wherein etching the first conductive material comprises reactive ion etching the first conductive material.

20. The method of any one of claims 12 to 19, wherein the substrate comprises a plurality of transistors formed therein and wherein forming at least one opening in the first insulative material comprises forming the at least one opening between two of the plurality of transistors.

21. The method of claim 12, wherein the substrate comprises a region that has a first doping concentration and another region underlying the region, the another region having a second different doping concentration, wherein etching the first conductive material so that the at least one opening forming the path to the substrate comprises etching the region so that the path is formed to the another region.

22. The method of claim 12, wherein etching the conductive material comprises etching the first conductive material so that the path is formed to a region of the substrate below the first surface.

23. A method of forming a semiconductor device, the method comprising:

forming a plurality of contact regions over a surface of a substrate;

forming a first insulative material over the plurality of contact regions;

forming at least one opening through the first insulative material and a portion of at least one contact of the plurality of contact regions;

forming a first conductive material over the first insulative material, so that the at least one opening is substantially free of the first conductive material;

forming a second insulative material over the first conductive material; and

forming a second conductive material over the second insulative material, wherein the second conductive material is formed in the at least one opening and forms an electrical contact with the substrate.

24. The method of claim 23, wherein forming the at least one opening comprises forming the at least one opening after forming the first conductive material so that the at least one opening is formed in the first insulative material and the first conductive material.

25. The method of claim 23 or 24, wherein forming the second conductive material comprises forming a resistive portion and a third conductive portion disposed upon the resistive portion.

26. The method of any one of claims 23 to 25, wherein forming the contact regions comprises forming a third insulative material and a polysilicon material on the substrate.

27. The method of claim 26, wherein forming the third insulative material and the polysilicon material comprises forming the third insulative material and the polysilicon material on substantially all of the surface of the substrate.

28. The method of any one of claims 23 to 27, wherein the substrate comprises a plurality of transistors formed therein and wherein forming the at least one opening in the first insulative material comprises forming the at least one opening between two of the plurality of transistors.

29. The method of claim 23, wherein forming the contact regions comprises forming a third insulative material and a polysilicon material in areas where the at least one opening is to be formed and forming field oxide in areas adjacent the third insulative material and the polysilicon material.

30. The method of claim 23, wherein the substrate comprises a region that has a first doping concentration and another region underlying the region, the another region having a second different doping concentration, wherein forming at least one opening comprises removing the region so that a path is formed to the another region from a top surface of the insulative material.

31. A method of forming a semiconductor device, the method comprising:

forming a first insulative material over a first surface of the substrate;

forming a first conductive material over the first insulative material;

etching the first conductive material to form at least one opening that forms a path to the substrate that is substantially free of the first conductive material and the first insulative material;

forming a second insulative material over the first conductive material; and

forming a second conductive material over the second insulative material, wherein the second conductive material is formed in the at least one opening and contacts regions of the substrate.

32. The method of claim 31, further comprising forming a third insulative material and a polysilicon material on the substrate prior to forming the first insulative material and wherein etching the first conductive material comprises etching the polysilicon material.

33. The method of claim 31 or 32, wherein forming the second conductive material comprises forming a resistive portion and a third conductive portion disposed upon the resistive portion.

34. The method of any one of claims 31 to 33, further comprising forming a field oxide on the substrate prior to forming the first insulative material.

35. The method of any one of claims 31 to 34, wherein etching the first conductive material comprises reactive ion etching the first conductive material.

36. The method of any one of claims 31 to 35, wherein the substrate comprises a plurality of transistors formed therein and wherein forming at least one opening in the first insulative material comprises forming the at least one opening between two of the plurality of transistors.

37. The method of any one of claims 31 to 36, further comprising forming one or more orifice layers over the second conductive material.

38. The method of any one of claims 31 to 35, wherein the substrate comprises a region that has a first doping concentration and another region underlying the region, the another region having a second different doping concentration, wherein etching the first conductive material so that the at least one opening forming the path to the substrate comprises etching the region so that the path is formed to the another region.

39. The method of any one of claims 31 to 34, wherein etching the first conductive material comprises etching the first conductive material so that the path is formed to a region of the substrate below the first surface.

40. A fluid ejection device comprising:

a substrate comprising a first surface;

a first insulative material disposed on at least a portion of the first surface, the first insulative material comprising a plurality of openings formed to the first surface;

a first conductive material disposed on the first insulative material, the first conductive material being disposed so that the plurality of openings are substantially free of the first conductive material;

a second insulative material disposed on the first conductive material and portions of the first insulative material, the second insulative material being disposed so that the plurality of openings are substantially free of the second insulative material;

a second conductive material being disposed on second insulative material and within plurality of openings so that some of the second conductive material disposed upon the second insulative material is in electrical contact with the substrate;

a plurality of chambers formed in a material on the surface of the substrate; and

a second plurality of openings formed to allow passage of a fluid from the plurality of chambers out through the second plurality of openings.

41. The fluid ejection device of claim 40, wherein the first insulative material comprises a gate oxide and a polysilicon material disposed upon the gate oxide, the polysilicon material being disposed so that that the plurality of openings are substantially free of the polysilicon material.

42. The fluid ejection device of claim 40, wherein the first insulative material comprises a field oxide and portions of the first insulative material where each opening of the plurality of openings are formed comprise a gate oxide.

43. The fluid ejection device of any one of claims 40 to 42, wherein the second conductive material comprises tantalum.

44. The fluid ejection device of any one of claims 40 to 42, wherein the second conductive material comprises a resistive portion and a conductive portion disposed upon the resistive portion.

45. The fluid ejection device of any one of claims 40 to 44, further comprising a plurality of doped regions formed within the substrate and wherein each of the plurality of openings is formed adjacent to the plurality of doped regions.

46. The fluid ejection device of any one of claims 40 to 45, further comprising a fluid handling slot that is fluidically coupled to the plurality of chambers.

47. The fluid ejection device of any one of claims 40 to 42, wherein the second insulative material comprises phosphosilicate glass.

48. The fluid ejection device of claim 40, wherein the first conductive material comprises a resistive portion and a conductive portion disposed upon the resistive portion.

49. The fluid ejection device of any one of claims 40 to 48, wherein the plurality of openings form a path to a region below the first surface of the substrate.

50. A fluid ejection device comprising:

a substrate;

a first insulative material overlying at least a portion of a first surface of the substrate, the first insulative material disposed to include a plurality of openings between portions that allow contact with the substrate;

a first conductive material overlying at least a portion of the first insulative material, the first conductive material being positioned so that the plurality of openings are substantially free of the first conductive material;

a second insulative material overlying at least a portion of the first conductive material and portions of the first insulative material, the second insulative material positioned so that the plurality of openings are substantially free of the second insulative material;

a second conductive material overlying at least a portion of the second insulative material and disposed within the plurality of openings so that some of the second conductive material disposed upon the second insulative material is in electrical contact with the substrate; and

a plurality of resistor elements configured to heat fluid in response to a current, the plurality of resistors being coupled to the first conductive material so that the current is conducted by the first conductive material.

51. The fluid ejection device of claim 50, further comprising a gate oxide and a polysilicon material underlying the first insulative material, the plurality of openings are substantially free of the polysilicon material and the gate oxide.

52. The fluid ejection device of claim 50, further comprising a field oxide underlying the first insulative material and wherein the plurality of openings are free of the field oxide.

53. The fluid ejection device of any one of claims 50 to 52, wherein the second conductive material comprises tantalum.

54. The fluid ejection device of any one of claims 50 to 52, wherein the second conductive material comprises a resistive portion and a conductive portion disposed upon the resistive portion.

55. The fluid ejection device of any one of claims 50 to 54, further comprising a plurality of doped regions formed within the substrate and wherein each of the plurality of openings is formed adjacent to one of the plurality of doped regions.

56. The fluid ejection device of claim 55, wherein the plurality of doped regions form transistors.

57. The fluid ejection device of any one of claims 50 to 56, further comprising a plurality of fluid chambers each disposed above one resistor of the plurality of resistors and an orifice positioned to allow ejection of fluid from the fluid chamber via the orifice.

58. The fluid ejection device of any one of claims 50 to 52, wherein the second insulative material comprises phosphosilicate glass.

59. The fluid ejection device of any one of claim 50, wherein the first conductive material comprises a resistive portion and a conductive portion overlying the resistive portion.

60. The fluid ejection device of any one of claims 50 to 59, wherein the plurality of openings form a path to a region below a surface of the substrate.

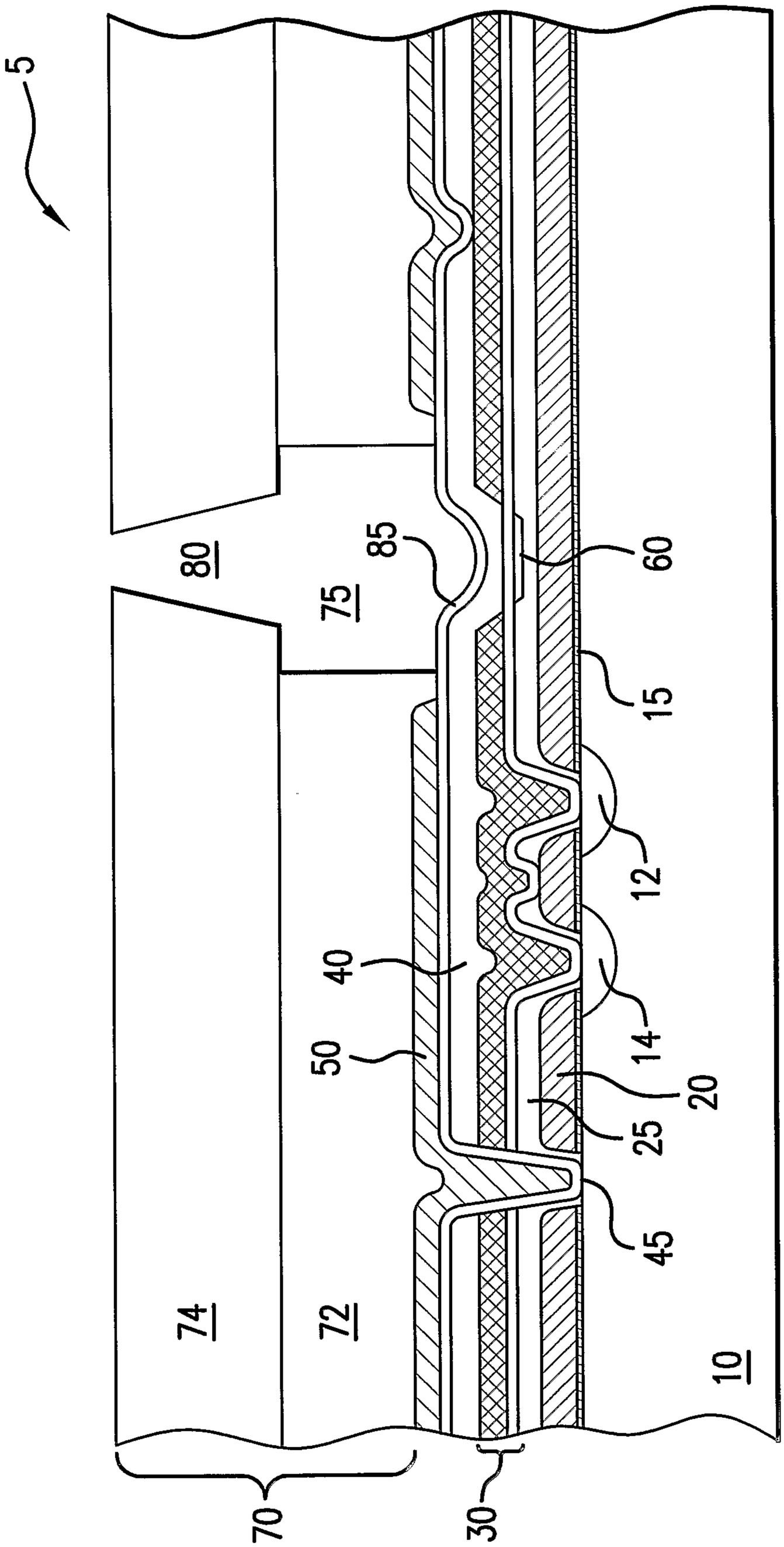


FIG. 1

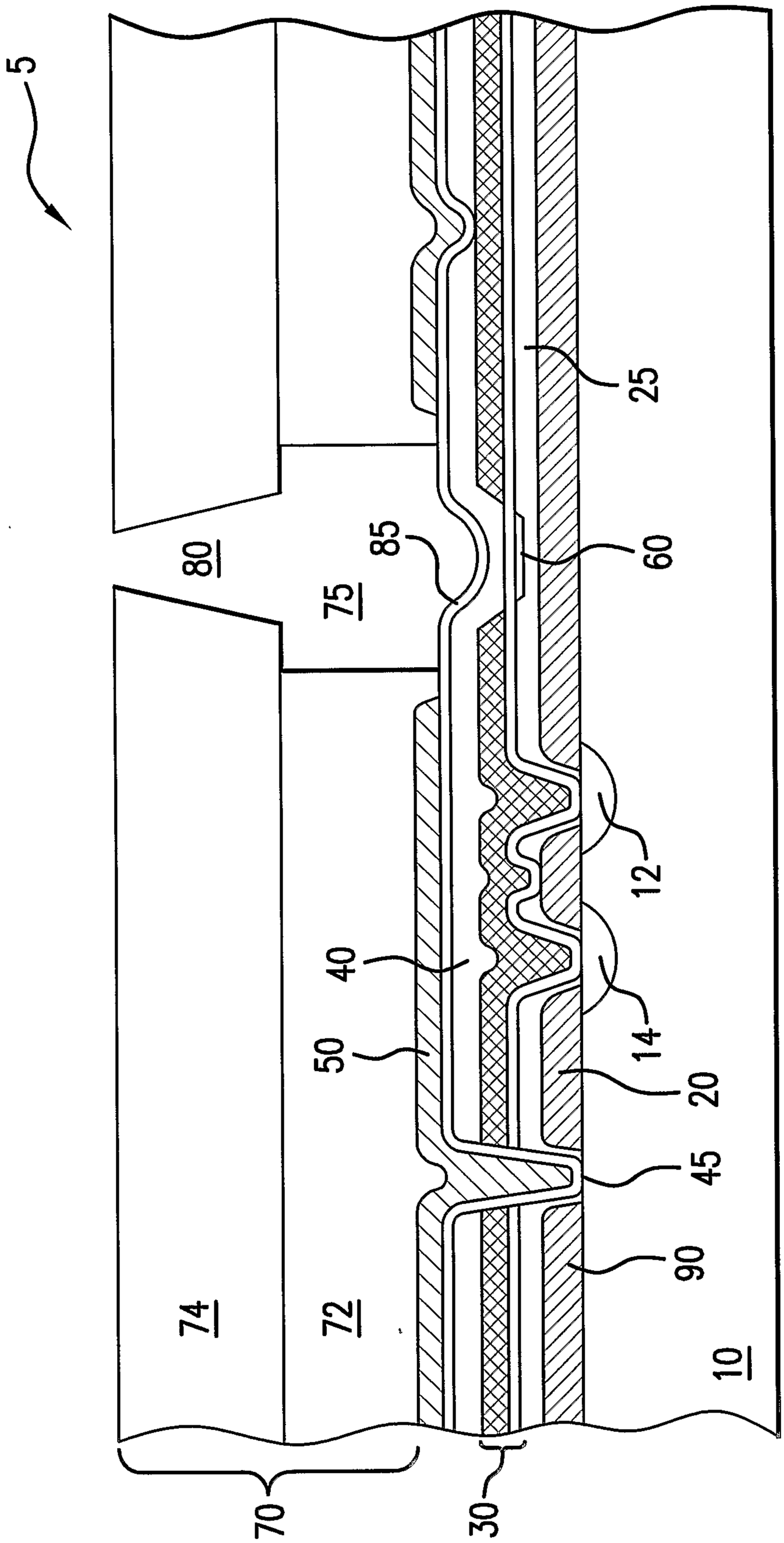


FIG.2

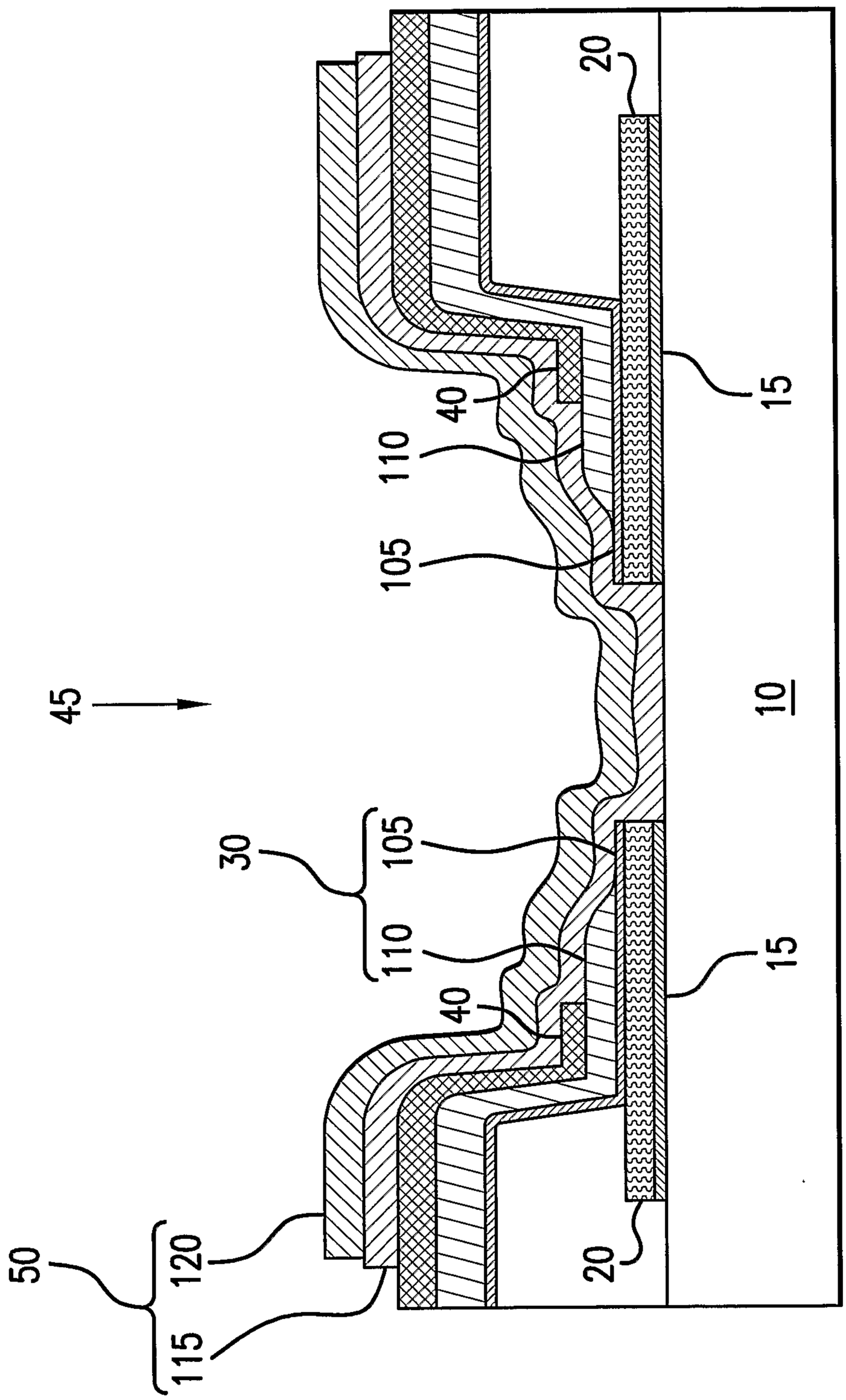


FIG.3

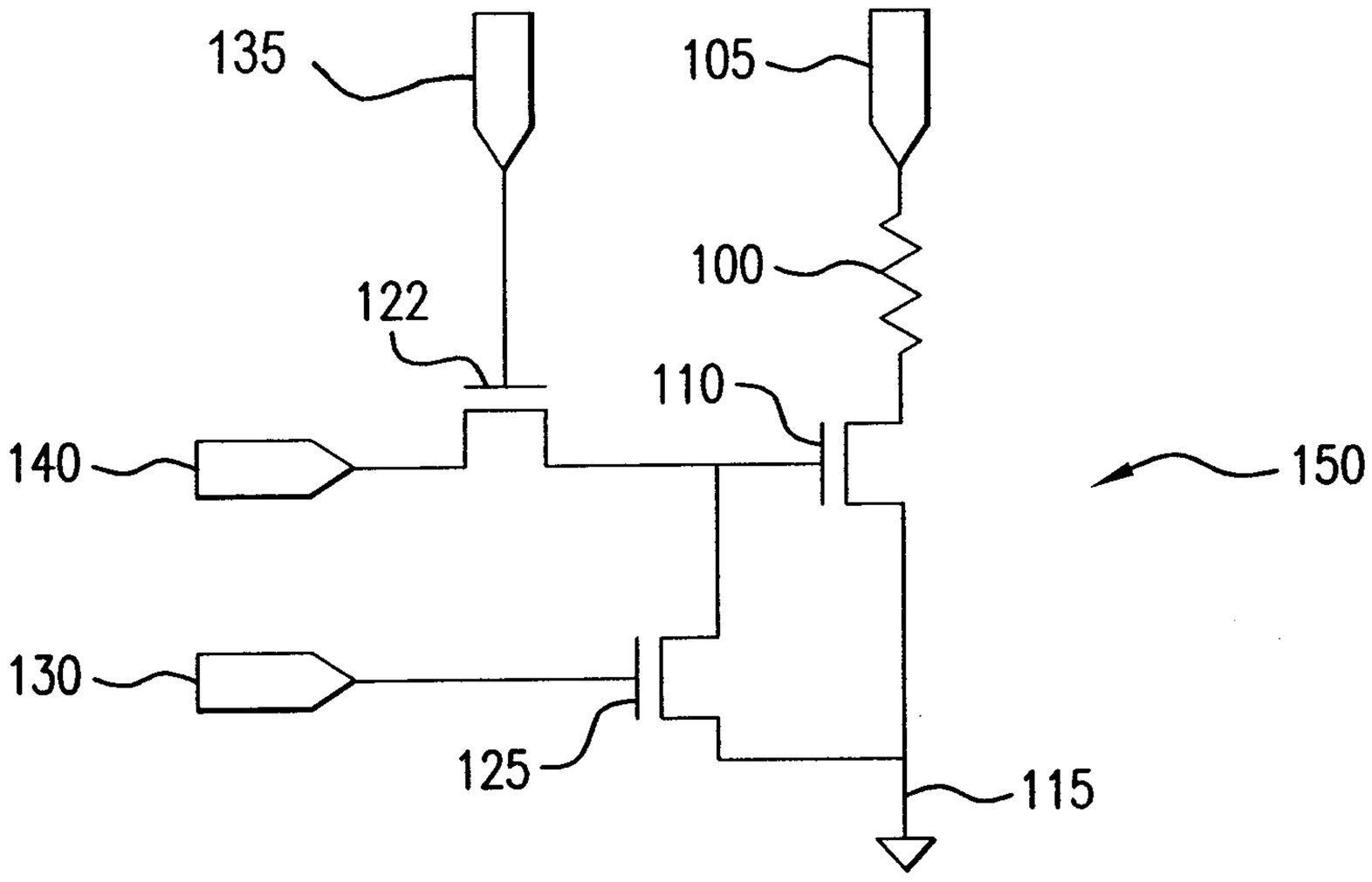


FIG.4

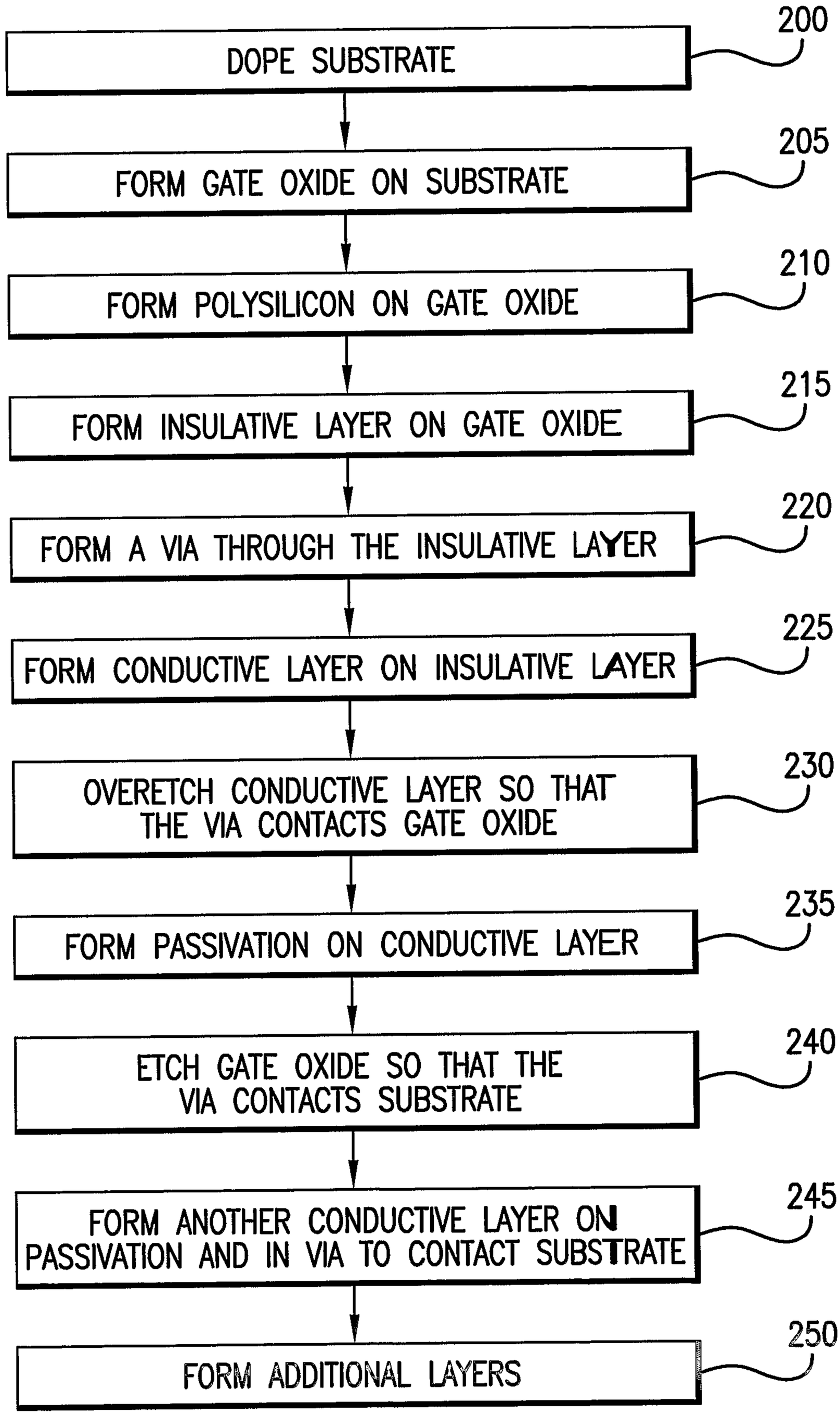

DOPE SUBSTRATE
200
FORM GATE OXIDE ON SUBSTRATE
205
FORM POLYSILICON ON GATE OXIDE
210
FORM INSULATIVE LAYER ON GATE OXIDE
215
FORM A VIA THROUGH THE INSULATIVE LAYER
220
FORM CONDUCTIVE LAYER ON INSULATIVE LAYER
225
OVERETCH CONDUCTIVE LAYER SO THAT THE VIA CONTACTS GATE OXIDE
230
FORM PASSIVATION ON CONDUCTIVE LAYER
235
ETCH GATE OXIDE SO THAT THE VIA CONTACTS SUBSTRATE
240
FORM ANOTHER CONDUCTIVE LAYER ON PASSIVATION AND IN VIA TO CONTACT SUBSTRATE
245
FORM ADDITIONAL LAYERS
250

FIG.5

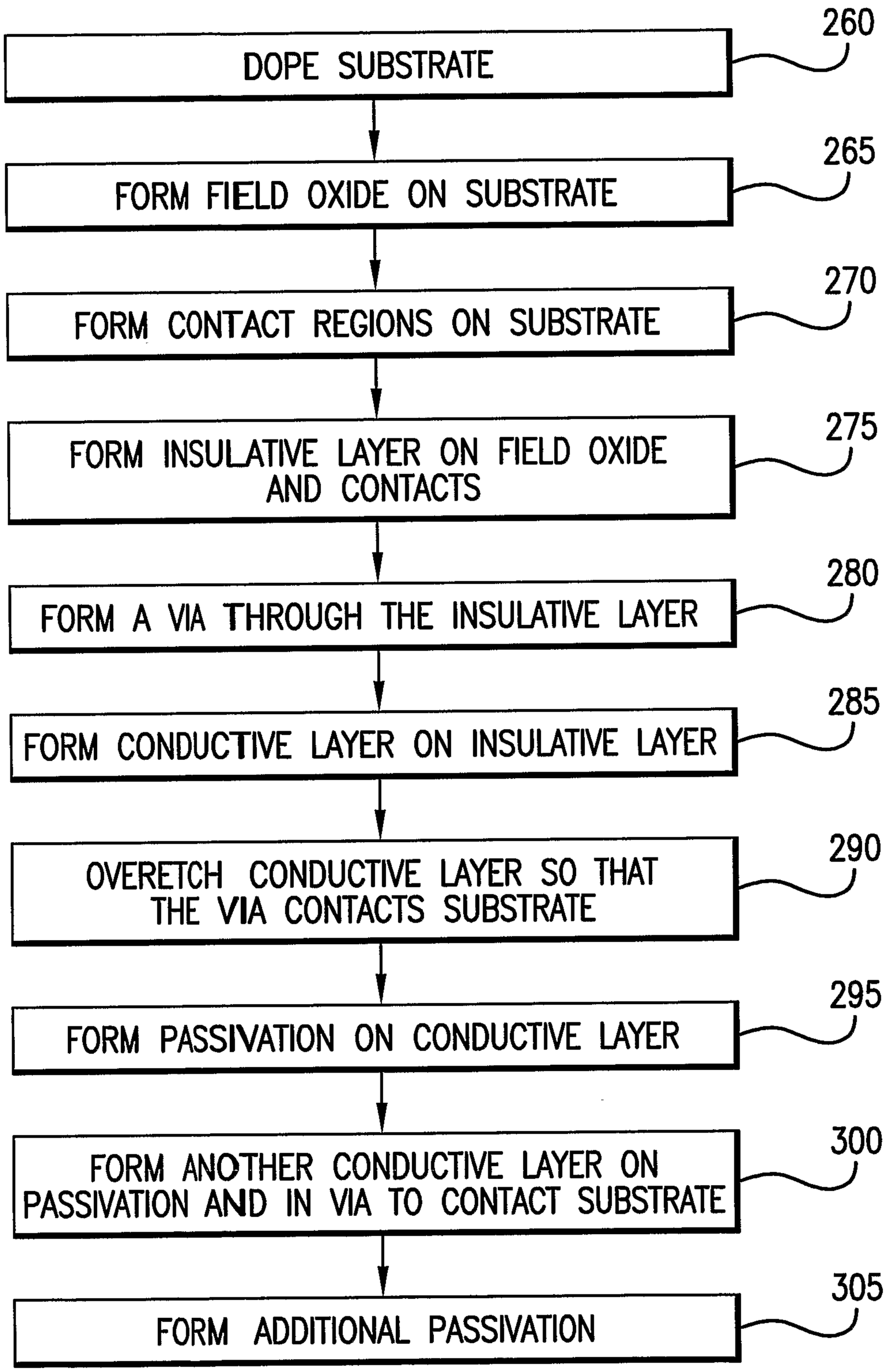

DOPE SUBSTRATE
260
FORM FIELD OXIDE ON SUBSTRATE
265
FORM CONTACT REGIONS ON SUBSTRATE
270
FORM INSULATIVE LAYER ON FIELD OXIDE AND CONTACTS
275
FORM A VIA THROUGH THE INSULATIVE LAYER
280
FORM CONDUCTIVE LAYER ON INSULATIVE LAYER
285
OVERETCH CONDUCTIVE LAYER SO THAT THE VIA CONTACTS SUBSTRATE
290
FORM PASSIVATION ON CONDUCTIVE LAYER
295
FORM ANOTHER CONDUCTIVE LAYER ON PASSIVATION AND IN VIA TO CONTACT SUBSTRATE
300
FORM ADDITIONAL PASSIVATION
305

FIG. 6

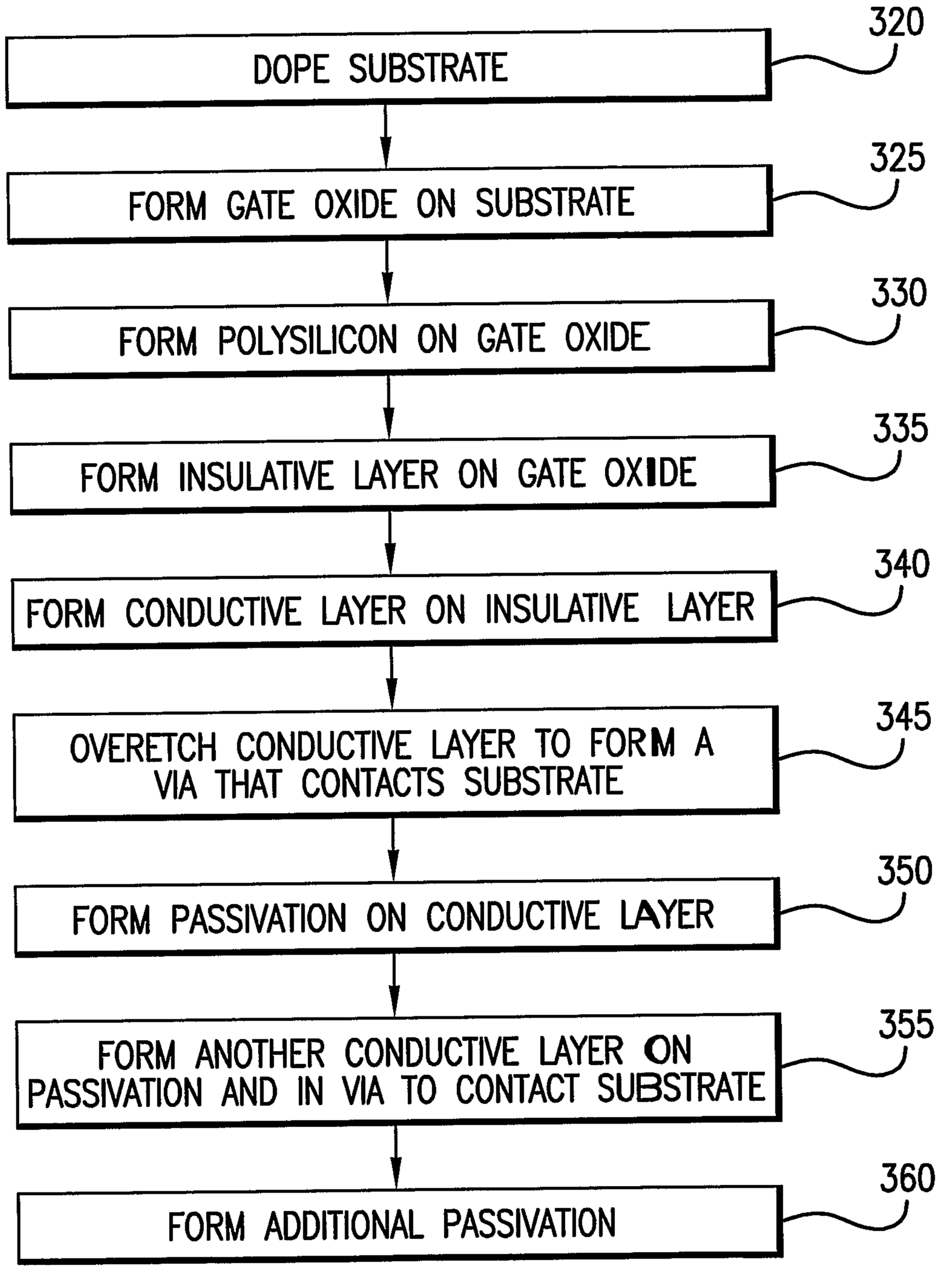

DOPE SUBSTRATE
320
FORM GATE OXIDE ON SUBSTRATE
325
FORM POLYSILICON ON GATE OXIDE
330
FORM INSULATIVE LAYER ON GATE OXIDE
335
FORM CONDUCTIVE LAYER ON INSULATIVE LAYER
340
OVERETCH CONDUCTIVE LAYER TO FORM A VIA THAT CONTACTS SUBSTRATE
345
FORM PASSIVATION ON CONDUCTIVE LAYER
350
FORM ANOTHER CONDUCTIVE LAYER ON PASSIVATION AND IN VIA TO CONTACT SUBSTRATE
355
FORM ADDITIONAL PASSIVATION
360

FIG.7

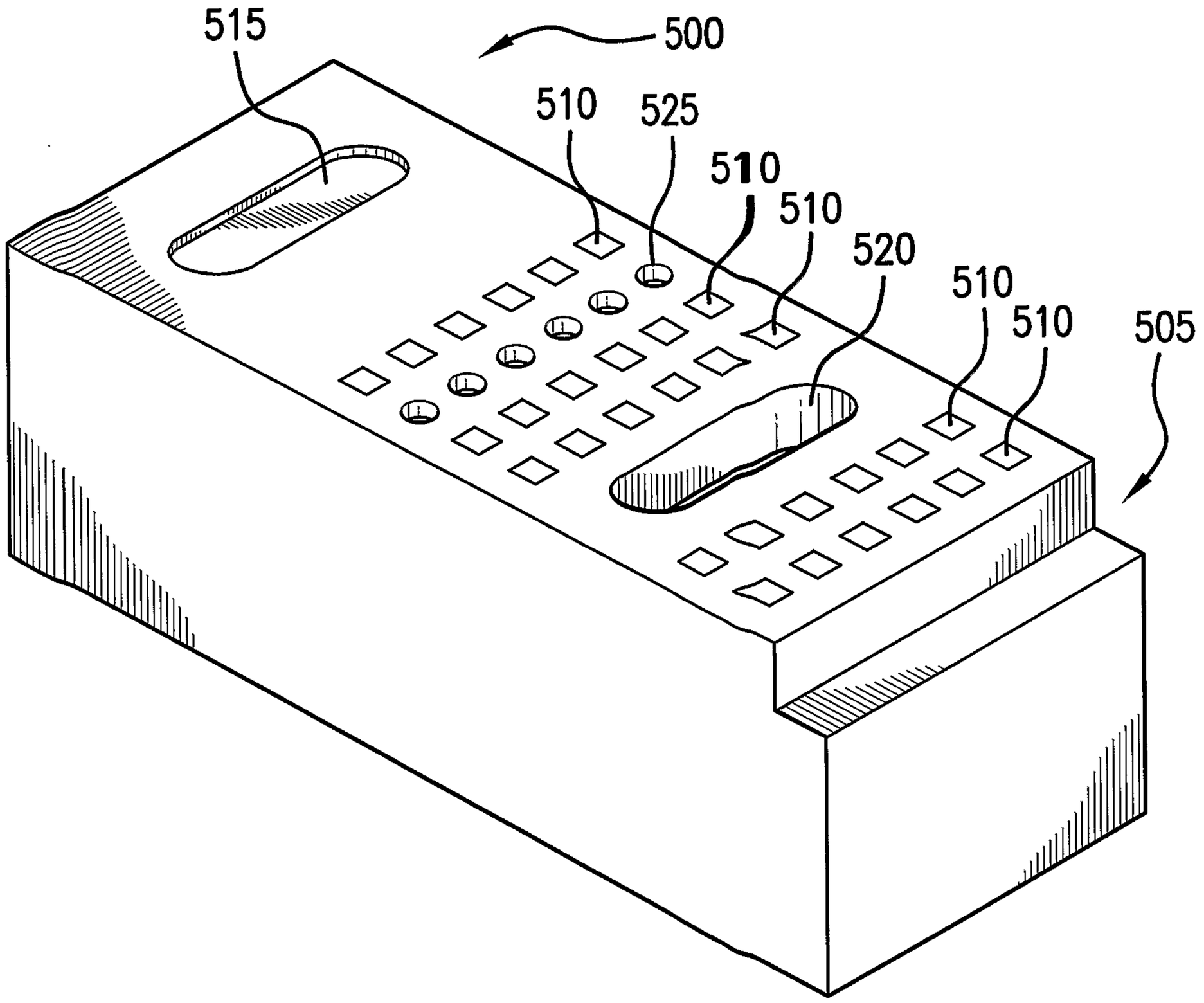


FIG.8

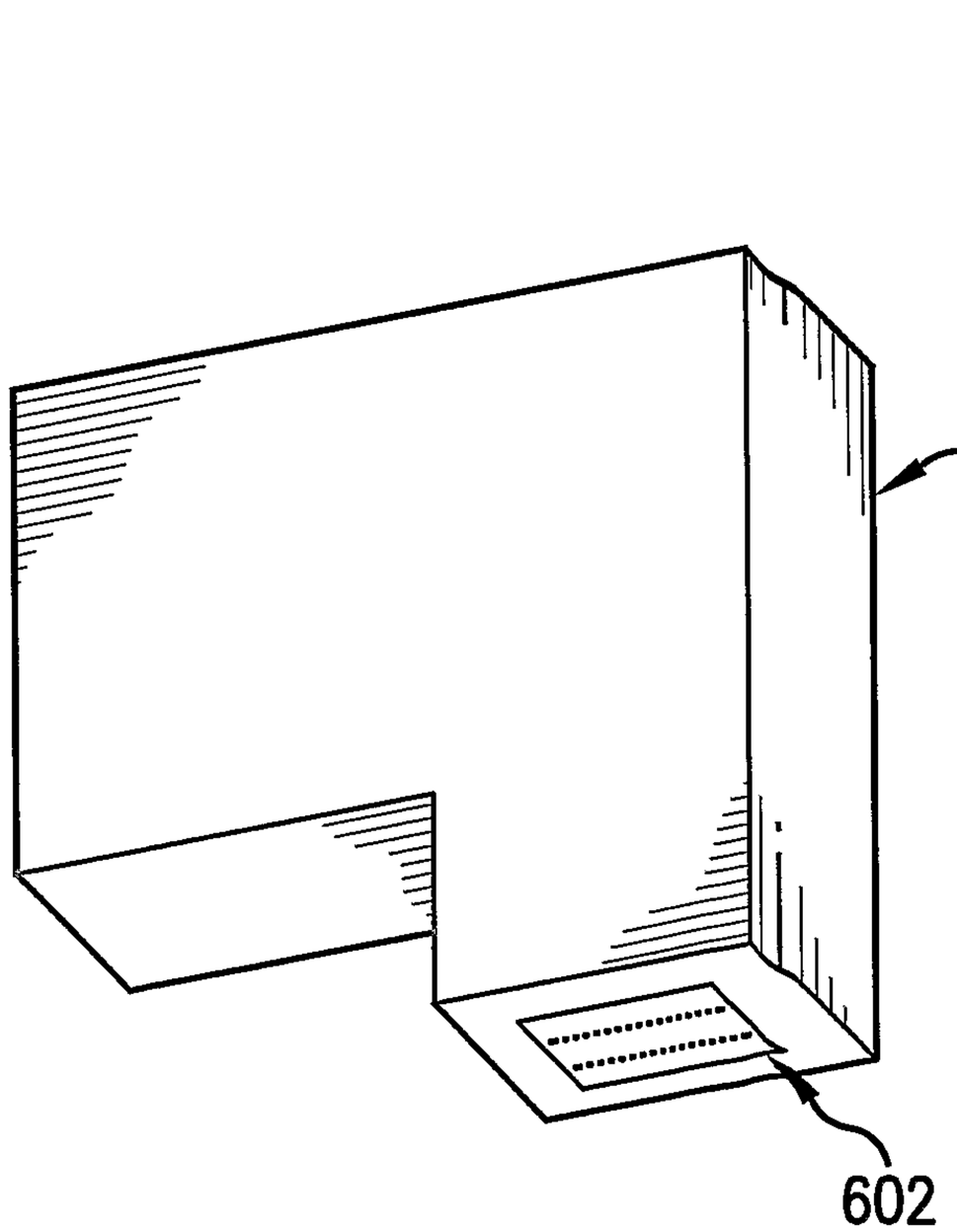
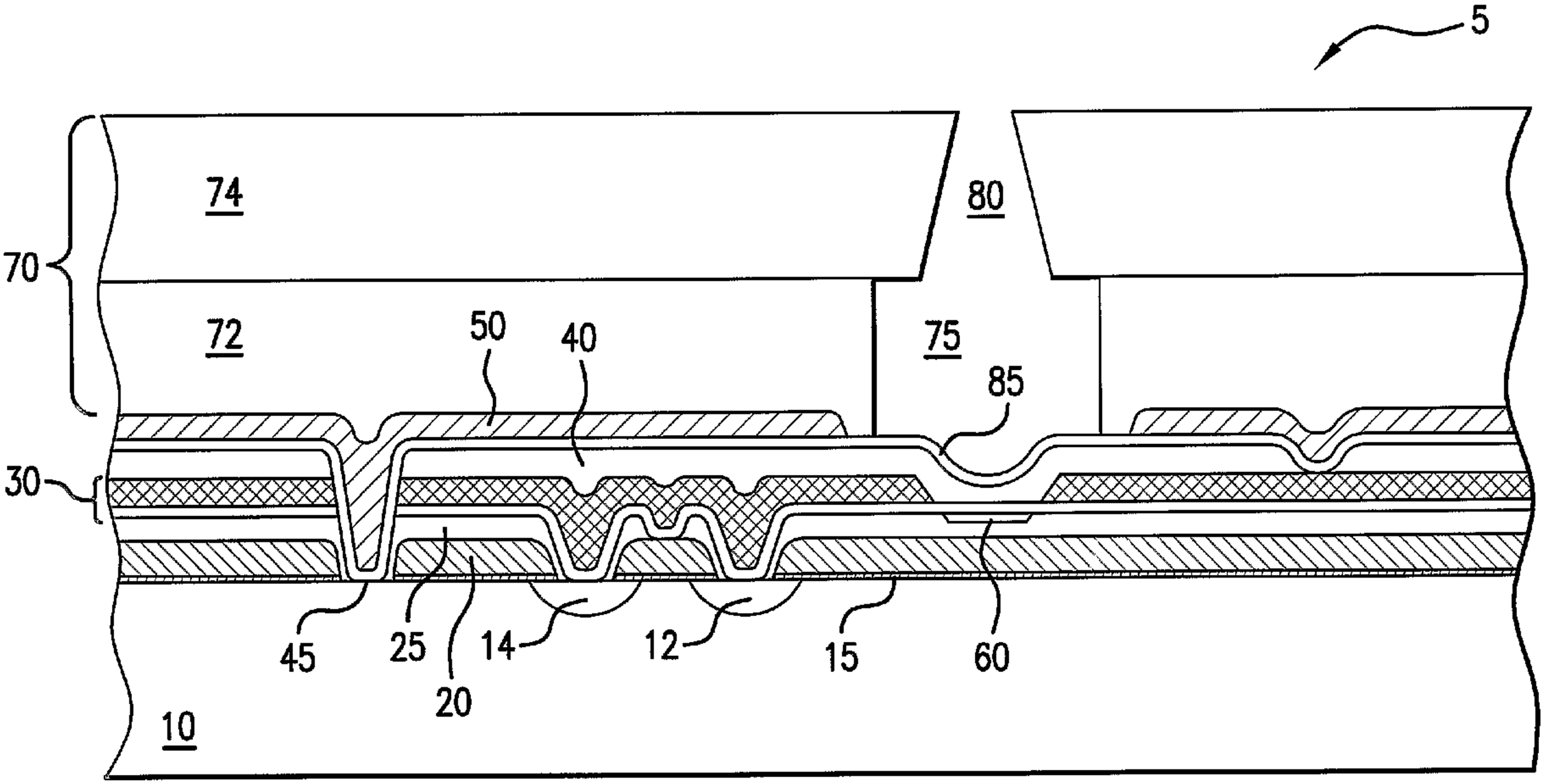


FIG.9


5
74
80
70
72
50
40
75
85
30
45
25
20
14
12
15
60
10