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(54) **COMPLEMENTARY METAL OXIDE SEMICONDUCTOR IMAGE SENSOR AND METHOD FOR FABRICATING THE SAME**

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(57) **ABSTRACT**

A complementary metal oxide semiconductor image sensor and a method for fabricating the same are disclosed, wherein a width of a depletion area of a photodiode is varied by variably applying a back bias voltage to a semiconductor substrate without using any color filter, thereby preventing a back bias voltage from influencing a transistor formed on the outside of a photodiode in a CMOS image sensor sensing optical color sensitivity of light rays irradiated to the photodiode. The CMOS image sensor includes a first conductive semiconductor substrate having a first region for forming a photodiode and a second region for forming transistors and having a back bias voltage for varying a width of a depletion area in the first region applied thereon, a plurality of transistors formed in the second region of the semiconductor substrate, a photodiode formed in the first region of the semiconductor substrate, a second conductive buried layer formed in the second region of the semiconductor substrate, so as to prevent the back bias voltage from influencing the transistors, and a first isolating barrier formed within the semiconductor substrate, so as to surround a side portion of the second region.

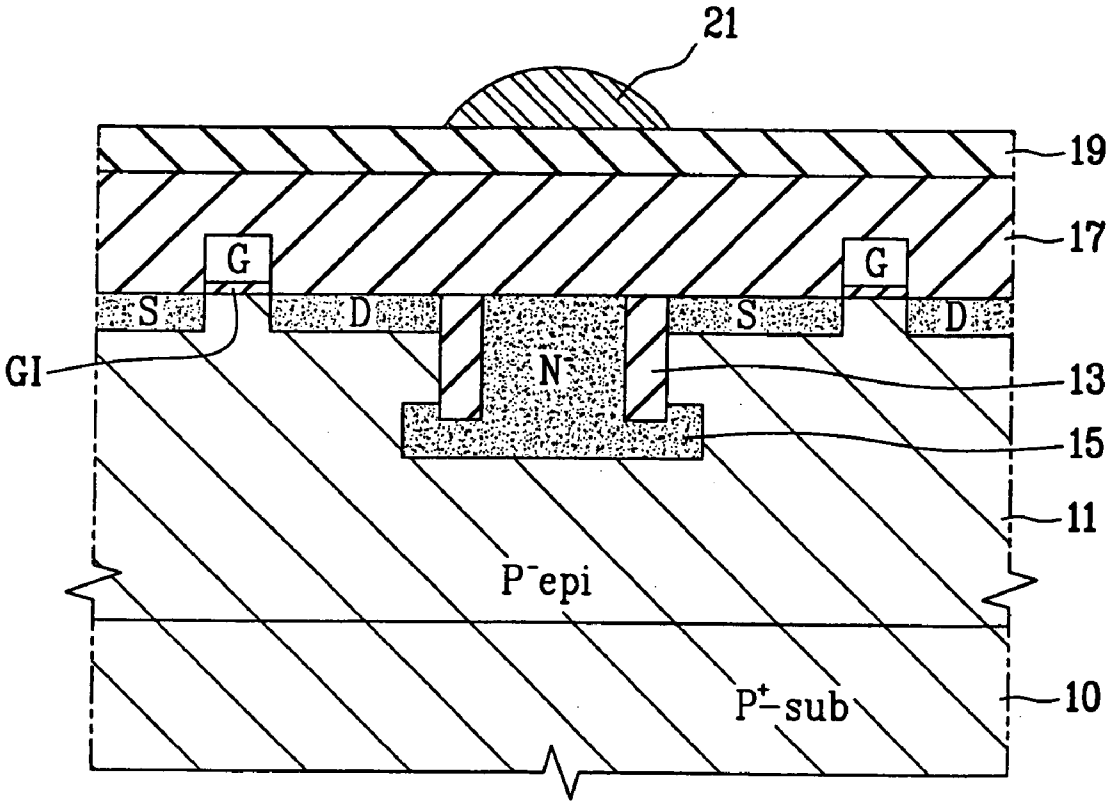


FIG. 1
Related Art

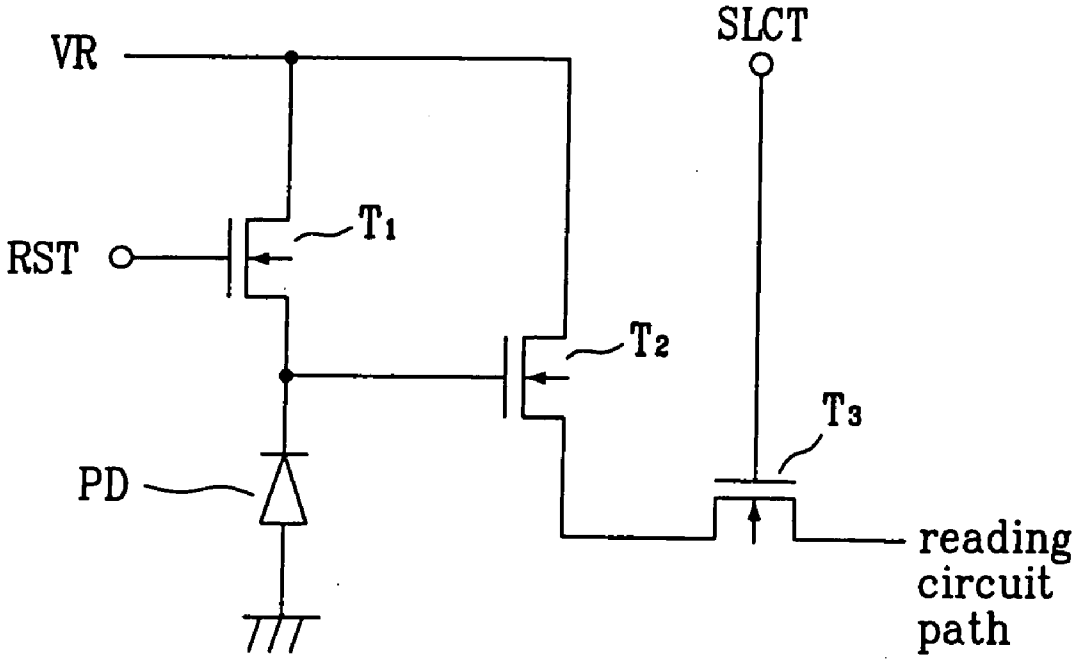


FIG. 2
Related Art

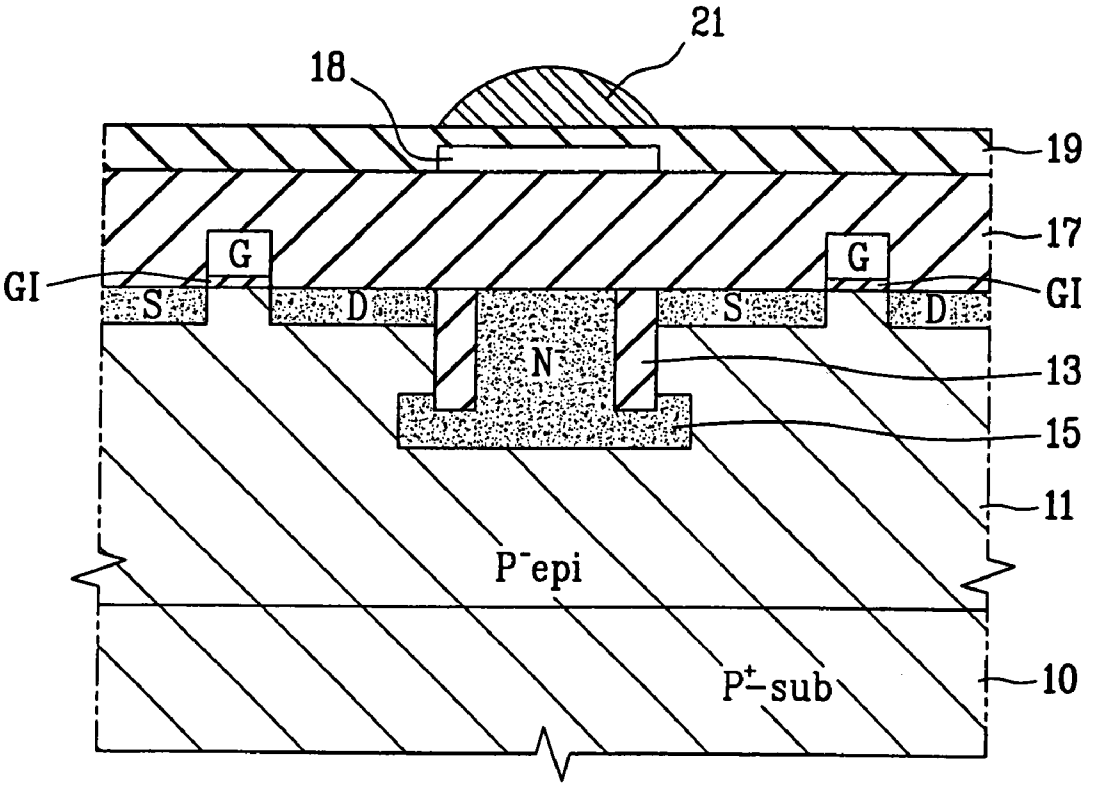


FIG. 3

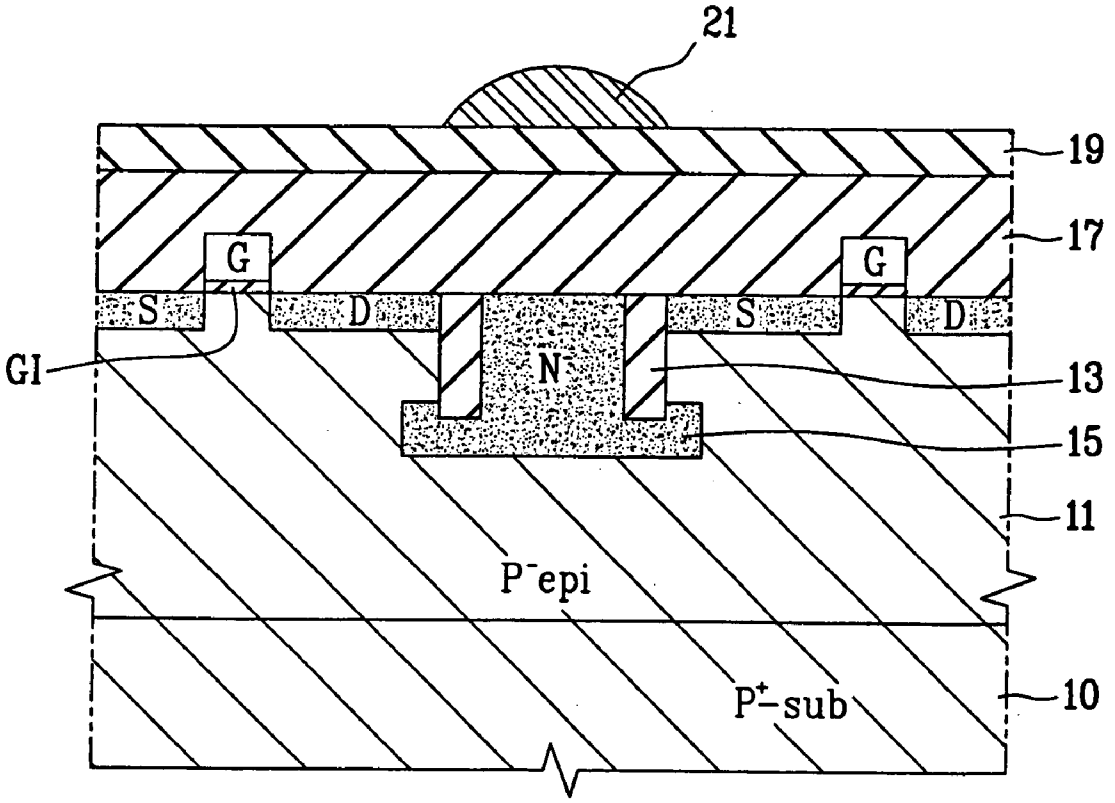


FIG. 4

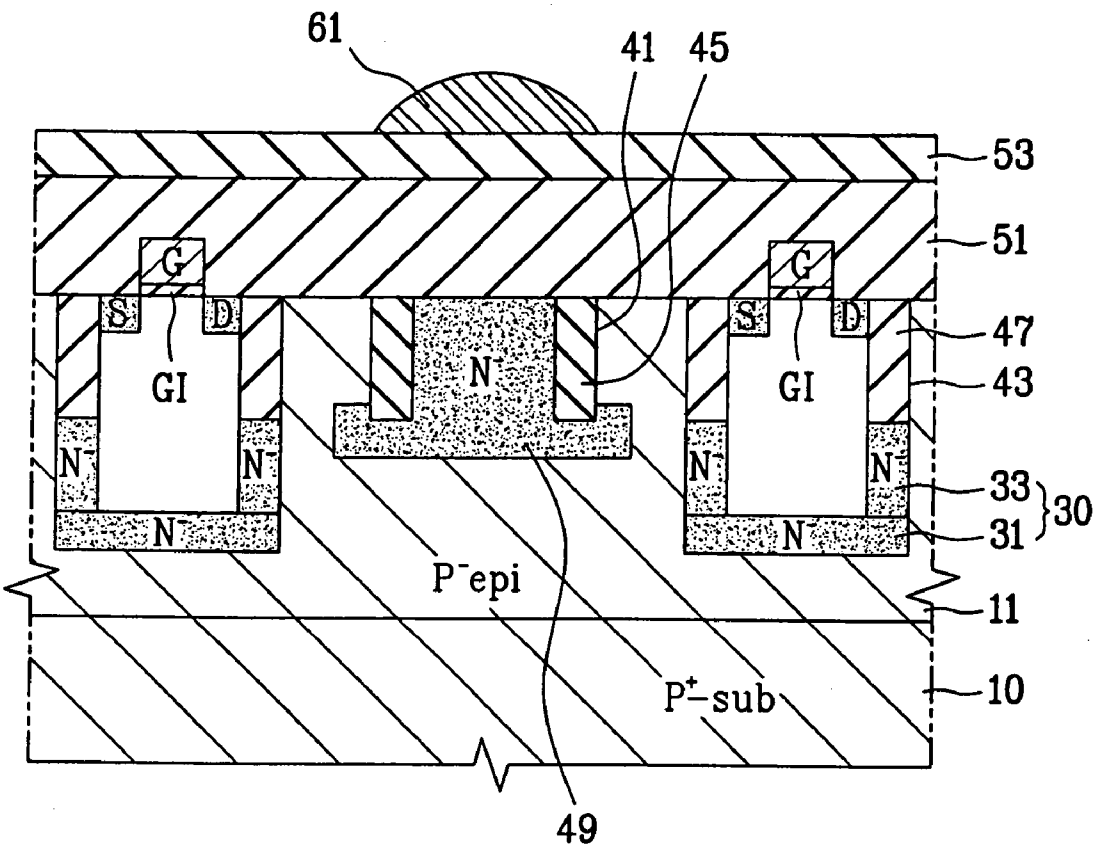


FIG. 5

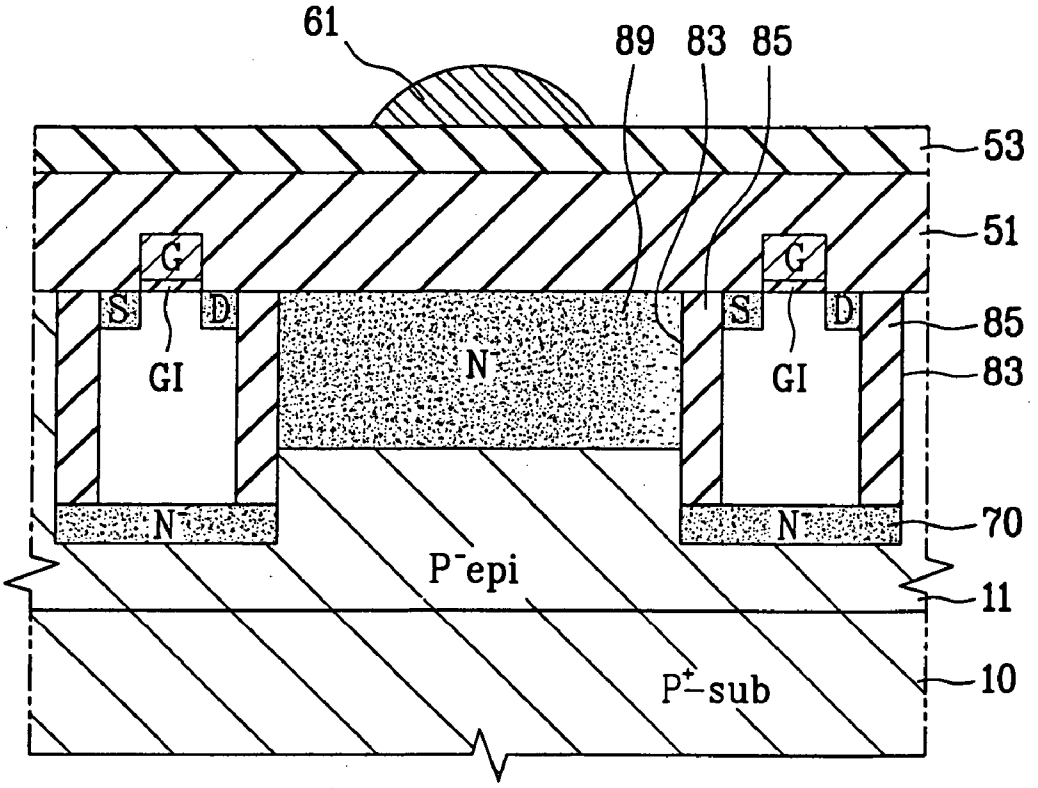


FIG. 6A

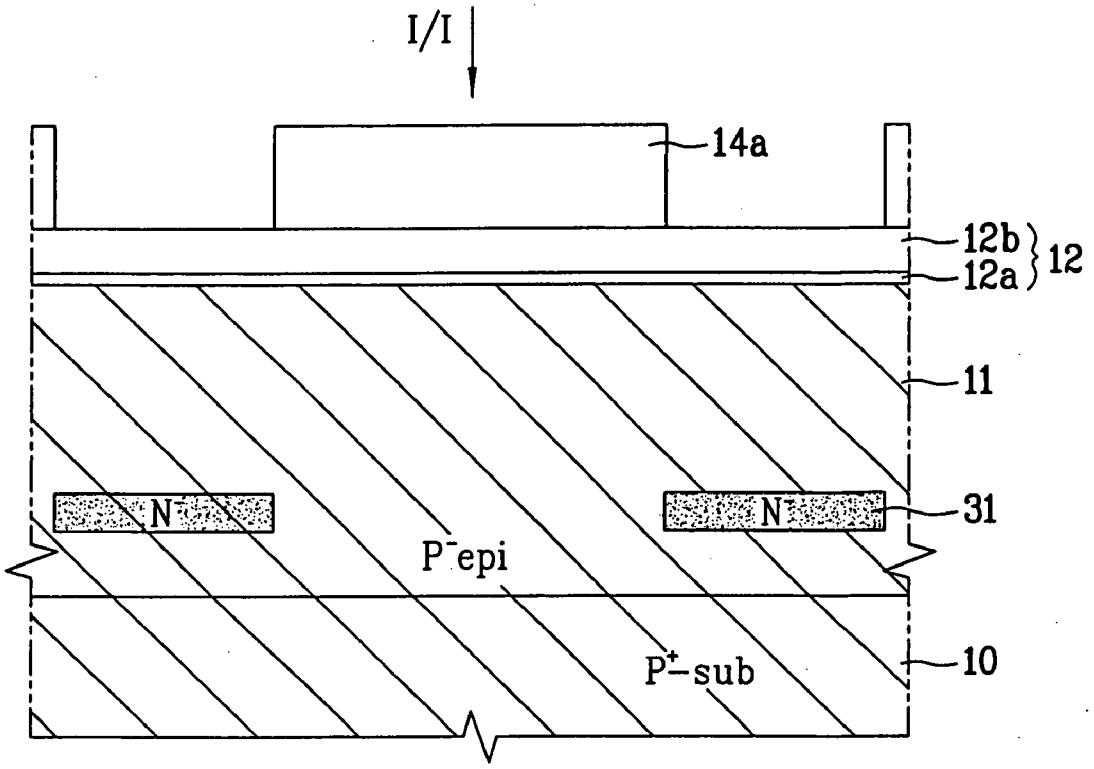


FIG. 6B

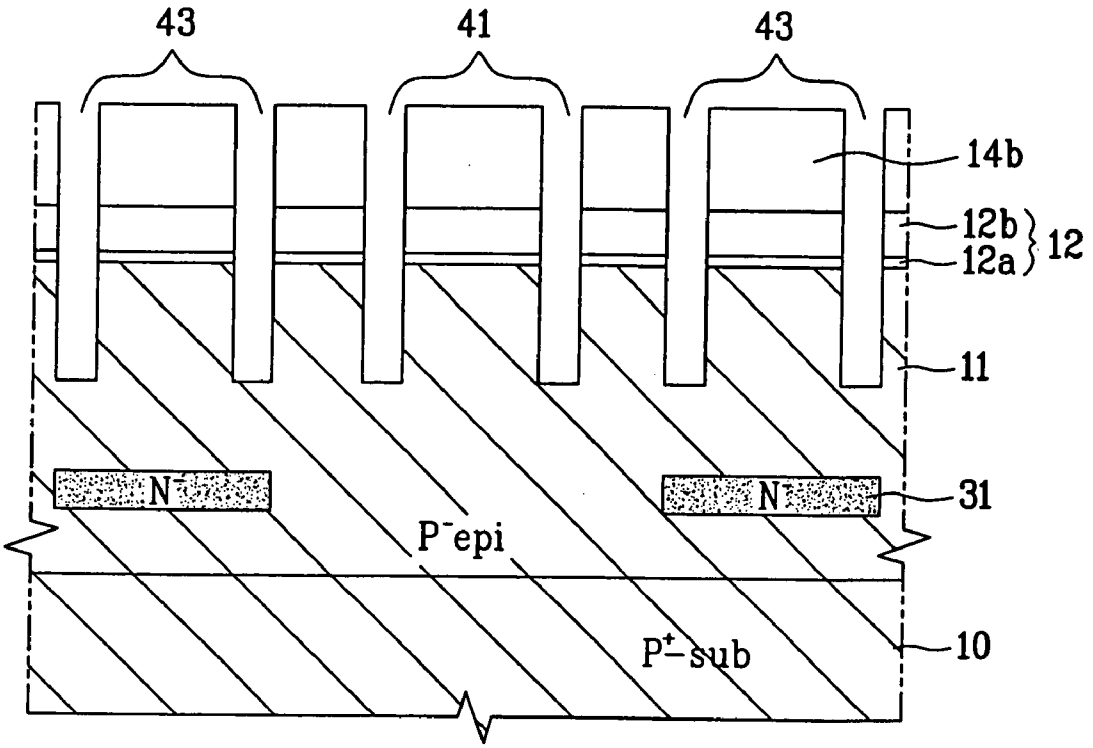


FIG. 6C

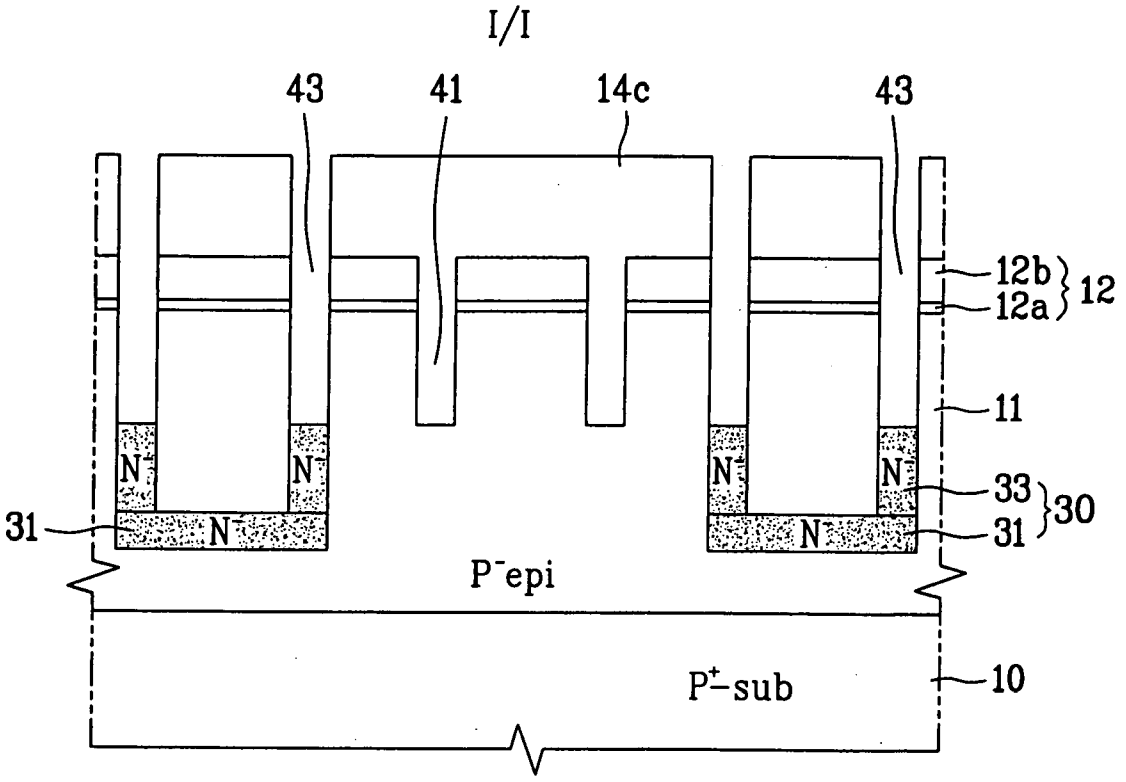


FIG. 6D

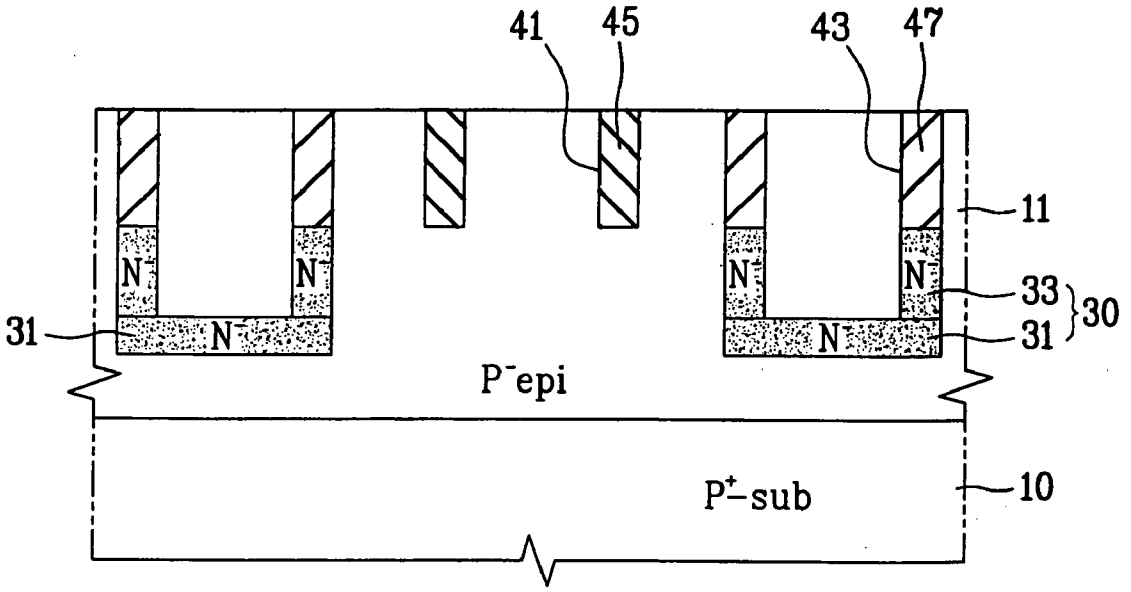


FIG. 6E

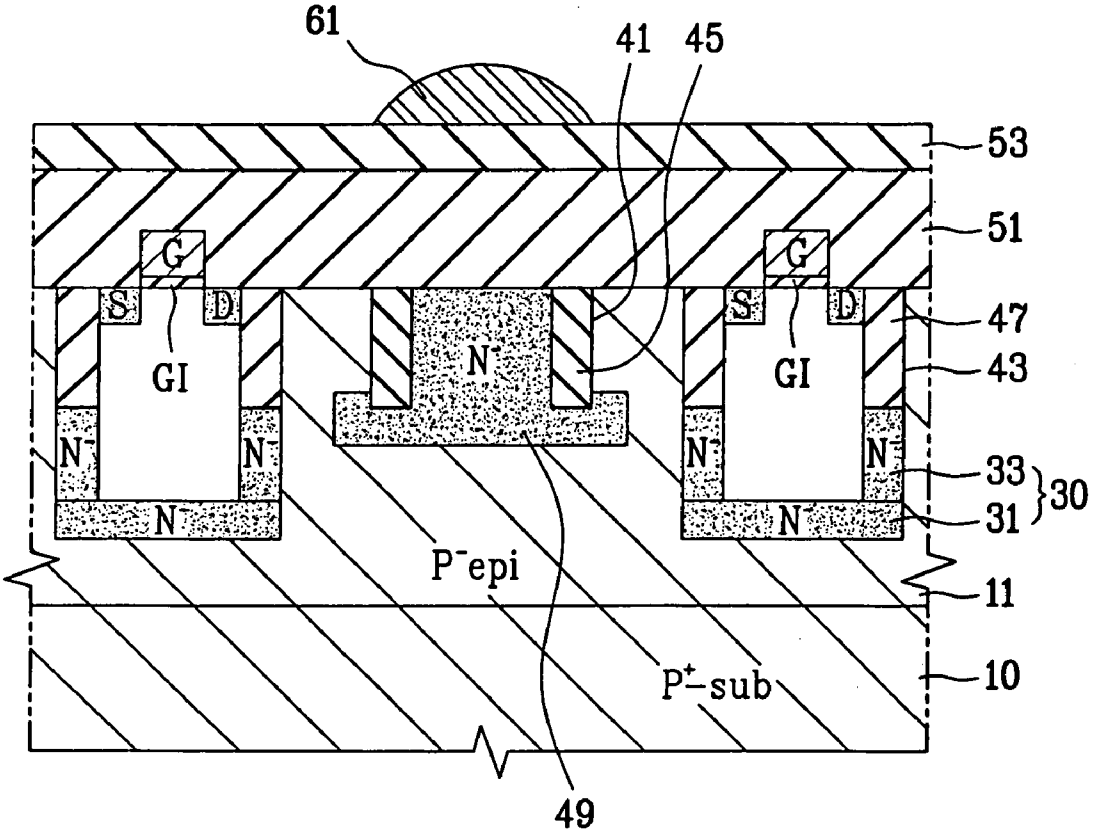


FIG. 7A

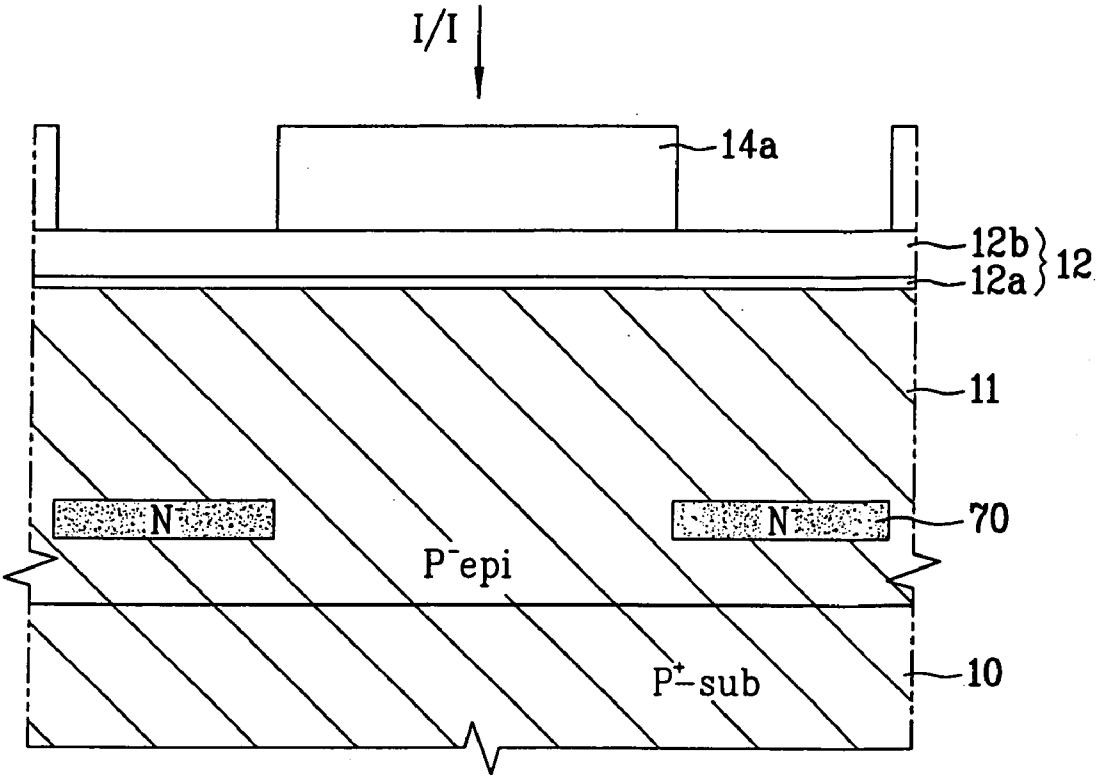


FIG. 7B

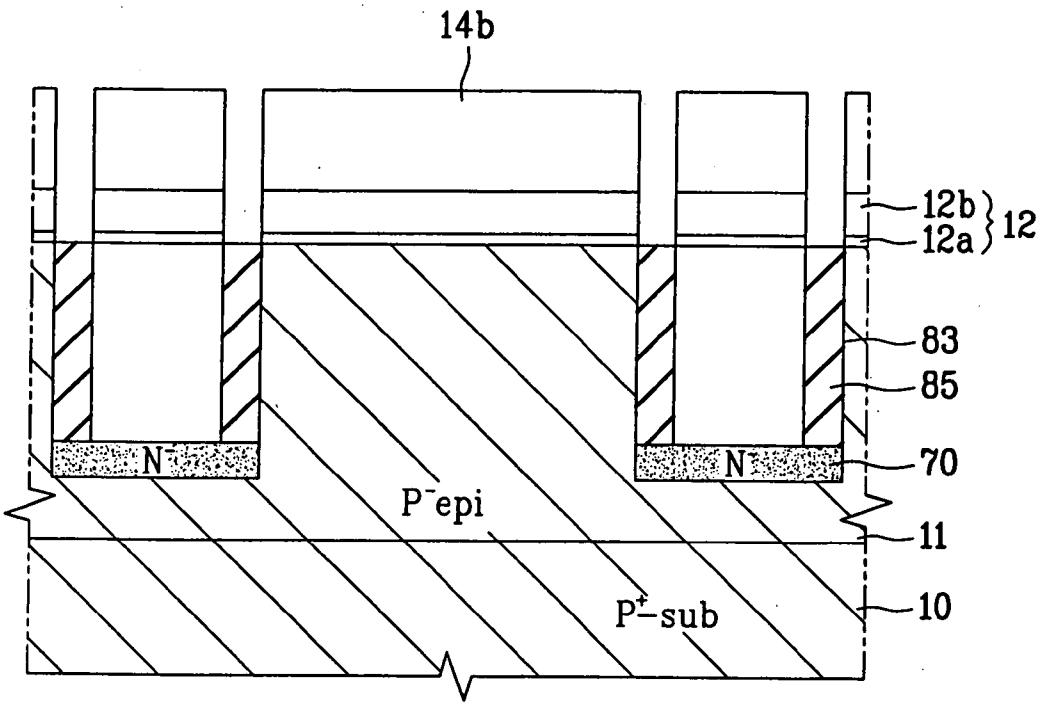
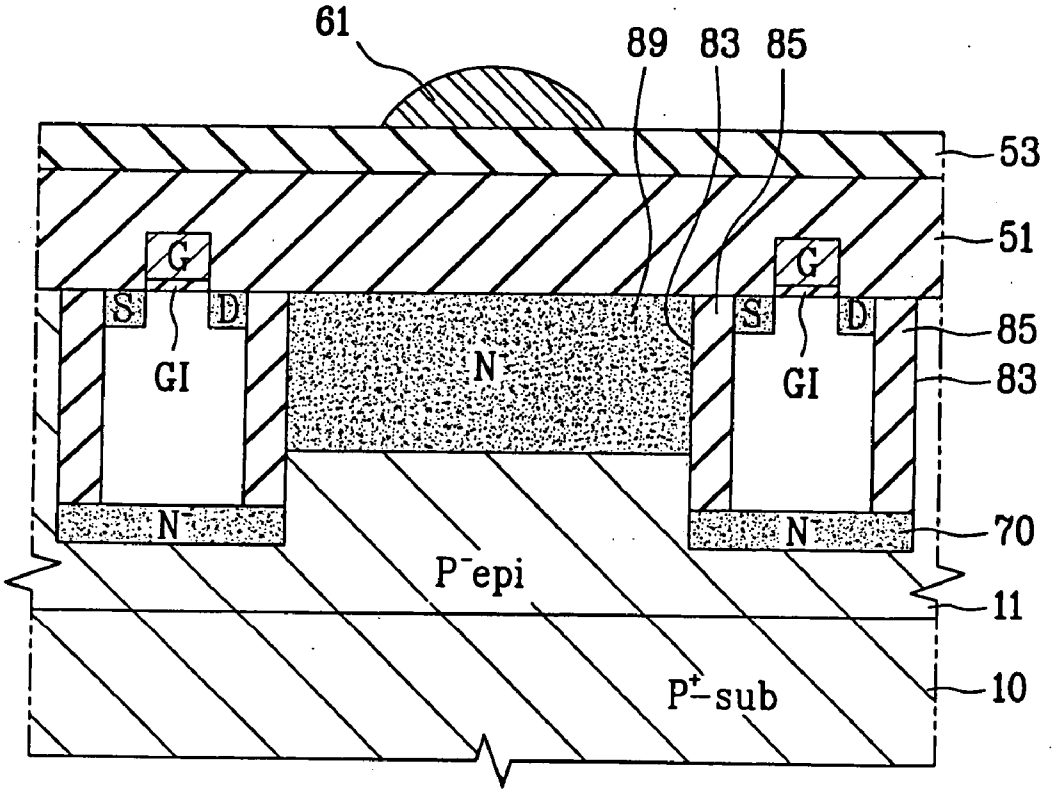


FIG. 7C



COMPLEMENTARY METAL OXIDE SEMICONDUCTOR IMAGE SENSOR AND METHOD FOR FABRICATING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of Korean Application No. P2003-100950, filed on Dec. 30, 2003, which is hereby incorporated by reference as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to an image sensor, and more particularly, to a complementary metal oxide semiconductor (CMOS) image sensor and a method for fabricating the same. Although the present invention is suitable for a wide scope of applications, it is particularly suitable for preventing a back bias voltage from influencing a transistor formed on the outside of a photodiode in a CMOS image sensor sensing optical color sensitivity of the colors of red, green, and blue, which are included in light rays irradiated to the photodiode, without using any color filters.

[0004] 2. Discussion of the Related Art

[0005] Generally, an image sensor is a semiconductor device for converting an optical image into an electric signal. The image sensor can be broadly categorized into a charge coupled device (CCD) and a complementary metal oxide semiconductor (CMOS) image sensor (CIS).

[0006] The charge coupled device (CCD) includes a plurality of photodiodes (PD) aligned in a matrix form and converting light signals into electric signals, a plurality of vertical charge coupled devices (VCCD) formed between each vertical photodiode aligned in a matrix form and vertically transmitting electric charges generated from each photodiode, a horizontal charge coupled device (HCCD) horizontally transmitting the electric charges transmitted by each of the vertical charged couple devices (VCCD), and a sense amplifier sensing and outputting the horizontally transmitted electric charges.

[0007] However, the charged couple device (CCD) has the disadvantages of a complicated driving method, high power consumption, and a complicated fabrication process requiring a multi-phased photo process. Also, in the charge coupled device (CCD), a control circuit, a signal processing circuit, an analog to digital (A/D) converter circuit, and so on cannot be easily integrated into a charge coupled device chip, thereby having the problem of forming compact size products.

[0008] Recently, the complementary metal oxide semiconductor (CMOS) image sensor has been considered to be the next generation image sensor that can resolve the problems and disadvantages of the charge coupled device (CCD). The CMOS image sensor is a device adopting a CMOS technology using the control circuit, the signal processing circuit, and so on as a peripheral circuit, so as to form MOS transistors corresponding to the number of unit pixels on a semiconductor substrate, in order to sequentially detect the electric signals of each unit pixel by using a switching method, thereby representing an image.

[0009] Since the CMOS image sensor uses a CMOS fabrication technology, the CMOS image sensor is advantageous in that it has low power consumption and has a simple fabrication method through less photo process steps. Also, in the CMOS image sensor, a control circuit, a signal processing circuit, an A/D converter circuit, and so on can be integrated in a CMOS image sensor chip, thereby enabling the product to be fabricated in a compact size. Accordingly, the CMOS image sensor is currently being extensively used in various applied technologies, such as digital still cameras and digital video cameras.

[0010] A general CMOS image sensor will now be described with reference to the accompanying drawings.

[0011] FIG. **1** illustrates a schematic view of an equivalent circuit of one unit pixel in a general CMOS image sensor, and FIG. **2** illustrates a cross-sectional view of a related art CMOS image sensor.

[0012] Referring to FIG. **1**, a unit pixel of a general CMOS image sensor is formed of one photodiode (PD) and three NMOS transistors (T**1**, T**2**, and T**3**). A cathode of the photodiode (PD) is integrated to a drain of a first nMOS transistor (T**1**) and a gate of a second nMOS transistor (T**2**). And, the sources of both first and second nMOS transistors (T**1** and T**2**) are connected to a power line supplying a reference voltage (VR). The gate of the first nMOS transistor (T**1**) is connected to a reset line providing a reset signal (RST). Also, a source of a third nMOS transistor (T**3**) is connected to the drain of the second nMOS transistor (T**2**), the drain of the third nMOS transistor (T**3**) is connected to a reading circuit (not shown) through a signal line, and the gate of the third nMOS transistor (T**3**) is connected to a column select line providing a select signal (SLCT). Therefore, the first nMOS transistor (T**1**) is referred to as the reset transistor; the second NMOS transistor (T**2**) is referred to as a driving transistor, and the third nMOS transistor (T**3**) is referred to as a selecting transistor.

[0013] The structure of the CMOS image sensor will now be described in detail.

[0014] Referring to FIG. **2**, a p-type epitaxial layer **11** having an active area and a field area defined thereon is formed on a p-type semiconductor substrate **10**, and a field insulating laser (not shown) is formed in the field area. In the active area, an isolating barrier **13** is formed between a first region for forming the photodiode and a second region for forming the transistors. And, an n-type diffusion area is formed by ion injecting n-type impurities in the first region for forming the photodiode (PD) of the active area.

[0015] In addition, a gate electrode (G) and a gate insulator (GI) are formed in the second region of the p-type epitaxial layer **11**. And, a source/drain (S/D) area is formed by ion-injecting impurities in the p-type epitaxial layer **11** on both sides of the gate electrode (G), thereby forming the transistor (TR). A transparent interlayer dielectric **17** is formed on an entire surface of the substrate including the photodiode (PD) and the transistor (TR). A color filter layer **18** is formed on the interlayer dielectric **17** formed above the photodiode (PD). A planarization layer **19** is formed on the interlayer dielectric **17** including the color filter layer **18**.

Then, a micro lens **21** is formed on the planarization layer **19** formed above the photodiode (PD).

[**0016**] Herein, the transistor (TR) is formed in an optical electric charge transmitter transmitting optical electric charges generated from the photodiode (PD). In the related art, only two transistors are aligned on the substrate **10** for simplicity, however, it is obvious to a person skilled in the art that a plurality of transistors is aligned on the substrate. Also, the semiconductor substrate **10** is formed of a p-type polycrystalline silicon substrate, and the color filter layer **18** is formed of photosensitive layers using red, green, and blue color dyes.

[**0017**] Generally, in the CMOS image sensor having the above-described structure, the color filter layer **18** is sequentially formed on the interlayer dielectric **17**. More specifically, the photosensitive layer using a red color dye is coated by using a spin-coating process, exposed to light, and developed. The developed photosensitive layer is then remained on the color filter forming area in the interlayer dielectric **17**, which is perpendicular to the photodiode (PD), and the photosensitive layer in the other areas is removed, thereby forming the color filter layer. By repeating the above-described method, the red, green, and blue color filter layers **18** are formed.

[**0018**] Therefore, in the related art, in order to form red, green, and blue color filter layers **18** having a color filter array, the coating, exposing, and developing processes should each be repeated three times, which not only complicates the fabrication process of the color filter array but also prevents the transmissivity of the red, green, and blue light rays each passing through the color filer layer from being uniformly maintained.

[**0019**] Recently, in order to resolve such problems of the color filter array, many alternative methods of sensing each of the red, green, and blue light rays without using the color filter have been proposed. Among the proposed methods, a method of using a micro prism is disclosed in the Korean Patent Application No. 10-2003-0056096. Also, a method of using a multiple slits is disclosed in the Korean Patent Application No. 10-2002-0039454. However, in the above-referenced methods, the fabrication processes of the micro prism and the multiple slits are very complicated and have many limitations in essentially resolving the problem of the complicated fabrication process of the CMOS image sensor.

SUMMARY OF THE INVENTION

[**0020**] Accordingly, the present invention is directed to a CMOS image sensor and a method for fabricating the same that substantially obviate one or more problems due to limitations and disadvantages of the related art.

[**0021**] An object of the present invention is to provide a CMOS image sensor and a method for fabricating the same that can easily sense red, green, and blue light rays by using a method of calculating a color sensitivity of red, green, and blue in accordance with an optical wave within a depletion area, wherein the width of the depletion area of the photodiode is varied by variably applying a back bias voltage to a semiconductor substrate without using the color filter.

[**0022**] Another object of the present invention is to provide a CMOS image sensor and a method for fabricating the same that can minimize the influence of a back bias voltage on a device on an outer side of the photodiode.

[**0023**] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[**0024**] To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a complementary metal oxide semiconductor (CMOS) image sensor including a first conductive semiconductor substrate having a first region for forming a photodiode and a second region for forming transistors and having a back bias voltage for varying a width of a depletion area in the first region applied thereon, a plurality of transistors formed in the second region of the semiconductor substrate, a photodiode formed in the first region of the semiconductor substrate, a second conductive buried layer formed in the second region of the semiconductor substrate, so as to prevent the back bias voltage from influencing the transistors, and a first isolating barrier formed within the semiconductor substrate, so as to surround a side portion of the second region.

[**0025**] Herein, the buried layer is formed of one of a U-shaped form and a horizontal linear form.

[**0026**] The U-shaped buried layer includes a first buried layer being formed horizontally, and a second buried layer formed between both side ends of the first buried layer and the isolating barrier.

[**0027**] The CMOS image sensor further includes a second isolating barrier formed within the semiconductor substrate, so as to surround a side portion of the first region.

[**0028**] The first isolating barrier of the side portion in the second region is formed of a conductive layer, and the second isolating barrier of the side portion in the first region is formed of an insulating layer.

[**0029**] Also, the first isolating barrier and the second isolating barrier are both formed of an insulating layer.

[**0030**] In another aspect of the present invention, a method for fabricating a complementary metal oxide semiconductor (CMOS) image sensor includes preparing a first conductive semiconductor substrate having a first region for forming a photodiode and a second region for forming transistors defined thereon, forming a first buried layer of a second conductive type formed to have a predetermined depth in the second region of the semiconductor substrate, forming a first trench in a region of the semiconductor substrate corresponding to an area surrounding the second region, and forming a second trench in a region of the semiconductor substrate corresponding to an area surrounding the first region, forming a second buried layer on the semiconductor substrate between the first trench and the first buried layer, forming an isolating barrier on the first trench and the second trench, and forming a photodiode in the first region of the semiconductor substrate, and forming a transistor in the second region of the semiconductor substrate.

[0031] Herein, the method for fabricating the CMOS image sensor further includes forming an interlayer dielectric on the semiconductor substrate including the transistor, forming a planarization layer on the interlayer dielectric, and forming a micro lens on the planarization layer, so as to be located on a horizontal line of the photodiode.

[0032] In a further aspect of the present invention, a method for fabricating a complementary metal oxide semiconductor (CMOS) image sensor includes preparing a first conductive semiconductor substrate having a first region for forming a photodiode and a second region for forming transistors defined thereon, forming a buried layer of a second conductive type formed to have a predetermined depth in the second region of the semiconductor substrate, forming a trench in a region of the semiconductor substrate corresponding to an area surrounding the second region, forming an isolating barrier on the trench, and forming a photodiode in the first region of the semiconductor substrate, and forming a transistor in the second region of the semiconductor substrate.

[0033] Therefore, by applying the back bias voltage to the semiconductor substrate, the width of the depletion area of the photodiode can be varied without having the back bias voltage influence the transistor.

[0034] It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0035] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiments of the invention and together with the description serve to explain the principle of the invention. In the drawings:

[0036] FIG. **1** illustrates a schematic view of an equivalent circuit of a unit pixel in a general CMOS image sensor;

[0037] FIG. **2** illustrates a cross-sectional view of a related art CMOS image sensor;

[0038] FIG. **3** illustrates a cross-sectional view of a CMOS image sensor according to a first embodiment of the present invention;

[0039] FIG. **4** illustrates a cross-sectional view of a CMOS image sensor according to a second embodiment of the present invention;

[0040] FIG. **5** illustrates a cross-sectional view of a CMOS image sensor according to a third embodiment of the present invention;

[0041] FIGS. **6**A to **6**E illustrate cross-sectional views showing the process steps of fabricating the CMOS image sensor of FIG. **4**; and

[0042] FIGS. **7**A and **7**B illustrate cross-sectional views showing the process steps of fabricating the CMOS image sensor of FIG. **5**.

DETAILED DESCRIPTION OF THE INVENTION

[0043] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0044] The complementary metal oxide semiconductor (CMOS) image sensor according to the present invention does not use any of the structures, such as the color filter layer, the micro prism, and the multiple slits. Instead, by varying the width of the depletion area of the photodiode by a variation of the back bias voltage (Vb) of the semiconductor device, the CMOS image sensor according to the present invention can sense the color sensitivity of the red, green, and blue color light rays, and the back bias voltage (Vb) does not influence other parts of the device apart from the photodiode.

[0045] Accordingly, a CMOS image sensor and a method for fabricating the same that can sense the color sensitivity of red, green, and blue light rays by varying the width of the depletion area of the photodiode through a variation in the back bias voltage (Vb) of the semiconductor device, without using any of the structures such as color filter layer, the micro prism, and the multiple slits, has been disclosed earlier (see Our Ref. No.: OPP-GZ-2004-0002-US-00).

[0046] The above-mentioned CMOS image sensor and the method for fabricating the same will now be described.

[0047] FIG. **3** illustrates a cross-sectional view of a CMOS image sensor according to a first embodiment of the present invention, which is disclosed in Our Ref. No.: OPP-GZ-2004-0002-US-00.

[0048] Referring to FIG. **3**, a p-type epitaxial layer **11** is formed on a semiconductor substrate **10**, such as a (p+)-type silicon substrate. An isolating barrier **13** is formed between a first region for forming a photodiode and a second region for forming transistors of the p-type epitaxial layer **11**. An (n−)-type diffusion area **15** for the photodiode (PD) is formed in the first region of the p-type epitaxial layer **11**. A source/drain (S/D) area and a gate electrode (G) for the transistor (TR) are formed in the second region of the p-type epitaxial layer **11**. A transparent interlayer dielectric **17** is formed on the photodiode (PD) and the transistor (TR). A planarization layer **19** is formed on the interlayer dielectric **17**. And, a micro lens **21** is formed on the planarization layer **19**, so as to be formed on the perpendicular line of the photodiode (PD).

[0049] Herein, the transistor (TR) includes an optical electric charge transmitter transmitting optical electric charge generated from the photodiode (PD), and an optical color sensitivity calculating unit sensing optical colors of red, green, and blue from the light ray irradiated to the photodiode. In the present invention, only two transistors are aligned on the substrate **10** for simplicity, however, it is obvious to a person skilled in the art that a plurality of transistors is aligned on the substrate.

[0050] In the above-described CMOS image sensor according to the first embodiment of the present invention, by varying and applying a back bias voltage (Vb) to a rear surface of the semiconductor substrate **10**, the depletion area of the photodiode (PD) is varied, and by using such variation, the optical color sensitivity of red, green, and blue including in the light ray irradiated on the photodiode can be sensed.

[0051] However, the back bias voltage can also be applied to the transistor (TR) forming the optical electric charge transmitter and the optical color sensitivity calculator, thereby changing the electrical characteristics of the transistor (i.e., threshold voltage, etc.). As a result, the optical color sensitivity of red, green, and blue cannot be accurately sensed. Therefore, the back bias voltage should be controlled, so that the back bias voltage does not influence devices (or transistors) other than the photodiode. The second and third embodiments of the present invention have been devised so that the back bias voltage does not influence devices (or transistors) other than the photodiode.

[0052] FIG. **4** illustrates a cross-sectional view of a CMOS image sensor according to a second embodiment of the present invention.

[0053] Referring to FIG. **4**, in the CMOS image sensor according to the present invention, a p-type epitaxial layer **11** is formed on a semiconductor substrate **10**, such as a polycrystalline silicon substrate of a first conductive type (e.g., (p−)-type). And, a low concentration buried layer **30** of a second conductive type (e.g., (n−)-type) is formed to have a U-shaped form of a predetermined depth in the second region of the p-type epitaxial layer **11**. The U-shaped (n−)-type buried layer **30** includes a horizontally formed first buried layer **31** and a second buried layer **33** formed perpendicularly formed at both ends of the first buried layer **31** and connected to the first buried layer **31**.

[0054] Also, a first trench **41** is formed to surround the side portion of the first region for forming the photodiode in the p-type epitaxial layer **11**. And, a second trench **43** having the same depth as the first trench **41** is formed to surround the side portion of the second region for forming the transistors in the p-type epitaxial layer **11**. At this point, the second trench **43** is formed above the second buried layer **33**. An isolating barrier **45** formed of an insulating layer is formed within the first trench **41**, and a conductive layer **47** (e.g., a polycrystalline silicon layer or a metal layer) is formed within the second trench **43**.

[0055] Additionally, an (n−)-type diffusion area **49** for the photodiode (PD) is formed in the first region of the p-type epitaxial layer **11**. A gate electrode (G) and a gate insulating layer (GI) of the transistor (TR) are formed on the p-type epitaxial layer **11** in the second region. And, a source/drain (S/D) area is formed at both sides of the gate electrode (G) of the p-type epitaxial layer **11** by an n-type impurity injection. Herein, the (n−)-type diffusion area **49** for the photodiode (PD) is formed to have depth smaller than that of the first buried layer **33**.

[0056] Furthermore, a transparent interlayer dielectric **51** is formed on the entire surface of the p-type epitaxial layer **11** including the gate electrode (G). Then, a planarization layer **53** is formed on the interlayer dielectric **51**, and a micro lens **21** is formed on the planarization layer **53**, so as to be formed on the perpendicular line of the (n−)-type diffusion area **49**. Herein, the interlayer dielectric **51** is formed to have a single layer, however, the interlayer dielectric **51** can also be formed of a transparent multi-layer. Also, also contact holes or metal wires of the transistor are omitted in the drawings, it is obvious to a person skilled in the art that the contact holes or the metal wires actually exist.

[0057] In the above-described CMOS image sensor according to the second embodiment of the present invention, the back bias voltage (Vb) is applied to the rear surface of the semiconductor substrate **10**. The back bias voltage (Vb) applied to the rear surface of the semiconductor substrate **10** passes through the p-type epitaxial layer **11**, so as to be applied to the (n−)-type diffusion area **49**. Accordingly, when the back bias voltage is varied, the width of the depletion area (not shown) in the (n−)-type diffusion area **49** is also varied. At this point, the buried layer **30** isolates the transistor, thereby minimizing the electrical influence of the back bias voltage (Vb) to the source/drain (S/D) area of the transistor.

[0058] Therefore, the CMOS image sensor according to the second embodiment of the present invention can prevent the change in the characteristics of devices such as the transistors including the optical electric charge transmitter, the optical color sensitivity calculator, and so on, which are formed on an outer side of the first region, and can also sense the optical color sensitivity of red, green, and blue included in the light rays irradiated to the (n−)-type diffusion area **49**. Herein, the method of sensing the optical color sensitivity has very little relation with the present invention, and a detailed description of the same will, therefore, be omitted.

[0059] FIG. **5** illustrates a cross-sectional view of a CMOS image sensor according to a third embodiment of the present invention.

[0060] Referring to FIG. **5**, in the CMOS image sensor according to the present invention, a p-type epitaxial layer **11** is formed on a semiconductor substrate **10**, such as a polycrystalline silicon substrate of a first conductive type (e.g., (p−)-type). And, a buried layer **30** of a second conductive type (e.g., (n−)-type) is horizontally formed to have a predetermined depth in the second region for forming the transistors of the p-type epitaxial layer **11**. A trench **83** is formed to surround the side portion of the second region in the p-type epitaxial layer **11**. And, an isolating barrier **85** formed of an insulating layer is formed inside the trench **83**. Herein, the trench **83** is formed to contact both sides of the (n−)-type buried layer **70**.

[0061] Additionally, an (n−)-type diffusion area **89** for the photodiode (PD) is formed in the first region for forming the photodiode of the p-type epitaxial layer **11**. A gate electrode (G) and a gate insulating layer (GI) are formed on the p-type epitaxial layer **11** in the second region. And, a source/drain (S/D) area for the transistor is formed at both sides of the gate electrode (G) of the p-type epitaxial layer **11**. Herein, the (n−)-type diffusion area **89** is formed to have depth smaller than that of the (n−)-type buried layer **70**.

[0062] Furthermore, a transparent interlayer dielectric **51** is formed on the entire surface of the semiconductor substrate **10** including the gate electrode (G). Then, a planarization layer **53** is formed on the interlayer dielectric **51**, and a micro lens **21** is formed on the planarization layer **53**, so as to be formed on the perpendicular line of the (n−)-type diffusion area **49**.

[0063] In the above-described CMOS image sensor according to the third embodiment of the present invention, the back bias voltage (Vb) is applied to the rear surface of the semiconductor substrate **10**. The back bias voltage (Vb) applied to the rear surface of the semiconductor substrate **10** passes through the p-type epitaxial layer **11**, so as to be applied to the (n−)-type diffusion area **89**. Accordingly,

when the back bias voltage is varied, the width of the depletion area (not shown) in the (n−)-type diffusion area **89** is also varied. At this point, the buried layer **70** and the isolating barrier **85** isolate the transistor, thereby minimizing the electrical influence of the back bias voltage (Vb) to the source/drain (S/D) area of the transistor.

[**0064**] Therefore, the CMOS image sensor according to the third embodiment of the present invention can prevent the change in the characteristics of devices such as the transistors including the optical electric charge transmitter, the optical color sensitivity calculator, and so on, which are formed on an outer side of the first region, and can also sense the optical color sensitivity of red, green, and blue included in the light rays irradiated to the (n−)-type diffusion area **89**. Herein, the method of sensing the optical color sensitivity has very little relation with the present invention, and a detailed description of the same will, therefore, be omitted.

[**0065**] Also, in the CMOS image sensor according to the third embodiment of the present invention, one trench is aligned between the first region for forming the photodiode and the second region for forming the transistors. Therefore, the surface area of the unit cell of the CMOS image sensor according to the third embodiment of the present invention can be reduced as compared to the surface area of the CMOS image sensor according to the second embodiment of the present invention, wherein two trenches are aligned between the first region and the second region.

[**0066**] The methods for fabricating the CMOS image sensors according to the second and third embodiment of the present invention will now be described in detail.

[**0067**] FIGS. **6**A to **6**E illustrate cross-sectional views showing the process steps of fabricating the CMOS image sensor of FIG. **4**.

[**0068**] In the method for fabricating the CMOS image sensor according to the second embodiment of the present invention, the p-type epitaxial layer **11** is grown on the semiconductor layer **10** of the first conductive (or p-type), as shown in FIG. **6**A. Subsequently, a sacrifice layer **12** having a multi-layered structure of a pad oxide layer **12***a* and a pad nitride layer **12***b* is formed on the p-type epitaxial layer **11**. Herein, the pad nitride layer **12***b* acts as a hard mask layer in a shallow trench isolation (STI) process that will follow and also acts as an etch-stop layer in a chemical mechanical polishing (CMP) process.

[**0069**] Thereafter, a first photosensitive layer **14***a* is deposited on the sacrifice layer **12**, which is then patterned through an exposure and development process, so as to open the second region. Then, the first photosensitive layer **14***a* is used as a mask to ion-inject n-type impurities to the p-type epitaxial layer **11** by using a high energy of about 1 MeV, thereby forming a first buried layer **31** of an n-type having a predetermined depth in the second region of the p-type epitaxial layer **11**. Herein, the first buried layer **31** is extendedly formed in a horizontal direction. At this point, the first buried layer **31** can also be formed by injecting n-type impurity ions at a high energy of about 1 MeV without using the photosensitive mask. Then, the p-type impurities can be counter doped, so as to recover the first region.

[**0070**] Referring to FIG. **6**B, the first photosensitive layer **14***a* is removed, and a second photosensitive layer **14***b* is deposited on the entire surface. Then, after an exposure and development process, the second photosensitive layer **14***b* is patterned so as to expose the sacrifice layer **12** on the side portion of the first region and the side portion of the second region.

[**0071**] Subsequently, the second photosensitive layer **14***b* is used as a mask to selectively remove the sacrifice layer **12** and the p-type epitaxial layer **11**, so as to form a first trench **43** surrounding the side portion of the second region in the p-type epitaxial layer **11**, and to form a second trench **41** surrounding the side portion of the first region in the p-type epitaxial layer **11**. At this point, each of the first and second trenches **43** and **41** is formed to have a depth smaller than that of the first buried layer **31**.

[**0072**] Referring to FIG. **6**C, the second photosensitive layer **14***b* is removed, and a third photosensitive layer **14***c* is deposited on the entire surface. The third photosensitive layer **14***c* is then patterned through an exposure and development process, so as to expose the first trench **43** area. Thereafter, n-type impurity ions are ion-injected to the p-type epitaxial layer **11** at the lower portion of the first trench **43**, thereby forming a second buried layer **33** between the first buried layer **31** and the first trench **43**. At this point, the first and second buried layers **31** and **33** and the first trench **43** isolate the second region.

[**0073**] As shown in FIG. **6**D, a conductive layer **47**, such as a polycrystalline silicon layer or a metal layer, is deposited to fill the first trench **43**, which is then planarized through a chemical mechanical polishing (CMP) process. Also, an insulating layer **45** such as an oxide layer is thickly deposited so as to fill the second trench **41**, which is then planarized through a chemical mechanical polishing (CMP) process. Then, an isolating barrier is formed by using the same method.

[**0074**] At this point, an insulating layer such as an oxide layer is thickly formed on the sacrifice layer so as to fill the first and second trenches **41** and **43**. By planarizing the insulating layer through the chemical mechanical polishing (CMP) process, an isolating barrier **45** and **47** can be formed in each of the first and second trenches **41** and **43**. Meanwhile, the second buried layer **33** can also be formed after forming the isolating barriers **45** and **47**.

[**0075**] Referring to FIG. **6**E, the sacrifice layer is removed, and by using an ordinary method, the (n−)-type diffusion area **49** for the photodiode is formed in the first region of the p-type epitaxial layer **11**. The gate electrode (G) is formed on the gate insulating layer (GI), the gate insulating layer (GI) being formed on the p-type epitaxial layer **11**. And, the source/drain (S/D) area is formed by ion-injecting impurities in the p-type epitaxial layer **11** at both sides of the gate electrode (G). At this point, the (n−)-type diffusion area **49** and the buried layer **30** should be sufficiently spaced apart from one another so that the (n−)-type diffusion area **49** and the buried layer **30** do not come into contact.

[**0076**] Thereafter, the interlayer dielectric **51** is formed on the entire surface of the p-type epitaxial layer **11** including the gate electrode (G) and the (n−)-type diffusion area **49**. Then, the planarization layer **53** is formed on the interlayer dielectric **51**. And, the micro lens **61** is formed on the planarization layer **53**, so as to be formed on the perpendicular line of the (n−)-type diffusion area **49**, thereby

completing the method for fabricating the CMOS image sensor according to the second embodiment of the present invention.

[0077] FIGS. **7**A and **7**B illustrate cross-sectional views showing the process steps of fabricating the CMOS image sensor of FIG. **5**.

[0078] In the method for fabricating the CMOS image sensor according to the second embodiment of the present invention, the p-type epitaxial layer **11** is grown on the p-type semiconductor layer **10**, as shown in FIG. **7**A. Subsequently, a sacrifice layer **12** having a multi-layered structure of a pad oxide layer **12***a* and a pad nitride layer **12***b* is formed on the p-type epitaxial layer **11**. Herein, the pad nitride layer **12***b* acts as a hard mask layer in a shallow trench isolation (STI) process that will follow and also acts as an etch stop layer in a chemical mechanical polishing (CMP) process.

[0079] Thereafter, a first photosensitive layer **14***a* is deposited on the sacrifice layer **12**, which is then patterned through an exposure and development process, so as to open the second region. Then, the first photosensitive layer **14***a* is used as a mask to ion-inject n-type impurities to the p-type epitaxial layer **11** by using a high energy of about 1 MeV, thereby forming an n-type buried layer **70** having a predetermined depth in the second region of the p-type epitaxial layer **11**. Herein, the buried layer **70** is extendedly formed in a horizontal direction. At this point, the buried layer **70** can also be formed by injecting n-type impurity ions at a high energy of about 1 MeV without using the photosensitive mask. Then, the p-type impurities can be counter doped, so as to recover the first region.

[0080] Referring to FIG. **7**B, the isolating barrier **85** formed of an insulating layer such as an oxide layer is formed by using the shallow trench isolation (STI) process. More specifically, the first photosensitive layer **14***a* is removed, and a second photosensitive layer **14***b* is deposited on the entire surface. Then, after an exposure and development process, the second photosensitive layer **14***b* is patterned so as to expose the sacrifice layer **12** on the side portion of the second region.

[0081] Subsequently, the second photosensitive layer **14***b* is used as a mask to selectively remove the sacrifice layer **12** and the p-type epitaxial layer **11**, so as to form a trench **83** surrounding the side portion of the second region in a portion of the p-type epitaxial layer **11**. At this point, the trench **83** is formed at a depth exposing each ends of the smaller than that of (n−)-type buried layer **70**. Thereafter, an insulating layer such as an oxide layer is thickly deposited in the inside of the trench **83** and on the sacrifice layer **12** for gap-filling the trench **83**. Then, by planarizing the insulating layer through the chemical mechanical polishing (CMP) process, the isolating barrier **85** is formed on the trench **83**.

[0082] Therefore, since the trench is formed only in the area surrounding the second region in the method for fabricating the CMOS image sensor according to the third embodiment of the present invention, the degree of integration can be enhanced as compared to that of the second embodiment. And, since the process of forming the second buried layer is removed, the fabrication process is more simplified.

[0083] Referring to FIG. **7**C, by using an ordinary method, the (n−)-type diffusion area **89** is formed in the first region of the p-type epitaxial layer **11**. The gate electrode (G) is formed on the gate insulating layer (GI), the gate insulating layer (GI) being formed on the p-type epitaxial layer **11**. And, the source/drain (S/D) area is formed in the p-type epitaxial layer **11** at both sides of the gate electrode (G).

[0084] Subsequently, the interlayer dielectric **51** is formed on the entire surface of the p-type epitaxial layer **11** including the gate electrode (G) and the (n−)-type diffusion area **89**. Then, the planarization layer **53** is formed on the interlayer dielectric **51**. And, the micro lens **61** is formed on the planarization layer **53**, so as to be formed on the perpendicular line of the (n−)-type diffusion area **89**, thereby completing the method for fabricating the CMOS image sensor according to the third embodiment of the present invention.

[0085] As described above, the CMOS image sensor and the method for fabricating the same according to the present invention has the following advantages.

[0086] A buried layer of an (n−)-type used for isolation is formed on a lower portion of a second region for forming transistors of a semiconductor substrate, an isolating barrier is formed on a side portion of a first region for forming a photodiode and a second region for forming transistors of the semiconductor substrate, and a photodiode and a transistor are respectively formed in the first and second regions of the semiconductor substrate. Therefore, without using a color filter layer, a back bias voltage is applied to the semiconductor layer, so as to vary the width of a depletion area of the photodiode, thereby sensing the optical color sensitivity of red, green, and blue light rays irradiated on the photodiode. Furthermore, since the buried layer and the isolating barrier isolate the transistor, the back bias voltage cannot influence the transistor, thereby allowing a more accurate sensing operation to be carried out.

[0087] It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the inventions. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

1. A complementary metal oxide semiconductor (CMOS) image sensor, comprising: a first conductive semiconductor substrate having a first region for forming a photodiode and a second region for forming transistors and having a back bias voltage for varying a width of a depletion area in the first region applied thereon;

a plurality of transistors formed in the second region of the semiconductor substrate; a photodiode formed in the first region of the semiconductor substrate;

a second conductive buried layer formed in the second region of the semiconductor substrate, so as to prevent the back bias voltage from influencing the transistors; and

a first isolating barrier formed within the semiconductor substrate, so as to surround a side portion of the second region.

2. The CMOS image sensor according to claim 1, wherein the buried layer is formed of one of a U-shaped form and a horizontal linear form.

3. The CMOS image sensor according to claim 2, wherein the U-shaped buried layer comprises a first buried layer being formed horizontally, and a second buried layer formed between both side ends of the first buried layer and the isolating barrier.

4. The CMOS image sensor according to claim 1, further comprising a second isolating barrier formed within the semiconductor substrate, so as to surround a side portion of the first region.

5. The CMOS image sensor according to claim 4, wherein the first isolating barrier of the side portion in the second region is formed of a conductive layer, and the second isolating barrier of the side portion in the first region is formed of an insulating layer.

6. The CMOS image sensor according to claim 4, wherein the first isolating barrier and the second isolating barrier are both formed of an insulating layer.

7. The CMOS image sensor according to claim 1, wherein the semiconductor layer comprises a first conductive epitaxial layer.

8. The CMOS image sensor according to claim 7, wherein the photodiode comprises the first conductive epitaxial layer and a second conductive diffusion layer formed on a surface of the first conductive epitaxial layer.

9. The CMOS image sensor according to claim 8, wherein the second conductive diffusion layer and the buried layer are isolated from one another.

10-19. (canceled)

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