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- (71) Applicant: X-CELEPRINT LIMITED [IE/IE]; Lee Maltings, Dyke Parade, Cork (IE).
- (72) Inventors: BOWER, Christopher; c/o X-Celeprint Limited, Lee Maltings, Dyke Parade, Cork (IE). MEITL, Matthew; c/o X-Celeprint Limited, Lee Maltings, Dyke Parade, Cork (IE).
- (74) Agent: GRAHAM WATT & CO LLP; St Botolph's House, 7-9 St Botolph's Road, Sevenoaks Kent TN13 3AJ (GB).
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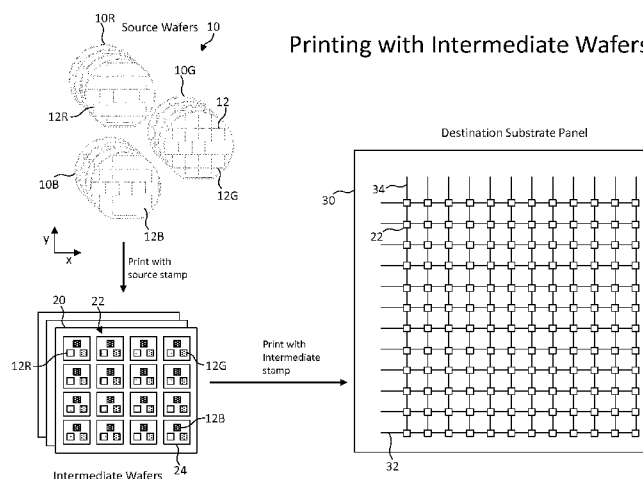


FIG. 2

(57) Abstract: A method of making a micro-transfer printed system includes providing a source wafer (10) having a plurality of micro-transfer printable source devices (12 arranged at a source spatial density; providing an intermediate wafer (20) having a plurality of micro-transfer printable intermediate supports (24) arranged at an intermediate spatial density less than or equal to the source spatial density; providing a destination substrate (30); micro-transfer printing the source devices from the source wafer to the intermediate supports of the intermediate wafer with a source stamp having a plurality of posts at a source transfer density to make an intermediate device (22) on each intermediate support; and micro-transfer printing the intermediate devices from the intermediate wafer to the destination substrate at a destination spatial density less than the source spatial density with an intermediate stamp having a plurality of posts at an intermediate transfer density less than the source transfer density.



**EFFICIENTLY MICRO-TRANSFER PRINTING MICRO-SCALE DEVICES ONTO LARGE-FORMAT
SUBSTRATES**

PRIORITY APPLICATION

5 This application claims priority to and benefit of U.S. Patent Application No. 62/300,040, filed February 25, 2016, entitled Efficiently Micro-Transfer Printing Micro-Scale Devices onto Large-Format Substrates, the content of which is hereby incorporated by reference.

CROSS REFERENCE TO RELATED APPLICATION

10 Reference is made to U.S. Patent Application Serial No. 14/822,868, entitled Compound Micro-Assembly Strategies and Devices by Bower et al., the disclosure of which is incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

15 The present invention relates to structures and methods for micro-transfer printing micro-scale devices from source wafers to large-format substrates.

BACKGROUND OF THE INVENTION

20 Substrates with electronically active components such as transistors or light-emitting diodes distributed over the extent of the substrate can be used in a variety of electronic systems, for example, flat-panel imaging devices such as flat-panel liquid crystal or organic light emitting diode (OLED) display devices and in flat-panel solar cells. A variety of methods may be used to distribute electronically active circuits over substrates, including forming the electronically active circuits on a substrate and forming the components on separate substrates
25 and placing them on a substrate. In the latter case, a variety of assembly technologies for device packaging may be used.

30 Electronically active components are typically formed on a substrate by sputtering a layer of inorganic semiconductor material or by spin-coating organic material over the entire substrate. Inorganic semiconductor materials can be processed to improve their electronic characteristics. For example, amorphous silicon can be treated to form low-temperature or high-temperature poly-crystalline silicon. In other process methods, microcrystalline semiconductor layers can be formed by using an underlying seeding layer. These methods

typically improve the electron mobility of the semiconductor layer. The substrate and layer of semiconductor material can be photo-lithographically processed to define electronically active components, such as transistors. Such transistors are known as thin-film transistors (TFTs) since they are formed in a thin layer of semiconductor material, typically silicon. Transistors may also
5 be formed in thin layers of organic materials. In these devices, the substrate is often made of glass, for example Corning Eagle® or Jade® glass designed for display applications.

The above techniques have some limitations. Despite processing methods used to improve the performance of thin-film transistors, such transistors may provide performance that is lower than the performance of other integrated circuits formed in mono-crystalline
10 semiconductor material. Semiconductor material and active components can be provided only on portions of the substrate, leading to wasted material and processing costs. The choice of substrate materials can also be limited by the processing steps necessary to process the semiconductor material and the photo-lithographic steps used to pattern the active components. For example, plastic substrates have a limited chemical and heat tolerance and do
15 not readily survive photo-lithographic processing. Furthermore, the manufacturing equipment used to process large substrates with thin-film circuitry is relatively expensive. Other substrate materials that may be used include quartz, for example, for integrated circuits using silicon-on-insulator structures as described in U.S. Patent Application 2010/0289115 and U.S. Patent Application 2010/0123134. However, such substrate materials can be more expensive or
20 difficult to process.

Other methods used for distributing electronically functional components over a substrate in the circuit board assembly industry include, for example, pick-and-place technologies for integrated circuits provided in a variety of packages, for example, pin-grid arrays, ball-grid arrays, and flip-chips. However, these techniques may be limited in the size of
25 the integrated circuits that can be placed.

In further manufacturing techniques, a mono-crystalline semiconductor wafer is employed as the substrate. While this approach can provide substrates with the same performance as integrated circuits, the size of such substrates may be limited, for example, to a 12-inch diameter circle, and the wafers are relatively expensive compared to other substrate
30 materials such as glass, polymer, or quartz.

In yet another approach, thin layers of semiconductor are bonded to a substrate and then processed. Such a method is known as semiconductor-on-glass or silicon-on-glass (SOG)

and is described, for example, in U.S. Patent No. 7,605,053, issued Oct. 20, 2009. If the semiconductor material is crystalline, high-performance thin-film circuits can be obtained. However, the bonding technique and the processing equipment for the substrates to form the thin-film active components on large substrates can be relatively expensive.

5 Publication No. 11-142878 of the Patent Abstracts of Japan entitled Formation of Display Transistor Array Panel describes etching a substrate to remove it from a thin-film transistor array on which the TFT array was formed. TFT circuits formed on a first substrate can be transferred to a second substrate by adhering the first substrate and the TFTs to the surface of the second substrate and then etching away the first substrate, leaving the TFTs bonded to
10 the second substrate. This method may require etching a significant quantity of material, and may risk damaging the exposed TFT array.

 Other methods of locating material on a substrate are described in U.S. Pat. No. 7,127,810. In this approach, a first substrate carries a thin-film object to be transferred to a second substrate. An adhesive is applied to the object to be transferred or to the second
15 substrate in the desired location of the object. The substrates are aligned and brought into contact. A laser beam irradiates the object to abrade the transferring thin film so that the transferred thin-film adheres to the second substrate. The first and second substrates are separated by peeling the film in the abraded areas from the first substrate and transferring it to
20 the second substrate. In one embodiment, a plurality of objects is selectively transferred by employing a plurality of laser beams to abrade selected area. Objects to be transferred can include thin-film circuits.

 U.S. Pat. No. 6,969,624 describes a method of transferring a device from a first substrate onto a holding substrate by selectively irradiating an interface with an energy beam. The interface is located between a device for transfer and the first substrate and includes a material
25 that generates ablation upon irradiation, thereby releasing the device from the substrate. For example, a light-emitting device (LED) is made of a nitride semiconductor on a sapphire substrate. The energy beam is directed to the interface between the sapphire substrate and the nitride semiconductor releasing the LED and allowing the LED to adhere to a holding substrate coated with an adhesive. The adhesive is then cured. These methods, however, may require the
30 patterned deposition of adhesive on the object(s) or on the second substrate. Moreover, the laser beam that irradiates the object may need to be shaped to match the shape of the object,

and the laser abrasion can damage the object to be transferred. Furthermore, the adhesive cure takes time, which may reduce the throughput of the manufacturing system.

Another method for transferring active components from one substrate to another is described in AMOLED Displays using Transfer-Printed Integrated Circuits published in the
5 Proceedings of the 2009 Society for Information Display International Symposium Jun. 2-5, 2009, in San Antonio Tex., US, vol. 40, Book 2, ISSN 0009-0966X, paper 63.2 p. 947. In this approach, small integrated circuits are formed over a buried oxide layer on the process side of a crystalline wafer. The small integrated circuits, or chiplets, are released from the wafer by etching the buried oxide layer formed beneath the circuits. A PDMS stamp is pressed against the wafer and
10 the process side of the chiplets is adhered to the stamp. The chiplets are pressed against a destination substrate or backplane coated with an adhesive and thereby adhered to the destination substrate. The adhesive is subsequently cured. In another example, U.S. Patent No. 8,722,458 entitled Optical Systems Fabricated by Printing-Based Assembly teaches transferring light-emitting, light-sensing, or light-collecting semiconductor elements from a wafer substrate
15 to a destination substrate or backplane.

In such methods it is generally necessary to electrically connect the small integrated circuits or chiplets to electrically conductive elements such as backplane contact pads on the destination substrate. By applying electrical signals to conductors on the destination substrate the small integrated circuits are energized and made operational. The electrical connections
20 between the small integrated circuits and the backplane contact pads are typically made by photolithographic processes in which a metal is evaporated or sputtered onto the small integrated circuits and the destination substrate to form a metal layer, the metal layer is coated with a photoresist that is exposed to a circuit connection pattern, and the metal layer and photoresist are developed by etching and washing to form the patterned electrical connections
25 between the small integrated circuits and the connection pads on the destination substrate. Additional layers, such as interlayer dielectric insulators can also be required. This process is expensive and requires a number of manufacturing steps. Moreover, the topographical structure of the small integrated circuits over the destination substrate renders the electrical connections problematic. For example, it can be difficult to form a continuous conductor from
30 the destination substrate to the small integrated circuit because of the differences in height over the surface between the small integrated circuits and the destination substrate. Moreover,

many transfer printing steps can be necessary to transfer the densely packed chiplets on the source wafer to the more sparsely packed chiplets on the destination substrate.

There is a need, therefore, for structures and methods that enable the disposition and electrical interconnection of small integrated circuits, such as micro transfer printed chiplets or light-emitting diodes, on large-format destination substrates.

SUMMARY OF THE INVENTION

In accordance with methods of the present invention, a source wafer having a plurality of micro-transfer printable source devices arranged in or on the source wafer at a source spatial density is provided. An intermediate wafer having a plurality of micro-transfer printable intermediate supports arranged in or on the intermediate wafer at an intermediate spatial density less than or equal to the source spatial density is also provided, as is a destination substrate that can have patterned electrical conductors. The source devices are micro-transfer printed from the source wafer to the intermediate supports of the intermediate wafer with a source stamp having a plurality of stamp posts at a source transfer density to make an intermediate device on each intermediate support. The intermediate devices are micro-transfer printed from the intermediate wafer to the destination substrate at a destination spatial density less than the source spatial density with an intermediate stamp having a plurality of stamp posts at an intermediate transfer density less than the source transfer density. Source devices can be light-emitting diodes (LEDs) such as inorganic light-emitting diodes made in crystalline inorganic semiconductor materials.

Because the source wafers are typically more expensive and smaller than the destination substrate and the spatial density of the source devices on the source wafer is much greater than the spatial density of the transferred source devices on the destination wafer, micro-transfer printing stamps transfer sparse arrays of source devices from the source wafer to the destination substrate. Because the arrays of source devices on the stamp are relatively sparse, a relatively large number of transfer steps with relatively fewer source devices is required. Since many transfer steps with fewer source devices takes a longer time than fewer transfer steps with more source devices, this process can take a longer time than is desirable.

Thus, according to methods of the present invention, an intermediate wafer having a patterned array of micro-transfer printable intermediate supports is provided and populated with source devices from the source wafer using a spatially dense source stamp. The

intermediate wafer is larger than the source wafer. The size of source wafers is limited because the source devices are processed using photolithographic tools designed for semiconductor wafers and the tools have a limited size handling capability, for example handling 4-, 6-, 8-, or 12-inch wafers. In contrast, the intermediate wafer does not have to be a semiconductor substrate and can therefore be larger and have an alternative shape, such as a rectangular shape.

Once the larger intermediate wafer is populated at high density using the spatially dense source stamp, the source devices are micro-transfer printed from the intermediate wafer to the destination substrate using a larger spatially sparse intermediate stamp. The destination substrate is larger than the intermediate substrate which is larger than the source wafer. Thus, the larger intermediate stamp can transfer more source devices from the intermediate substrate to the destination substrate with fewer stamping operations than the smaller source stamp.

In a further embodiment, a plurality of source wafers with different source devices are provided and a plurality of the different source devices are micro-transfer printed onto the intermediate wafer. For example, the source wafers can supply red, green, and blue LEDs so that each intermediate device includes one each of the red, green, and blue LEDs and forms a full-color pixel in a display. In another embodiment, a small integrated circuit (chiplet) controller is also micro-transfer printed onto the intermediate support to control other source devices, for example, an active-matrix controller can control a full-color pixel having red, green, and blue LEDs.

In another embodiment, the plurality of devices in an intermediate device are electrically connected with electrical connections on the intermediate support. Because the intermediate wafer is smaller than the destination substrate, it is easier to provide higher resolution electrical connections at lower cost on the intermediate wafer than on the destination substrate. Electrical connections can also be provided on the destination substrate at a lower resolution than on the intermediate wafer.

In alternative embodiments of the present invention, the source devices or the intermediate devices, or both, include connection posts or spikes electrically connected to elements of the source or intermediate devices. The connection posts can contact electrical connections or electrical contact pads when the devices are micro-transfer printed. This method avoids forming electrical connections using photolithography after micro-transfer printing.

A system for making a multi-component device includes a source wafer having a plurality of micro-transfer printable source devices arranged in or on the source wafer at a source spatial density; an intermediate wafer having a plurality of micro-transfer printable intermediate supports arranged in or on the intermediate wafer at an intermediate spatial
5 density less than or equal to the source spatial density; a destination substrate; a source stamp having a source transfer density; and an intermediate stamp having an intermediate transfer density less than the source transfer density. A micro-transfer printer for micro-transfer printing the source devices from the source wafer to the intermediate wafer at an intermediate spatial
10 density less than or equal to the source spatial density with a source stamp at a source transfer density to make an intermediate device on each intermediate support and a micro-transfer printer for micro-transfer printing the intermediate devices from the intermediate wafer to the destination substrate at a destination spatial density less than the source spatial density with an intermediate stamp at an intermediate transfer density less than the source transfer density are included.

15 Embodiments of the present invention enable the micro-transfer printing of spatially dense source devices from a relatively small source wafer to a spatially sparse arrangement of source devices, or intermediate devices including source devices, on a relatively large destination substrate with fewer printing steps, thereby reducing manufacturing time and cost.

In one aspect, the disclosed technology includes a method of making a micro-transfer
20 printed system, including: providing a source wafer having a plurality of micro-transfer printable source devices arranged in or on the source wafer at a source spatial density; providing an intermediate wafer having a plurality of micro-transfer printable intermediate supports arranged in or on the intermediate wafer at an intermediate spatial density less than or equal to the source spatial density; providing a destination substrate; micro-transfer printing the source
25 devices from the source wafer to the intermediate supports of the intermediate wafer with a source stamp having a plurality of stamp posts at a source transfer density to make an intermediate device on each intermediate support; and micro-transfer printing the intermediate devices from the intermediate wafer to the destination substrate at a destination spatial density less than the source spatial density with an intermediate stamp having a plurality of stamp posts
30 at an intermediate transfer density less than the source transfer density.

In certain embodiments, the method includes providing a plurality of source wafers, each source wafer having a plurality of micro-transfer printable source devices arranged on or in

the respective source wafers at a respective source spatial density, and micro-transfer printing the source devices from the plurality of source wafers to the intermediate supports of the intermediate wafer with one or more source stamps at the source transfer density so that each intermediate device has a plurality of source devices.

5 In certain embodiments, the source wafer is a first source wafer, the source devices are first source devices, the source stamp is a first source stamp, and the source spatial density is a first source spatial density and comprising providing a second source wafer having a plurality of micro-transfer printable second source devices arranged on or in the second source wafers at a second source spatial density, and micro-transfer printing the second source devices from the
10 second source wafer to the intermediate supports of the intermediate wafer with one or more second source stamps at the second source transfer density so that each intermediate device has a first source device and a second source device.

 In certain embodiments, the method includes forming intermediate electrical connections between the source devices on the intermediate support at an intermediate
15 resolution and forming destination electrical connections between the intermediate devices on the destination substrate at a destination resolution less than the intermediate resolution.

 In certain embodiments, the method includes forming intermediate electrical connections at an intermediate resolution of less than or equal to 10 microns, 5 microns, two microns or one micro and forming destination electrical connections at a destination resolution
20 of greater than or equal to 5 microns, 10 microns, 20 microns or 50 microns.

 In certain embodiments, the method includes providing the intermediate stamp with a larger extent over the intermediate wafer than the source stamp over the source wafer.

 In certain embodiments, the method includes providing the source wafer with a 12-inch diameter, an 8-inch diameter, a 6-inch diameter, or a 4-inch diameter and comprising providing
25 the intermediate wafer with a diameter, diagonal, or side of 8 inches, 12 inches, 16 inches, 20 inches, 24 inches, 32 inches, 40 inches, 48 inches, or 64 inches.

 In certain embodiments, the method includes providing a red source wafer having source devices that are red light-emitting diodes that can emit red light, providing a green source wafer having source devices that are green light-emitting diodes that can emit green
30 light, providing a blue source wafer having source devices that are blue light-emitting diodes that can emit blue light, and wherein each intermediate device includes a red, a green, and a blue light-emitting diode.

In certain embodiments, the method includes providing a chiplet source wafer having integrated circuit control chiplet source devices, and wherein each intermediate device includes an integrated circuit control chiplet.

5 In certain embodiments, the method includes one or more of providing the intermediate wafer with a larger extent than the source wafer, providing the destination substrate with a larger extent than the intermediate wafer, and providing the intermediate support with an extent that is greater than the extent of the source device.

10 In certain embodiments, the method includes one or more of providing the intermediate wafer with a spatial format matched to the source stamp or the intermediate stamp, providing the destination substrate with a spatial format matched to the intermediate stamp, and providing the intermediate wafer with a spatial format matched to the destination substrate.

In certain embodiments, the method includes providing the intermediate stamp with an extent larger than that of the source stamp.

15 In certain embodiments, the method includes providing the source stamp with a diameter, diagonal, or edge of less than or equal to 1 cm, 2 cm, 5 cm, 10 cm, 15 cm, or 20 cm and providing the intermediate stamp with a diameter, diagonal, or edge of greater than or equal to 5 cm, 10 cm, 15 cm, 20 cm, 40 cm, 50 cm, 75 cm, or 100 cm.

20 In certain embodiments, the method includes micro-transfer printing more source devices from the source wafer to the intermediate wafer with the source stamp in a single stamp operation than are transferred by micro-transfer printing intermediate devices from the intermediate wafer to the destination substrate with the intermediate stamp in a single stamp operation.

25 In certain embodiments, the method includes providing the source wafer with micro-transfer printable source devices having connection posts or providing the intermediate wafer with micro-transfer printable intermediate supports having connection posts.

In certain embodiments, the method includes providing destination electrical connections on the destination substrate and electrically connecting the intermediate devices to the electrical connections on the destination substrate with the connection posts.

30 In certain embodiments, the method includes providing intermediate electrical connections on the intermediate support and electrically connecting the source devices to the electrical connections on the intermediate support with the connection posts.

In certain embodiments, the method includes providing the source devices as light-emitting diodes or providing the destination substrate as a display substrate.

In another aspect, the disclosed technology includes a system for making a micro-transfer printed device, including: a source wafer having a plurality of micro-transfer printable source devices arranged in or on the source wafer at a source spatial density; an intermediate
5 wafer having a plurality of micro-transfer printable intermediate supports arranged in or on the intermediate wafer at an intermediate spatial density less than or equal to the source spatial density; a destination substrate; a source stamp having a source transfer density; an intermediate stamp having an intermediate transfer density less than the source transfer
10 density; a micro-transfer printer for micro-transfer printing the source devices from the source wafer to the intermediate supports of the intermediate wafer with a source stamp at a source transfer density to make an intermediate device on each intermediate support; and a micro-transfer printer for micro-transfer printing the intermediate devices from the intermediate
15 wafer to the destination substrate at a destination spatial density less than the source spatial density with an intermediate stamp at an intermediate transfer density less than the source transfer density.

In certain embodiments, the source devices are light-emitting diodes or the destination substrate is a display substrate.

20

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects, features, and advantages of the present disclosure will become more apparent and better understood by referring to the following description taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a flow chart illustrating a method of the present invention;

25

Fig. 2 is a schematic illustration of a source wafer, an intermediate wafer, a destination substrate, and a method of constructing a destination substrate with a sparse array of source devices according to an embodiment of the present invention;

Fig. 3 is a schematic illustration of a source wafer, a destination substrate, and a method of constructing a destination substrate with a sparse array of source devices;

30

Fig. 4 is a cross section of a source wafer and source device according to an embodiment of the present invention having micro-transfer printable LED components with connection posts;

Fig. 5 is a cross section of an intermediate wafer and intermediate device according to an embodiment of the present invention having micro-transfer printable full-color pixel components with connection posts;

5 Fig. 6 is a schematic illustration corresponding to Fig. 3 including exemplary descriptive material; and

Fig. 7 is a schematic illustration corresponding to Fig. 2 with additional exemplary information.

10 The features and advantages of the present disclosure will become more apparent from the detailed description set forth below when taken in conjunction with the drawings, in which like reference characters identify corresponding elements throughout. In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. The figures are not drawn to scale since the variation in size of various elements in the Figures is too great to permit depiction to scale.

15

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides structures and methods for efficiently micro-transfer printing source devices from a source wafer to a destination substrate. Referring to the flow chart of Fig. 1 and the schematic illustration of Fig. 2, in an embodiment of the present invention
20 a method of making a micro-transfer printed system or device includes providing a source wafer 10 in step 100. The source wafer 10 can be, for example, a semiconductor wafer or a compound semiconductor wafer. The source wafer 10 is provided in step 105 with a plurality of micro-transfer printable source devices 12 arranged in or on the source wafer 10 at a source spatial density. The source spatial density is the number of source devices 12 per unit area of the
25 source wafer 10. The source devices 12 can be formed using integrated circuit photolithographic processes and, in certain embodiment, the source devices 12 are or include electronic elements such as light-emitting diodes (LEDs). In certain embodiments the source devices 12 are or include electronic elements such as small integrated circuits such as chiplets including digital or analog logic circuits.

30 In step 110, an intermediate wafer 20 is provided. The intermediate wafer 20 can be glass, polymer, metal, ceramic, or a semiconductor wafer such as a silicon wafer. In step 115, a plurality of micro-transfer printable intermediate supports 24 are formed in the intermediate

wafer 20 at an intermediate spatial density that is less than or equal to the source spatial density. The intermediate spatial density is the number of intermediate substrates 24 per unit area of the intermediate wafer 20. The intermediate wafer 20 can be or include glass, polymer, quartz, metal, or semiconductor and can be any substrate on which the source devices 12 can be micro-transfer printed or interconnected on the micro-transfer printable intermediate supports 24. A destination substrate 30 is provided in step 120 and can have electrical conductors (e.g., row conductors 32 and column conductors 34 arranged in orthogonal arrays) formed in step 125. The destination substrate 30 can be, but is not necessarily, a display substrate 30 used in a flat-panel display (e.g., including glass, polymer, ceramic, or metal) and the row and column conductors 32, 34 can be metal wires or electrical conductors formed using photolithographic methods and tools.

Referring next to step 130, the source devices 12 are micro-transfer printed from the source wafer 10 to the intermediate supports 24 of the intermediate wafer 20 with a source stamp to make an intermediate device 22 on each intermediate support 24. The source stamp has a plurality of source stamp posts at a source transfer density defined as the number of effective source stamp posts per unit area of the source stamp. An effective source stamp post is a source stamp post that picks up a source device 12. The source transfer density can be less than or the same as the source spatial density. In certain embodiments, electrical conductors 28 (Fig. 5) are formed to electrically connect the source devices 12 (not shown in Fig. 1) on a respective intermediate support 24. In step 140, the intermediate devices 22 on the intermediate supports 24 of the intermediate wafer 20 are micro-transfer printed to the destination substrate 30 at a destination spatial density that is less than the source spatial density with an intermediate stamp. The intermediate stamp can have a plurality of intermediate stamp posts at an intermediate transfer density less than the source transfer density, the intermediate transfer density defined as the number of effective intermediate stamp posts per unit area of the intermediate stamp. An effective intermediate stamp post is an intermediate stamp post that picks up an intermediate device 22. The intermediate devices 22 can be electrically connected on the destination substrate 30 with electrical conductors (e.g., row conductors 32 and column conductors 34) using photolithographic methods and materials in step 145.

As also shown in Fig. 2, in a further embodiment of the present invention a plurality of source wafers 10 are provided. Each source wafer 10 has a plurality of micro-transfer printable

source devices 12 arranged in or on the respective source wafers 10 at a respective source spatial density. The source devices 12 from the plurality of source wafers 10 are micro-transfer printed to the intermediate wafer 20 with one or more source stamps at the respective source transfer density so that each intermediate device 22 has a plurality of source devices 12. For example, first and second source wafers 10 can be provided having respective first and second source devices 12 at respective first and second source spatial densities that are micro-transfer printed to the intermediate wafer 20 using respective first and second source stamps at respective first and second source transfer densities so that each intermediate device 22 has a first source device 12 and a second source device 12. The first and second source spatial densities can be the same, or different and the first and second source transfer densities can also be the same, or different. Additional source wafers and source stamps may be used. A source stamp may be used to pick up and print devices from multiple source wafers (i.e., in different print operations) such that a single stamp can be used to print multiple devices to the same intermediate support.

As shown in Fig. 2, the plurality of source wafers 10 can include a red source wafer 10R having source devices 12R that are red light-emitting diodes that can emit red light, a green source wafer 10G having source devices 12G that are green light-emitting diodes that can emit green light, and a blue source wafer 10B having source devices 12B that are blue light-emitting diodes that can emit blue light. Thus, each intermediate device 22 includes a red, a green, and a blue light-emitting diode on each respective intermediate support 24 and can be a full-color pixel in a display. In a further embodiment of the present invention, a chiplet source wafer 10 having integrated circuit control chiplet source devices 12 is provided so that each intermediate device 22 includes an integrated circuit control chiplet on the intermediate support 24. The integrated circuit control chiplet source device 12 can control other source devices 12 in the intermediate device 22. For example, the integrated circuit control chiplet source device 12 can provide active-matrix control to LEDs in a full-color pixel intermediate device 22. Active-matrix control circuits can be formed in small integrated circuits using photolithographic integrated circuit methods, tools, and materials.

Referring to Fig. 4, a source wafer 10 includes a source wafer substrate 50 having a patterned sacrificial layer 52 forming a plurality of sacrificial portions 54 spatially and laterally separated by anchors 58. The anchors 58 can be portions of the source wafer substrate 50. The source wafer substrate 50 can be a semiconductor or compound semiconductor. A source

device 12, for example, including an LED made of a compound semiconductor such as GaN, is disposed or formed on or over each sacrificial portion 54. In the example of Fig. 4, the LED includes source device electrical contacts 14 and patterned dielectric materials 16 to electrically insulate portions of the LED. The source device electrical contacts 14 are electrically connected to electrodes 15. In certain embodiments, as shown here, and the entire source device 12 is encapsulated with an encapsulation layer 18 for environmental protection and to provide mechanical robustness.

In an embodiment, the electrodes 15 are electrically connected on the intermediate support 24 or the destination substrate 30 using photolithography. In an alternative embodiment, and as shown in Fig. 4, the electrodes 15 form source connection posts 17 or spikes. When the source device 12 is micro-transfer printed, the source connection posts 17 can contact intermediate electrical conductors 28 (Fig. 5) to form an electrical connection. Demonstrations have shown that the source connection posts 17 can deform or pierce the intermediate electrical conductors 28 to form the electrical connection. Connection posts 17 are discussed in more detail, in U.S. Patent No. 8,889,485, entitled Methods for Surface Attachment of Flipped Active Components by Christopher Bower, and in U.S. Patent Application Serial No. 14/822,864, entitled Chiplets with Connection Posts by Prevatte et al., the disclosures of which are incorporated herein by reference in their entirety. Additionally, systems and methods for driving display systems are described in U.S. Patent Application No. 15/003,721, filed January 21, 2016, entitled Serial Row-Select Matrix-Addressed System, which is incorporated herein by reference in its entirety. Printable LEDs are described in U.S. Patent Application No. 15/373,865, filed December 9, 2016, entitled Micro-Transfer Printable LED Component, which is incorporated herein by reference in its entirety.

The sacrificial layer 52 can be an oxide layer or a selected portion of the source wafer substrate 50 that can be anisotropically etched. The patterned dielectric material 16 can be silicon nitride or silicon dioxide, as can the encapsulation layer 18. The electrodes 15 can be a metal, for example aluminum, gold, silver, tungsten, tantalum, titanium or other metals or metal alloys. These elements can be deposited (e.g., by evaporation or coating) and patterned (e.g., with photo-sensitive material and exposure masks) using photolithographic methods, materials, and tools.

The structure of Fig. 4 can be made by providing the source wafer substrate 50, depositing and then patterning the sacrificial layer 52 to form the sacrificial portions 54 and

anchors 58. Forms for the spikes are pattern-wise etched into the sacrificial portions 54. In one embodiment, a desired element (such as an LED or integrated circuit chiplet) is disposed on the sacrificial portions 54 by micro-transfer printing from a device substrate. In another embodiment, the desired element is formed on the sacrificial portions 54 using
5 photolithographic techniques. In one method, a patterned epitaxial growth layer is provided upon the sacrificial layer 52 and structures are formed on the epitaxial growth layer. The electrodes 15 are then deposited and patterned, as is the encapsulation layer 18.

In a method of the present invention, the patterned sacrificial layer 52 is a patterned layer of material different from the source wafer substrate 50 material that can be etched to
10 form a gap between the source device 12 and the source wafer substrate 50. In another method of the present invention, the patterned sacrificial layer 52 is a defined portion of the source wafer substrate 50 that can be anisotropically etched to form a gap between the source device 12 and the source wafer substrate 50. In an embodiment, the sacrificial portions 54 are gaps. In any case, the gap results in a tether 56 that physically connects the source device 12 to the
15 anchor 58 so that a stamp post of a micro-transfer stamp can contact the source device 12, fracture the tether 56 to release the source device 12 from the source wafer 10, and adhere the source device 12 to the stamp post and thereby enable the source device 12 to be micro-transferred to the intermediate support 24.

Referring to Fig. 5, an intermediate wafer 20 includes an intermediate wafer substrate
20 60 having a patterned sacrificial layer 52 forming a plurality of sacrificial portions 54 spatially separated by anchors 58. The anchors 58 can be portions of the intermediate wafer substrate 60. An intermediate support 24 is disposed on each sacrificial portion 54 and one or more source devices 12, such as red, green, and blue source devices 12R, 12G, 12B, are disposed on or over each intermediate support 24. Intermediate electrical conductors 28 (such as wires) can be
25 formed on the intermediate support 24 and electrically connect the source devices 12 and the connection posts 26 (if present). For clarity, the red, green, and blue source devices 12R, 12G, 12B are illustrated in a linear arrangement rather than the triangular arrangement of Fig. 2. However, the source devices 12 can be disposed on the intermediate support 24 in any desired arrangement.

30 In an embodiment, the electrodes 15 of the source devices 12 are electrically connected to the intermediate electrical conductors 28 using photolithography or the intermediate electrical conductors 28 are formed using photolithography. In an alternative embodiment, and

as shown in Fig. 5, the electrodes 15 form source connection posts 17 (Fig. 4) that impinge upon or pierce the intermediate electrical conductors 28 to form an electrical connection. In a further embodiment, the intermediate electrical conductors 28 form intermediate connection posts 26 or spikes. When the intermediate device 22 is micro-transfer printed, the intermediate
5 connection posts 26 can contact electrical conductors (e.g., row and column conductors 32, 34) on a destination substrate 30 to form an electrical connection.

The sacrificial layer 52 can be an oxide layer or a selected portion of the intermediate wafer substrate 60 that can be anisotropically etched, the intermediate support 24 can be silicon nitride, silicon dioxide, a resin, a cured resin, or a polymer. In various embodiments, the
10 patterned intermediate supports 24 can be glass, resin, an oxide, or a nitride and can be deposited by coating, evaporation, or sputtering. In an embodiment, the intermediate device 22 is encapsulated (not shown), for example with a resin. The intermediate electrical conductors 28, row conductors 32, or column conductors 34 can be a metal, for example aluminum, gold, silver, tungsten, tantalum, titanium or other metals or metal alloys. These elements can be
15 deposited (e.g., by evaporation or coating) and patterned (e.g., with photo-sensitive material and exposure masks) using photolithographic methods, materials, and tools.

The structure of Fig. 5 can be made by providing the intermediate wafer substrate 60, depositing and then patterning the sacrificial layer 52 to form the sacrificial portions 54 and anchors 58. An intermediate support 24 is provided, for example by evaporation or coating and
20 patterned using photolithographic methods. Forms for the spikes are etched into the intermediate support 24 or sacrificial portions 54. The source devices 12 are disposed on the intermediate support 24 by micro-transfer printing from the source wafer 10. If source connection posts 17 are not used, the intermediate electrical conductors 28 are then deposited and patterned, as is the encapsulation layer, if present.

25 In a method of the present invention, the patterned sacrificial layer 52 is a patterned layer of material different from the source wafer substrate 50 material that can be etched to form a gap between the intermediate support 24 and the intermediate wafer substrate 60. In another method of the present invention, the patterned sacrificial layer 52 is a defined portion of the intermediate wafer substrate 60 that can be anisotropically etched to form a gap
30 between the intermediate device 22 and the intermediate wafer substrate 60. In an embodiment, the sacrificial portions 54 are gaps. In any case, the gap results in a tether 56 that physically connects the intermediate device 22 to the anchor 58 so that a stamp post of a micro-

transfer stamp can contact the intermediate device 22, fracture the tether 56 to release the intermediate device 22 from the intermediate wafer 60 and adhere the intermediate device 22 to the stamp post and thereby enable the intermediate device 22 to be micro-transfer printed to the destination substrate 30. In various embodiments of the present invention, the patterned sacrificial layer 52 or the sacrificial portions 54 are a pattern of etchable material distinct from the source wafer substrate 50 material, are a pattern of defined portions of the source wafer substrate 50 material that are anisotropically etchable, or are a pattern of gaps forming a space between the source devices 12 and the source wafer substrate 50.

In another embodiment of the present invention, the source devices 12 micro-transfer printed onto the intermediate support 24 are electrically connected with intermediate electrical conductors 28 between the source devices 12 on the intermediate support 24 at an intermediate resolution. Destination substrate electrical conductors (e.g., the row conductors 32 and column conductors 34) electrically connect the intermediate devices 22 on the destination substrate 30 at a destination resolution less than the intermediate resolution. The resolution of an electrical conductor or connection is the size of the smallest element in a dimension over an area that can be reliably made or the minimum spacing between components that can be reliably achieved without electrical shorts. In various embodiments, the intermediate electrical connections have an intermediate resolution of less than or equal to 10 microns, less than or equal to 5 microns, less than or equal to two microns or less than or equal to one micro and the destination electrical connections have a destination resolution of greater than or equal to 5 microns, greater than or equal to 10 microns, greater than or equal to 20 microns or greater than or equal to 50 microns.

In an embodiment of the present invention, the intermediate stamp is provided with a larger extent over the intermediate wafer 20 than the source stamp is provided with over the source wafer 10. Wafers are typically relatively thin and flat, having an area with dimensions (typically represented as the x and y dimensions as shown in Fig. 2) that are much greater than the thickness of the wafer (typically represented as the z dimension). The stamp extent is the contiguous area enclosed by a convex hull perimeter surrounding the stamp posts. In various embodiments, the source stamp is provided with a diameter, diagonal, or edge of less than or equal to 1 cm, less than or equal to 2 cm, less than or equal to 5 cm, less than or equal to 10 cm, less than or equal to 15 cm, or less than or equal to 20 cm. The intermediate stamp can be provided with a diameter, diagonal, or edge of greater than or equal to 5 cm, 10 cm, greater

than or equal to 15 cm, greater than or equal to 20 cm, greater than or equal to 40 cm, greater than or equal to 50 cm, greater than or equal to 75 cm, or greater than or equal to 100 cm.

In an embodiment of the present invention, the intermediate wafer 20 is provided with a larger extent than the source wafer 10 and the destination substrate 30 is provided with a larger extent than the intermediate wafer 20. Furthermore, the intermediate support 24 can be provided with an extent that is greater than the extent of the source device 12. The extent of a wafer or substrate is the area of the wafer or substrate in the x, y dimensions or the contiguous area enclosed by a convex hull perimeter surrounding the source devices 12 on the wafer or substrate surface. The source wafers 10 can be provided with a 12-inch diameter, an 8-inch diameter, a 6-inch diameter, a 4-inch diameter, or a 2-inch diameter, or less. The intermediate wafer 20 can be provided with a diameter, diagonal, or side of 4 inches, 8 inches, 12 inches, 16 inches, 20 inches, 24 inches, 32 inches, 40 inches, 48 inches, 64 inches, or more. In general, the source wafers 10 have a circular cross section with a flat edge forming a chord. The intermediate wafer 20 can have the shape of a conventional semiconductor wafer or have a rectangular shape as can the display substrate 30.

In another embodiment, the intermediate wafer 20 is provided with a spatial format matched to the source stamp or the intermediate stamp. Alternatively or in addition, the destination substrate 30 is provided with a spatial format matched to the intermediate stamp. In yet another embodiment, the intermediate wafer 20 is provided with a spatial format matched to the destination substrate 30. The spatial format of a wafer or substrate is the shape of the wafer or substrate, for example rectangular, square, or circular. Alternatively, the spatial format of a wafer or substrate is the shape of a contiguous area enclosed by a convex hull perimeter surrounding the source devices 12 or intermediate supports 24 on the wafer or substrate surface.

In a further embodiment of the present invention, more source devices 12 are micro-transfer printed from the source wafer 10 to the intermediate wafer 20 with the source stamp in a single stamp operation than are transferred by micro-transfer printing intermediate devices 22 from the intermediate wafer 20 to the destination substrate 30 with the intermediate stamp in a single stamp operation. In general, the source stamp will have a denser arrangement of stamp posts and a smaller extent than the intermediate stamp and the intermediate stamp will have a sparser arrangement of stamp posts and a greater extent than the source stamp.

In an embodiment of the present invention and as illustrated in Fig. 4, the source wafer 10 is provided with micro-transfer printable source devices 12 having source connection posts 17. The source connection posts 17 can electrically connect the electrodes 15 (Fig. 1) to the intermediate electrical connections 28 on the intermediate support 24 to electrically connect the source devices 12 to the intermediate electrical connections 28 on the intermediate support 24 and to the intermediate connection posts 26 of the intermediate support 24. Similarly, as illustrated in Fig. 5, the intermediate wafer 20 is provided with micro-transfer printable intermediate supports 24 having intermediate connection posts 26. The intermediate connection posts 26 can electrically connect the intermediate electrical connections 28 (and electrodes 15 of Fig. 4) to the destination electrical connections (e.g., row conductors 32 and column conductors 34) on the destination substrate 30 to electrically connect the source devices 12 to the row and column conductors 32, 34 of the destination substrate 30.

In operation, a controller (not shown) provides electrical signals, power, and a ground reference to the row conductors 32 and column conductors 34 on the destination substrate 30. The electrical signals pass through the row conductors 32 and column conductors 34, the intermediate connection posts 26, the intermediate electrical conductors 28 of the intermediate wafer 20, the source connection posts 17, and the electrodes 15 to the source electronic element, such as an LED, to control the electronic element.

A system for making a micro-transfer printed device includes a source wafer 10 having a plurality of micro-transfer printable source devices 12 arranged in or on the source wafer 10 at a source spatial density; an intermediate wafer 20 having a plurality of micro-transfer printable intermediate supports 24 arranged in or on the intermediate wafer 20 at an intermediate spatial density less than or equal to the source spatial density; a destination substrate 30; a source stamp having a source transfer density; an intermediate stamp having an intermediate transfer density less than the source transfer density; a micro-transfer printer for micro-transfer printing the source devices 12 from the source wafer 10 to the intermediate supports 24 of the intermediate wafer 20 with a source stamp at a source transfer density to make an intermediate device 22 on each intermediate support 24; a micro-transfer printer for micro-transfer printing the intermediate devices 22 from the intermediate wafer 20 to the destination substrate 30 at a destination spatial density less than the source spatial density with an intermediate stamp at an intermediate transfer density less than the source transfer density. The source devices 12 can be light-emitting diodes. The destination substrate 30 can be a display substrate.

In a simplified theoretical illustration of the advantages of the present invention, the destination substrate 30 is a display substrate and the source devices 12 are LEDs 12. A source wafer 10 has a 100 x 100 array of LEDs 12, each LED 12 having an area of 15 microns x 15 microns on a 100-micron pitch, so that the source wafer 10 has 10,000 LEDs 12 and an extent of 1 cm x 1 cm. The destination substrate 30 requires a 1,000 x 1,000 array of LEDs 12 on a 1 mm pitch so that the destination substrate 30 has 1,000,000 LEDs 12 and an extent of 1 m x 1 m. Thus, the spatial density of the LEDs on the source wafer 10 is 100 times the spatial density of the LEDs on the destination substrate 30. Referring to Fig. 3, the LEDs 12 on the source wafer 10 can be directly micro-transfer printed to the destination substrate 30 with a source stamp.

Because of the size and density of the source wafer 10 compared to the destination substrate 30, the source stamp can transfer a 10 x 10 array of LEDs 12 on a 1 mm pitch in each of the x and y dimensions. Therefore, 100 LEDs 12 are transferred in each stamp operation so that to completely populate the destination substrate 30 requires 10,000 stamp operations.

In contrast, and according to an embodiment of the present invention, referring again to Fig. 2, the LEDs 12 are micro-transfer printed from the source wafer 10 to the intermediate wafer 20. This transfer can be done multiple times at the same spatial density so that all 10,000 of the LEDs (i.e., LEDs 12) on a source wafer 10 are transferred in one source stamp operation and the entire 1,000 x 1,000 array of LEDs (i.e., LEDs 12) can be disposed on the intermediate substrate in 100 stamp operations from 100 different source wafers (i.e., source wafers 10). The intermediate wafer (i.e., intermediate wafer 20) must have an array of intermediate substrates (i.e., intermediate substrates 24) at the same 100-micron pitch in each of the x and y dimensions and a size of 10 cm in each dimension (1,000 x 100 microns). The intermediate substrates (i.e., intermediate substrates 24) can have any size up to 100 microns on a side, for example 75 microns x 75 microns. The intermediate devices (i.e., intermediate devices 22) (including an LED 12 and intermediate support 24) are then micro-transfer printed to the destination substrate (i.e., destination substrate 30). The intermediate stamp can transfer an array of 100 x 100 intermediate devices (i.e., intermediate devices 22) in each intermediate stamp operation since the difference in spatial density between the intermediate wafer (i.e., intermediate wafer 20) and the destination substrate (i.e., destination substrate 30) is a factor of 10 in each of the x and y dimensions. Therefore, 10,000 intermediate devices (i.e., intermediate devices 22) are transferred in each intermediate stamp operation and 100 intermediate stamp operations are needed to fully populate the destination substrate (i.e., destination substrate 30). Thus,

according to this example of the present invention, 100 plus 100 equals 200 stamp operations are needed to micro-transfer print the LEDs 12 from the source wafer (i.e., source wafer 10) to the destination substrate (i.e., destination substrate 30) compared to 10,000 operations using a direct micro-transfer printing method, resulting in a reduction of 98% in stamp operations.

5 In a further example, the display is a full-color display and three source devices (i.e., source devices 12 – a red LED 12R, a green LED 12G, and a blue LED 12B) are micro-transfer printed from the red, green, and blue source wafers (i.e., wafers 10R, 10G, and 10B). Using the direct printing method of Fig. 3, three times the number of transfers are necessary, for a total of 30,000 transfers. Using a method of the present invention as illustrated in Fig. 2, three times the
10 number of transfers are needed to populate the intermediate supports (i.e., intermediate supports 24) of the intermediate wafer (i.e., intermediate wafer 20), totaling 300 micro transfer print operations. Each intermediate support (i.e., intermediate support 24) can have a size of 75 microns x 75 microns and will then have one each of a red LED 12R, a green LED 12G, and a blue LED 12B to make up the intermediate device (i.e., intermediate device 22). The intermediate
15 devices (i.e., intermediate devices 22) are then micro-transfer printed to the destination substrate (i.e., destination substrate 30) in 100 print operations as before for a total of 400 micro-transfer print operations. This compares with the 30,000 print operations required in the illustration of Fig. 3 and is a reduction of 98.7% in stamp operations.

 In one example, red, green, and blue LEDs (i.e., 12R, 12G, 12B) are provided on source
20 wafers (i.e., 10R, 10G, 10B), each source wafer (i.e., source wafer 10) having 2540 LEDs (i.e., LEDs 12) per inch and 125,440,000 LEDs in total on the source wafer. One each of the red, green, and blue LED source wafers 10 can supply 408 displays with 72.5 pixels per inch for a VGA-resolution 640 x 480 display of 224 mm by 168 mm and 307,200 pixels per display. Using the direct print method of Fig. 3, 153 print steps are required to populate the display, as shown
25 in Fig. 6. As illustrated in Fig. 7, using the method of Fig. 2 and according to an embodiment of the present invention, an intermediate wafer (i.e., intermediate wafer 20) has 508 LEDs (i.e., LEDs 12) per inch and 15,052,800 intermediate supports (i.e., intermediate supports 24), each forming a full-color pixel intermediate device (i.e., intermediate device 22) with a red, green, and blue LED (e.g., 12R, 12G, 12B). Each intermediate wafer (i.e., intermediate wafer 20) can
30 supply enough intermediate devices (i.e., intermediate devices 22) for 49 displays. Each display of 307,200 pixels can be micro-transfer printed in a single step, representing (on average) 4.12

transfer printing operations per display, a reduction of 97% in micro-transfer print operations compared to the direct print approach.

In another example, red, green, and blue LED 12R, 12G, 12B are provided on 150 mm source wafers 10R, 10G, 10B each having 2540 x 1270 LEDs per inch and 62,720,000 LEDs (i.e.,
5 LEDs 12) per source wafer 10 sufficient to supply 204 VGA (640 x 480) displays. Using a stamp size of 28 mm x 28 mm, it would again require 153 direct micro-transfer print operations using the direct micro-transfer printing method of Fig. 3. A 300 mm intermediate wafer can be completely populated in 153 steps and can supply 49 displays, each display micro-transfer printed in a single micro-transfer print operation, representing (on average) 4.12 transfer
10 printing operations per display, a reduction of 97% in micro-transfer print operations compared to the direct print approach. In this example, the intermediate resolution can be 2-micron lines and spaces and the destination resolution can be 15-micron lines and spaces.

In another example using a single rectangle layout for the red, green, and blue LEDs 12R, 12G, 12B on the respective source wafers 10R, 10G, 10B, each source wafer (i.e., source wafer
15 10) has 47,040,000 LEDs (i.e., LEDs 12), enough to supply 153 displays. Using a larger stamp size of 112 x 84 mm², the number of micro-transfer print steps for the direct approach is reduced to 12. The equivalent number of steps using a method of the present invention is 1.245 prints per display, for an improvement of 90%. In general, if the wafers and stamps are larger and more expensive, the relative advantage of the method of the present invention is decreased, for
20 example to 90%, and if the wafers and stamps are smaller, the relative advantage is increased, for example to 98%. Cost modeling demonstrates that methods of the present invention provide manufacturing cost savings.

The source devices 12 can be active components, for example including one or more active elements such as electronic transistors or diodes or light-emitting diodes and
25 photodiodes that produce an electrical current in response to ambient light as well as passive components such as resistors, capacitors, or conductors. The source devices 12 can be semiconductor devices having one or more semiconductor layers, such as an integrated circuit. The source devices 12 can be unpackaged die. In yet another embodiment, the intermediate devices 22 are compound elements having a plurality of active or passive elements, such as
30 multiple semiconductor devices with separate substrates, each with one or more active elements or passive elements, or both.

The source devices 12 made by methods of the present invention can include or be a variety of chiplets having semiconductor structures, including a diode, a light-emitting diode (LED), a transistor, or a laser. The source devices 12 can include inorganic materials such as silicon or gallium arsenide, or inorganic materials having various structures, including crystalline, microcrystalline, polycrystalline, or amorphous structures. The source devices 12 or intermediate devices 22 can also include insulating layers and structures such as silicon dioxide, nitride, and passivation layers and conductive layers or structures such as wires made of aluminum, titanium, silver, or gold that form an electronic circuit.

Chiplets are small integrated circuits and can be unpackaged dies released from a source wafer 10 and can be micro transfer printed. Chiplets can have at least one of a width, length, and height from 2 to 5 μm , 5 to 10 μm , 10 to 20 μm , or 20 to 50 μm . Chiplets can have a doped or undoped semiconductor substrate thickness of 2 to 5 μm , 5 to 10 μm , 10 to 20 μm , or 20 to 50 μm . The chiplet or source devices 12 can be micro-light-emitting diodes with a length greater than width, for example having an aspect ratio greater than or equal to 2, 4, 8, 10, 20, or 50 and electrical contact pads 14 that are adjacent to the ends of the printable semiconductor source devices 12 along the length of the printable semiconductor source devices 12. This structure enables low-precision manufacturing processes to electrically connect wires to the source device electrical contact pads 14 without creating registration problems and possible unwanted electrical shorts or opens.

The chiplet source devices 12 can be made in a source semiconductor wafer (e.g., a silicon or GaN wafer) having a process side and a back side used to handle and transport the wafer. Source devices 12 are formed using lithographic processes in an active layer on or in the process side of the source wafer 10. An empty release layer space (e.g., the etched sacrificial layer 52) is formed beneath the source devices 12 with tethers 56 connecting the source devices 12 to the source wafer 10 in such a way that mechanical pressure applied against the source devices 12 breaks the tethers 56 to release the source devices 12 from the source wafer 10. Methods of forming such structures are described, for example, in the paper AMOLED Displays using Transfer-Printed Integrated Circuits and U.S. Patent No. 8,889,485. Lithographic processes for forming source devices 12 in a source wafer 10, for example transistors, wires, and capacitors, can be found in the integrated circuit art. U.S. Patent Application Serial No. 14/743,981, filed June 18, 2015, entitled Micro Assembled Micro LED Displays and Lighting Elements, incorporated herein by reference describes micro-transfer printing structures and

processes useful with the present invention. For a discussion of micro-transfer printing techniques see also U.S. Patent Nos. 8,722,458, 7,622,367 and 8,506,867, each of which is hereby incorporated by reference in its entirety. Micro-transfer printing using compound micro assembly structures and methods can also be used with the present invention, for example, as
5 described in U.S. Patent Application Serial No. 14/822,868, filed August 10, 2015, entitled Compound Micro-Assembly Strategies and Devices, which is hereby incorporated by reference in its entirety.

According to various embodiments of the present invention, the native source wafer 10
10 can be provided with the source devices 12, sacrificial layer 52, tethers 56, anchors 58, and source connection posts 17 already formed, or they can be constructed as part of the process of the present invention. In certain embodiments, the source device electrical contact pads 14 are planar electrical connections formed on the process side of the source devices 12 and source wafer 10. Such source device electrical contact pads 14 are typically formed from metals such as aluminum or polysilicon using masking and deposition processes.

15 The intermediate devices 22 can include active elements such as electronic circuits formed using lithographic processes and can include passive elements such as electrical connections, e.g., wires, to the source device electrical contact pads 14 and intermediate connection posts 26.

20 Connection posts 17, 26 are electrical connections that extend generally perpendicular to the surface of the source device 12 or intermediate device 22. Such connection posts 17, 26 can be formed from metals such as aluminum, titanium, tungsten, copper, silver, gold, or other conductive metals. The connection posts 17, 26 (as shown in Figs. 4 and 5) can be formed by repeated masking and deposition processes that build up three-dimensional structures or by using a form. In some embodiments, the connection posts 17, 26 are made of one or more high
25 elastic modulus metals, such as tungsten. As used herein, a high elastic modulus is an elastic modulus sufficient to maintain the function and structure of the connection post 17, 26 when pressed into an intermediate electrical conductor 28, row conductors 32, or column conductors 34 (or electrical contact pads, not shown).

30 In certain embodiments, the intermediate electrical connections 28 or row and column conductors 32, 34 include patterned metal layers forming electrical contact pads. The electrical contact pads can be made using integrated circuit photolithographic methods. Likewise, the connection posts 17, 26 can be made by etching one or more layers of evaporated or sputtered

metal. Such structures can also be made by forming a layers, etching a well into a surface, filling the well with a conductive material such as metal, and then removing the layer.

The connection posts 17, 26 can have a variety of aspect ratios and typically have a peak area smaller than a base area. The connection posts 17, 26 can have a sharp point for
5 embedding in or piercing electrical contact pads. Structures with protruding connection posts 17, 26 generally are discussed in U.S. Patent No. 8,889,485, referenced above, whose contents are incorporated by reference herein in their entirety.

In micro-transfer printing process, a stamp (e.g., the source stamp or intermediate stamp) includes a plurality of stamp posts (also referred to as pillars) that are pressed against
10 corresponding released components (e.g., source devices 12 or intermediate devices 22) to adhere the components to the stamp posts to transfer the pressed components from the source wafer 10 to the stamp posts. By pressing the stamp against the components, the tethers 56 are broken and the components are adhered to the stamp posts, for example by van der Waal's forces. The stamp is removed from the source wafer 10, leaving the components adhered to the
15 stamp posts.

An optional adhesive layer is coated over the intermediate wafer 20 or destination substrate 30 (the substrate). The stamp is then placed adjacent to the substrate. The components on the stamp posts of the transfer stamp are brought into alignment with the electrical conductors (e.g., row and column conductors 32, 32 or electrical contact pads of the
20 destination substrate 30 or intermediate electrical conductors 28 of the intermediate support 24) and pressed onto or into them by micro-transfer printing with sufficient mechanical pressure against the electrical conductors to drive the connection posts 17, 26 into or through a surface of the electrical conductors to form a robust electrical contact between the connection posts 17, 26 of the component and the substrate electrical conductors. A sufficient mechanical pressure
25 can be an amount of force needed to cause the substrate electrical conductors or connection post 17, 26 to plastically deform as the connection post 17, 26 is pressed into the substrate electrical conductors. Thus, in this embodiment, the connection posts 17, 26 on the components may have sharp points and/or a high elastic modulus, for example, by incorporating tungsten. A connection post 17, 26 can have a sharp point, for example, if the top of the post has an area
30 less than 10 microns square, less than 5 microns square, or less than one micron square. The substrate electrical conductors can also provide adhesion to help adhere the components to the substrate. In an alternative embodiment, the components do not have connection posts 17, 26

but are adhered to the substrate with the adhesive and photolithographic methods are used to form the electrical connections.

The adhesion between the components and the receiving side of the substrate should be greater than the adhesion between the components and the stamp posts of the transfer stamp. Thus, when the transfer stamp is removed from the receiving side of the substrate, the components adhere more strongly to the substrate than to the transfer stamp, thereby transferring the components from the transfer stamp to the receiving side of the destination substrate 30.

The transfer stamp is then removed leaving the components adhered to the substrate. An optional heat treatment can solder or weld the connection posts 17, 26 (if present) of the components to the substrate electrical contacts. Thus, in a further method of the present invention, the substrate electrical contacts (or connection posts 17, 26) are heated, causing the substrate electrical contact metal to reflow and improve adhesion between the components and the substrate and improve the electrical connection to the connection posts 17, 26.

The spatial distribution of the source devices 12 or intermediate devices 22 is a matter of design choice for the end product desired.

The connection posts 17, 26 can be made by pattern-wise etching a forming layer. For example, a silicon 100 wafer can be etched by a combination of dielectric hard masks, photolithography, mask etching, and anisotropic silicon wet etching with, for example KOH or TMAH, or dry etching. A layer of conductive material is deposited, for example with evaporation, e-beam deposition, sputtering, or CVD, and patterned by etching through a patterned photo-resist mask, to form connection posts 17, 26 at least in the form and optionally also on the planar surface of the underlying substrate (e.g., source wafer 10 or intermediate wafer 20) and components (e.g., source device 12) to form electrical conductors (e.g., electrodes 15 or intermediate electrical conductors 28). Soft metals can be used, such as gold, silver, tin, solders, or hard materials such as Ti, W, Mo, Ta, Al, or Cu.

The intermediate wafer 20 or destination substrate 30 (the substrate) for receiving transfer-printed printable components can include a surface on or in which a plurality of non-planar contact pads or electrical conductors are formed and exposed on the surface so that electrical connections can be made to the electrical conductors, such as electrical contact pads. The electrical contact pads can be multi-layer contact pads and can include a layer of solder. Alternatively, the electrical contact pads can be coated with a non-conductive layer or formed

on a compliant non-conductive layer, to facilitate electrical connection and adhesion. The non-conductive layer can be a polymer or an adhesive or the compliant non-conductive layer can be a polymer.

5 A shrinkable material can be disposed in and underfill the volume between the printable component and the substrate. The shrinkable material can be an adhesive and can adhere the printable component and the substrate. By underfill is meant that the shrinkable material does not fill the volume between the printable component and the substrate. Furthermore, with a heat treatment provided after disposing the shrinkable material, the shrinkable material shrinks and provides compression between the printable component and the substrate to further
10 strengthen and make robust the electrical connection between the connection posts 17, 26 and the electrical conductors or contact pads.

According to one embodiment of the present invention, the source wafer 10 can be provided with electronic elements, electrodes 15, and connection posts 17 already formed on the source wafer 10. Alternatively, an unprocessed source wafer 10 can be provided and the
15 electronic elements, electrodes 15, and connection posts 17 formed on the source wafer 10. An unprocessed source wafer 10 is a substrate that does not yet include the electronic elements, electrodes 15, and connection posts 17. The unprocessed source wafer 10 can have other processing steps completed, for example, cleaning, deposition of material layers, or heat or chemical treatments. Source devices 12 are formed, for example using photo-lithographic
20 processes including forming masks over the source wafer 10, etching materials, removing masks, and depositing materials. Using such processes, source devices 12 are formed on or in the source wafer 10.

In some embodiments, the source devices 12 are small integrated circuits formed in a semiconductor wafer, for example gallium arsenide or silicon, which can have a crystalline
25 structure. Processing technologies for these materials typically employ high heat and reactive chemicals. However, by employing transfer technologies that do not stress the source devices 12 or substrate materials, more benign environmental conditions can be used compared to thin-film manufacturing processes. Thus, the present invention has an advantage in that flexible substrates, such as polymeric substrates, that are intolerant of extreme processing conditions
30 (e.g. heat, chemical, or mechanical processes) can be employed for the destination substrates 30. Furthermore, it has been demonstrated that crystalline silicon substrates have strong mechanical properties and, in small sizes, can be relatively flexible and tolerant of mechanical

stress. This is particularly true for substrates having 5-micron, 10-micron, 20-micron, 50-micron, or even 100-micron thicknesses. Alternatively, the components can be formed in a microcrystalline, polycrystalline, or amorphous semiconductor layer.

The source devices 12 can be constructed using foundry fabrication processes. Layers of materials can be used, including materials such as metals, oxides, nitrides and other materials. Each source device 12 can be a complete semiconductor integrated circuit and can include, for example, transistors. The source devices 12 can have different sizes, for example, 1000 square microns or 10,000 square microns, 100,000 square microns, or 1 square mm, or larger, and can have variable aspect ratios, for example 1:1, 2:1, 5:1, or 10:1. The source devices 12 can be rectangular or can have other shapes.

Embodiments of the present invention provide advantages over other methods described in the prior art. By employing connection posts 17, 26 on source devices 12 and intermediate wafers 20 and a printing method that provides connection posts 17 adjacent to the intermediate support 24 or connection posts 26 adjacent to the destination substrate 30, a low-cost method for printing chiplets in large quantities over a destination substrate 30 is enabled. Furthermore, additional process steps for electrically connecting the source devices 12 to the destination substrate 30 are obviated.

The source wafer 10 and source devices 12, source transfer stamp, intermediate wafer 20, intermediate transfer stamp, and destination substrate 30 can be made separately and at different times or in different temporal orders or locations and provided in various process states.

The method of the present invention can be iteratively applied to a single or multiple intermediate wafers 20 or destination substrates 30. By repeatedly transferring sub-arrays of source devices 12 with a transfer stamp to an intermediate wafer 20 or destination substrate 30 and relatively moving the transfer stamp and intermediate wafer 20 or destination substrate 30 between stamping operations by a distance equal to the spacing of the selected source devices 12 in the transferred sub-array between each transfer of source devices 12, an array of source devices 12 formed at a high density on a source wafer 10 can be transferred to an intermediate wafer 20 or destination substrate 30 at a much lower spatial density. In practice, the source wafer 10 is likely to be expensive, and forming source devices 12 with a high density on the source wafer 10 will reduce the cost of the source devices 12, especially as compared to forming components on the destination substrate 30.

In particular, in the case wherein the active source device 12 is an integrated circuit formed in a crystalline semiconductor material, the integrated circuit substrate provides sufficient cohesion, strength, and flexibility that it can adhere to the destination substrate 30 without breaking as the transfer stamp is removed.

5 In comparison to thin-film manufacturing methods, using densely populated source wafers 10 and transferring source devices 12 to a destination substrate 30 that requires only a sparse array of source devices 12 located thereon does not waste or require active layer material on a destination substrate 30. The present invention can also be used in transferring source devices 12 made with crystalline semiconductor materials that have higher performance
10 than thin-film active components. Furthermore, the flatness, smoothness, chemical stability, and heat stability requirements for a destination substrate 30 used in embodiments of the present invention may be reduced because the adhesion and transfer process is not substantially limited by the material properties of the destination substrate 30. Manufacturing and material costs may be reduced because of high utilization rates of more expensive materials
15 (e.g., the source substrate) and reduced material and processing requirements for the destination substrate 30.

As is understood by those skilled in the art, the terms “over” and “under” are relative terms and can be interchanged in reference to different orientations of the layers, elements, and substrates included in the present invention. For example, a first layer on a second layer, in
20 some implementations means a first layer directly on and in contact with a second layer. In other implementations a first layer on a second layer includes a first layer and a second layer with another layer therebetween.

Having described certain implementations of embodiments, it will now become apparent to one of skill in the art that other implementations incorporating the concepts of the
25 disclosure may be used. Therefore, the disclosure should not be limited to certain implementations, but rather should be limited only by the spirit and scope of the following claims.

The various described embodiments of the invention may be used in conjunction with one or more other embodiments unless technically incompatible.

30 Throughout the description, where apparatus and systems are described as having, including, or comprising specific components, or where processes and methods are described as having, including, or comprising specific steps, it is contemplated that, additionally, there are

apparatus, and systems of the disclosed technology that consist essentially of, or consist of, the recited components, and that there are processes and methods according to the disclosed technology that consist essentially of, or consist of, the recited processing steps.

It should be understood that the order of steps or order for performing certain action is immaterial so long as the disclosed technology remains operable. Moreover, two or more steps or actions in some circumstances can be conducted simultaneously. The invention has been described in detail with particular reference to certain embodiments thereof, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

10

PARTS LIST

10	source wafer
10R	red source wafer
15	10G green source wafer
10B	blue source wafer
12	source device / LED
12R	red LED
12G	green LED
20	12B blue LED
14	source device electrical contact / pads
15	electrode
16	patterned dielectric material
17	source connection post / spike
25	18 encapsulation layer
20	intermediate wafer
22	intermediate device
24	intermediate support
26	intermediate connection post / spike
30	28 intermediate electrical conductor / electrical connection
30	destination substrate / display substrate
32	row conductors
34	column conductors

	50	source wafer substrate
	52	sacrificial layer
	54	sacrificial portion
	56	tether
5	58	anchor
	60	intermediate wafer substrate
	100	provide source wafer step
	105	form micro-transfer printable LEDs step
	110	provide intermediate wafer step
10	115	form micro-transfer printable substrates step
	120	provide destination substrate step
	125	form electrical conductors step
	130	micro-transfer print LEDs onto intermediate wafer step
	140	micro-transfer print intermediate devices onto destination substrate step
15	145	electrically connect intermediate devices on destination substrate step

CLAIMS:

1. A method of making a micro-transfer printed system, comprising:
providing a source wafer having a plurality of micro-transfer printable source devices
5 arranged in or on the source wafer at a source spatial density;
providing an intermediate wafer having a plurality of micro-transfer printable
intermediate supports arranged in or on the intermediate wafer at an intermediate spatial
density less than or equal to the source spatial density;
providing a destination substrate;
10 micro-transfer printing the source devices from the source wafer to the intermediate
supports of the intermediate wafer with a source stamp having a plurality of stamp posts at a
source transfer density to make an intermediate device on each intermediate support; and
micro-transfer printing the intermediate devices from the intermediate wafer to the
destination substrate at a destination spatial density less than the source spatial density with an
15 intermediate stamp having a plurality of stamp posts at an intermediate transfer density less
than the source transfer density.
2. The method of claim 1, comprising providing a plurality of source wafers, each source
wafer having a plurality of micro-transfer printable source devices arranged on or in the
20 respective source wafers at a respective source spatial density, and micro-transfer printing the
source devices from the plurality of source wafers to the intermediate supports of the
intermediate wafer with one or more source stamps at the source transfer density so that each
intermediate device has a plurality of source devices.
- 25 3. The method of claim 1 or 2, wherein the source wafer is a first source wafer, the source
devices are first source devices, the source stamp is a first source stamp, and the source spatial
density is a first source spatial density and comprising providing a second source wafer having a
plurality of micro-transfer printable second source devices arranged on or in the second source
wafers at a second source spatial density, and micro-transfer printing the second source devices
30 from the second source wafer to the intermediate supports of the intermediate wafer with one
or more second source stamps at the second source transfer density so that each intermediate
device has a first source device and a second source device.

4. The method of claim 2, comprising forming intermediate electrical connections between the source devices on the intermediate support at an intermediate resolution and forming destination electrical connections between the intermediate devices on the destination
5 substrate at a destination resolution less than the intermediate resolution.
5. The method of claim 4, comprising forming intermediate electrical connections at an intermediate resolution of less than or equal to 10 microns, 5 microns, two microns or one
10 micro and forming destination electrical connections at a destination resolution of greater than or equal to 5 microns, 10 microns, 20 microns or 50 microns.
6. The method of claim 2, comprising providing the intermediate stamp with a larger extent over the intermediate wafer than the source stamp over the source wafer.
- 15 7. The method of claim 6, comprising providing the source wafer with a 12-inch diameter, an 8-inch diameter, a 6-inch diameter, or a 4-inch diameter and comprising providing the intermediate wafer with a diameter, diagonal, or side of 8 inches, 12 inches, 16 inches, 20 inches, 24 inches, 32 inches, 40 inches, 48 inches, or 64 inches.
- 20 8. The method of claim 2, comprising providing a red source wafer having source devices that are red light-emitting diodes that can emit red light, providing a green source wafer having source devices that are green light-emitting diodes that can emit green light, providing a blue source wafer having source devices that are blue light-emitting diodes that can emit blue light, and wherein each intermediate device includes a red, a green, and a blue light-emitting diode.
25
9. The method of claim 2, comprising providing a chiplet source wafer having integrated circuit control chiplet source devices, and wherein each intermediate device includes an integrated circuit control chiplet.
- 30 10. The method of any one of the preceding claims, comprising one or more of providing the intermediate wafer with a larger extent than the source wafer, providing the destination

substrate with a larger extent than the intermediate wafer, and providing the intermediate support with an extent that is greater than the extent of the source device.

11. The method of any one of the preceding claims, comprising one or more of providing
5 the intermediate wafer with a spatial format matched to the source stamp or the intermediate stamp, providing the destination substrate with a spatial format matched to the intermediate stamp, and providing the intermediate wafer with a spatial format matched to the destination substrate.

10 12. The method of any one of the preceding claims, comprising providing the intermediate stamp with an extent larger than that of the source stamp.

13. The method of claim 12, comprising providing the source stamp with a diameter,
diagonal, or edge of less than or equal to 1 cm, 2 cm, 5 cm, 10 cm, 15 cm, or 20 cm and
15 providing the intermediate stamp with a diameter, diagonal, or edge of greater than or equal to 5 cm, 10 cm, 15 cm, 20 cm, 40 cm, 50 cm, 75 cm, or 100 cm.

14. The method of any one of the preceding claims, comprising micro-transfer printing
more source devices from the source wafer to the intermediate wafer with the source stamp in
20 a single stamp operation than are transferred by micro-transfer printing intermediate devices from the intermediate wafer to the destination substrate with the intermediate stamp in a single stamp operation.

15. The method of any one of the preceding claims, comprising providing the source wafer
25 with micro-transfer printable source devices having connection posts or providing the intermediate wafer with micro-transfer printable intermediate supports having connection posts.

16. The method of claim 15, comprising providing destination electrical connections on the
30 destination substrate and electrically connecting the intermediate devices to the electrical connections on the destination substrate with the connection posts.

17. The method of claim 15, comprising providing intermediate electrical connections on the intermediate support and electrically connecting the source devices to the electrical connections on the intermediate support with the connection posts.

5 18. The method of any one of the preceding claims, comprising providing the source devices as light-emitting diodes or providing the destination substrate as a display substrate.

19. A system for making a micro-transfer printed device, comprising:
a source wafer having a plurality of micro-transfer printable source devices arranged in

10 or on the source wafer at a source spatial density;

an intermediate wafer having a plurality of micro-transfer printable intermediate supports arranged in or on the intermediate wafer at an intermediate spatial density less than or equal to the source spatial density;

a destination substrate;

15 a source stamp having a source transfer density;

an intermediate stamp having an intermediate transfer density less than the source transfer density;

a micro-transfer printer for micro-transfer printing the source devices from the source wafer to the intermediate supports of the intermediate wafer with a source stamp at a source transfer density to make an intermediate device on each intermediate support; and

20 a micro-transfer printer for micro-transfer printing the intermediate devices from the intermediate wafer to the destination substrate at a destination spatial density less than the source spatial density with an intermediate stamp at an intermediate transfer density less than the source transfer density.

25

20. The system of claim 19, wherein the source devices are light-emitting diodes or the destination substrate is a display substrate.

AMENDED CLAIMS

received by the International Bureau on 21 July 2017 (21.07.2017)

1. A method of making a micro-transfer printed system, comprising:
providing a source wafer having a plurality of micro-transfer printable source devices
5 arranged in or on the source wafer at a source spatial density;
providing an intermediate wafer having a plurality of micro-transfer printable intermediate supports arranged in or on the intermediate wafer at an intermediate spatial density less than or equal to the source spatial density;
providing a destination substrate;
10 micro-transfer printing the source devices from the source wafer to the intermediate supports of the intermediate wafer with a source stamp having a plurality of stamp posts at a source transfer density to make an intermediate device on each intermediate support; and
micro-transfer printing the intermediate devices from the intermediate wafer to the destination substrate at a destination spatial density less than the source spatial density with an
15 intermediate stamp having a plurality of stamp posts at an intermediate transfer density less than the source transfer density, wherein the destination spatial density is less than the intermediate spatial density.
2. The method of claim 1, comprising providing a plurality of source wafers, each source wafer
20 having a plurality of micro-transfer printable source devices arranged on or in the respective source wafers at a respective source spatial density, and micro-transfer printing the source devices from the plurality of source wafers to the intermediate supports of the intermediate wafer with one or more source stamps at the source transfer density so that each intermediate device has a plurality of source devices.
- 25
3. The method of claim 1 or 2, wherein the source wafer is a first source wafer, the source devices are first source devices, the source stamp is a first source stamp, and the source spatial density is a first source spatial density and comprising providing a second source wafer having a
30 plurality of micro-transfer printable second source devices arranged on or in the second source wafers at a second source spatial density, and micro-transfer printing the second source devices from the second source wafer to the intermediate supports of the intermediate wafer with one or more second source stamps at the second source transfer density so that each intermediate device has a first source device and a second source device.

4. The method of claim 2, comprising forming intermediate electrical connections between the source devices on the intermediate support at an intermediate resolution and forming destination electrical connections between the intermediate devices on the destination substrate at a destination resolution less than the intermediate resolution.
- 5
5. The method of claim 4, comprising forming intermediate electrical connections at an intermediate resolution of less than or equal to 10 microns, 5 microns, two microns or one micro and forming destination electrical connections at a destination resolution of greater than or equal to 5 microns, 10 microns, 20 microns or 50 microns.
- 10
6. The method of claim 2, comprising providing the intermediate stamp with a larger extent over the intermediate wafer than the source stamp over the source wafer.
7. The method of claim 6, comprising providing the source wafer with a 12-inch diameter, an 8-
15 inch diameter, a 6-inch diameter, or a 4-inch diameter and comprising providing the intermediate wafer with a diameter, diagonal, or side of 8 inches, 12 inches, 16 inches, 20 inches, 24 inches, 32 inches, 40 inches, 48 inches, or 64 inches.
8. The method of claim 2, comprising providing a red source wafer having source devices that
20 are red light-emitting diodes that can emit red light, providing a green source wafer having source devices that are green light-emitting diodes that can emit green light, providing a blue source wafer having source devices that are blue light-emitting diodes that can emit blue light, and wherein each intermediate device includes a red, a green, and a blue light-emitting diode.
- 25
9. The method of claim 2, comprising providing a chiplet source wafer having integrated circuit control chiplet source devices, and wherein each intermediate device includes an integrated circuit control chiplet.
10. The method of any one of the preceding claims, comprising one or more of providing the
30 intermediate wafer with a larger extent than the source wafer, providing the destination substrate with a larger extent than the intermediate wafer, and providing the intermediate support with an extent that is greater than the extent of the source device.

11. The method of any one of the preceding claims, comprising one or more of providing the intermediate wafer with a spatial format matched to the source stamp or the intermediate stamp, providing the destination substrate with a spatial format matched to the intermediate stamp, and providing the intermediate wafer with a spatial format matched to the destination substrate.
- 5
12. The method of any one of the preceding claims, comprising providing the intermediate stamp with an extent larger than that of the source stamp.
13. The method of claim 12, comprising providing the source stamp with a diameter, diagonal, 10 or edge of less than or equal to 1 cm, 2 cm, 5 cm, 10 cm, 15 cm, or 20 cm and providing the intermediate stamp with a diameter, diagonal, or edge of greater than or equal to 5 cm, 10 cm, 15 cm, 20 cm, 40 cm, 50 cm, 75 cm, or 100 cm.
14. The method of any one of the preceding claims, comprising micro-transfer printing more 15 source devices from the source wafer to the intermediate wafer with the source stamp in a single stamp operation than are transferred by micro-transfer printing intermediate devices from the intermediate wafer to the destination substrate with the intermediate stamp in a single stamp operation.
- 20 15. The method of any one of the preceding claims, comprising providing the source wafer with micro-transfer printable source devices having connection posts or providing the intermediate wafer with micro-transfer printable intermediate supports having connection posts.
16. The method of claim 15, comprising providing destination electrical connections on the 25 destination substrate and electrically connecting the intermediate devices to the electrical connections on the destination substrate with the connection posts.
17. The method of claim 15, comprising providing intermediate electrical connections on the 30 intermediate support and electrically connecting the source devices to the electrical connections on the intermediate support with the connection posts.
18. The method of any one of the preceding claims, comprising providing the source devices as light-emitting diodes or providing the destination substrate as a display substrate.

19. A system for making a micro-transfer printed device, comprising:
a source wafer having a plurality of micro-transfer printable source devices arranged in or on the source wafer at a source spatial density;
an intermediate wafer having a plurality of micro-transfer printable intermediate supports
5 arranged in or on the intermediate wafer at an intermediate spatial density less than or equal to the source spatial density;
a destination substrate;
a source stamp having a source transfer density;
an intermediate stamp having an intermediate transfer density less than the source transfer
10 density;
a micro-transfer printer for micro-transfer printing the source devices from the source wafer to the intermediate supports of the intermediate wafer with a source stamp at a source transfer density to make an intermediate device on each intermediate support; and
a micro-transfer printer for micro-transfer printing the intermediate devices from the
15 intermediate wafer to the destination substrate at a destination spatial density less than the source spatial density with an intermediate stamp at an intermediate transfer density less than the source transfer density, wherein the destination spatial density is less than the intermediate spatial density.
20. The system of claim 19, wherein the source devices are light-emitting diodes or the
20 destination substrate is a display substrate.

STATEMENT UNDER ARTICLE 19 (1)

Claims 1 and 19 are amended to recite that "the destination spatial density is less than the intermediate spatial density." Micro-transfer printable devices on a source wafer are printed onto micro-transfer printable intermediate supports on an intermediate wafer, where a spatial density of micro-transfer printable intermediate supports is less than a spatial density of micro-transfer printable devices. Then, micro-transfer printable intermediate devices formed from the intermediate supports are printed onto a destination substrate, where a spatial density of the intermediate devices on the destination substrate is less than the spatial density of the intermediate supports on the intermediate wafer. The use of a source spatial density that is greater than an intermediate spatial density that is itself greater than a destination spatial density allows devices and systems to be fabricated using a reduced number of printing steps. Reducing the number of printing steps can reduce the cost of device fabrication.

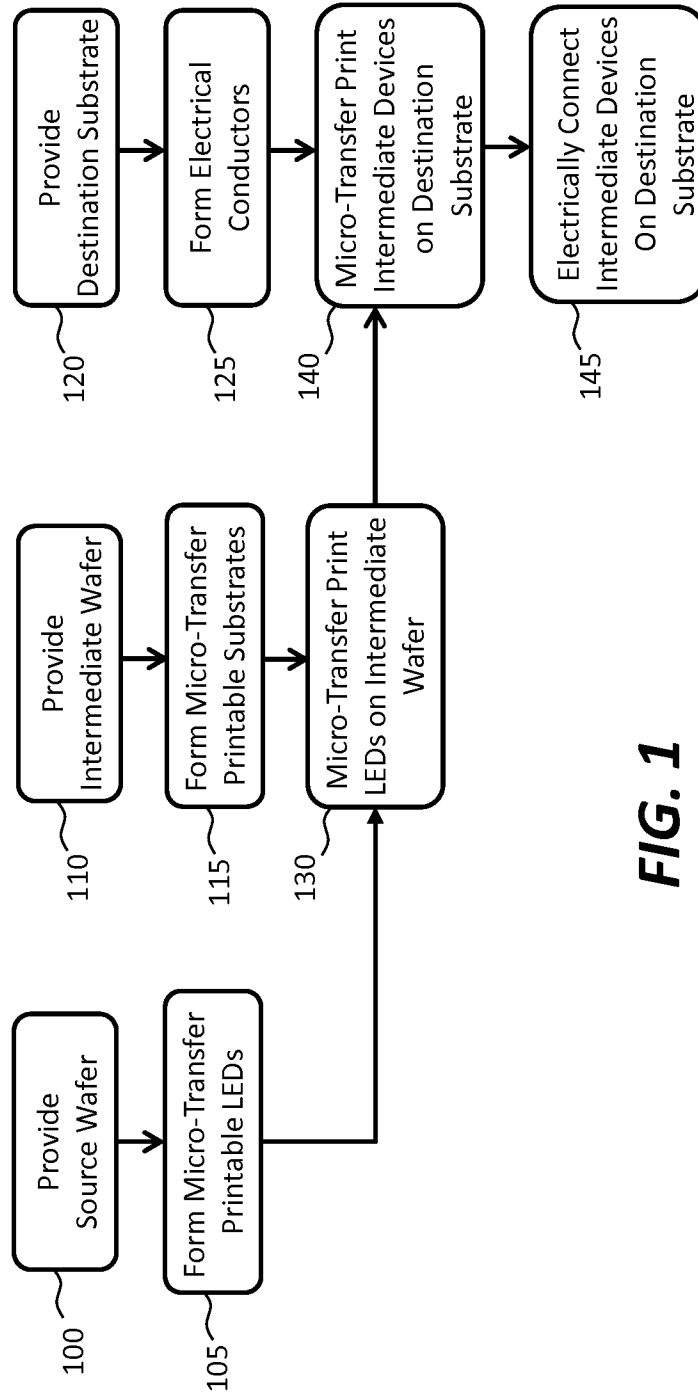


FIG. 1

Printing with Intermediate Wafers

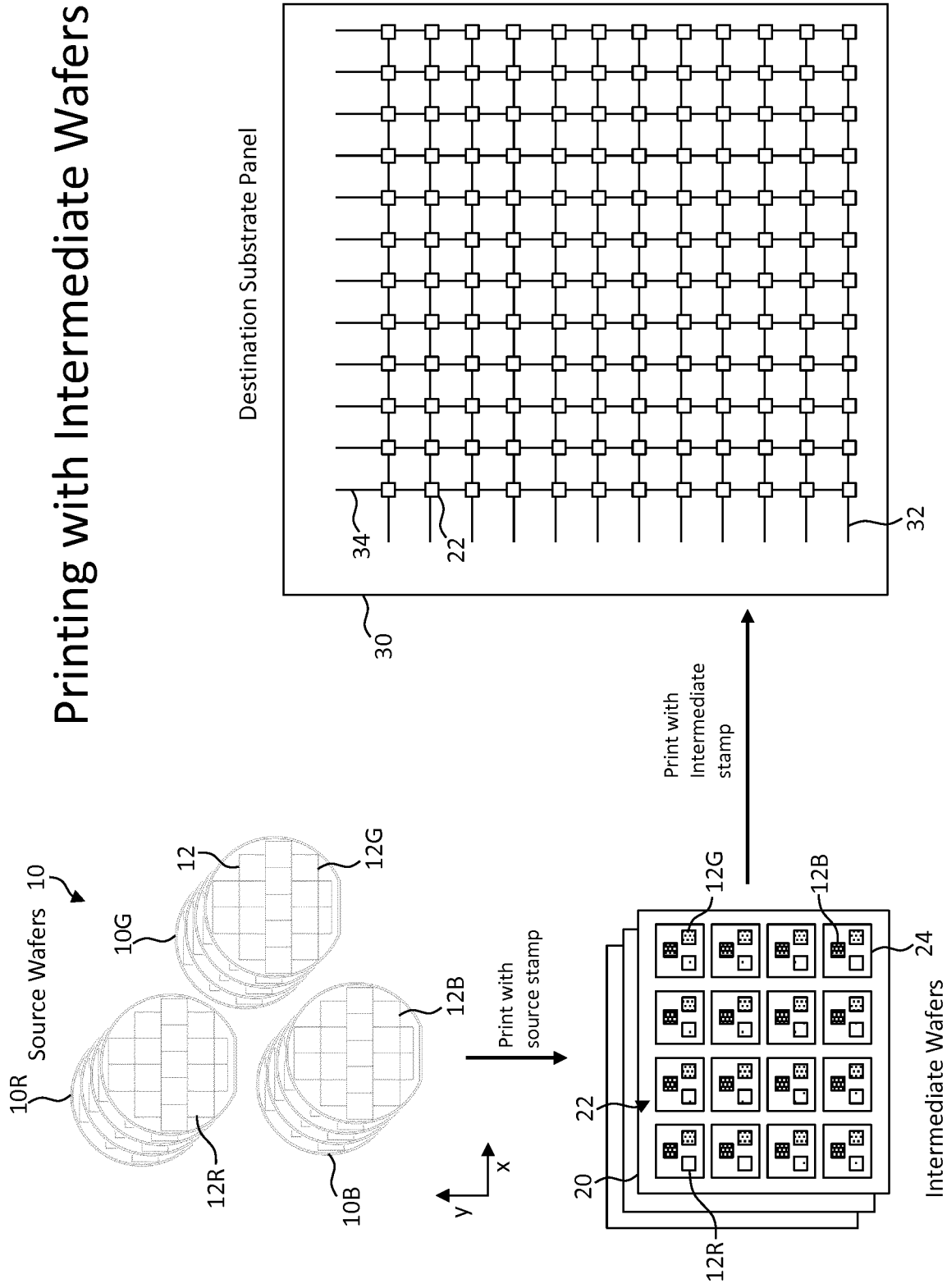


FIG. 2

Printing directly to Panels

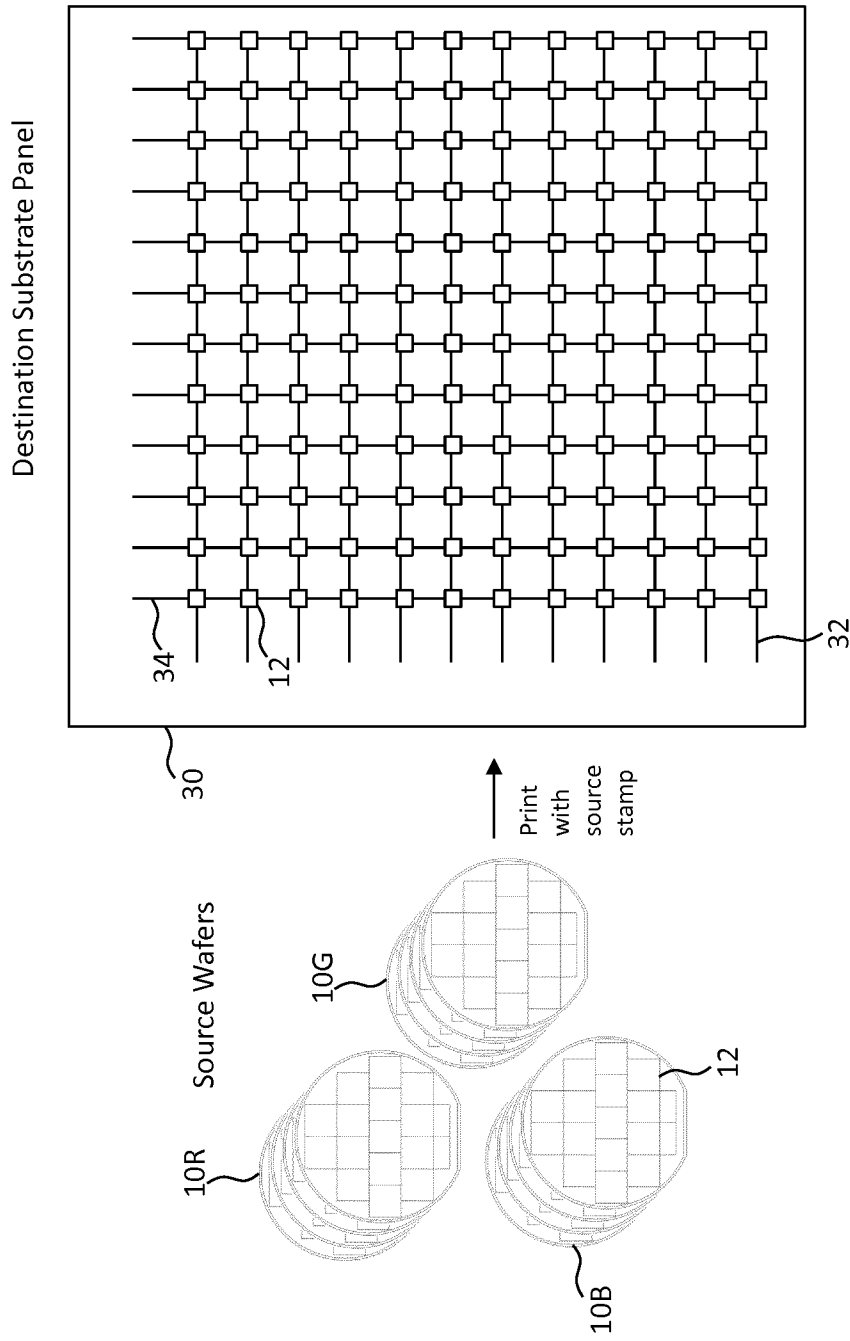


FIG. 3

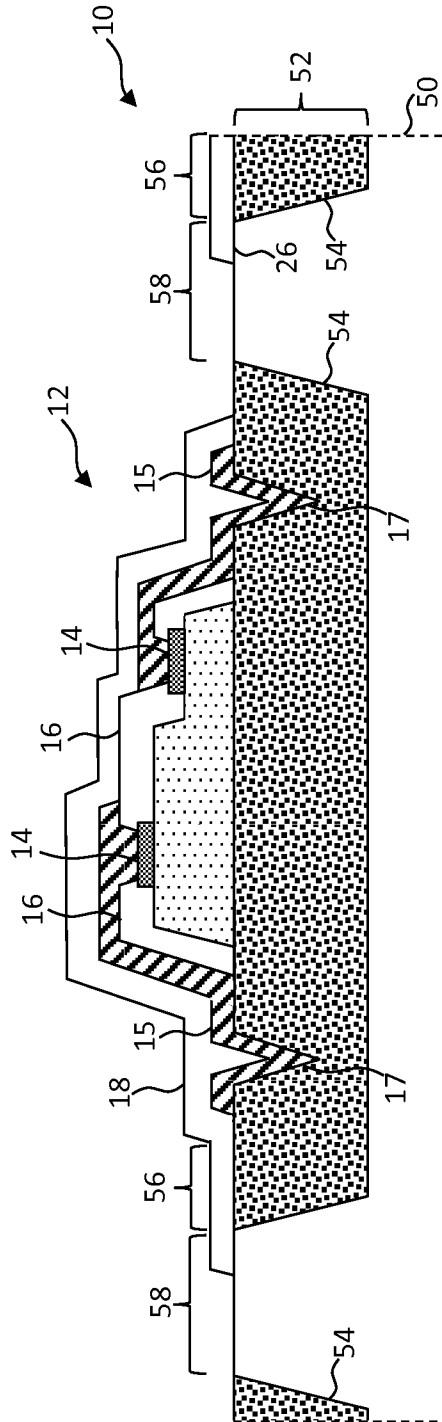


FIG. 4

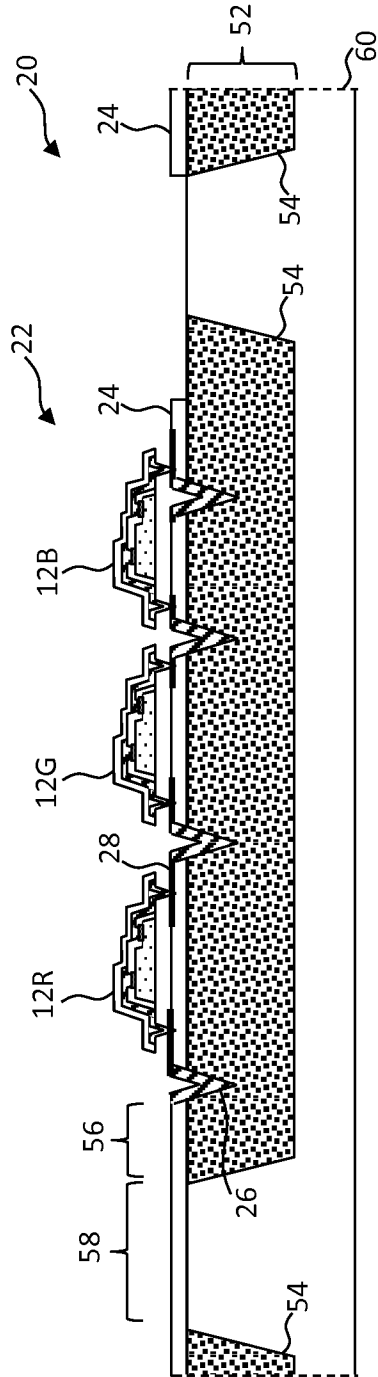


FIG. 5

Printing directly to Panels

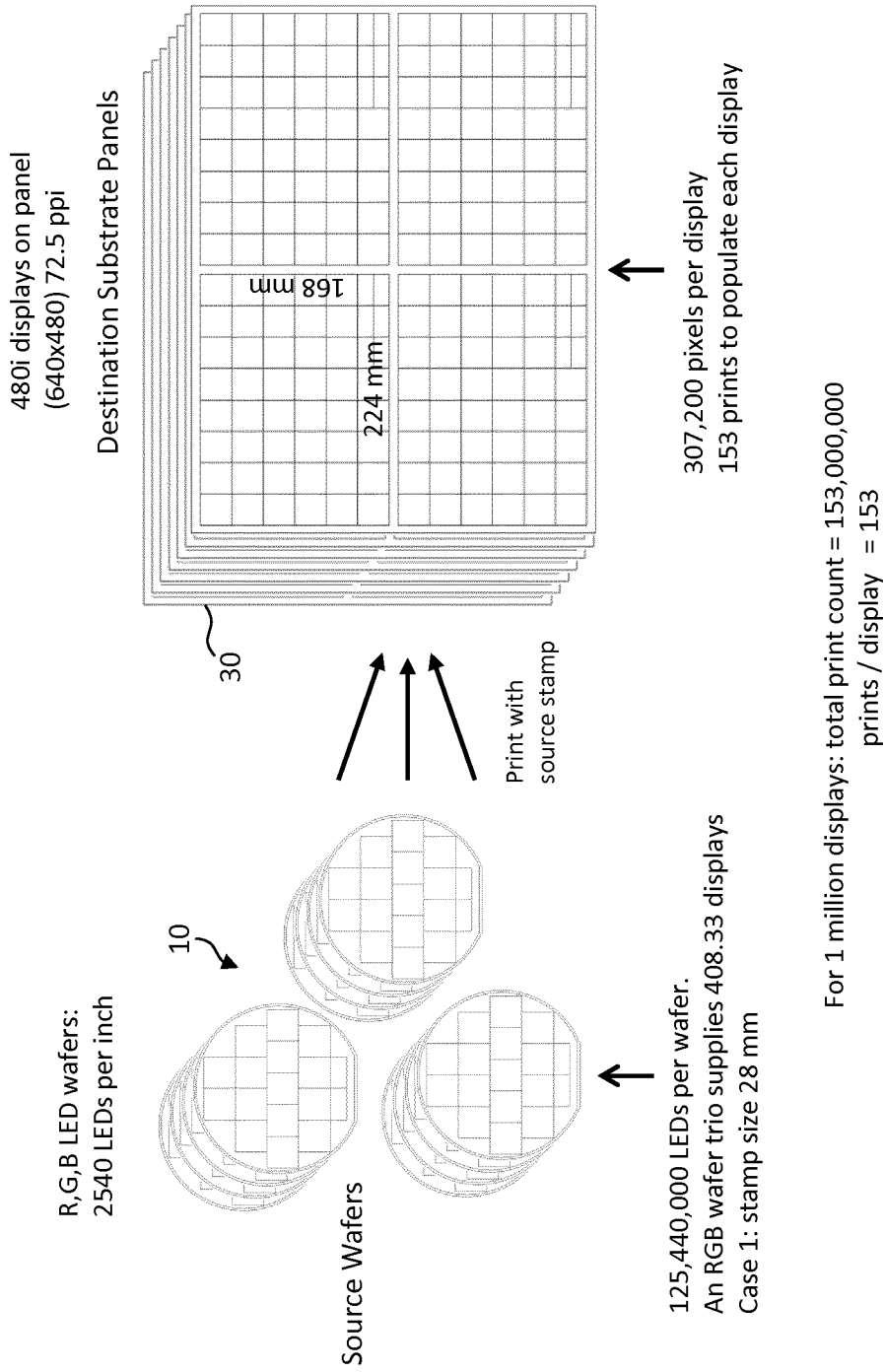


FIG. 6

Printing with Intermediate Wafers

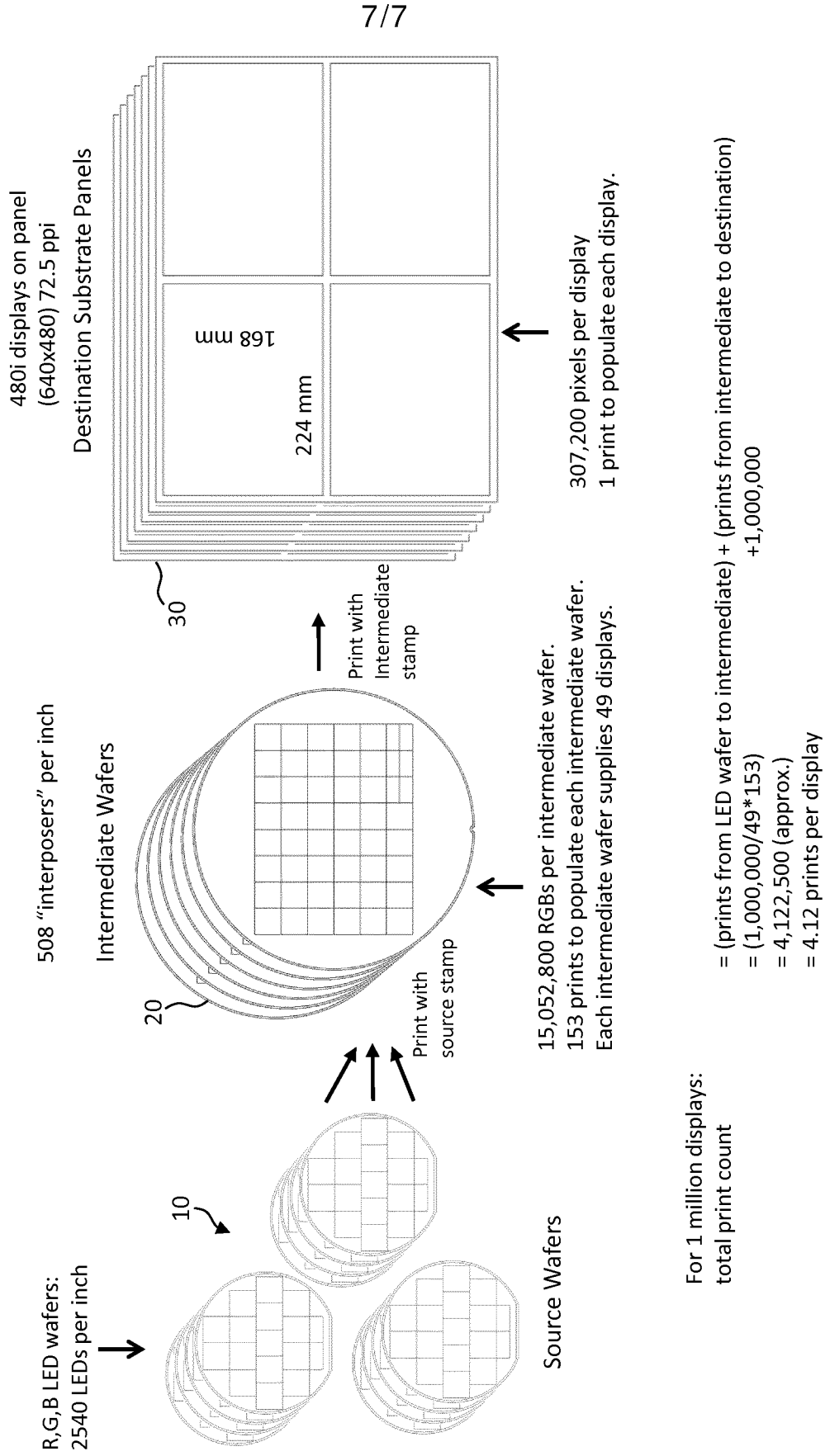


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2017/054140

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/683
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
H01L
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015/372393 A1 (BOWER CHRISTOPHER [US] ET AL) 24 December 2015 (2015-12-24) figures 1A-1C paragraphs [0008], [0009], [0015], [0073], [0079], [0085] - [0087]	1-20
X,P	US 2016/093600 A1 (BOWER CHRISTOPHER [US] ET AL) 31 March 2016 (2016-03-31) figures 3, 6 paragraphs [0108] - [0113], [0120] - [0121]	1-20

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier application or patent but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search 11 May 2017	Date of mailing of the international search report 22/05/2017
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Crampin, Nicola

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2017/054140

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	LU NANSHU ET AL: "Bio-integrated electronics", 2014 IEEE INTERNATIONAL CONFERENCE ON IC DESIGN & TECHNOLOGY, IEEE, 28 May 2014 (2014-05-28), pages 1-5, XP032609034, DOI: 10.1109/ICICDT.2014.6838615 [retrieved on 2014-06-17] figure 3 Section III -----	1-20

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2017/054140

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		US 2015372393 A1	24-12-2015
		WO 2015193433 A2	23-12-2015

US 2016093600 A1	31-03-2016	TW 201626542 A	16-07-2016
		US 2016093600 A1	31-03-2016
		WO 2016046283 A2	31-03-2016
