



(51) International Patent Classification:
H02M 7/00 (2006.01) *H02G 5/00* (2006.01)

(21) International Application Number:
PCT/EP2019/025364

(22) International Filing Date:
24 October 2019 (24.10.2019)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
16/170880 25 October 2018 (25.10.2018) US

(71) Applicant: **EATON INTELLIGENT POWER LIMITED** [IE/IE]; 30 Pembroke Road, Dublin, 4 (IE).

(72) Inventor: **NOJIMA, Geraldo**; 15806 Reynolds Drive, Fort Mill, SC 29707 (US).

(74) Agent: **BRP RENAUD UND PARTNER MBB**; Rechtsanwälte Patentanwälte Steuerberater, Königstrasse 28, 70173 Stuttgart (DE).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,

(54) Title: LOW INDUCTANCE BUS ASSEMBLY AND POWER CONVERTER APPARATUS INCLUDING THE SAME

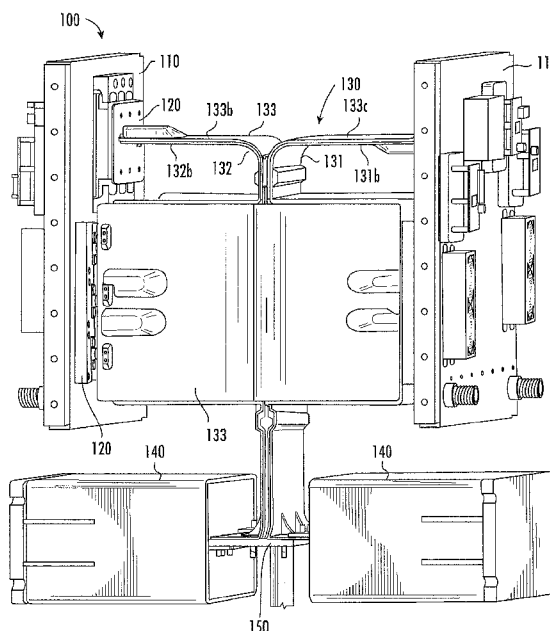


FIG. 1

(57) Abstract: An apparatus, such as a power converter, includes first, second and third core bus plates arranged in parallel. The apparatus also includes a first bus extension plate joined to the first core bus plate and extending therefrom at a first angle and a second bus extension plate joined to the second core bus plate and extending therefrom at a second angle. The apparatus further includes a third bus extension plate joined with the third core bus plate and disposed parallel to the first bus extension plate and a fourth bus extension plate joined with the third core bus plate and disposed parallel to the second bus extension plate.



MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

- *with international search report (Art. 21(3))*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

LOW INDUCTANCE BUS ASSEMBLY AND POWER CONVERTER APPARATUS INCLUDING THE SAME

STATEMENT OF GOVERNMENT SUPPORT

5 **[0001]** This invention was made with Government support under Contract #DE-EE0007253
awarded by the U.S. Department of Energy. The Government has certain rights in this invention.

BACKGROUND

10 **[0002]** The inventive subject matter relates to power conversion apparatus and, more
particularly, to power converter bus structures and power converter systems incorporating the
same.

15 **[0003]** Conventional power converter apparatus commonly use silicon-based semiconductor
switching devices, such as insulated gate bipolar transistors (IGBTs). Such devices are typically
limited to operating voltages less than 10kV and switching frequencies less than 100 kHz. For
applications requiring higher operating voltages and frequencies, wide bandgap semiconductor
switching devices, such as silicon carbide (SiC) MOSFETs, have been developed to replace
conventional silicon IGBT-based solutions.

20 **[0004]** Wide bandgap semiconductor switching devices may be operated at frequencies on
the order of 20 times greater than the maximum operating frequencies of conventional silicon
IGBTs. At these higher switching speeds, circuit parasitics, such as parasitic inductance and
capacitance associated with interconnecting bus bars, can cause significant voltage and current
transients that can be detrimental to operation of a power converter and limit full utilization of
the capabilities of these higher performance devices.

SUMMARY OF THE INVENTION

25 **[0005]** Some embodiments of the inventive subject matter provide an apparatus including
first, second and third core bus plates arranged in parallel. The apparatus also includes a first bus
extension plate joined to the first core bus plate and extending therefrom at a first angle and a
second bus extension plate joined to the second core bus plate and extending therefrom at a
30 second angle. The apparatus further includes a third bus extension plated joined with the third

core bus plate and disposed parallel to the first bus extension plate and a fourth bus extension plate joined with the third core bus plate and disposed parallel to the second bus extension plate.

[0006] In some embodiments, the third core bus plate may be disposed between the first and second core bus plates. The first bus extension plate may extend from the first core bus plate in a first direction perpendicular to a plane of the first core bus plate and the second bus extension plate may extend from the second core bus plate in a second direction opposite the first bus direction. The third bus extension plate may extend from the third core bus plate in the first direction and the fourth bus extension plate may extend from the third core bus plate in the second direction.

[0007] In further embodiments, the first bus extension plate may include a first planar member that joins the first core bus plate at a first arcuate joint. The second bus extension plate may include a second planar member that joins the second core bus plate at a second arcuate joint. The third and fourth bus extension plates may include third and fourth planar members that join the third core bus plate at a rounded Y joint.

[0008] According to some embodiments, the first bus extension plate may join the first core bus plate at a first edge thereof and the second bus extension plate may join the second core bus plate at a first edge thereof. The apparatus may further include a fifth bus extension plate joining the first core bus plate at a second edge thereof and extending therefrom at a third angle, a sixth bus extension plate joining the second core bus plate at a second edge thereof and extending therefrom at a fourth angle, a fourth core bus plate disposed in parallel with the first, second and third core bus plates, a seventh bus extension plate joined to the fourth core bus plate and disposed parallel to the fifth bus extension plate, and an eighth bus extension plate joined to the fourth core bus plate and disposed parallel to the sixth bus extension plate. The first and fifth bus extension plates may extend from the first core bus plate in a first direction perpendicular to a plane of the first core bus plate and the second and sixth bus extension plates may extend from the second core bus plate in a second direction opposite the first direction. The third and fourth core bus plates may be disposed between the first and second core bus plates.

[0009] The apparatus may further include a ninth bus extension plate joining the first core bus plate at a third edge thereof and extending therefrom at a fifth angle, a tenth bus extension plate joining the second core bus plate at a third edge thereof and extending therefrom at a sixth angle, a fifth core bus plate arranged in parallel with the first, second, third and fourth core bus

plates, an eleventh bus extension plate joined to the fifth core bus plate and disposed parallel to the ninth bus extension plate, and a twelfth bus extension plate joined to the fifth core bus plate and disposed parallel to the tenth bus extension plate. The first, fifth and ninth bus extension plates may extend from the first core bus plate in the first direction and the second, sixth and tenth bus extension plates may extend perpendicularly from the second core bus plate in the second direction. The third, fourth and fifth core bus plates may be disposed between the first and second core bus plates.

[0010] According to some aspects, the apparatus may further include a first semiconductor switching device electrically connected to ends of the first and third bus extension plates and a second semiconductor switching device electrically connected to ends of the second and fourth bus extension plates. The apparatus may include a power converter circuit including the first and second semiconductor devices, wherein the first core bus plate and the first bus extension plate are components of a first DC bus of the power converter circuit, wherein the second core bus plate the second bus extension plate are components of a second DC bus of the power converter circuit, and wherein the third core bus plate, the third bus extension plate and the fourth bus extension plate are components of an input bus and/or an output bus of the power converter circuit.

[0011] A first capacitor may be electrically connected to the first bus core plate and a second capacitor may be electrically connected to the second bus core plate. The apparatus may further include a fifth bus extension plate joined to the first bus core plate, extending at an angle therefrom and electrically connected to a first terminal of the first capacitor, a sixth bus extension plate joined to the second bus core plate, extending at an angle therefrom and electrically connected to a first terminal of the second capacitor, and a common plate parallel to the fifth and sixth bus extension plates and electrically connected to second terminals of the first and second capacitors, wherein the third bus core plate has a portion extending between the fifth and sixth bus extension plates and through an opening in the common plate.

[0012] Further embodiments of the inventive subject matter provide an apparatus including first, second and third buses arranged in parallel, the third bus disposed between the first and second buses, a first bus extension extending from the first bus in first direction perpendicular to the first bus, a second bus extension extending from the second bus in a second direction perpendicular to the second bus and opposite the first direction, a third bus extension extending

from the third bus in parallel with the first bus extension, and a fourth bus extension extending from the third bus in parallel with the second bus extension. A first semiconductor switching device is coupled to an end of the first bus extension and to an end of the third bus extension and a second semiconductor switching device is coupled to an end of the second bus extension and to an end of the fourth bus extension.

[0013] The first, second and third buses may include respective first, second and third planar members. The first bus extension may be joined to the first bus at a first edge of the first planar member, the second bus extension may be joined to the second bus at a first edge of the second planar member, and the third and fourth bus extensions may be joined to the third bus at a first edge of the third planar member. The apparatus may further include a fourth bus including a fourth planar member arranged in parallel with the first, second and third buses, a fifth bus extension joined to the first bus at a second edge of the first planar member extending from the first bus in the first direction, a sixth bus extension joined to the second bus at a second edge of the second planar member and extending from the second bus in the a second direction, a seventh bus extension joined to the fourth bus at a first edge of the fourth planar member and extending in parallel with the fifth bus extension, and an eighth bus extension joined to the fourth bus at the first edge of the fourth planar member and extending in parallel with the sixth bus extension. A third semiconductor switching device may be coupled to an end of the fifth bus extension and to an end of the seventh bus extension, and a fourth semiconductor switching device may be coupled to an end of the sixth bus extension and to an end of the eighth bus extension.

[0014] Still further embodiments provide an apparatus including first and second semiconductor switching devices disposed opposite one another at respective ones of opposing first and second surfaces, a first bus including a first conductive plate disposed between the first and second surfaces and extending in a first direction towards the first surface to electrically connect to the first semiconductor switching device, a second bus including a second conductive plate disposed between the first and second surfaces and extending in a second direction perpendicular to the first direction towards the second surface to electrically connect to the second semiconductor switching device, and a third bus including a third conductive plate disposed parallel to the first conductive plate and electrically connected to the first semiconductor switching device and a fourth conductive plate disposed parallel to the second

conductive plate and electrically connected to the second semiconductor switching device and the third conductive plate.

BRIEF DESCRIPTION OF THE DRAWINGS

- 5 [0015] FIGs. 1 and 2 are perspective views illustrating a power converter apparatus according to some embodiments.
- [0016] FIG. 3 is a perspective view of a bus assembly of the power converter apparatus of FIG. 1.
- [0017] FIG. 4 is an isolated perspective view of a DC bus of the bus assembly of FIG. 3.
- 10 [0018] FIG. 5 is an isolated perspective view of input/output buses of the bus assembly of FIG. 3.
- [0019] FIG. 6 is a detailed perspective view of core plates of the input/output buses of FIG. 4.
- [0020] FIG. 7 is an isolated perspective view of one of the input/output buses of FIG. 3.
- 15 [0021] FIGs. 8 and 9 are detailed perspective views of connections of the bus assembly and a power transistor module in the power converter apparatus of FIGs. 1 and 2.
- [0022] FIG. 10 is a cutaway view illustrating connection of a DC bus to a power transistor module in the power converter apparatus of FIGs. 1 and 2.
- [0023] FIGs. 11-13 are perspective views of a power transistor module of the power
- 20 converter apparatus of FIGs. 1 and 2.
- [0024] FIGs. 14-16 are perspective views of connection of a bus assembly to storage capacitors in the power converter apparatus of FIGs. 1 and 2.
- [0025] FIG. 17 is a schematic diagram illustrating a half-bridge circuit in the power
- 25 converter apparatus of FIGs. 1 and 2.

DETAILED DESCRIPTION

- [0026] Specific exemplary embodiments of the inventive subject matter now will be described with reference to the accompanying drawings. This inventive subject matter may, however, be embodied in many different forms and should not be construed as limited to the
- 30 embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the inventive subject matter to

those skilled in the art. In the drawings, like numbers refer to like items. It will be understood that when an item is referred to as being "connected" or "coupled" to another item, it can be directly connected or coupled to the other item or intervening items may be present. As used herein the term "and/or" includes any and all combinations of one or more of the associated
5 listed items.

[0027] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the inventive subject matter. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless expressly stated otherwise. It will be further understood that the terms "includes," "comprises,"
10 "including" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, items, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, items, components, and/or groups thereof.

[0028] Unless otherwise defined, all terms (including technical and scientific terms) used
15 herein have the same meaning as commonly understood by one of ordinary skill in the art to which this inventive subject matter belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0029] FIGs. 1 and 2 illustrate a power converter apparatus 100 according to some
20 embodiments of the inventive subject matter. The apparatus 100 includes semiconductor switching devices, here shown as power transistor modules 120, which are mounted on opposing parallel heat sinks 110. Each of the modules 120 includes one or more power transistors. For example, each of the modules may include six power MOSFET transistors, which may be
25 connected in parallel to increase current capability. A bus assembly 130 interconnects the modules 120 and includes first and second DC buses 131, 132 and three input/output buses 133 (one per phase), which interconnect the transistor modules 120 to implement a three-phase converter including three half-bridge circuits, such as the half-bridge circuit 1700 shown schematically in FIG. 17. It will be appreciated that such a converter may be operated as an
30 inverter, a rectifier or a bidirectional converter.

[0030] As further illustrated in FIGs. 1 and 2, the converter apparatus 100 also includes storage capacitors 140, which have first terminals coupled to respective ones of the DC busses 131, 132 and second terminals coupled in common to a common bus 150. As explained in greater detail below, the DC busses 131, 132 and the input/output busses 133 are configured to provide low-inductance interconnections of the capacitors 140 and the transistor modules 120, which can be particularly advantageous for applications in which the transistor modules 120 include wide bandgap switching devices, such as Group III-V wide bandgap MOSFETs, that can be operated at high switching speeds and operating voltages.

[0031] FIGs. 3-7 illustrate details of the bus assembly 130. Referring to FIGs. 3 and 4, the first DC bus 131 includes a core plate 131a from which first, second and third bus extension plates 131b, 131c, 131d extend in a perpendicular fashion to connect to the transistor modules 120. The first, second and third bus extension plates 131b, 131c, 131d are joined to the core plate 131a by rounded, arcuate joints 131e, 131f, 131g, which can provide a more uniform current distribution and reduce the likelihood of arcing that can arise from the presences of sharp edges or similar features. Additional fourth and fifth bus extension plates 131h, 131i extend laterally from the core plate 131a to provide connections to a DC source and/or load. It will be appreciated that the second DC bus 132 has a similar structure.

[0032] FIGs. 5-7 illustrate the structure of the input/output busses 133. Each of the input/output busses 133 includes a core plate 133a, from which first and second bus extension plates 133b, 133c extend perpendicularly from the core plate 133a in opposite first and second directions. The first and second bus extension plates 133b, 133c are joined to the core plate 133a at a rounded Y-cross section joint that provides arcuate junctions between the bus extension plates 133b, 133c and the core plate 133a. As explained above, this configuration can improve current distribution and reduce the likelihood of arcing. Referring to FIG. 6, the core plates 133a of the input/output busses 133 are arranged in parallel and separated by insulating material (not shown), resulting in composite input/output bus structure as shown in FIG. 5.

[0033] Referring again to FIG. 3, respective ones of the input/output bus extension plates 133b, 133c are disposed parallel to and generally conform to the contours of respective ones of the DC bus extension plates 131b, 132b of the first and second DC busses 131, 132. As shown in FIGs. 1 and 2, ends of the parallel DC and input/output bus extension plates 131b, 133c are electrically connected a first one of the transistor modules 120, while ends of the parallel bus

extension plates 132b, 133b are electrically connected to a second one of the transistor modules 120. The use of relatively wide, plate-type bus conductors and close, conformal parallel routing of the ingoing and outgoing buses connected to each transistor module 120 can reduce stray inductance in comparison to conventional designs. The symmetrical configuration of the bus structure 130 with respect to the capacitors 140 can also provide substantially equal current sharing among the transistors in the modules 120.

[0034] The DC buses 131, 132 and the input/output buses 133 can be provided with additional features to, for example, achieve desirable current distribution characteristics and/or limit arcing at high operating voltages. For example, as shown in FIG. 1, lateral edges of the parallel DC bus extension plates 131b, 132b and the corresponding parallel input/output bus extension plates 133b, 133c can be slightly offset to reduce the likelihood of arcing between these edges. The DC buses 131, 132 and the input/output buses 133 can be fabricated using any of a number of different techniques to achieve desired topological and other features. For example, in some embodiments, the DC buses 131, 132 and the input/output buses 133 could be fabricated using three-dimensional (3D) printing techniques, such as direct metal laser sintering (DMLS), which can be used to introduce features such as variable thickness regions, variable resistance regions, openings, meshes and the like. Such features may be used, for example, to achieve a desired current distribution and/or limit the likelihood of arcing between the buses and adjacent structures.

[0035] FIGs. 8-10 illustrate details of interconnections of the bus extension plates to the transistor modules 120. First contacts 121 of a transistor module 120 are contacted by a flange 135 at the end of the input/output bus extension plate 133c. Second contacts 122 of the transistor module 120 are connected to the extension plate 131b of the first DC bus 131. This contact arrangement can provided the connectivity illustrated in FIG. 17.

[0036] FIGs. 11-13 illustrate the mounting of the transistor module 120 on the heat sink 110. The base of the transistor module 120 is disposed on the heat sink 110, with a thermally conductive and electrically insulating ceramic pad 124 separating the transistor module 120 from the surface of the heat sink 110. Insulating ceramic clamps 123 on respective first and second sides of the transistor module 120 are used to secure the transistor module 120 to the heat sink 110 without an electrical connection between the transistor module 120 and the heatsink 110. This enables fabrication of the heatsink 110 from electrically conductive material (e.g.,

aluminum) and allows for grounding of the heatsink 110. The illustrated mounting arrangement using the insulating ceramic clamps 123 can also reduce the likelihood of arcing between the terminals 121, 122 of the transistor module 120 and adjacent metal structures in high voltage applications.

5 **[0037]** FIGs. 14-16 illustrate details of the connection of the DC buses 131, 132 to the capacitors 140 shown in FIGs. 1 and 2. As shown in FIG. 16, the DC buses 131, 132 have perpendicular bus extensions 131j, 132j that are configured to be attached to first terminals 141 of the capacitors 140. The common plate 150 is configured to be attached to second terminals of the capacitors 140. Bus extensions of the input-output buses 133 pass through an opening in the
10 common plate, as can be seen in FIG. 15.

[0038] In the drawings and specification, there have been disclosed exemplary embodiments of the inventive subject matter. Although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the inventive subject matter being defined by the following claims.

15

THAT WHICH IS CLAIMED:

1. An apparatus comprising:

first, second and third core bus plates arranged in parallel;

5 a first bus extension plate joined to the first core bus plate and extending therefrom at a first angle;

a second bus extension plate joined to the second core bus plate and extending therefrom at a second angle; and

10 a third bus extension plate joined with the third core bus plate and disposed parallel to the first bus extension plate; and

a fourth bus extension plate joined with the third core bus plate and disposed parallel to the second bus extension plate.

15 2. The apparatus of claim 1, wherein the third core bus plate is disposed between the first and second core bus plates.

3. The apparatus of claim 1:

wherein the first bus extension plate extends from the first core bus plate in a first direction perpendicular to a plane of the first core bus plate;

20 wherein the second bus extension plate extends from the second core bus plate in a second direction opposite the first bus direction;

wherein the third bus extension plate extends from the third core bus plate in the first direction; and

25 wherein the fourth bus extension plate extends from the third core bus plate in the second direction.

4. The apparatus of claim 3, wherein the third and fourth bus extension plates lie in the same plane.

5. The apparatus of claim 3, wherein the first bus extension plate comprises a first planar member that joins the first core bus plate at a first arcuate joint, wherein the second bus extension plate comprises a second planar member that joins the second core bus plate at a second arcuate joint and wherein the third and fourth bus extension plates comprise third and fourth planar members that join the third core bus plate at a rounded Y joint.

6. The apparatus of claim 1, wherein the first bus extension plate joins the first core bus plate at a first edge thereof and wherein the second bus extension plate joins the second core bus plate at a first edge thereof, and wherein the apparatus further comprises:

a fifth bus extension plate joining the first core bus plate at a second edge thereof and extending therefrom at a third angle;

a sixth bus extension plate joining the second core bus plate at a second edge thereof and extending therefrom at a fourth angle;

a fourth core bus plate disposed in parallel with the first, second and third core bus plates;

a seventh bus extension plate joined to the fourth core bus plate and disposed parallel to the fifth bus extension plate; and

an eighth bus extension plate joined to the fourth core bus plate and disposed parallel to the sixth bus extension plate.

7. The apparatus of claim 6, wherein the first and fifth bus extension plates extend from the first core bus plate in a first direction perpendicular to a plane of the first core bus plate, wherein the second and sixth bus extension plates extend from the second core bus plate in a second direction opposite the first direction.

8. The apparatus of claim 7, further comprising:

a ninth bus extension plate joining the first core bus plate at a third edge thereof and extending therefrom at a fifth angle;

5 a tenth bus extension plate joining the second core bus plate at a third edge thereof and extending therefrom at a sixth angle;

a fifth core bus plate arranged in parallel with the first, second, third and fourth core bus plates;

10 an eleventh bus extension plate joined to the fifth core bus plate and disposed parallel to the ninth bus extension plate; and

a twelfth bus extension plate joined to the fifth core bus plate and disposed parallel to the tenth bus extension plate.

9. The apparatus of claim 8, wherein the first, fifth and ninth bus extension plates
15 extend from the first core bus plate in the first direction and wherein the second, sixth and tenth bus extension plates extend perpendicularly from the second core bus plate in the second direction.

10. The apparatus of claim 8, wherein the third, fourth and fifth core bus plates are
20 disposed between the first and second core bus plates.

11. The apparatus of claim 6, wherein the third and fourth core bus plates are disposed between the first and second core bus plates.

25 12. The apparatus of claim 1, further comprising:

a first semiconductor switching device electrically connected to ends of the first and third bus extension plates; and

a second semiconductor switching device electrically connected to ends of the second and fourth bus extension plates.

30

13. The apparatus of claim 12, comprising a power converter circuit including the first and second semiconductor devices , wherein the first core bus plate and the first bus extension plate are components of a first DC bus of the power converter circuit, wherein the second core bus plate the second bus extension plate are components of a second DC bus of the power converter circuit, and wherein the third core bus plate, the third bus extension plate and the fourth bus extension plate are components of an input bus and/or an output bus of the power converter circuit.

14. The apparatus of claim 13, further comprising:

a first capacitor electrically connected to the first bus core plate; and
a second capacitor electrically connected to the second bus core plate.

15. The apparatus of claim 14, further comprising:

a fifth bus extension plate joined to the first bus core plate, extending at an angle therefrom and electrically connected to a first terminal of the first capacitor;

a sixth bus extension plate joined to the second bus core plate, extending at an angle therefrom and electrically connected to a first terminal of the second capacitor; and

a common plate parallel to the fifth and sixth bus extension plates and electrically connected to second terminals of the first and second capacitors,

wherein the third bus core plate has a portion extending between the fifth and sixth bus extension plates and through an opening in the common plate.

16. An apparatus comprising:

first, second and third buses arranged in parallel, the third bus disposed between the first and second buses;

5 a first bus extension extending from the first bus in first direction perpendicular to the first bus;

a second bus extension extending from the second bus in a second direction perpendicular to the second bus and opposite the first direction;

a third bus extension extending from the third bus in parallel with the first bus extension;

10 a fourth bus extension extending from the third bus in parallel with the second bus extension;

a first semiconductor switching device coupled to an end of the first bus extension and to an end of the third bus extension; and

15 a second semiconductor switching device coupled to an end of the second bus extension and to an end of the fourth bus extension.

17. The apparatus of claim 16, wherein the first, second and third buses comprise respective first, second and third planar members.

20 18. The apparatus of claim 17, wherein the first bus extension is joined to the first bus at a first edge of the first planar member, wherein the second bus extension is joined to the second bus at a first edge of the second planar member, wherein the third and fourth bus extensions are joined to the third bus at a first edge of the third planar member, and wherein the apparatus further comprises:

25 a fourth bus comprising a fourth planar member arranged in parallel with the first, second and third buses;

a fifth bus extension joined to the first bus at a second edge of the first planar member extending from the first bus in the first direction;

30 a sixth bus extension joined to the second bus at a second edge of the second planar member and extending from the second bus in the a second direction;

a seventh bus extension joined to the fourth bus at a first edge of the fourth planar member and extending in parallel with the fifth bus extension;

an eighth bus extension joined to the fourth bus at the first edge of the fourth planar member and extending in parallel with the sixth bus extension;

5 a third semiconductor switching device coupled to an end of the fifth bus extension and to an end of the seventh bus extension; and

a fourth semiconductor switching device coupled to an end of the sixth bus extension and to an end of the eighth bus extension.

10 19. An apparatus comprising:

first and second semiconductor switching devices disposed opposite one another at respective ones of opposing first and second surfaces;

a first bus comprising a first conductive plate disposed between the first and second surfaces and extending in a first direction towards the first surface to electrically connect to the
15 first semiconductor switching device;

a second bus comprising a second conductive plate disposed between the first and second surfaces and extending in a second direction perpendicular to the first direction towards the second surface to electrically connect to the second semiconductor switching device; and

a third bus comprising:

20 a third conductive plate disposed parallel to the first conductive plate and electrically connected to the first semiconductor switching device; and

a fourth conductive plate disposed parallel to the second conductive plate and electrically connected to the second semiconductor switching device and the third conductive plate.

25

20. The apparatus of claim 19:

wherein the first bus further comprises a fifth conductive plate disposed between the first and second surfaces and parallel thereto and joined to the first conductive plate;

5 wherein the second bus comprises a sixth conductive plate disposed between the first and second surfaces and parallel to the fifth conductive plate and joined to the second conductive plate; and

wherein the third bus comprises a seventh conductive plate disposed between the fifth and sixth conductive plates and joined to the third and fourth conductive plates.

1/15

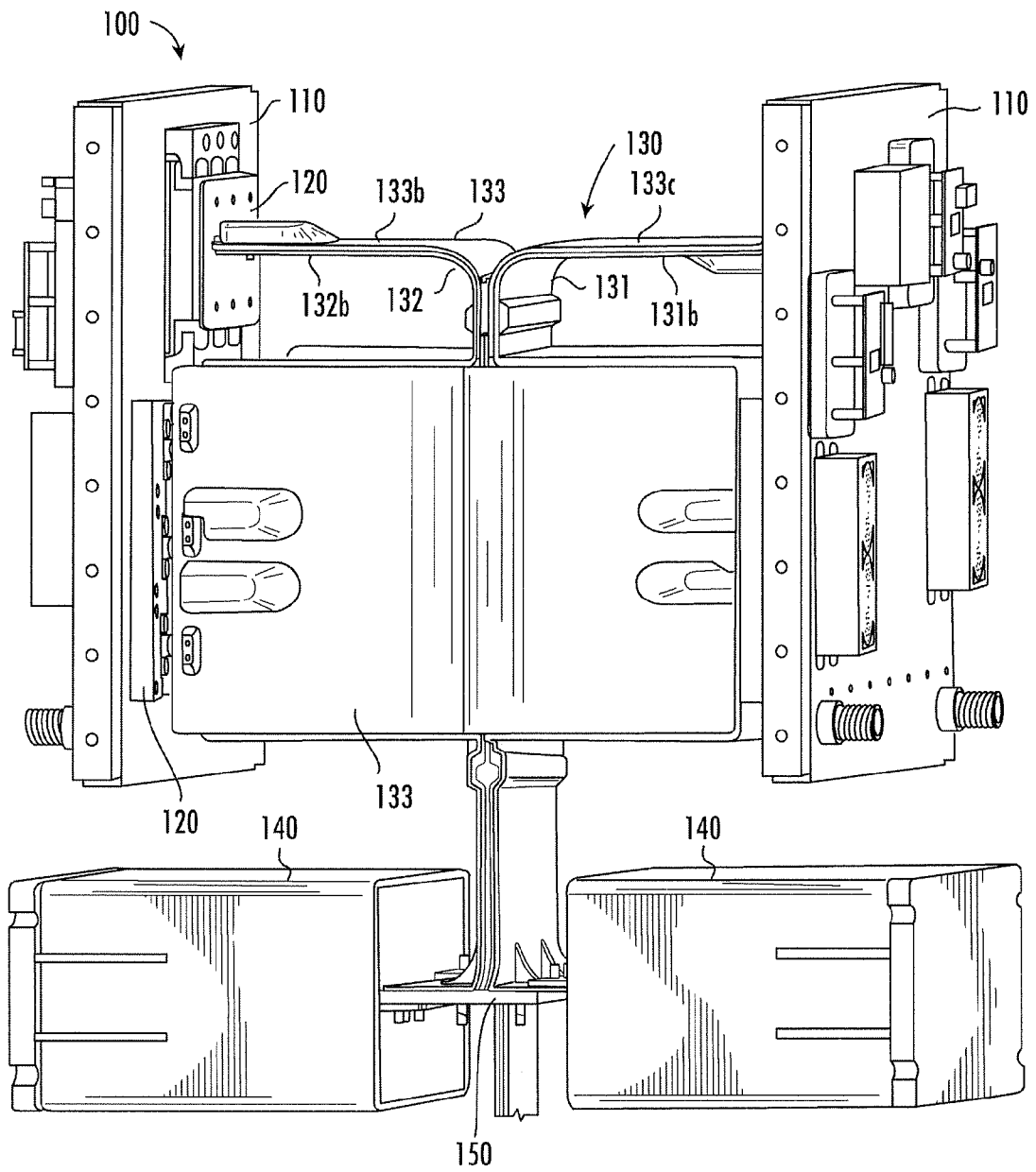


FIG. 1

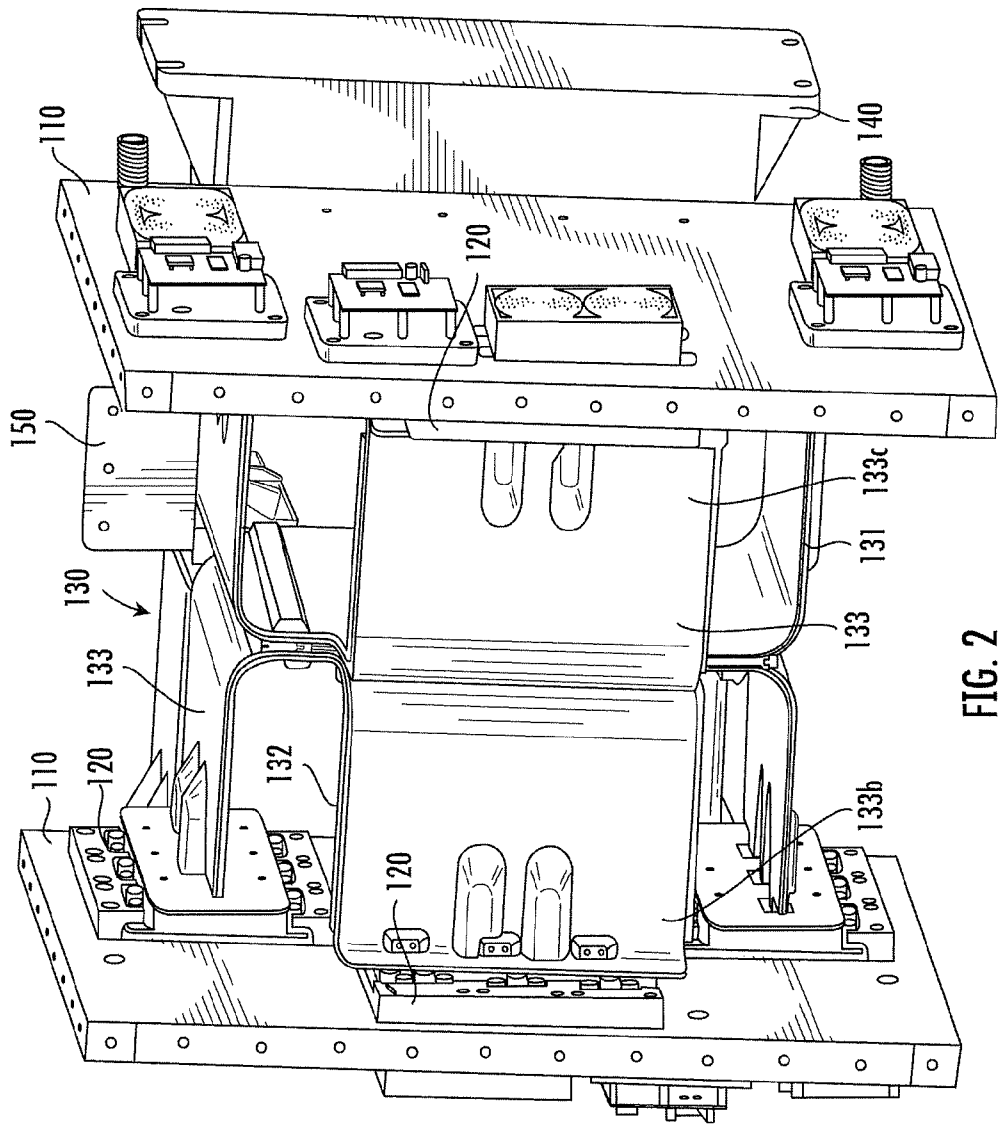


FIG. 2

3/15

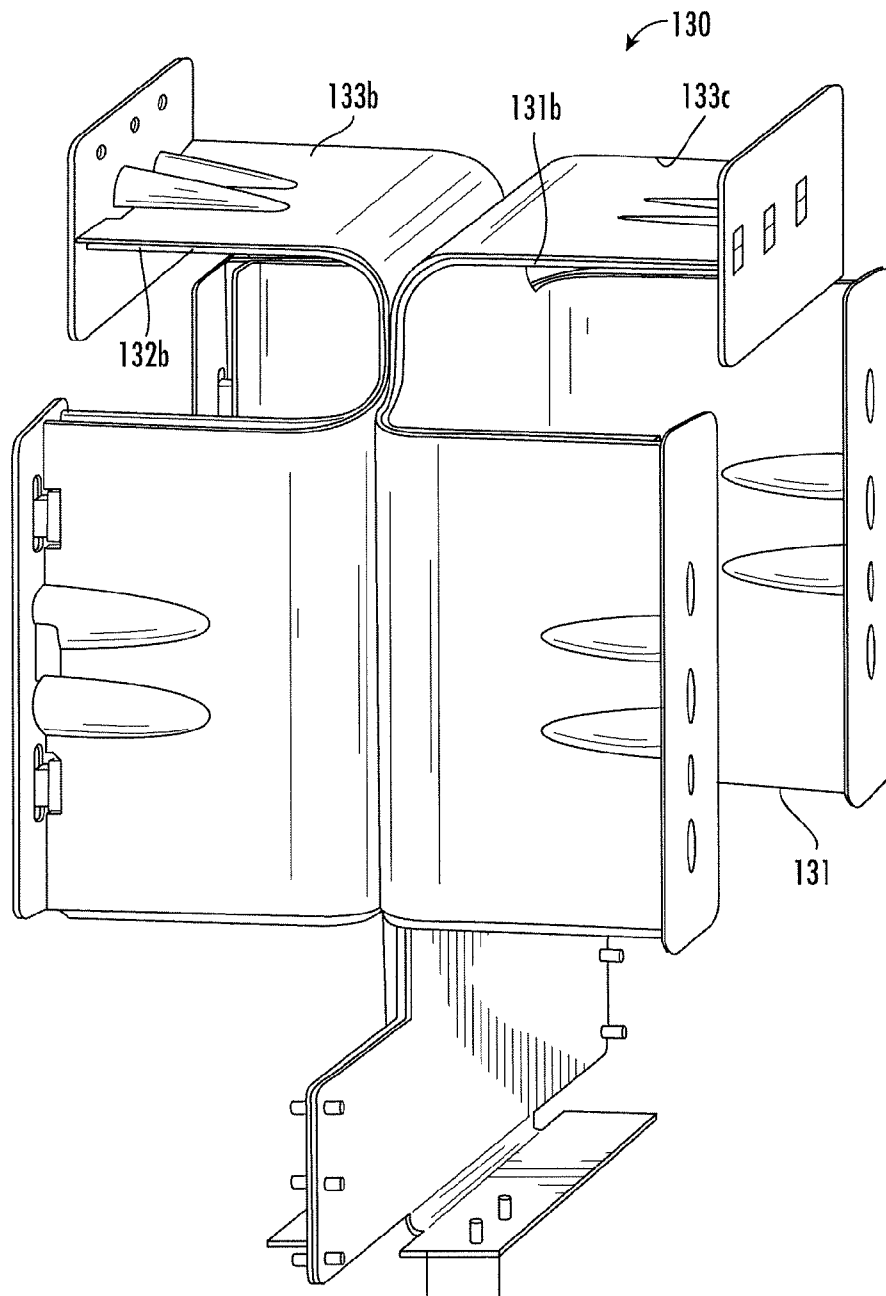


FIG. 3

4/15

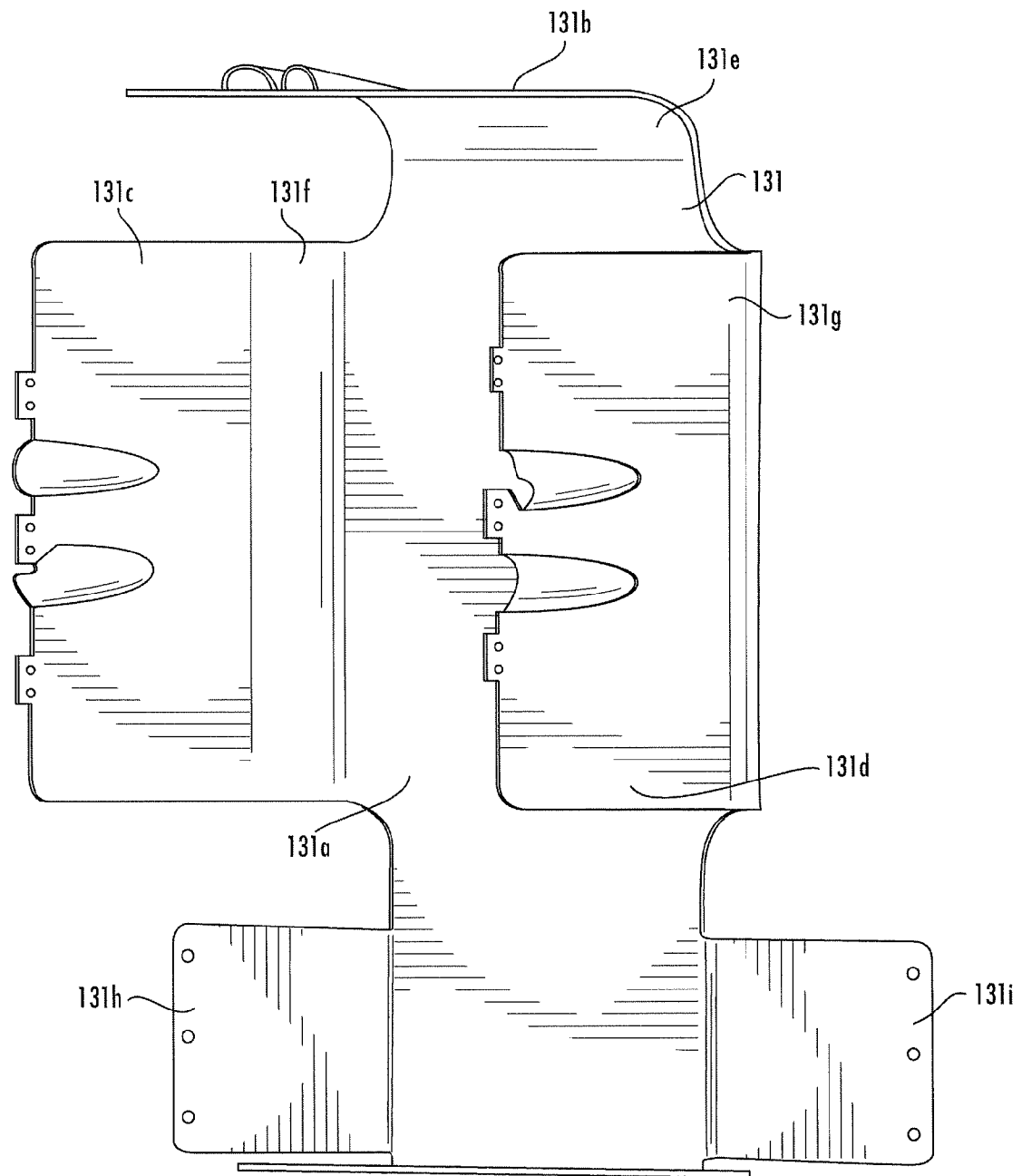
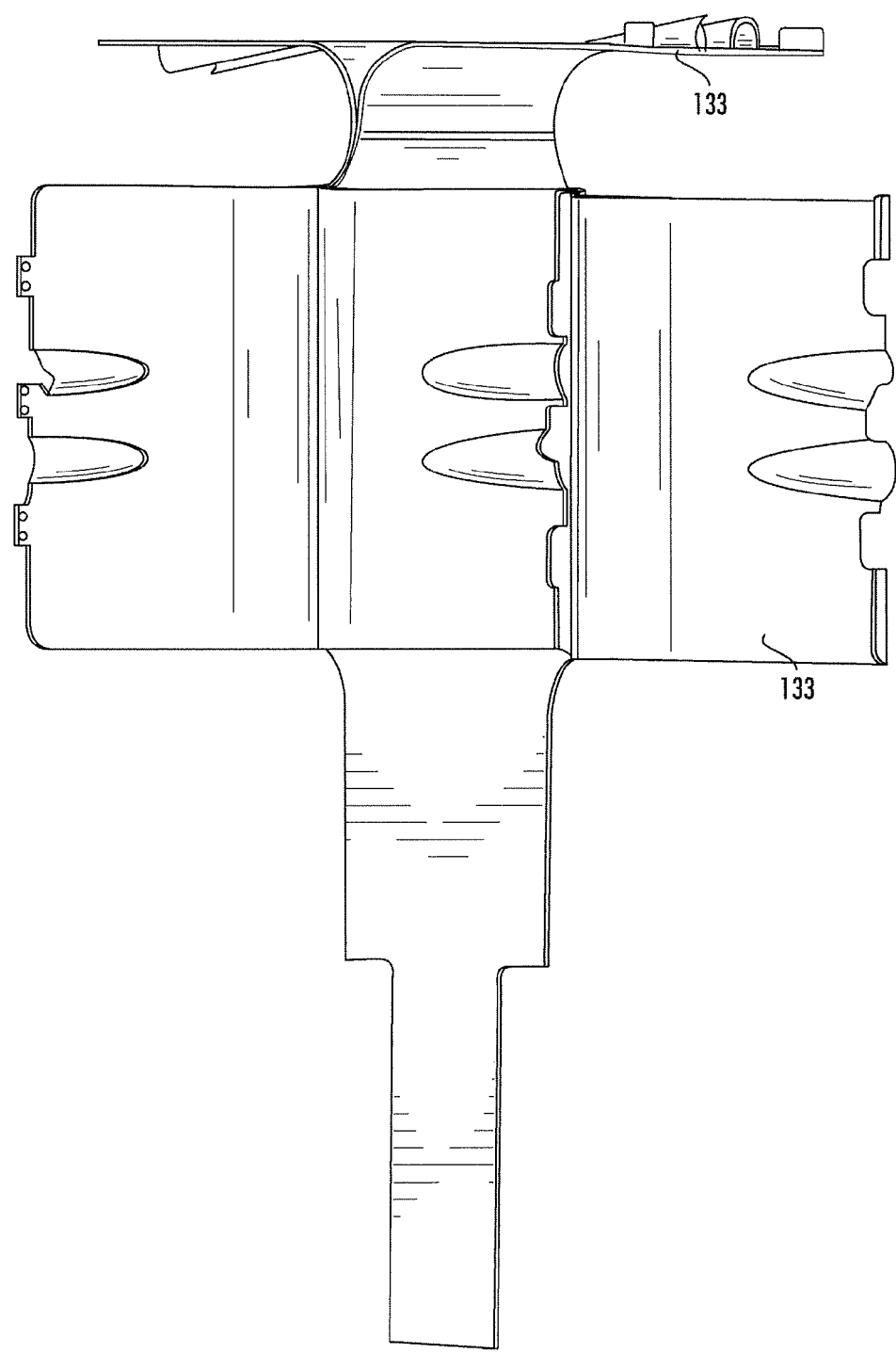


FIG. 4



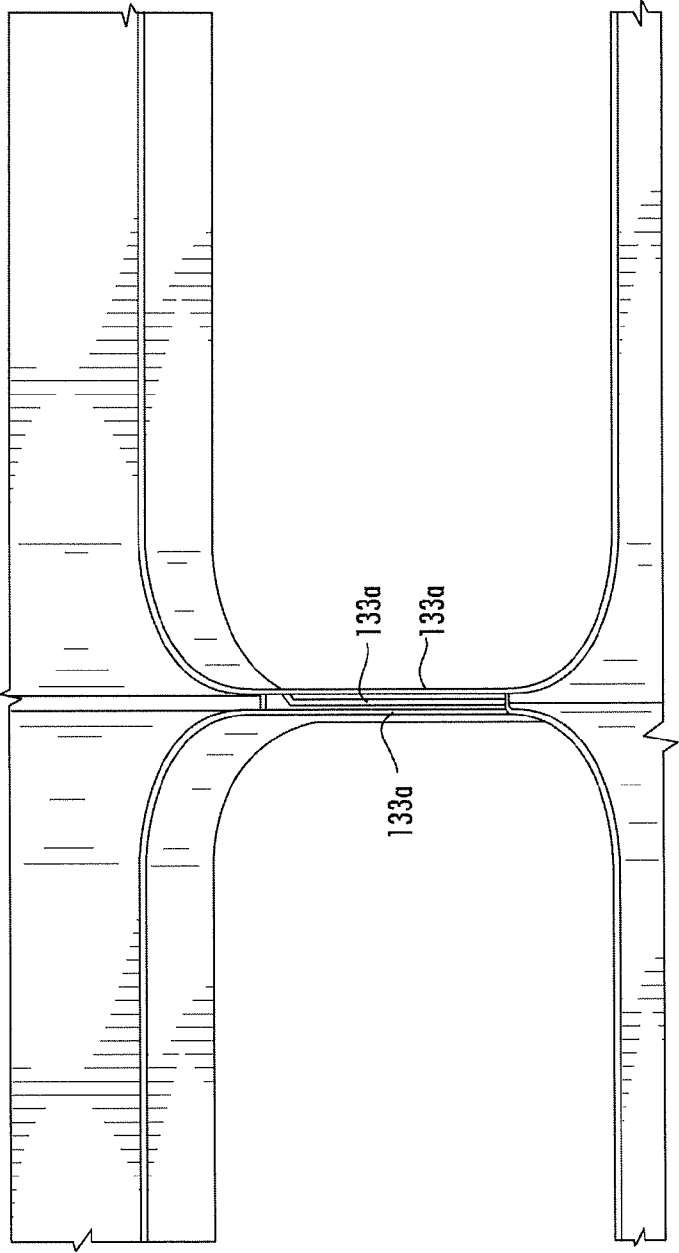


FIG. 6

7/15

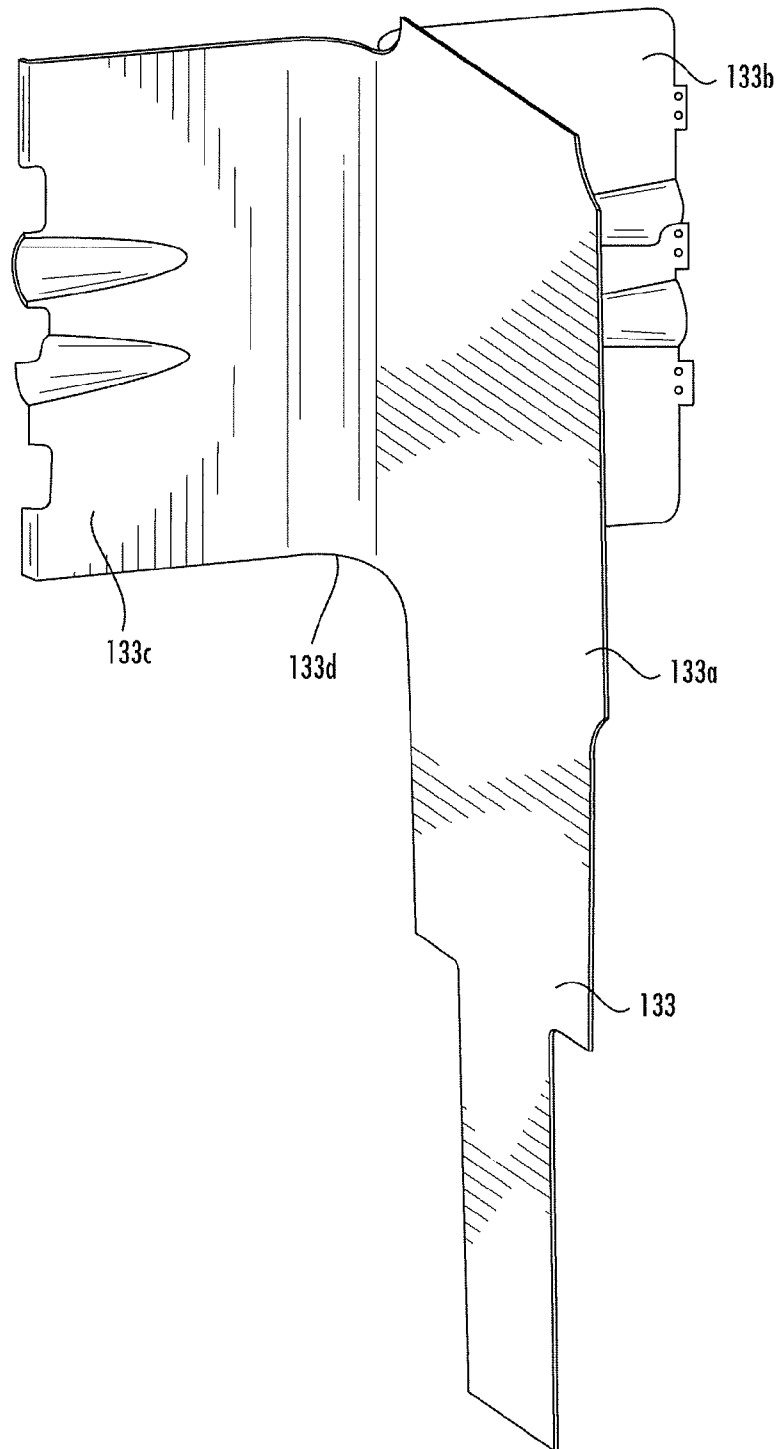


FIG. 7

8/15

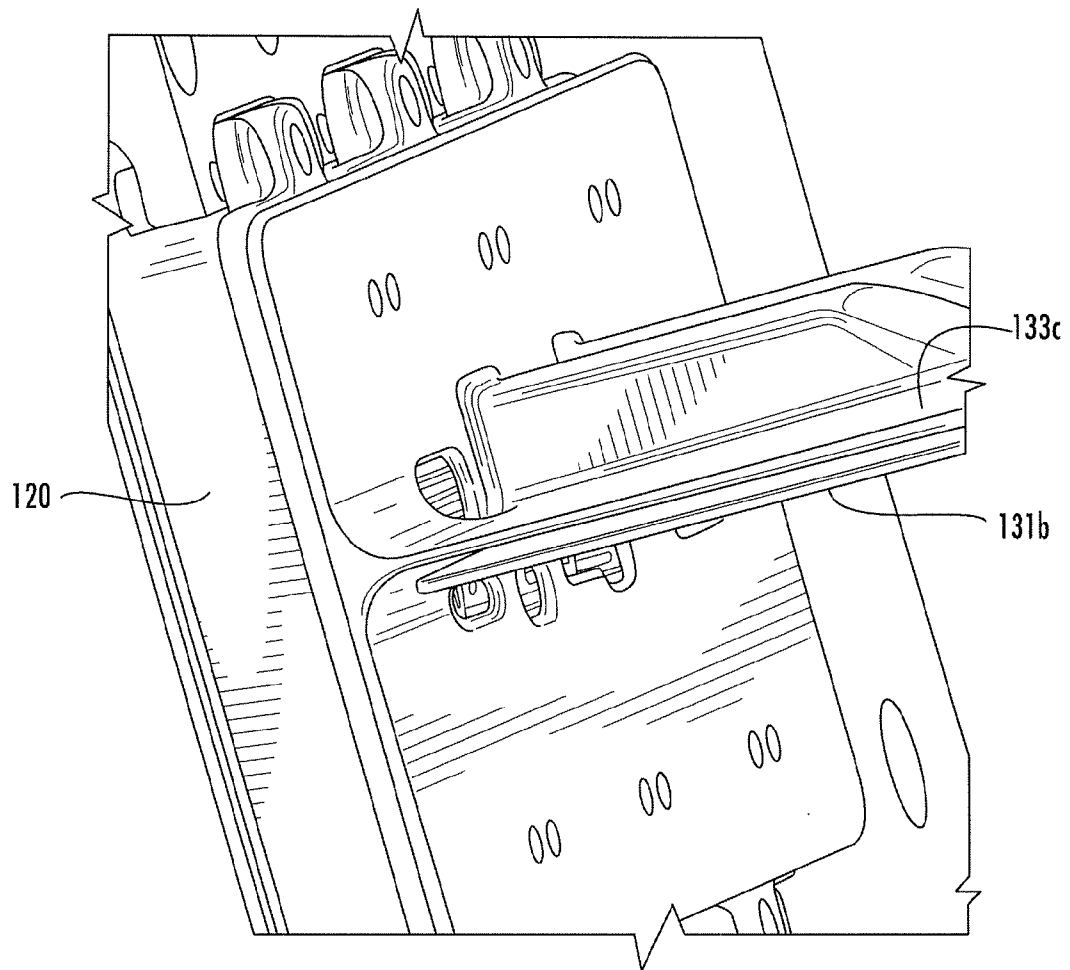


FIG. 8

9/15

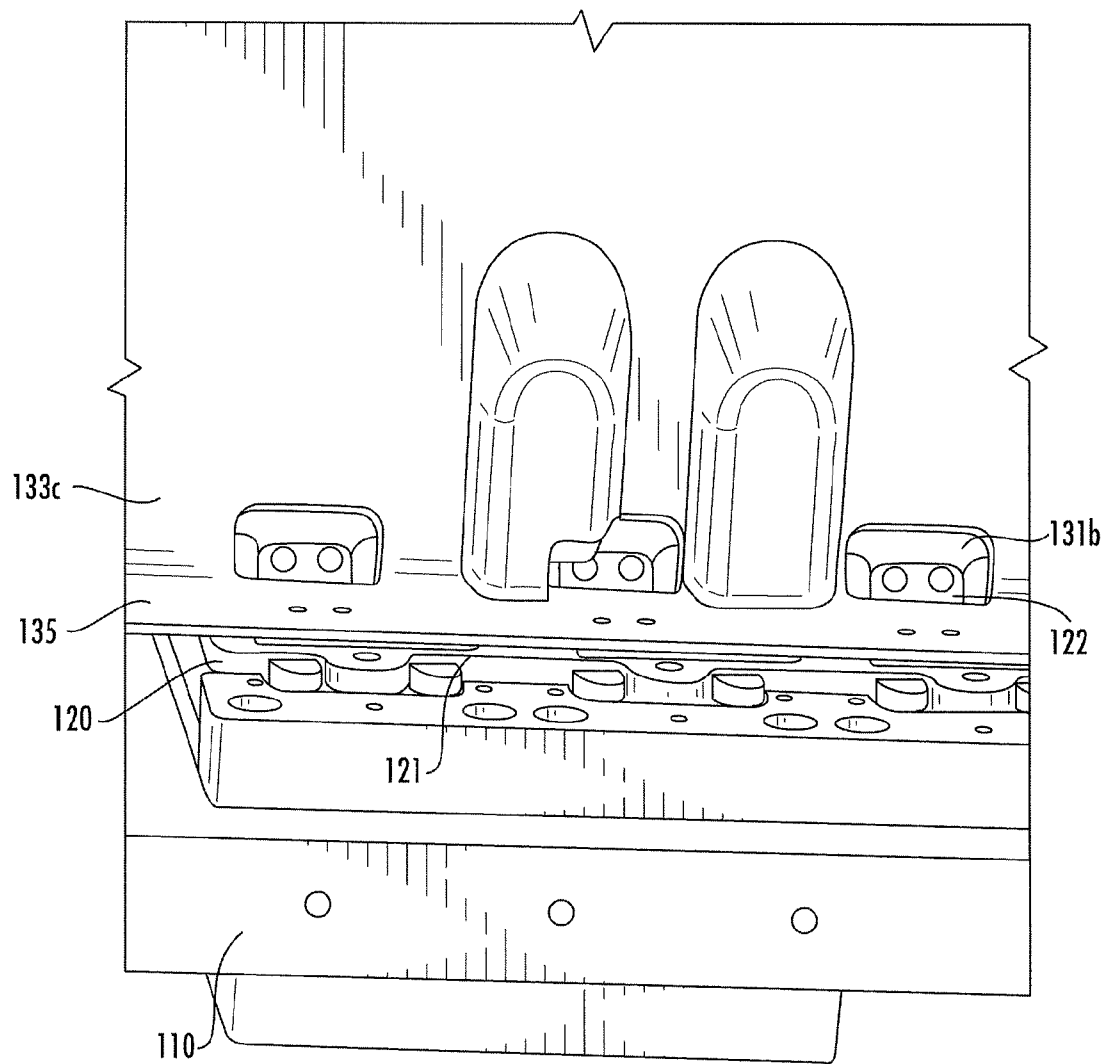


FIG. 9

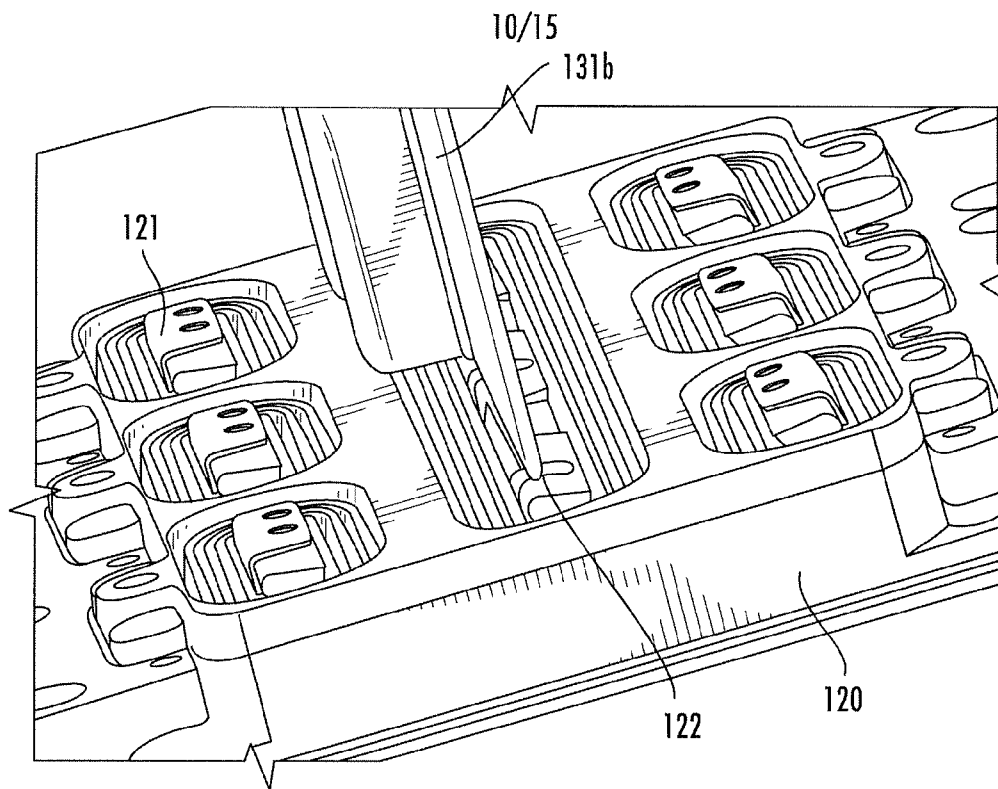


FIG. 10

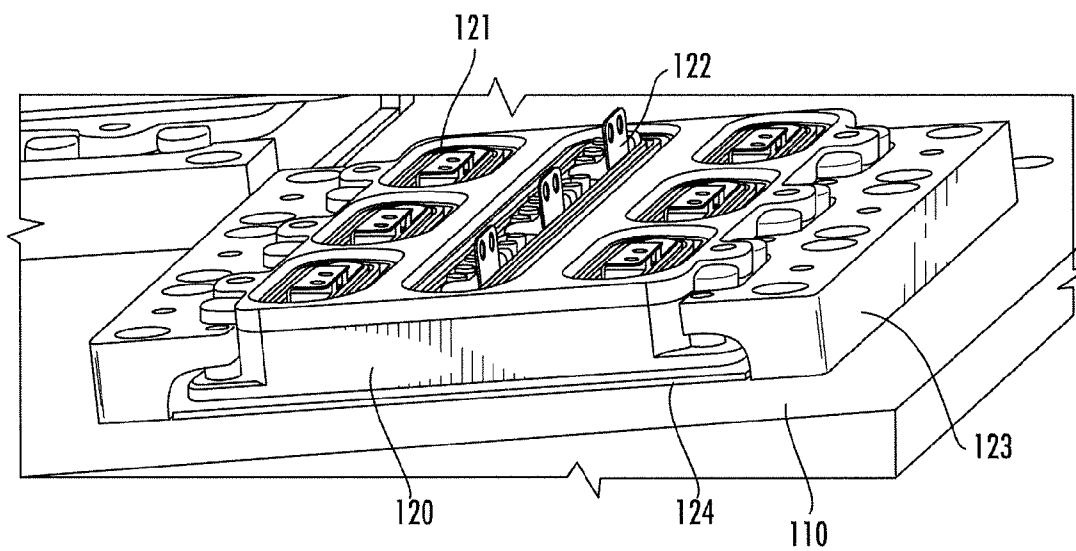


FIG. 11

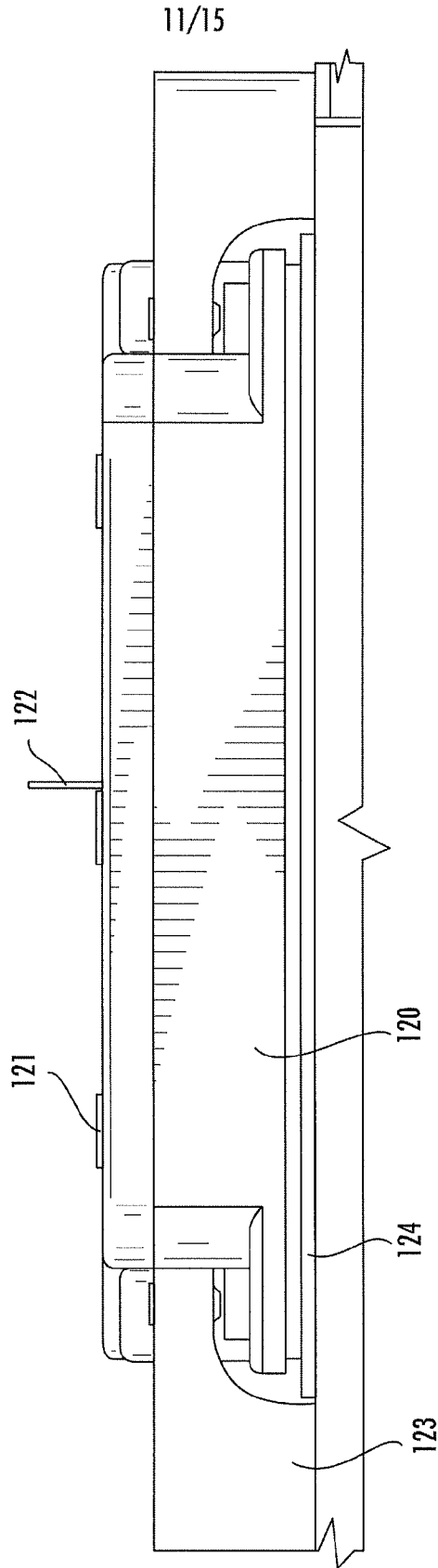


FIG. 12

12/15

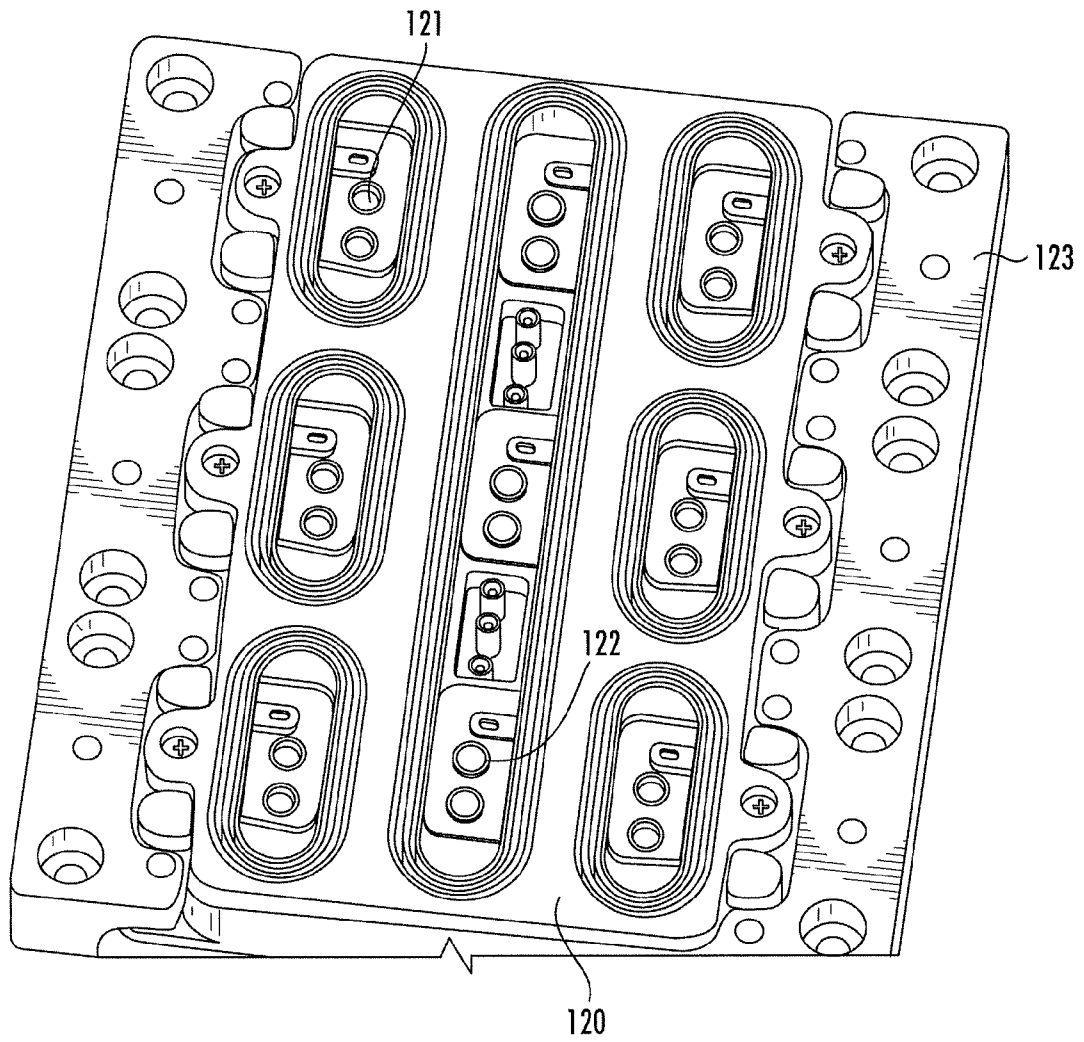


FIG. 13

13/15

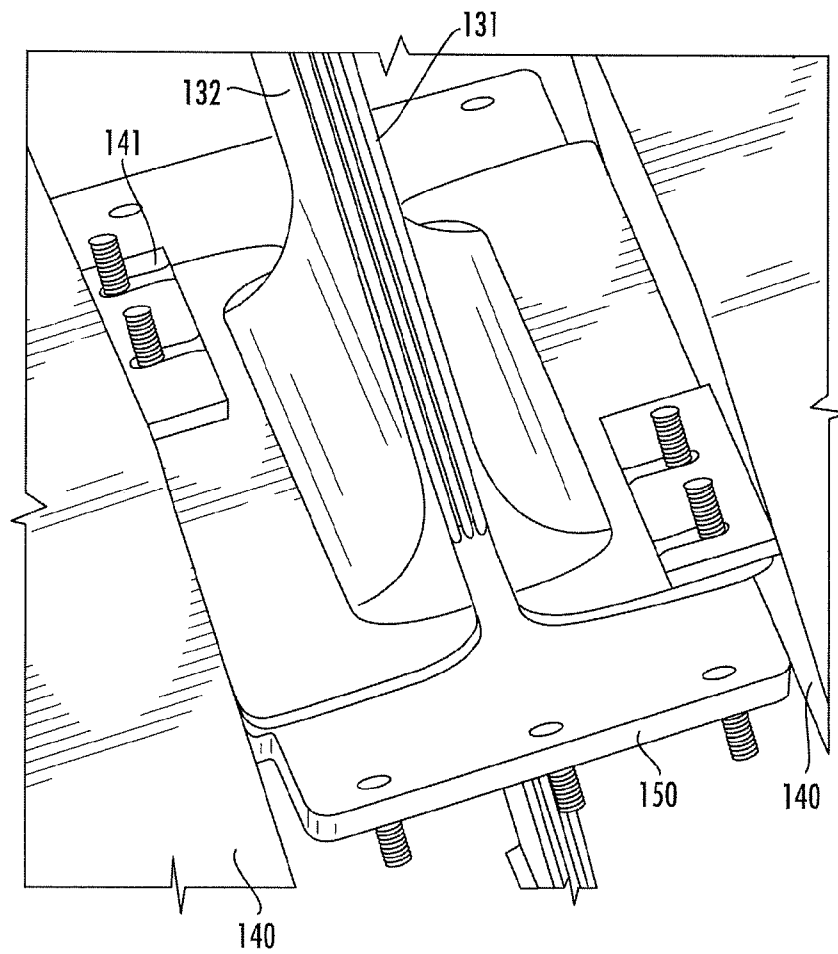


FIG. 14

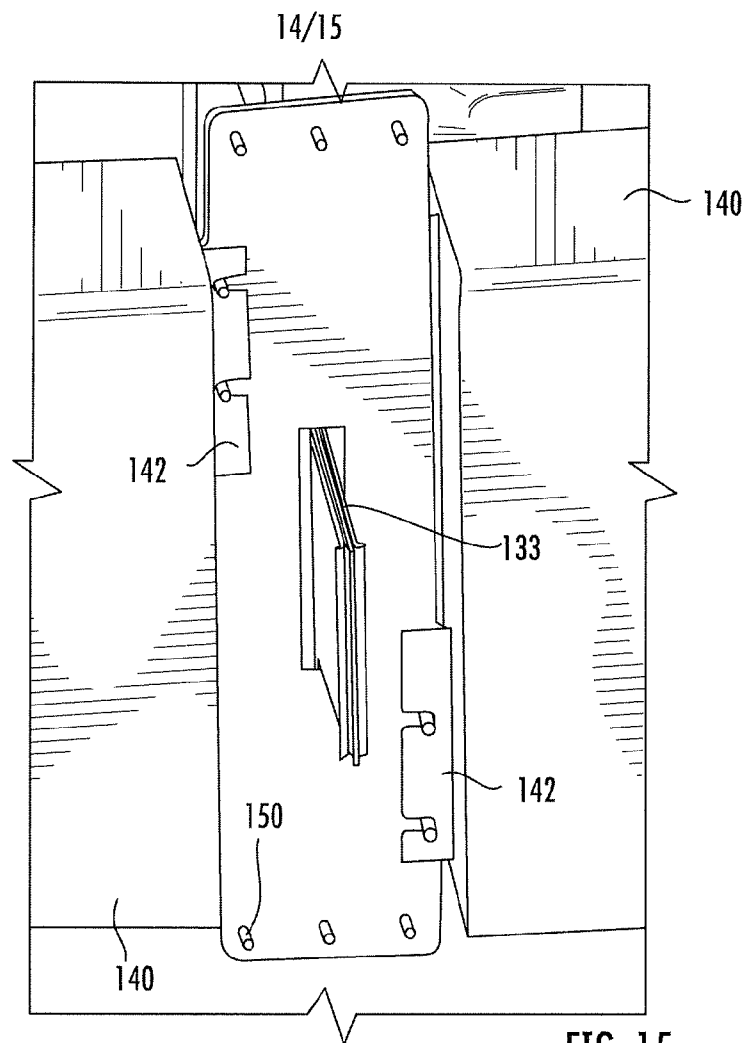


FIG. 15

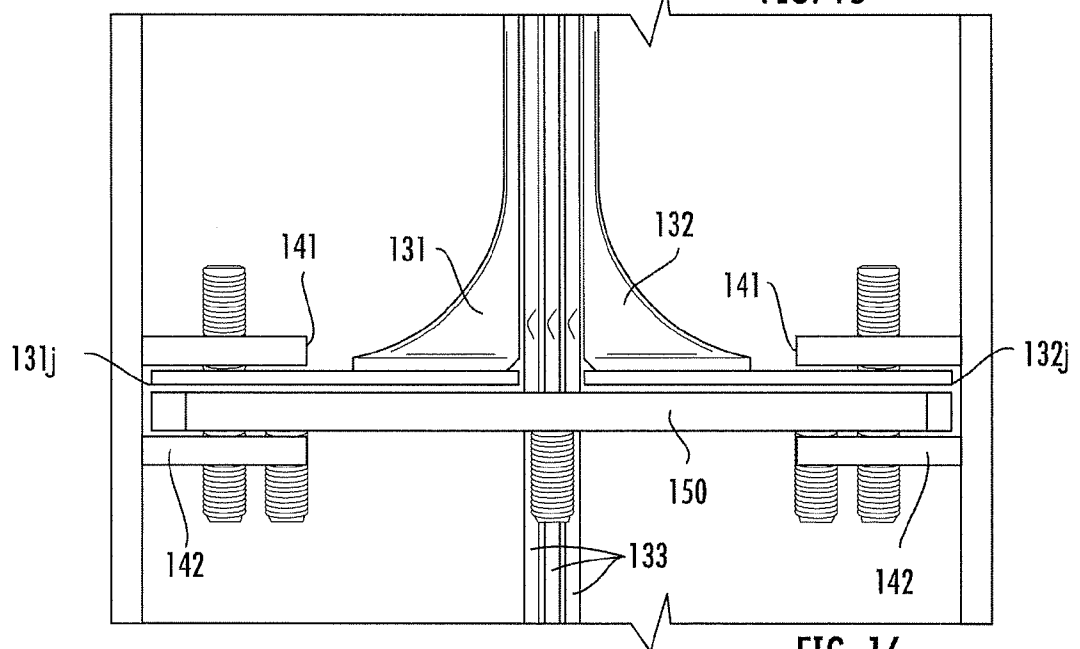


FIG. 16

15/15

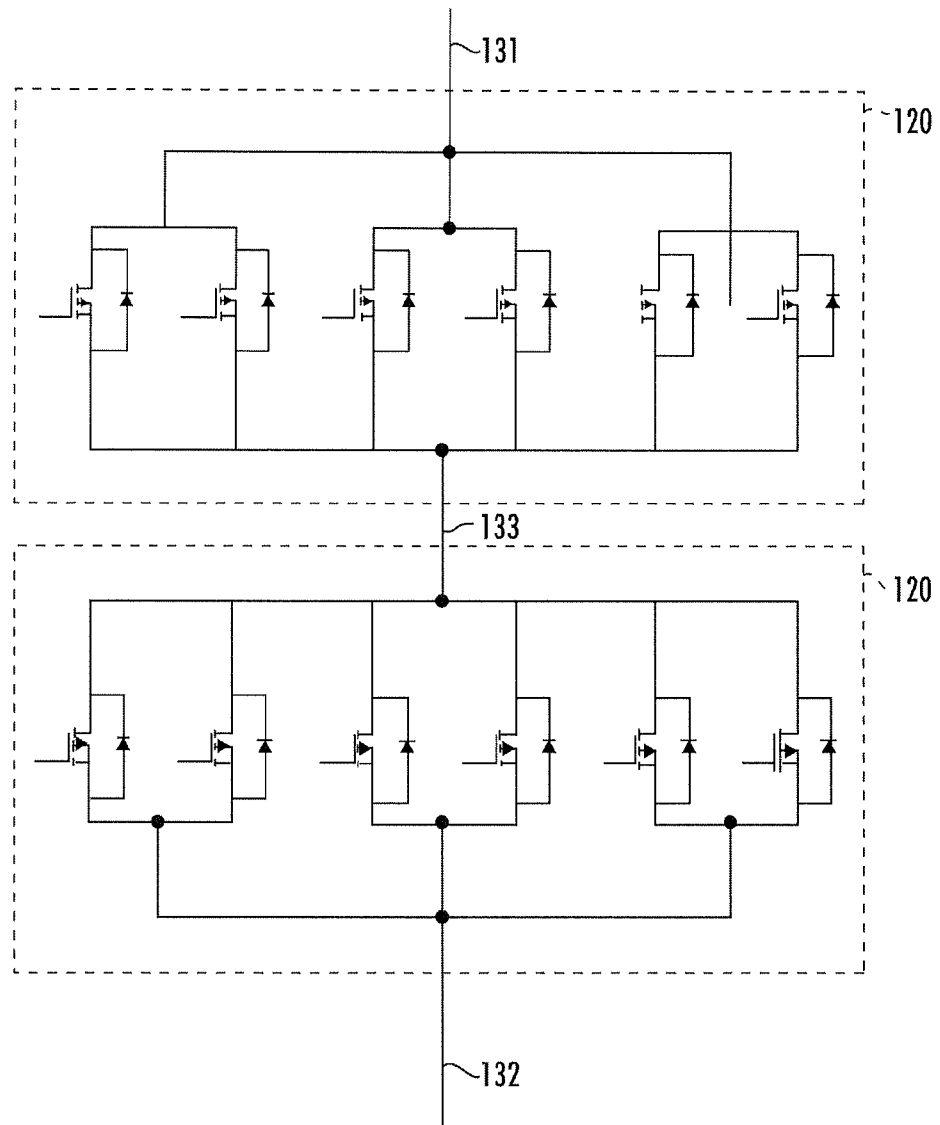


FIG. 17

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2019/025364

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M7/00 H02G5/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M H02G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 3 300 086 A1 (SUNCALL CORP [JP]; STANLEY ELECTRIC CO LTD [JP]) 28 March 2018 (2018-03-28) paragraphs [0056], [0057]; figure 8A -----	1-15
A	DE 196 22 895 A1 (SCHNEIDER ELECTRIC SA [FR]) 12 December 1996 (1996-12-12) column 2, lines 48-56 column 3, lines 49-58; figures 4, 5 -----	1-15
A	US 2014/116751 A1 (HATORI KOUJI [JP]) 1 May 2014 (2014-05-01) paragraphs [0005], [0089]; figures 1, 19-25 -----	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

31 January 2020

Date of mailing of the international search report

18/02/2020

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Zeljko, Sandra

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2019/025364

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 3300086	A1	28-03-2018	EP 3300086 A1 28-03-2018
		JP 6487769 B2	20-03-2019
		JP 2016216766 A	22-12-2016
		US 2018148855 A1	31-05-2018
		WO 2016185706 A1	24-11-2016

DE 19622895	A1	12-12-1996	DE 19622895 A1 12-12-1996
		FR 2735289 A1	13-12-1996

US 2014116751	A1	01-05-2014	CN 103795269 A 14-05-2014
		JP 5821822 B2	24-11-2015
		JP 2014090115 A	15-05-2014
		US 2014116751 A1	01-05-2014
